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Exploiting Within-Channel Tunneling in a Nanoscale Tunnel Field-Effect Transistor

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ABSTRACT In this paper, using device simulations, we investigate electrical characteristics of a tunnel field-effect transistor (TFET) in which band-to-band tunneling (BTBT) occurs dominantly within the channel, rather than at source-channel junction. The within-channel BTBT is enabled by sharp band-bending induced by the dual material gate (DMG). The work-functions of two metal gates are chosen, such that the surface potential profile exhibits a distinct step at the DMG interface. Consequently, even under equilibrium condition, a high lateral electric field and an abrupt tunneling junction exist at the DMG interface. When a small gate voltage is applied, the inherent lateral electric field aids in creating an abrupt band alignment and obtaining a small tunneling width. As a result, an excellent average subthreshold swing is obtained in the proposed device. We have also investigated scaling of channel lengths in the proposed device and have demonstrated that within-channel tunneling can be exploited for channel lengths of 40*nm* and above. Furthermore, low drain threshold voltage and suppressed drain-induced barrier lowering can be obtained in the proposed device. Moreover, in contrast to conventional TFETs, electrical characteristics of the proposed device are less susceptible to source doping variations and shift in gate-edge with respect to the source-channel junction.

INDEX TERMS Tunnel field-effect transistor, dual material gate, lateral electric field, process-induced variations, subthreshold swing, threshold voltage.

I. INTRODUCTION

Tunnel field-effect transistor (TFET) is one of the most promising alternatives to metal-oxide semiconductor FET (MOSFET) for futuristic low-power applications [1]–[3]. TFETs work on the principle of gate-modulated band-to-band tunneling (BTBT). Due to the mechanism of operation, a TFET can exhibit subthreshold swing (SS) lower than 60 mV/decade at room temperature. Therefore, TFETs can be used as energy-efficient switches and in low supply voltage circuits [4]–[7].

Traditionally, TFETs are designed such that the BTBT at the source-channel junction is enabled by the application of gate voltage [3], [5], [7]. To maximize the BTBT at the source–channel junction and boost the ON-state current (I_{ON}), in general, a high source doping concentration is used [5], [7], [8]. Furthermore, to boost the BTBT at the source–channel junction, the source doping profile must be abrupt [2], [5], [9], [10]. However, obtaining an abrupt doping profile is challenging in fabrication [11], [12].

In general, TFETs exhibit exponential onset in the output characteristics because of the dependence of the BTBT on the gate-to-source voltage V_{GS} and drain-to-source voltage V_{DS}, in contrast to the conventional MOSFET [13], [14]. Therefore, in a TFET, there exist two types of threshold voltages: gate threshold voltage ($V_{TH,G}$) and drain threshold voltage ($V_{TH,D}$). For digital circuit applications, for achieving improved performance, a TFET should have a low $V_{TH,D}$ [13]–[15].

In this work, using simulations, we investigate exploiting within-channel BTBT using dual material gate (DMG) architecture in Double Gate TFET (DGTFET). In literature, DMGs are shown to improve the electrical characteristics in a TFET by enhancing BTBT on the source side and suppressing BTBT on the drain side [7], [16]–[18]. In this paper, we utilize DMG

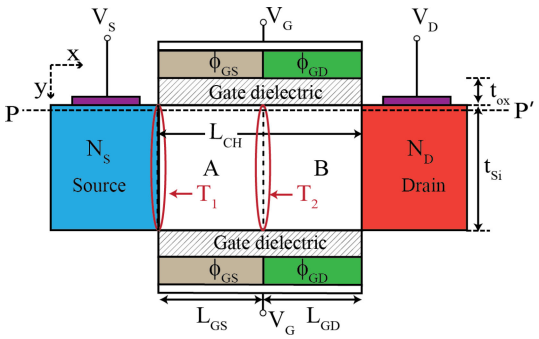

FIGURE 1. Schematic cross-section of the proposed TFET.

TABLE 1. Parameters of the Proposed TFET

Parameter	Value
Supply voltage (V_{DD})	0.5 V
Silicon film thickness (t_{si})	10 nm
Effective oxide thickness (EOT)	0.5 nm (HfO_2)
s-gate work-function (ϕ_{GS})	5.93 eV
d-gate work-function (ϕ_{GD})	4.2 eV
Source doping (N_S) (p-type)	$1 \times 10^{19} atoms/cm^3$
Drain doping (N_D) (n-type)	$1 \times 10^{19} atoms/cm^3$
Channel doping (N_C) (p-type)	$1 \times 10^{17} atoms/cm^3$
Channel length (L_{CH})	$20 - 100$ nm
s-gate length (L_{GS})	$10 - 50$ nm
d-gate length (L_{GD})	$10 - 50$ nm

in obtaining a sharp transition in the energy bands at the junction of high–low work-function materials and enabling within-channel BTBT. Due to the existence of an inherent lateral electric field, a strong gate control over the BTBT region and the shift of BTBT region from the source–channel junction towards the drain, several electrical parameters improve in the proposed TFET. Moreover, it is demonstrated that in contrast to the conventional TFETs, the proposed device is less susceptible to variations in source doping and shift in the gate-edge with respect to the source-channel junction.

The rest of this paper is organized as follows: In Section II, the proposed device structure and simulation model is discussed. In Section III, the operation, characteristics and issues related to process-induced variations are discussed. Finally, in Section IV conclusions are made.

II. DEVICE STRUCTURE AND SIMULATION SETUP

Fig. 1 shows the schematic cross–sectional view of the proposed device. The top and the bottom gates are composed of materials with different work-functions, similar to DMG-DGTFET in [16]. The gate closer to the source is having a work-function ϕ_{GS} and is termed as s–gate and the gate closer to the drain is having a work-function ϕ_{GD} and is termed as d–gate. The channel region under the s–gate is denoted as "A" and under the d–gate as "B". The device in this work is different from the DMG-TFET proposed in [16], in the mechanism of operation. In this work, the device parameters are chosen such that a sharp transition in the energy bands is obtained at the junction of high–low work-function materials T_2 rather than at the source–channel junction T_1. Consequently, within-channel BTBT at the junction T_2 constitute the dominant component of the ON-state current. Furthermore, suppression of source–channel junction BTBT exhibits certain interesting characteristics which are investigated in detail. The simulation parameters used in this work are shown in Table 1.

In literature, dual-material gate devices have been widely studied and fabricated [7], [16], [18]–[20]. To realize a DMG architecture, techniques such as tilt angle evaporation and lithography, metal inter-diffusion technique and metal wet etching techniques can be used [18], [21], [22]. In the tilt angle evaporation method, one of the gate material is evaporated with a carefully controlled tilt angle, and then the other material is deposited using conventional evaporation [20]. In metal inter-diffusion technique to fabricate the DMG architecture, the two materials with different work-functions are deposited one after other. Subsequently, one of the metals is selectively removed from unwanted regions [23]. Additionally, metal wet etching and other advanced fabrication processes can be used for fabricating DMG, as demonstrated in [24]–[26].

In this paper, all simulations have been carried out using the ATLAS version 5.22.1.R [27]. Non–local BTBT model is used to compute the current [27]. Fermi–Dirac statistics and Shockley–Read–Hall recombination models are also considered in the simulations. All doping profiles are assumed to be abrupt. The simulation setup has been calibrated using [28] and has been used in [16], [29], [30]. In this work, we have taken silicon film thickness as 10 *nm*. Therefore, we have not considered the quantum confinement effect since this becomes appreciable when the silicon film thickness is less than 7 *nm* [11], [31], [32].

III. DEVICE OPERATION AND CHARACTERISTICS

In the proposed device, within-channel tunneling (at the junction T_2) is enabled by DMG. Fig. 2(a) shows the magnitude of the lateral electric field ($E_{field,x}$) at equilibrium ($V_{GS} = 0$, $V_{DS} = 0$). In the proposed device ($\phi_{GS} = 5.93\ eV$, $\phi_{GD} = 4.2\ eV$), there is a high electric field at the junction T_2. A high inherent $E_{field,x}$ leads to improved electrical characteristics, as explained in the following paragraphs [7], [33], [34]. In contrast, in the conventional device ($\phi_{GS} = \phi_{GD} = 4.2\ eV$), the peak $E_{field,x}$ occurs at the junction T_1. Moreover, the step in the potential profile in the proposed device is manifested in the energy band diagram, as shown in Fig. 2(b). It leads to a small tunneling barrier width and appropriate energy band alignment at the junction T_2. In the equilibrium state, despite small tunneling width, negligible band overlap exists, which inhibits BTBT and the device remains in the OFF-state. However, when a small gate–to–source voltage (V_{GS}) is applied, band overlap occurs and due to a small tunneling width, the proposed device switches ON abruptly. Therefore, an excellent average subthreshold swing (SS_{avg}) is expected in a TFET that exploits within-channel tunneling.

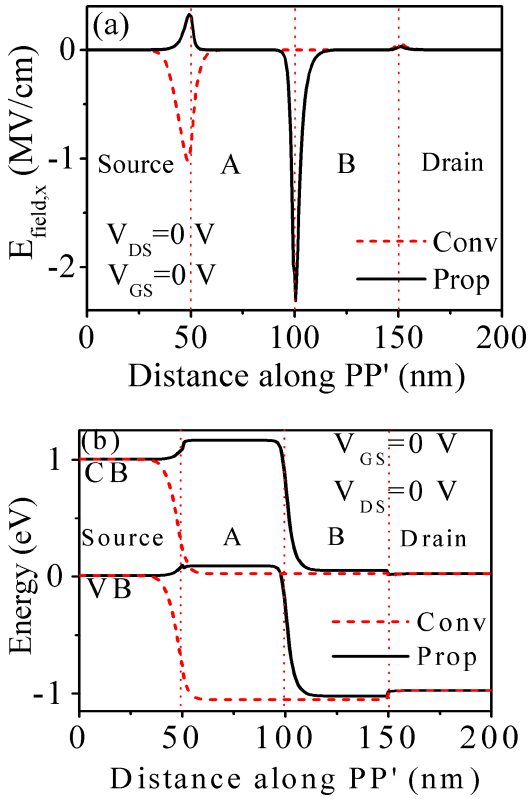

FIGURE 2. Devices under equilibrium (a) Lateral electric field (b) Energy band diagram along the cut-line *PP'*.

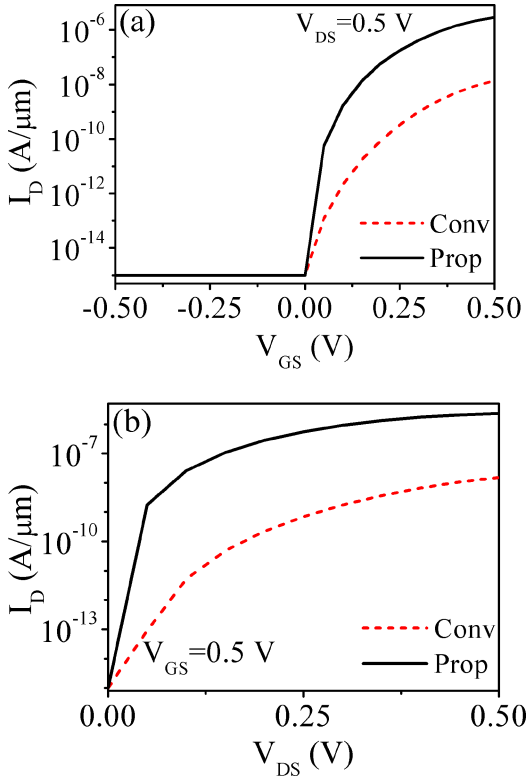

FIGURE 3. Comparison of the conventional and proposed devices (a) Transfer characteristics (b) Output characteristics.

Fig. 3(a) compares the transfer characteristics of the conventional and the proposed device. In this work, the threshold voltage (V_{th}) is taken as the V_{GS} when the drain current (I_D) reaches $1 \times 10^{-8}\ A/\mu m$. The V_{th} is found to be 145 mV and 457 mV for the proposed device and the conventional device, respectively. Furthermore, the SS_{avg} in the proposed device is 21 mV/dec, in contrast to 65 mV/dec in the conventional device. A low V_{th} and an excellent SS_{avg} in the proposed device is due to the inherent lateral electric field supporting BTBT. However, the ON–state current (I_{ON}) in the proposed device is $2.6 \times 10^{-6}\ A/\mu m$. A low I_{ON} in a silicon-based TFET is a known problem, which this paper does not address, and can be attributed to the high bandgap of silicon [5]. It should be noted that for $V_{GS} < 0\ V$, the drain current is constant. The work function of the gates in both the devices has been adjusted such that the ambipolar current (drain current when $V_{GS} < 0\ V$) is minimized and the drain current starts to take off at $V_{GS} = 0\ V$. When $V_{GS} < 0\ V$, there is no conduction–valence band overlap, and the band-to-band tunneling is inhibited to a large extent in the device. However, a small current exists due to direct source-to-drain BTBT and thermal effects [7], [35], [36]. Since a slight variation in the current around $1 \times 10^{-15} A/\mu m$ obtained by the simulator is purely a simulation artifact rather than due to any physical phenomenon we have not shown them to avoid unnecessary confusion.

Next, we compare the output characteristics of the conventional and the proposed devices in Fig. 3(b). The distinct feature of the output characteristics in a TFET such as exponential onset and existence of drain threshold voltage ($V_{th,d}$) is evident [7], [14]. In general, a low $V_{th,d}$ is desirable in a TFET to reduce the transition time in CMOS-type TFET-based digital circuits [15], [37]. To quantify $V_{th,d}$, we define $V_{th,d}$ as the drain voltage required to make I_D reach 10% of the saturation current level. The extracted $V_{th,d}$ is found to be 0.16 V for the proposed device and 0.24 V for the conventional device. The presence of an inherent lateral electric field in the proposed device enables it to be turned-ON at lower V_{DS}, achieving low $V_{th,d}$ and suppressing super–linear onset [7], [34], [37]. It is worth mentioning that the characteristics of both the conventional device and the proposed device depend on the source doping concentration. In Fig. 3(a), we have shown the device characteristics for $N_S = 1 \times 10^{19} atoms/cm^3$. The characteristics of these devices at other source doping concentrations and profiles are shown in the subsequent sections.

In general, TFETs suffer from drain-induced barrier lowering (DIBL) due to a stronger impact of the drain voltage (V_{DS}) on BTBT [7], [30]. To quantify the DIBL effect, we measure the shift in the transfer characteristics due to drain voltage at a fixed drain current $I_{DIBL} = 10^{-12} A/\mu m$, as shown in Fig. 4 [16], [30]:

$$DIBL = \frac{V_{GS,2} - V_{GS,1}}{V_{DS,2} - V_{DS,1}} \tag{1}$$

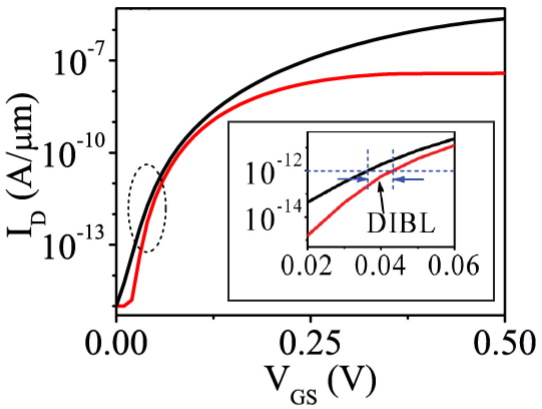

FIGURE 4. Illustration of DIBL in the proposed device (red line denotes $V_{DS} = 0.1\ V$ and black line denotes $V_{DS} = 0.5\ V$).

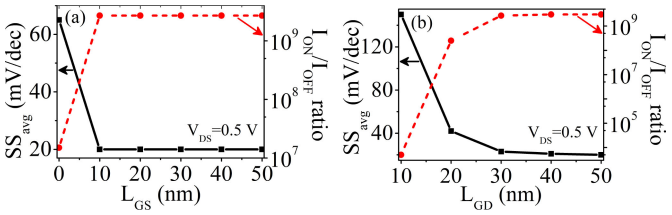

FIGURE 5. SS_{avg} and I_{ON}/I_{OFF} ratio for the proposed TFET with (a) with varying L_{GS} ($L_{GD} = 50\ nm$) (b) varying L_{GD} ($L_{GS} = 50\ nm$).

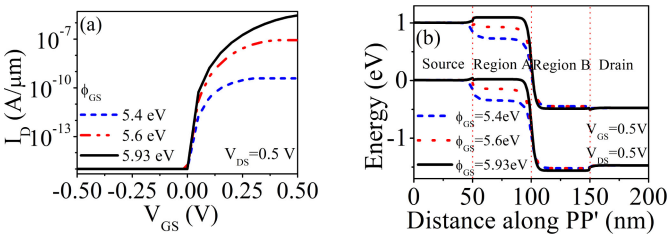

FIGURE 6. (a) Transfer characteristics (b) Energy band diagram of the proposed device keeping $\phi_{GD} = 4.2\ eV$ and varying the ϕ_{GS}.

where, $V_{GS,2}$ is the gate voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,2} = V_{DD}$. Similarly, $V_{GS,1}$ is the gate voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,1} = 0.1\ V$. The extracted value of DIBL is 20 mV/V for the proposed TFET and 280 mV/V for the conventional TFET. A high inherent lateral electric field at the BTBT junction in the proposed device suppresses the further impact of drain-induced electric field leading to a smaller DIBL effect.

In contrast to a MOSFET, gate–to–drain capacitance (C_{GD}) dominates over the gate–to–source capacitance (C_{GS}) in a TFET [7], [38]–[40]. Our simulations show that, for the conventional device in the ON-state, $C_{GD} = 7.1\ fF/\mu m$ and $C_{GS} = 0.1\ fF/\mu m$. However, for the proposed device in the ON-state, $C_{GD} = 2.5\ fF/\mu m$ and $C_{GS} = 3.8\ fF/\mu m$. The absence of reverse-biased junction at the source–channel interface and the decrease of effective distance between the drain and the BTBT region can explain the observed behavior. It has been shown that CMOS-type TFET-based digital circuits suffer from the increased delay due to high C_{GD} and Miller effect [7], [38]. Though the total ON-state gate capacitance is similar in both the conventional and the proposed devices, the decreased C_{GD} in the proposed device can ameliorate this problem.

A. SCALING OF GATE LENGTH

Considering the futuristic applications, it is important to analyze the scaling trend of the proposed device. In this section, we find the minimum values of L_{GS} and L_{GD} such that the device characteristics are not affected significantly. Fig. 5(a) and 5(b) show the trend of I_{ON}/I_{OFF} ratio and SS_{avg} of the proposed device with respect to changes in the L_{GS} and L_{GD}, respectively. Fig. 5(a) shows that as the L_{GS} is decreased upto 10 nm, there is no effect on the I_{ON}/I_{OFF} ratio and SS_{avg}. However, as L_{GS} is decreased below 10 nm, the I_{ON}/I_{OFF} ratio decreases by 2 orders and SS_{avg} increases by around 200%. In fact, at $L_{GS} = 10\ nm$ the characteristics of the proposed device is similar to the conventional device. This is expected since with a large reduction in L_{GS}, the distinction between within-channel tunneling and source–channel junction tunneling disappears. Therefore, we choose $L_{GS,min} = 10\ nm$. Similarly, when L_{GD} decreases from 30 nm to 10 nm (keeping $L_{GS} = 10\ nm$), the I_{ON}/I_{OFF} ratio decreases by 6 orders of magnitude and the SS_{avg} increases by 5×, as shown in Fig. 5(b). However, above $L_{GD} = 30$, there is no significant change in the I_{ON}/I_{OFF} ratio and SS_{avg} of the device. Therefore, $L_{GD,min}$ is chosen to be 30 nm. Therefore, $L_{G,min} = L_{GS,min} + L_{GD,minopt} = 40\ nm$ is needed for obtaining within-channel tunneling in the proposed device.

B. FINDING OPTIMUM VALUES OF ϕ_{GS} AND ϕ_{GD}

We have used dual material gate with the workfunctions ϕ_{GS} and ϕ_{GD} in the proposed device. In this section, the optimization of the workfunction for the proposed device is explained. Fig. 6(a) shows that as ϕ_{GS} increases, the I_{ON} increases. Therefore, a high ϕ_{GS} is desirable. However, the increase in ϕ_{GS} above 5.93 eV do not lead to any appreciable improvement in the I_{ON}. Therefore, an optimum ϕ_{GS} is chosen to be 5.93 eV. The corresponding energy band diagram of the device along cutline PP' is shown in Fig. 6(b). It shows that as the ϕ_{GS} increases, the tunneling width decreases and the band overlap increases, resulting in an increase in the BTBT. The gate with $\phi_{GS} = 5.93\ eV$ can be realized using platinum. Furthermore, when ϕ_{GD} is increased, the transfer characteristics shift towards right, as shown in Fig. 7(a). Therefore, $\phi_{GD} = 4.2\ eV$ is chosen such that the take–off point of the transfer characteristics remains at $V_{GS} = 0\ V$. This ensures that the minimum I_{OFF} is obtained. The corresponding band diagram is shown in Fig. 7(b).

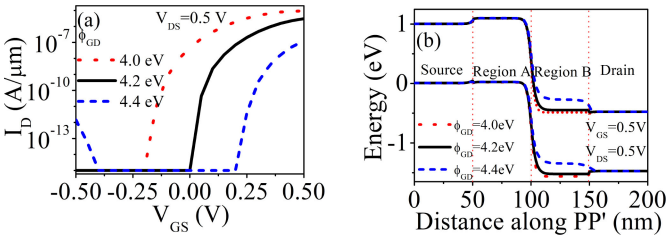

FIGURE 7. (a) Transfer characteristics (b) Energy band diagram of the proposed device keeping $\phi_{GS} = 5.93\ eV$ and varying the ϕ_{GD}.

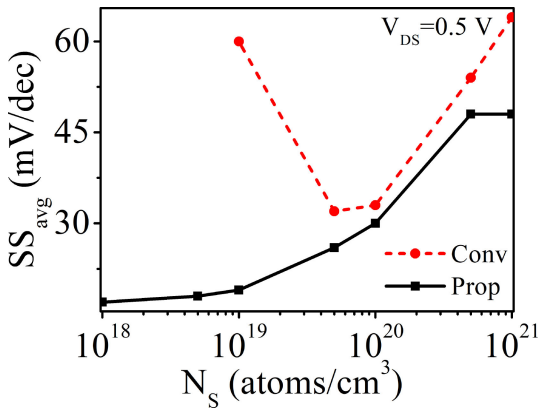

FIGURE 8. SS_{avg} for the conventional and proposed TFET with varying N_S at $V_{DS} = 0.5\ V$.

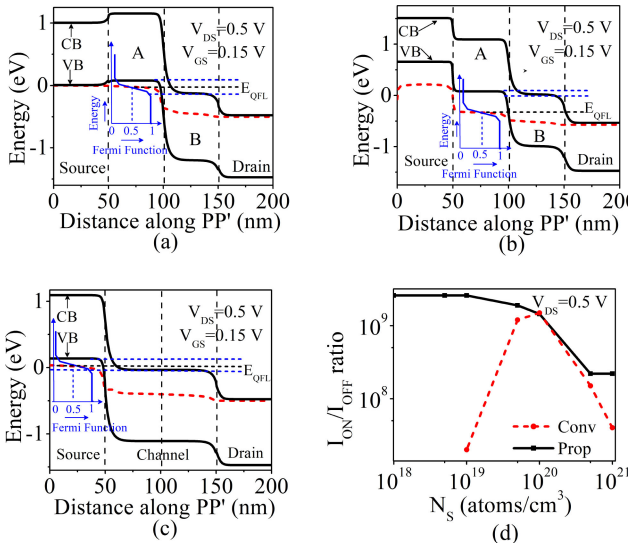

FIGURE 9. Energy band diagram along the cut-line PP' at $V_{GS} = 0.15\ V$ and $V_{DS} = V_{DD}$ (a) For proposed TFET when $N_S = 1 \times 10^{19} atoms/cm^3$ (b) For proposed TFET when $N_S = 1 \times 10^{21} atoms/cm^3$ (c) For conventional TFET when $N_S = 1 \times 10^{20} atoms/cm^3$ (d) I_{ON}/I_{OFF} ratio for the conventional and proposed TFET with varying N_S at $V_{DS} = 0.5\ V$.

C. EFFECT OF SOURCE DOPING CONCENTRATION

Next, we analyze the performance of the proposed device as a function of the source doping concentration. In a conventional TFET, an optimum source doping is shown to achieve a minimum SS_{avg} [5], [8], [41]. Fig. 8 compares the change in the SS_{avg} with the source doping (N_s) for a conventional and the proposed device. It is found that in the conventional device, the lowest SS_{avg} can be obtained in the range $N_S = 5 \times 10^{19} - 1 \times 10^{20} atoms/cm^3$. However, in the proposed device, a much lower SS_{avg} can be achieved for a lower range $N_s = 1 \times 10^{18} - 1 \times 10^{19} atoms/cm^3$. Above this range, the SS_{avg} increases and becomes similar to the SS_{avg} exhibited by the conventional TFET at $N_S = 1 \times 10^{20} atoms/cm^3$.

The above trend for the SS_{avg} can be explained based on the band diagrams when the drain current starts to take-off and the position of quasi-Fermi level (QFL). To obtain a sharp OFF–ON transition or lower subthreshold swing, it is required that the electrons occupying energy levels close to the Fermi level contribute to the BTBT in a TFET [5], [7], [9]. If electrons occupying the tails of the Fermi distribution function contribute to a large extent in BTBT, then an abrupt OFF–ON transition cannot be obtained in a TFET. Fig. 9(a) shows the alignment of the conduction band (CB), valence band (VB) and the electron QFL for $N_S = 1 \times 10^{19} atoms/cm^3$ for the proposed device at $V_{GS} = 0.15\ V$ and $V_{DS} = 0.5\ V$. It can be noted that the electrons with energy close to the QFL in the region A contribute to the tunneling current. Therefore, a sharp transition or lower SS_{avg} is obtained in the proposed device for $N_S = 1 \times 10^{19} atoms/cm^3$. In contrast, when $N_S = 1 \times 10^{21} atoms/cm^3$ in the proposed device, it can be noted from Fig. 9(b) that the electrons having energy much greater than the QFL in region A contribute to the BTBT. Therefore, a gentler transition or higher SS_{avg} is observed in this case.

Next, we show the band alignment for the conventional TFET and the position of the QFL at $N_S = 1 \times 10^{20} atoms/cm^3$, in Fig. 9(c). It can be noted that the electrons with energy close to the QFL in the source contribute to the BTBT. Therefore, a low SS_{avg} is obtained at $N_S = 1 \times 10^{20} atoms/cm^3$ in a conventional TFET. However, it is observed that when $N_S = 1 \times 10^{19} atoms/cm^3$ or $N_S = 1 \times 10^{21} atoms/cm^3$, the electrons with energy away from the QFL contribute to the BTBT. Therefore, in both these cases, a higher SS_{avg} is obtained, in the conventional device, as indicated in Fig 8.

Further, Fig. 9(d), compares the variation in the I_{ON}/I_{OFF} ratio with the source doping (N_S) for a conventional and the proposed device. It is found that in the proposed device, the highest I_{ON}/I_{OFF} ratio can be obtained in the range of $N_S = 1 \times 10^{18} - 1 \times 10^{19}\ atoms/cm^3$. This is in contrast to the conventional device, where the highest I_{ON}/I_{OFF} ratio is obtained in the range $N_S = 5 \times 10^{19}$ - $1 \times 10^{20}\ atoms/cm^3$. Furthermore, at $N_S = 1 \times 10^{20}$, the I_{ON}/I_{OFF} ratio of both the devices is similar.

D. EFFECT OF SOURCE DOPING PROFILE

We have assumed that the source doping profile is abrupt throughout this paper. However, obtaining an abrupt doping profile is challenging. Practically, during ion-implantation, some dopants extend laterally from the source towards the

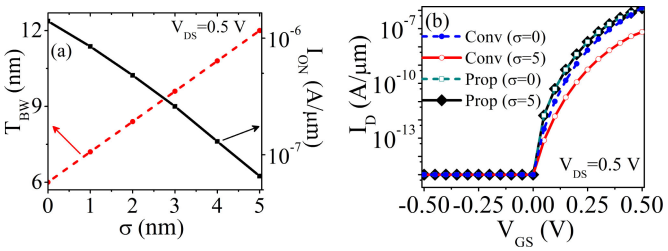

FIGURE 10. (a) T_{BW} and I_{ON} for the conventional and the proposed TFET with varying lateral straggle parameter, σ at $V_{DS} = 0.5\ V$ (b) Transfer characteristics of the conventional and the proposed TFET at $N_S = 1 \times 10^{20} atoms/cm^3$ with $\sigma = 0\ nm$ (abrupt) and $\sigma = 5\ nm$ (non-abrupt) source doping profile.

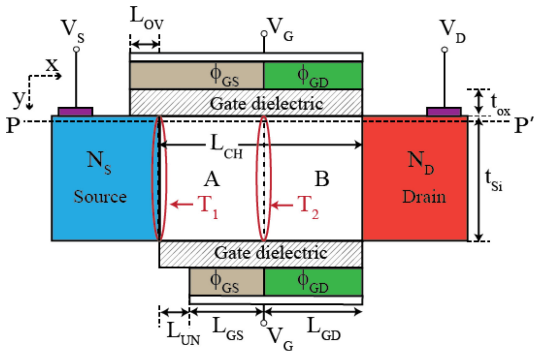

FIGURE 11. Schematic cross-section of the proposed TFET demonstrating gate-underlap or gate-overlap, at the source-channel junction.

channel [42], [43]. Therefore, we examine the electrical characteristics of the devices with the Gaussian source doping profile with lateral straggle (σ) varying between 0 *nm* (abrupt doping) to 5 *nm* keeping the peak doping concentration, $N_S = 1 \times 10^{20} atoms/cm^3$. It is found that when the source doping profile becomes non-abrupt (σ increases), the tunneling barrier width (T_{BW}) increases in the conventional device, as shown in Fig. 10(a). Consequently, the I_{ON} decreases in a conventional device as the doping profile becomes non-abrupt. In contrast, there is no significant effect of the abruptness of the source doping profile on the I_{ON} in the proposed device. This is intuitive since in the proposed device the tunneling is occurring within the channel rather than the source-channel interface. Fig. 10(b) shows the transfer characteristics of the conventional and the proposed device with lateral straggle parameter $\sigma = 0\ nm$ and $\sigma = 5\ nm$. Thus, the proposed device can tolerate the variations in the source doping profile to a greater extent.

E. EFFECT OF SHIFT IN GATE-EDGE WITH RESPECT TO SOURCE-CHANNEL JUNCTION

While fabricating a device, specifically during patterning steps such as lithography, etching, deposition etc., the edges can deviate from the reference straight line, thus resulting in a misalignment of gate-edge to the source-channel junction [44]. This creates an underlap or overlap in the device as shown in Fig. 11 [45]. In this work, we evaluate the sensitivity of I_{ON} and SS_{avg} due to the gate-overlap or gate-underlap, at the source-channel junction. It is found that, in the conventional TFET, for a 10 *nm* overlap ($L_{OV} = 10\ nm$), the I_{ON} can decrease by 65.8% and the SS_{avg} can increase by 1.14× with respect to the nominal value ($L_{OV} = 0$), as shown in Fig. 12(a) and 12(b), respectively. Similarly, for a 10 *nm* underlap ($L_{UN} = 10\ nm$), the I_{ON} can decrease by 97% and the SS_{avg} can increase by 4× with respect to the nominal value ($L_{UN} = 0$), as shown in Fig. 13(a) and 13(b), respectively. This degradation is expected since, in the conventional TFET, BTBT occurs at the source-channel edge and a shift of the gate-edge leads to a change in the tunneling barrier width and the resultant BTBT current. On the other hand, when a TFET utilizes within-channel tunneling, the underlap and

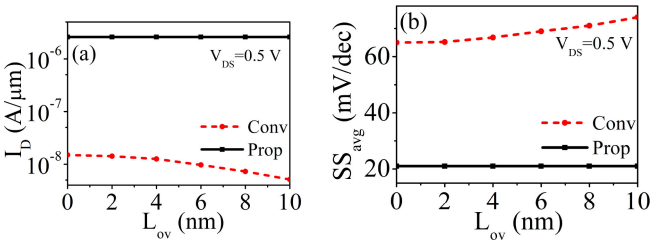

FIGURE 12. (a) I_{ON} (b) SS_{avg} for the conventional and proposed TFET with varying L_{OV} ($L_{UN} = 0$) at $V_{DS} = 0.5\ V$.

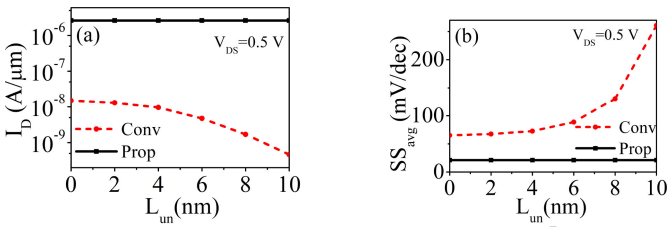

FIGURE 13. (a) I_{ON} (b) SS_{avg} for the conventional and proposed TFET with varying L_{UN} ($L_{OV} = 0$) at $V_{DS} = 0.5\ V$.

overlap of gates do not impact the electrical characteristics of the device as shown in Fig. 12 and 13. This is expected because in the proposed device, tunneling does not occur at the source–channel junction and, therefore, the BTBT is not affected by the underlap and the overlap of gates.

F. EFFECT OF WORK-FUNCTION VARIATIONS

TFETs are shown to be susceptible to work-function variations (WFV) [45], [46]. In general, a gate electrode consists of multiple crystalline grains, each having a different work-function. These grain orientations can lead to different effective work-function of a gate metal [46], [47]. For instance, the work-function for Tantalum nitride can vary from 4.0 *eV* to 4.8 *eV* depending on the grain orientation [45]. In general, to assess the impact of WFV, random grain orientation and statistical analysis is required [45]. In this work, to assess the impact of the WFV on the electrical characteristics of a TFET in a simplistic manner, we take a work-function variation of

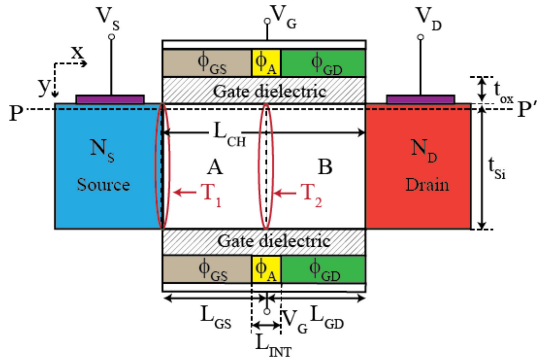

FIGURE 14. Schematic cross-section of the proposed TFET with averaged work-function ϕ_A at the DMG interface.

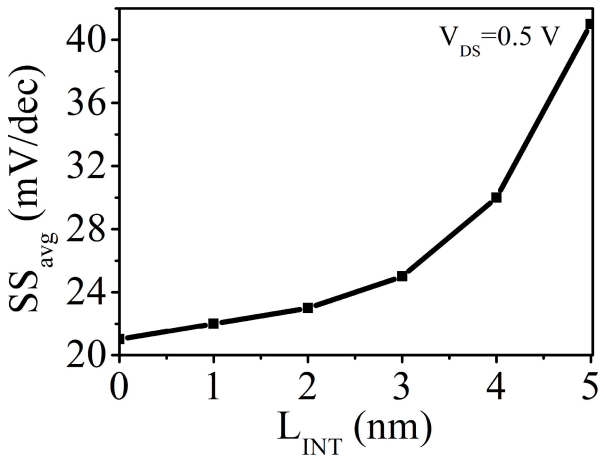

FIGURE 15. SS_{avg} for the proposed TFET with varying L_{INT} at $V_{DS} = 0.5\ V$.

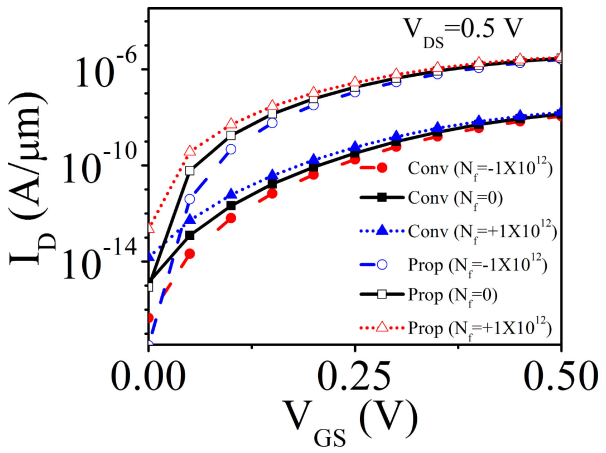

FIGURE 16. Transfer characteristics of the conventional and proposed TFET for acceptor, donor, and no ITCs.

$\pm 0.1\ eV$ around the nominal value [48]. In the conventional TFET, a change in gate work-function leads to a lateral shift in the transfer characteristics. As a result, with a uniform $\pm 0.1\ eV$ change in the gate work-function, the I_{ON} changes by $3\times$ and the SS_{avg} is not affected. It is worthy to point out that, if high work-function grains are concentrated near the source and the low work-function grains are concentrated next to them, the SS_{avg} can also exhibit degradation in a conventional TFET [46].

In the proposed device, since the BTBT occurs at the abrupt tunnel junction created at the interface of the work-function ϕ_{GS} and ϕ_{GD}, it is expected that the proposed device will be susceptible to the WFV. To quantify the variations, we have varied the work-functions of both ϕ_{GS} and ϕ_{GD} by $\pm 0.1\ eV$. The worst case degradation in the I_{ON} and the SS_{avg} is noticed when the ϕ_{GS} is decreased by $0.1\ eV$ and the ϕ_{GD} is increased by $0.1\ eV$, simultaneously. In this case, the I_{ON} decreases by $6\times$ and the SS_{avg} degrades by 17%. Therefore, in the proposed device, techniques such as amorphization should be employed to reduce the impact of WFV [46].

Furthermore, in the proposed device, since tunneling occurs at the interface of the two work-functions, the interface needs to be sharp. Due to process-induced variations, it can be difficult to obtain a sharp 5.93–4.2 eV interface for DMG [16], [22]. Therefore, we examine the proposed device by keeping the work-function $\phi_A = 5.0\ eV$ (average of $5.93\ eV$ and $4.2\ eV$) at the A-B interface for a length (L_{INT}) of $2\ nm$, $3\ nm$, $4\ nm$ and $5\ nm$ (beyond this length the work-function is taken as $5.93\ eV$ and $4.2\ eV$) as shown in Fig. 14. Our simulations reveal that in the proposed device, the SS_{avg} degrades from $21\ mV/dec$ to $40\ mV/dec$, as L_{INT} vary from $0\ nm$ to $5\ nm$, as shown in Fig. 15. Thus, if the DMG interface is not sharp, then the abruptness of switching reduces to some extent. Therefore, the techniques for fabricating a good DMG interface are important.

G. EFFECT OF INTERFACE TRAP CHARGES

In this section, we analyze the impact of the interface trap charges (ITCs) on the device performance. The ITCs can be process-induced, radiation-induced, or stress-induced. The ITCs can decrease device reliability and lifetime [49], [50]. Therefore, it is important to assess the impact of ITCs on device performance. The interface charges can be positive (donor) ITCs or negative (acceptor) ITCs. In this work, we have considered the density of these charges as $N_f = \pm 10^{12} cm^{-2} eV^{-1}$. This value is chosen based on various experimental observations and simulation studies that have considered the trap density of $\pm 10^{11} - \pm 10^{13} cm^{-2} eV^{-1}$ [51]–[53]. To include the ITCs in our simulations, we have used the INTERFACE statement in ATLAS, which considers the density of interface fixed charges at the silicon-oxide interface [27].

Fig. 16 compares the transfer characteristics of the conventional and the proposed devices in the presence of the ITCs. It can be seen that presence of negative (acceptor) ITCs do not result in degradation in the device performance as far as electrostatic performance is concerned. However, the positive (donor) ITCs result in a higher I_{OFF} in both the devices, resulting in a lower I_{ON}/I_{OFF} ratio. The I_{ON}/I_{OFF} ratio degrades from 2×10^7 to 1×10^6 in the conventional device and

from 2.6×10^9 to 1.4×10^7 in the proposed device. Further, it is important to point out that the location of the traps is also critical in the device. The presence of the interface traps around the source is more harmful to the device performance in the conventional device. However, the presence of the traps around the DMG interface is more harmful to the proposed device. This is expected since the electric field and BTBT is maximum at the source–channel interface in the conventional device and, at the DMG interface in the proposed device. Furthermore, it is important to mention that we have only considered electrostatic degradation due to ITCs. The bulk trap states and trap assisted tunneling (TAT) can also degrade device performance. Therefore, a more in-depth analysis involving bulk traps and TAT is required to truly assess the impact of traps on DMG-TFETs.

IV. CONCLUSION

In this paper, we have proposed to exploit within-channel tunneling using DMG and reported novel attributes of the proposed device. Though we have demonstrated the technique of exploiting within-channel tunneling in a silicon-based TFET, with proper device optimization, the concept can be extended to TFETs based on other materials as well. Due to the inherent lateral electric field, a strong gate control over the BTBT region and the shift of BTBT region towards the drain, some of the electrical characteristics improve compared to a conventional TFET. We have also demonstrated that within-channel tunneling can be exploited for channel lengths of 40 *nm* and above. Additionally, it is demonstrated that the proposed TFET is immune to variations in source doping concentration and gate-edge shift at the source-channel interface. However, the impact of work-function variations and interface trap charges in the proposed device is important and needs to be tackled.

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