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Straintronics: Digital and Analog Electronics With Strain-Switched Nanomagnets

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ABSTRACT The search for a binary switch that is more energy-efficient than a transistor has led to many ideas, notable among which is the notion of using a nanomagnet with two stable magnetization orientations that will encode the binary bits 0 and 1. The nanomagnet is switched between them with electrically generated mechanical strain. A tiny amount of voltage is required for switching, with energy dissipation on the order of a few to few tens of aJ. Logic gates and memory, predicated on this technology, have been demonstrated in our group. While they indeed dissipate very little energy, they are unfortunately plagued by unacceptably high switching error probability that hinders their application in most types of Boolean logic. Fortunately, they can still be used in applications that are more forgiving of switching errors, e.g. probabilistic computing, analog arithmetic circuits, belief networks, artificial neurons, restricted Boltzmann machines, image processing, and others where the collective activity of many devices acting cooperatively elicit the computing or signal processing function and the failure of a single or few devices does not matter critically. These ultra-energy-efficient strain-switched nanomagnets can also be used for non-computing devices such as microwave oscillators that perform better than spin-torque-nano-oscillators. This short review provides an introduction to this exciting burgeoning field.

INDEX TERMS Straintronics, nanomagnets, non-Boolean computing, energy-efficient information processing.

I. INTRODUCTION

Most practitioners of electrical engineering are familiar with how an electronic switch implemented with the celebrated metal-oxide-semiconductor field effect transistor (MOSFET) works. When charge carriers (electrons in an n-channel MOSFET and holes in a p-channel MOSFET) flood into the transistor's channel region, the device switches on because a conducting path is established between the source and the drain contacts. When these charge carriers are expelled from the channel, the conducting path is disrupted and the transistor switches off. This is shown in Fig. 1. The high-conductance (ON) and low-conductance (OFF) states of the transistor encode the two binary bits 0 and 1. In the case of an n-channel MOSFET, a positive voltage applied to the gate terminal sitting on top of the channel will pull electrons into the channel from the source and drain contacts by Coulomb attraction and turn the n-MOSFET on. Similarly, a negative gate voltage will repel the channel electrons, sending them back to the source and drain contacts, and turn the n-MOSFET off. The opposite situation will hold for a p-MOSFET. The MOSFET thus works primarily on the basis of Coulomb interaction.

What is important to note is that the two states ON and OFF are demarcated by the amount of electrical charge stored in the channel. A larger amount of channel charge Q_1 represents the ON-state and a smaller amount of charge Q_2 represents the OFF-state. This principle is true of any charge-based switch, not just the transistor. After all, charge is a *scalar* quantity and has only "magnitude" and no "direction". Therefore, if we wish to encode binary bits in charge, we must do so using two different magnitudes (or amounts) of charge. Every time we switch a charge based device, we must move charge into or out of the device to change the amount of charge from Q_1 to Q_2, or vice versa. This will invariably cause the flow of a (time-averaged) current given by

$$I = |Q_1 - Q_2| / \Delta t = \Delta Q / \Delta t, \tag{1}$$

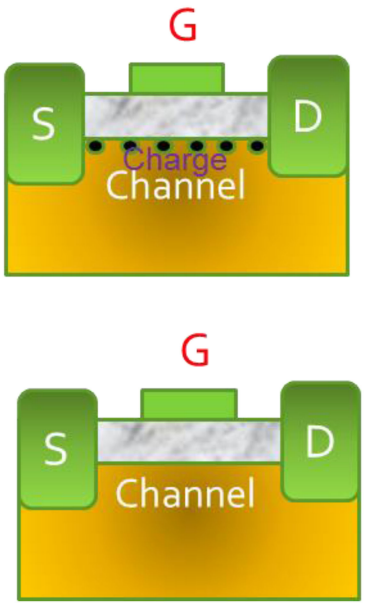

FIGURE 1. Basic working principle of a MOSFET. S = source contact, D = drain contact and G = gate contact. The transistor is on when charges reside in the channel and off when charges are expelled from the channel.

where Δt is the amount of time it takes to change the channel charge from Q_1 to Q_2, or vice versa. This will then cause energy dissipation of the amount

$$E_d = I^2 R \Delta t = (\Delta Q/\Delta t)\, IR \Delta t = \Delta Q I R = \Delta Q \Delta V, \quad (2)$$

where R is the resistance in the path of the current and $\Delta V = IR$. We can think of ΔV as the amount of voltage needed to be imposed at the gate to change the charge in the channel by the amount ΔQ. Note that the energy dissipation given in Equation (2) is *not* independent of the switching time, because ΔV depends on the switching time for a fixed ΔQ and $R(\Delta V = \Delta Q R/\Delta t)$. We can actually write the energy dissipation in Equation (2) also as $E_d = (\Delta Q)^2 R/\Delta t$, which clearly shows that we will dissipate *more* energy if we switch *faster* (smaller Δt). Therefore, a more meaningful quantity to benchmark a device may be the energy-delay product which is $E_d \Delta t = (\Delta Q)^2 R$. We might think that we can reduce this quantity by reducing ΔQ, but that is not always possible since we need to be able to distinguish between bits 0 and 1. That needs ΔQ to be sufficiently large, especially when operating in a noisy environment. The other alternative is to reduce R by increasing the cross-section of the current path. However, that runs counter to the notion of miniaturization and device down-scaling (in size), and therefore not really practical. Therefore, we are stuck with a minimum amount of energy delay product that we must tolerate as long as we work with a charge-based device.

The obvious question at this point is why do we care about energy dissipation or the energy-delay product? This is best answered by considering a modern day MOSFET (or FINFET which is an advanced avatar of the MOSFET). The Intel Core^{TM} i7-6700K processor released in 2015 uses 14-nm scale FINFETs, operates with a power supply voltage of 1.2 V and clock frequency of 4 GHz, while dissipating 91 W of power. It has roughly 1.75 billion transistors, which dissipate the bulk of the power, and about 10% of them switch at any given time during the chip's operation (i.e. the so-called "activity level" is 10%). We can therefore estimate the average energy dissipation per transistor as

$$E_d^{\text{FINFET}} = P_d/(Naf) = 91/\left(1.75 \times 10^9 \times 0.1 \times 4 \times 10^9\right) = 130 \text{ aJ}, \quad (3)$$

where P_d is the power dissipation, N is the number of transistors in the chip, a is the activity level and f is the clock frequency.

Fast forward to the year 2025 when we should have more than 40 billion transistors on a chip if we could keep pace with Moore's law [1]. We would also like the clock frequency to increase to at least 10 GHz by then. Assuming that the transistor still dissipates 130 aJ to switch, the power that we would be dissipating (see Equation (3)) would become 5.2 kW! This could very well overwhelm thermal management in the chip and require exotic heat sinking technologies that would not be cost-effective. It is a very serious menace and is the reason why we care about energy dissipation (or energy-delay product) in a switch.

We will try to conclude this section by trying to estimate what is the minimum energy that a FINFET type device could dissipate while still being operational. The FINFET of circa 2015 dissipates 130 aJ while working with a voltage supply of 1.2 V. Hence, from Equation (2), the amount of charge that is moved in the channel of the FINFET to switch it on and off is roughly

$$\Delta Q = E_d/\Delta V = 130 \times 10^{-18}/1.2 = 1.08 \times 10^{-16} \text{Coulombs}, \quad (4)$$

which is the charge carried by a mere 673 electrons or holes. Thus, only ~**670** charge carriers are moved in a transistor of 2015 vintage to switch it on or off. Obviously, the number of charge carriers must greatly exceed the number that can spontaneously appear in the channel due to noise and thermal fluctuations. The latter is the charge fluctuation in the transistor's "gate" and is given by [2]

$$\Delta Q|_{\text{fluctuation}} = \sqrt{C_g kT}, \quad (5)$$

where C_g is the gate capacitance, k is the Boltzmann constant and T is the absolute temperature. The gate capacitance for the FINFET structure can be estimated roughly as (this includes contributions of line capacitance, etc.)

$$C_g = \Delta Q/\Delta V = 1.08 \times 10^{-16}/1.2 = 90 \text{ aF}, \quad (6)$$

which makes $\Delta Q|_{\text{fluctuation}} = 6.45 \times 10^{-19}$ Coulombs at room temperature, and that is the charge of only ~4 charge carriers.

The minimum amount of ΔQ that we will need to move through the switch in order to be able to distinguish between the bits (i.e. the ON and OFF states) and switch reliably should

be considerably larger than $\Delta Q|_{\text{fluctuation}}$ and let us say that it is $\Delta Q_{\min} = \xi \Delta Q|_{\text{fluctuation}}$, where we can interpret ξ as a measure of the reliability of switching. In that case, the minimum energy that we must dissipate to switch a FINFEET/MOSFET type device will be

$$E_d^{\min} = \Delta Q_{\min} \Delta V_{\min} = (\Delta Q_{\min})^2 / C_g$$
$$= \xi^2 (\Delta Q|_{\text{fluctuation}})^2 / C_g = \xi^2 kT. \quad (7)$$

Equation (7) is very instructive. It tells us that the minimum energy that we must dissipate is determined by the minimum reliability that we are able to tolerate. There is a trade-off between energy dissipation and reliability; we can buy energy efficiency at the cost of reliability and vice versa. In other words, there is never any free lunch. It turns out that this general principle also holds for magnetic devices that we will discuss next.

II. MAGNETIC SWITCHES

We have seen so far that charge-based devices encode binary bit information in two different amounts (or magnitudes) of charge in the device. Hence switching such a device invariably involves moving charge in or out of the device with an accompanying current flow and energy dissipation. Instead of encoding information (binary bit value) in the charge degree of freedom of one or more electrons, we could also perhaps encode it in their quantum mechanical *spin degree of freedom*. Classically, we can think of *spin* as a tiny magnetic moment attached to the electron, which has a fixed magnitude $\hbar/2$($\hbar$ = reduced Planck's constant) of but a variable direction. We can therefore think of it as a quasi-vector whose magnitude is invariable, but whose direction is not. If we place an electron in a magnetic field, then the spin can point either parallel to the field or anti-parallel to it, since these are the only two allowed quantum mechanical eigenstates (other orientations are neither stable nor metastable). These two states are not degenerate in energy; one of them will be higher in potential energy than the other, but that is not consequential for what we will be discussing. The two spin orientations could encode the binary bits 0 and 1. Switching a bit will simply involve flipping the spin direction, *without having to physically move the electron in space and causing a current flow* (with its associated energy dissipation). Of course, some energy will have to be dissipated to flip the spin, but it could be far less than the energy dissipation associated with charge movement or current flow. The spin-based approach and the charge-based approach are contrasted in Fig. 2.

The idea of encoding binary bits in single electron spin orientations, with each electron housed in a semiconductor quantum dot, and then utilizing spin-spin (exchange) interactions between these single-spin-switches to fashion universal Boolean logic gates, and ultimately combinatorial and sequential logic circuits, was first proposed in the mid-1990s and extensively explored for about a decade [3]–[6]. In many ways, this is the progenitor of spin-based quantum gates [7]–[10], which later lead to the idea of universal single-spin based

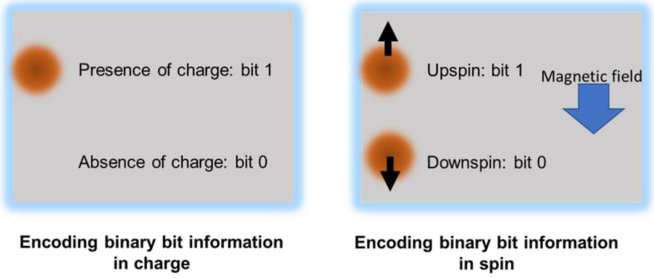

FIGURE 2. Encoding bit information in charge and spin.

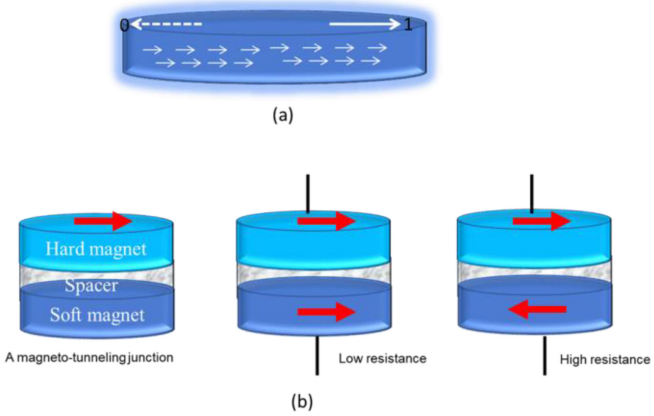

FIGURE 3. (a) A single domain nanomagnet whose magnetization orientation encodes a binary bit. (b) A magneto-tunneling junction whose resistance allows one to determine the magnetization orientation of the soft nanomagnet which stores the bit. This allows reading of the stored bit.

quantum gates [11]. The drawback of a single-spin bit is that it is extremely fragile since small unavoidable perturbations can easily flip a spin and destroy bit information. Additionally, single-spin-logic gates rely on spin-spin (exchange) interactions which decay rapidly with increasing separation between two neighboring spins. For reasonable separations that are achievable with current technology, the interactions are so weak that the logic gates must operate at sub-K temperature for stability and reliability. There are, however, some claims that in graphene nanoflakes, the interactions can be strong enough that even room temperature operation can be contemplated [12]. This is a fascinating area of research in its own right, but more "practical" approaches are currently available and they involve executing Boolean logic operations with *nanomagnets* which contain not a single spin, but about 10^4 spins. Nanomagnets are far more stable than single spins and share some of the advantages of single spin logic, especially when the nanomagnet is composed of a single ferromagnetic domain. They also work quite well at room temperature and do not need cryogenic operation.

Fig. 3(a) shows a nanoscale ferromagnet shaped like a thin elliptical disk. If its volume is small enough (but not so small that it behaves like a super-paramagnet, instead of a ferromagnet, at the operating temperature) and the eccentricity

of the ellipse is large enough, then this entity behaves as a *single-domain nanomagnet* whose magnetization can point only along the major axis – either pointing to the right or to the left – and these two magnetization orientations encode the binary bits 0 and 1. Typically, this would require the nanomagnet's lateral dimension to be between 50 and 100 nm and the thickness less than 10 nm. There may be $\sim 10^4$ electron spins in this nanomagnet, but because of exchange interaction among them, they will always all *point in the same direction*. If we flip the magnetization from right to left, or vice versa, *all* the 10^4 spins will rotate together in unison, thus acting like one giant classical spin [13]. Unlike in a charge-based device like the MOSFET, where N different charge carriers in the channel will act independently like N different degrees of freedom, here all the N spins act collectively like a *single* degree of freedom. This can reduce energy dissipation during the switching action dramatically [14]. Note that there is no need for any current to flow through the nanomagnet in order to flip its magnetization, and hence there is no unavoidable dissipation associated with current flow. Of course, there will be some dissipation associated with the flipping action and that may or may not involve some current flow external to the nanomagnet, but whether that dissipation is larger or smaller than the dissipation incurred in a comparable charge-based device (with inevitable current flow through the device) depends on how the flipping is accomplished. We will discuss that shortly, but prior to that, we will discuss a few other items.

Note a very significant advantage of the nanomagnet switch, namely that it is *non-volatile*. If we left a MOSFET in the high conductance state and switched the power off, the channel charges will drain out with time rather quickly and the bit information will be lost very soon. In contrast, if we left the nanomagnet with its magnetization oriented, say, to the left, then it will persist in that state for centuries or decades after all power is turned off. This feature can not only be exploited to build non-volatile memory (which is obvious), but it can also be utilized for non-von-Neumann data processing architectures and several other non-traditional circuitry that may eclipse their more conventional counterparts in many applications such as Bayesian inference engines for computing in the presence of uncertainty [15], [16], content addressable memory [17], [18], machine learning [19], belief networks [20], etc. In a von-Neumann architecture, the processor and memory are two physically separate units and there is a partition between them. Data will flow back and forth between them via a "switch". The processor is made of volatile elements and hence cannot store instruction sets. The instructions are stored in memory and have to be fetched to the processor for execution. This makes the computer less reliable and slow. In fact, this is responsible for the boot delay. However, if the instruction sets can be stored *in-situ* in the processors that are made of non-volatile elements, then the communication between the processor and memory is obviated. In that case, it may be possible to realize instant-on computers (like a television set) with no boot delay at all! It is the possibility of such features in non-von-Neumann architectures that has stimulated much of the interest in non-volatile logic.

Reading of a bit encoded in a nanomagnetic switch's magnetization orientation: How does one read the magnetization of a nanomagnet *electrically* to read the stored bit? This is done with a construct known as a "magneto-tunneling junction (MTJ)" shown in Fig. 3(b). This device has three layers – a "soft" ferromagnetic layer, an insulating spacer, and a "hard" ferromagnetic layer – all of nanometer dimensions vertically and few tens of nanometers laterally. The magnetization of the last layer is made "hard" or stiff, usually by using various material combinations, so that it remains always fixed and pointing in one pre-determined direction along the major axis of the elliptical hard layer. The soft layer's magnetization is much more pliable and can be flipped with an external agent. When the magnetizations of the hard and soft layers are mutually parallel, the electrical resistance of the MTJ (measured between the hard and the soft layers) is small because of spin-dependent tunneling of electrons from the hard layer to the soft, or vice versa. When the two magnetizations are anti-parallel, the resistance is high. Therefore, by measuring the resistance and knowing the magnetization of the hard layer (which is invariant), we can tell in which direction the magnetization of the soft layer is pointing. Since the soft layer's magnetization encodes the bit, by measuring the MTJ's resistance, we can effectively "read" the stored bit. Fig. 3(b) illustrates this modality. Just as the high-conductance state of a MOSFET encodes one bit and the low-conductance state the other, similarly the high-conductance state of the MTJ encodes one bit and the low-conductance state the other. The difference is that the conductance state of the MOSFET is volatile, whereas the conductance state of the MTJ is not. Additionally, one may be able to switch the conductance state of the MTJ (and hence "write" a bit state) while dissipating much less energy than would be dissipated in switching the conductance state of (and writing a bit in) a MOSFET. On the flip side, the disadvantage is that the conductance on/off ratio for an MTJ is much smaller than that of a MOSFET and that may preclude certain applications for the MTJ.

Switching a nanomagnet's magnetization orientation and writing a bit: The magnetization of a nanomagnet (used as the soft layer of an MTJ) can be flipped (or aligned along a specific direction along its major axis) in many ways. The obvious way would be to use a local magnetic field directed along the desired orientation. However, it is very difficult to localize a magnetic field to an individual nanomagnet and even if that could be done, it takes a considerable amount of current to produce the required magnetic field. Therefore, this would be a very energy-inefficient approach. A better approach is to switch by passing a spin-polarized current through the soft nanomagnet, which will allow us to address individual nanomagnets easily. For example, if we connected a battery across the MTJ, with the battery's negative pole connected to the hard layer, then electrons would be injected from the hard layer into the soft layer. These electrons will have their spins

mostly pointing in the direction of the hard layer's magnetization. They will then transfer their angular momenta to the resident spins in the soft layer and turn them in the direction of the hard layer's magnetization. This will ultimately make the magnetization of the soft layer parallel to that of the hard layer and enforce the high-conductance state, thereby writing bit information (say bit 0). In order to write the complementary bit (bit 1), we have to make the magnetization of the soft layer antiparallel to that of the hard layer so the low-conductance state is reached. To do this, we simply reverse the polarity of the battery, connecting the negative terminal to the soft layer. Electrons then exit the soft layer through the hard layer, but because of spin-dependent tunneling through the spacer, those electrons whose spins are pointing in the direction of the hard layer's magnetization exit preferentially. This action depletes the soft layer of those spins, as a result of which the majority of the spins in the soft layer ultimately point in the direction opposite to the magnetization of the hard layer. At that point, the magnetizations of the two layers become mutually antiparallel and the low-conductance state is attained, which then writes the complementary bit 1. This switching mechanism is termed *spin-transfer-torque* (STT) [21] and is utilized in spin transfer torque random access memory (STT-RAM), which is becoming increasingly commonplace because of its excellent endurance and high density.

A variant of this mechanism is called *spin-orbit-torque* (SOT) [22], where a charge current is passed through a heavy metal layer that the soft layer of the MTJ is in contact with. The charge current injects a spin current into the soft layer (the spin orientation depends on the direction of charge current) by virtue of an effect known as the spin Hall effect [23]–[25] and this spin current orients the magnetization of the soft layer along one of the two stable directions, thereby writing the bit. The SOT is usually more energy-efficient than the STT, but since it results in a 3-terminal memory as opposed to a 2-terminal one, it is less preferred because it reduces memory density.

In our group, we have worked on a different modality of switching, which we had termed "straintronics". The idea is to use a *magnetostrictive* soft layer that is in elastic contact with an underlying (poled) piezoelectric film. This system makes up a "two-phase multiferroic". Application of a voltage over the piezoelectric film with electrodes delineated on the film generates biaxial strain in it, which, depending on the disposition of the electrodes and the voltage polarity, will generate either tensile strain along the major axis of the elliptical soft layer and compressive strain along the minor axis, or vice versa [26]. As long as the product $\lambda_s \varepsilon$ (λ_s = saturation magnetostriction of the soft layer, ε = strain along the major axis) is negative, the magnetization of the soft layer will turn away from the major axis and rotate towards the minor axis. If, *as soon as* the 90^0 rotation is completed and the magnetization aligns along the minor axis, the strain is withdrawn, then the magnetization will continue to rotate further under an inertial torque and complete 180^0 rotation or full reversal [27]. This is shown in Fig. 4(a). Therefore, in order to write a desired

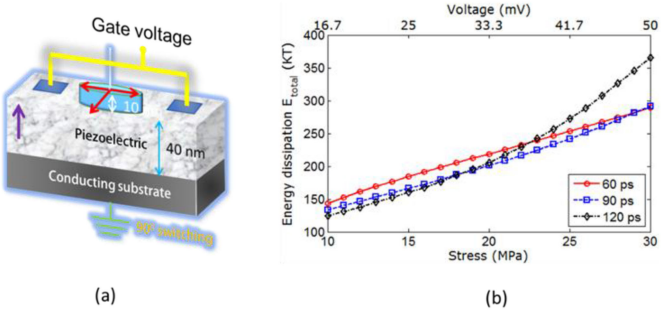

FIGURE 4. (a) Flipping the magnetization of a magnetostrictive elliptical nanomagnet, elastically coupled to an underlying vertically poled piezoelectric film, with a precisely timed strain pulse generated with the gate voltage. (b) Calculated energy dissipation as a function of the stress (and the corresponding gate voltage needed to generate the required stress) for three different stress ramp times (60, 90, 120 ps). Reproduced from [28] with permission of the American Institute of Physics.

bit, we will first read the already stored bit. If it is the same as the desired bit, we will do nothing. Otherwise, we will flip the magnetization as just described and this will write the desired bit. This kind of memory is called "toggle memory" since all we can do is toggle the magnetization. As a result, it is always necessary to read the bit first and then take (or not take) action. STT-RAM, on the other hand, is non-toggle memory where the write action does not have to be preceded by a read action. We can always write the desired bit by choosing the correct polarity of the voltage source, regardless of the bit already stored. There are non-toggle versions of straintronic memory as well, but we will not discuss them here.

Fig. 4(b) shows the calculated energy dissipation (incurred during switching) as a function of the stress (and the voltage needed to generate the stress) for the structure shown in Fig. 4(a) where the nanomagnet is assumed to be made of the highly magnetostrictive alloy Terfenol-D and has a thickness of 10 nm, while the piezoelectric is lead zirconium titanate (PZT) of 40 nm thickness [28]. The switching is accomplished in less than 1 ns and the energy dissipation is less than 1 aJ [28].

One serious problem with this approach is that timing the stress pulse accurately is a challenge. Because of thermal noise, there is a spread in the time it takes for the magnetization to complete the 90^0 rotation, which makes it difficult to time the stress/strain pulse precisely. A better strategy is to apply two uniaxial stresses in two different directions sequentially and that can complete the 180^0 rotation in steps [29]. This latter strategy has been demonstrated experimentally [30] (see Fig. 5).

III. NON-BOOLEAN STRAINTRONIC DEVICES AND SYSTEMS

It has been observed both experimentally [31], [33] and theoretically [34], [35] that strain, albeit energy-efficient, does not switch nanomagnets reliably, especially real nanomagnets that contain defects. This is the most serious drawback

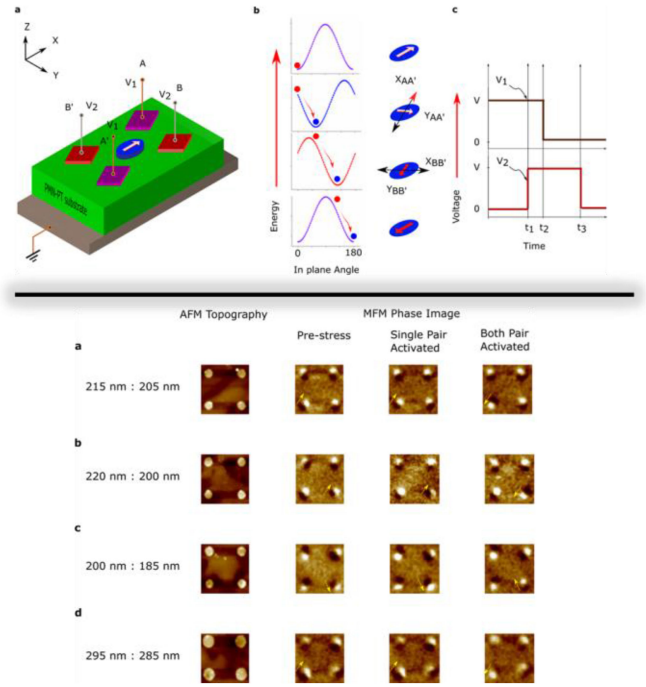

FIGURE 5. **(Top panel) a. Arrangement for applying uniaxial stresses to the elliptical nanomagnet in two different directions (neither collinear with a principal axis) by sequentially activating the electrode pairs AA′ and BB′. b. Potential energy profile of the nanomagnet as a function of the angle subtended by the magnetization with the major axis (direction of the arrow shown) - with no electrode activated, only AA′ activated, BB′ activated and AA′ de-activated, and all electrodes de-activated. c. Timing sequence of the voltage V_1 applied to electrode pair AA′ and V_2 applied to electrode pair BB′. (Bottom panel). Atomic and magnetic force micrographs of four different sets of nanomagnet assemblies (with different major and minor axes dimensions) subjected to this stress sequence. The magnetic force micrographs are shown at three different stages of electrode activation. One out of four nanomagnets flip completely (180^0 rotation) upon completion of the stress cycle. Reproduced from [30].**

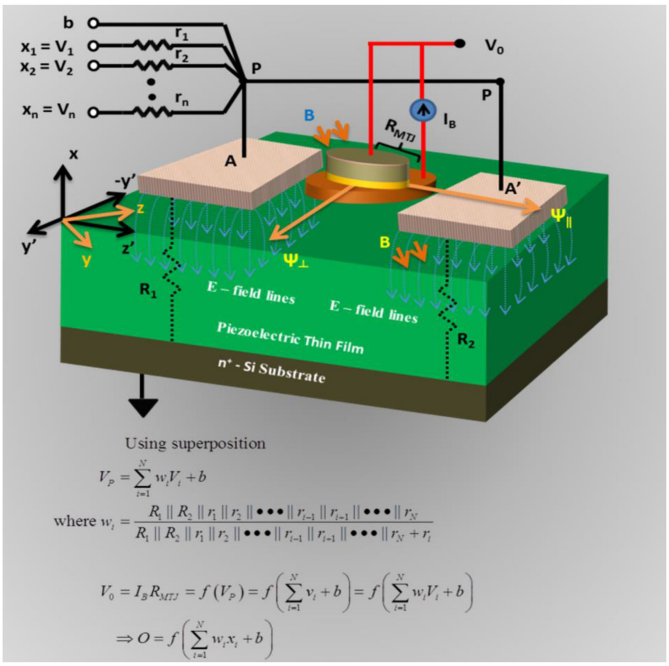

FIGURE 6. **A threshold neuron (with resistive synapses) implemented with a straintronic magneto-tunneling junction. Reproduced from [39] with permission of the Institute of Physics.**

of magneto-elastic switching which is at the heart of straintronics. Otherwise, straintronics would have been extremely attractive because of its unprecedented energy-efficiency. The switching error probability, i.e. the probability of not switching under stress, is so high in real nanomagnets that straintronics may not be viable for Boolean logic which has stringent requirements for error tolerance (the maximum tolerable error probability for a single majority logic gate to operate was shown by von Neumann to be 0.0073 in 1956 [36], and in a modern-day logic chip, the switching error probability of a single switch will probably have to be no more than 10^{-15} [37]). This is a bridge too far for straintronics. Consequently, attention has focused on non-Boolean applications, such as neurons and synapses for neuromorphic computation, analog arithmetic operators (adders, subtractors, multipliers and dividers), content addressable memory, belief networks, machine learning, and even applications that are far removed from computing, such as microwave sources and extreme sub-wavelength antennas. These applications are relatively error-tolerant and can benefit from the low switching energy dissipation and other attributes that are peculiar to straintronic switching.

Fig. 6 shows a threshold neuron implemented with a "skewed" straintronic magneto-tunneling junction (ss-MTJ) whose hard and soft layers do not have their major axes mutually parallel (hence "skewed"). Straintronic MTJs have been demonstrated experimentally [38] and making them "skewed" merely requires tweaking the hard layer growth process slightly. The soft layer is magnetostrictive and in elastic contact with the underlying piezoelectric film. The two contact pads, A and A', are electrically shorted and the voltage dropped between them and the ground terminal generates strain in the piezoelectric which is partially or wholly transferred to the soft layer and makes its magnetization rotate. The output of the neuron (the output voltage V_0 dropped over the ss-MTJ) is a non-linear (threshold) function of the weighted sum of the input voltages. The details of operation can be found in [39]. This is a very low energy neuron and therefore attractive for many applications. In the celebrated chess match between Garry Kasparov and IBM's Deep Blue supercomputer that took place in 1996, the computer won, but it dissipated several kW of power during the match, while Kasparov's brain dissipated a mere ∼20 W. In order to successfully mimic human cognition and learning, neural networks have to be energy-efficient (among other things) and straintronic neurons are a promising step in that direction.

Fig. 7 shows a microwave oscillator realized with a straintronic MTJ. Because of complex interactions between three agents – (1) the stress anisotropy energy generated in the

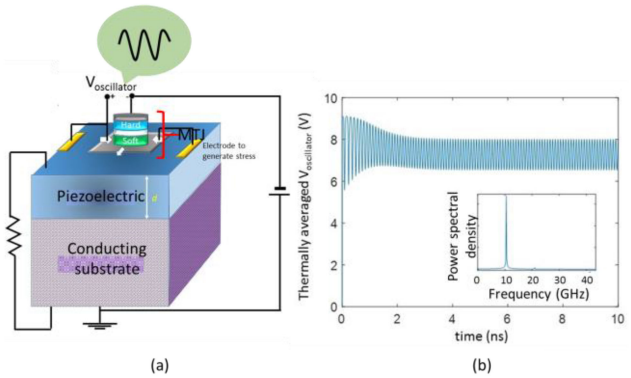

FIGURE 7. (a) Schematic of a microwave oscillator implemented with a straintronic magneto-tunneling junction (MTJ). (b) Calculated oscillations in the voltage dropped over the MTJ. The inset shows the fast Fourier transform of the calculated oscillations. Reproduced from [40] with permission of the American Physical Society.

soft layer by the potential dropped over the piezoelectric film owing to the voltage source, (2) the spin transfer torque caused by the current injected into the soft layer by the same voltage source, and (3) dipole interaction between the hard and soft layers, the magnetization of the soft layer oscillates in time if these interactions are carefully engineered, making the MTJ resistance also oscillate in time. The latter oscillation results in an oscillating voltage across the MTJ which oscillates at microwave frequencies. The details can be found in [40]. This type of oscillator is spectrally pure (almost a single output frequency with high quality factor) and has better spectral quality than spin torque nano oscillators. They can find applications in neuromorphic computing [41] and microwave assisted writing in memory [42].

IV. CONCLUSION

In this review article, I have attempted to provide a glimpse of the exciting world of "straintronics" that deals with switching nanomagnets with electrically generated mechanical strain and its myriad applications in computing, signal processing and signal generation. This technology is founded on an extremely energy-efficient switching methodology for a binary switch, which may be too error-prone to be viable for traditional Boolean logic, but which has many other engineering applications that are much more error-tolerant than Boolean logic and can benefit from the energy efficiency [43]–[49].

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REFERENCES

[1] G. E. Moore, "Cramming more components onto electronic circuits," *Electron. Mag.*, vol. 38, p. 4, 1965.
[2] L. B. Kish, "End of Moore's law: Thermal noise death of integration in micro- and nano-electronics," *Phys. Lett. A*, vol. 305, pp. 144–149, 2002.
[3] S. Bandyopadhyay, B. Das, and A. E. Miller, "Supercomputing with spin-polarized single electrons in a quantum coupled architecture," *Nanotechnology*, 5, 1994, Art. no. 113.
[4] S. N. Molotkov and S. S. Nazin, "Single-electron spin logical gates," *J. Exp. Theoretical Phys. Lett.*, vol. 62, 1995, Art. no. 273.
[5] H. Agarwal, S. Pramanik, and S. Bandyopadhyay, "Single spin universal Boolean logic gate," *New J. Phys.*, vol. 10, 2008, Art. no. 015001.
[6] T. Basu, S. K. Sarkar, and S. Bandyopadhyay, "Arithmetic logic unit of a computer based on spin-polarized single electrons," *IET Circ. Dev. Syst.*, vol. 1, pp. 194–199, 2007.
[7] S. Bandyopadhyay, A. Balandin, V. P. Roychowdhury, and F. Vatan, "Nanoelectronic implementations of reversible and quantum logic," *Superlattices Microstructures*, vol. 23, pp. 445–464, 1998.
[8] S. Bandyopadhyay and V. P. Roychowdhury, "Switching in a reversible spin logic gate," *Superlattices Microstructure*, vol. 22, pp. 411–416, 1997.
[9] A. R. Trivedi and S. Bandyopadhyay, "Single-spin Toffoli-Fredkin logic gate," *J. Appl. Phys.*, vol. 103, 2008, Art. no. 104311.
[10] S. Bandyopadhyay, "Self-assembled nanoelectronic quantum computer based on the Rashba effect in quantum dots," *Phys. Rev. B*, vol. 61,2000, Art. no. 13813.
[11] D. Loss and D. P. DiVincenzo, "Quantum computation with quantum dots," *Phys. Rev. A*, vol. 57, pp. 120–126, 1998.
[12] W. L. Wang, O. V. Yazyev, S. Meng, and E. Kaxiras, "Topological frustration in graphene nanoflakes: Magnetic order and spin logic devices," *Phys. Rev. Lett.*, vol. 102, 2009, Art. no. 157201.
[13] R. P. Cowburn, D. K. Koltsov, A. O.Adeyeye, M. E. Welland, and D. M. Tricker, "Single-domain circular nanomagnets," *Phys. Rev. Lett.*, vol. 83, 1999, Art. no. 1042.
[14] S. Salahuddin and S. Datta, "Interacting systems for self-correcting low power switching," *Appl. Phys. Lett.*, vol. 90, 2007, Art. no. 093503.
[15] S. Khasanvis *et al.*, "Self-similar magneto-electric nanocircuit technology for probabilistic inference engines," *IEEE Trans. Nanotechnol.* vol. 14, no. 6, pp. 980–991, Nov. 2015.
[16] S. Khasanvis *et al.*, "Architecting for causal intelligence at nanoscale," *Computer*, vol. 48, no. 12, pp. 54–64, Dec. 2015.
[17] S. Dey Manasi, M. M. Al-Rashid, J. Atulasimha, S. Bandyopadhyay, and A. R. Trivedi, "Skewed straintronic magneto-tunneling junction based ternary content-addressable memory – Part I," *IEEE Trans. Elect. Devices*, vol. 64, no. 7, pp. 2835–2841, Jul. 2017.
[18] S. Dey Manasi, M. M. Al-Rashid, J. Atulasimha, S. Bandyopadhyay, and A. R. Trivedi, "Skewed straintronic magneto-tunneling junction based ternary content-addressable memory – Part II, *IEEE Trans. Elect. Devices*, vol. 64, no. 7, pp. 2842–2848, Jul. 2017.
[19] S. Nasrin, J. L. Drobitch, S. Bandyopadhyay, and A. R. Trivedi, "Low-power restricted Boltzmann machine using mixed-mode magneto-tunneling junctions," *IEEE Elect. Devices Lett.*, vol. 40, no. 2, pp. 345–348, Feb. 2019.
[20] S. Nasrin, J. L. Drobitch, P. Shukla, T. Tulabandhula, S. Bandyopadhyay, and A. R. Trivedi, "Bayesian reasoning machine on a magneto-tunneling junction network," *Nanotechnol. (Special Issue Non-Boolean Comput. Nanomagnets)*, to be published.
[21] D. C. Ralph and M. D. Stiles, "Spin transfer torques," *J. Magn. Magn. Mater.*, vol. 320, 2008, Art. no. 1190.
[22] I. M. Miron *et al.*, "Perpendicular switching of a single ferromagnetic layer induced by in-plane current injection," *Nature*, vol. 476, pp. 189–193, 2011.
[23] M. I. Dyakonov and V. I. Perel', "Possibility of orienting electron spins with current," *Sov. Phys. J. Exp. Theoretical Phys. Lett.*, vol. 13, pp. 467–469, 1971.
[24] J. E. Hirsch, "Spin hall effect," *Phys. Rev. Lett.*, vol. 83, 1999, Art. no. 1834.
[25] Y. Kato, R. C. Myers, A. C. Gossard, and D. D. Awschalom, "Observation of the spin Hall effect in semiconductors," *Science*, vol. 306, pp. 1910–1913, 2004.
[26] J. Cui *et al.*, "A method to control magnetism in individual strain-mediated magnetoelectric islands," *Appl. Phys. Lett.*, vol. 103, 2013, Art. no. 232905.

[27] K. Roy, S. Bandyopadhyay, and J. Atulasimha, "Binary switching in a "symmetric" potential landscape," *Sci. Rep.*, vol. 3, 2013, Art. no. 3038.
[28] K. Roy, S. Bandyopadhyay, and J. Atulasimha, "Energy dissipation and switching delay in stress-induced switching of multiferroic nanomagnets in the presence of thermal fluctuations," *J. Appl. Phys.*, vol. 112, 2012, Art. no. 023914.
[29] A. K. Biswas, S. Bandyopadhyay, and J. Atulasimha, "Complete magnetization reversal in a magnetostrictive nanomagnet with voltage-generated stress: A reliable energy-efficient non-volatile magneto-elastic memory," *Appl. Phys. Lett.*, vol. 105, 2014, Art. no. 072408.
[30] A. K. Biswas, H. Ahmad, J. Atulasimha, and S. Bandyopadhyay, "Experimental demonstration of complete 180^0 reversal of magnetization in isolated Co nanomagnets on a PMN-PT substrate with voltage-generated strain," *Nano Lett.*, vol. 17, pp. 3478–3484, 2017.
[31] N. D'Souza, M. Salehi-Fashami, S. Bandyopadhyay, and J. Atulasimha, "Experimental clocking of nanomagnets with strain for ultralow power Boolean logic," *Nano Lett.*, vol. 16, pp. 1069–1075, 2016.
[32] V. Sampath, N. D'Souza, G. M. Atkinson, S. Bandyopadhyay, and J. Atulasimha, "Experimental demonstration of acoustic wave induced magnetization switching in dipole-coupled magnetostrictive nanomagnets for ultralow power computing," *Appl. Phys. Lett.*, vol. 109, 2016, Art. no. 102403.
[33] H. Ahmad, J. Atulasimha, and S. Bandyopadhyay, "Electric field control of magnetic states in isolated and dipole-coupled FeGa nanomagnets delineated on a PMN-PT substrate," *Nanotechnology*, vol. 26, 2015, Art. no. 401001.
[34] M. A. Abeed, J. Atulasimha, and S. Bandyopadhyay, "Magneto-elastic switching of magnetostricitve nanomagnets with in-plane anisotropy: The effect of material defects," *J. Phys: Condens. Matt.*, vol. 30, 2018, Art. no. 394001.
[35] D. Winters, M. A. Abeed, S. Sahoo, A. Barman, and S. Bandyopadhyay, "Reliability of magneto-elastic switching of non-ideal nanomagents with defects: A case study for the viability of straintronic logic and memory," *Phys. Rev. Appl.*, vol. 12, 2019, Art. no. 034010.
[36] J. von Neumann, "Probabilistic logic and the synthesis of reliable organisms from unreliable components," *Autom. Stud.*, vol. 34, pp. 43–98, 1956.
[37] A. D. Patil, S. Manipatruni, D. Nikonov, I. A. Young, and N. R. Shanbhag, "Shannon-inspired statistical computing to enable spintronics," *arXiv:1702.06119*.
[38] Z. Zhao *et al.*, "Giant manipulation of MgO-based magnetic tunnel junctions via localized strain: A pathway to ultra-energy-efficient memory technology," *Appl. Phys. Lett.*, vol. 109, 2016, Art. no. 092403.
[39] A. K. Biswas, J. Atulasimha, and S. Bandyopadhyay, "The straintronic spin neuron," *Nanotechnology*, vol. 26, 2015, Art. no. 285201.
[40] M. A. Abeed, J. L. Drobitch, and S. Bandyopadhyay, "Microwave oscillator based on a single straintronic magneto-tunneling junction," *Phys. Rev. Appl.*, vol. 11, 2019, Art. no. 054069.
[41] J. Torrejon *et al.*, "Neuromorphic computing with nanoscale spintronic oscillators," *Nature*, vol. 547, pp. 428–431, 2017.
[42] S. Okamoto, N. Kikuchi, M. Furuta, O. Kitakami, and T. Shimatsu, "Microwave assisted magnetic recording technologies and related physics," *J. Phys. D: Appl. Phys.*, vol. 48, 2015, Art. no. 353001.
[43] M. A. Abeed and S. Bandyopadhyay, "Experimental demonstration of an extreme sub-wavelength acoustic antenna actuated by spin-orbit torque from a heavy metal nanostrip," *Adv. Mater. Technol.*, vol. 5, 2020, Art. no. 1901076.
[44] N. D'Souza, J. Atulasimha, and S. Bandyopadhyay, "An ultrafast image recovery and recognition system implemented with nanomagnets possessing biaxial magneto-crystalline anisotropy," *IEEE Trans. Nanotechnol.*, vol. 11, no. 5, pp. 896–901, Sep. 2012.
[45] M. A. Abeed, A. K. Biswas, M. M. Al-Rashid, J. Atulasimha, and S. Bandyopadhyay, "Image processing with dipole-coupled nanomagnets: Noise suppression and edge enhancement detection," *IEEE Trans. Elect. Dev.*, vol. 64, no. 5, pp. 2417–2424, May 2017.
[46] A. K. Biswas, J. Atulasimha, and S. Bandyopadhyay, "Energy-efficient hybrid spintronic-straintronic non-volatile reconfigurable equality bit comparator," *Spin*, vol. 7, 2017, Art. no. 1750004.
[47] H. Ahmad, J. Atulasimha, and S. Bandyopadhyay, "Reversible strain induced magnetization switching in FeGa nanomagnets: Pathway to rewritable, non-volatile, non-toggle, extremely low energy straintronic memory," *Sci. Rep.*, vol. 5, 2015, Art. no. 18264.
[48] M. A. Abeed and S. Bandyopadhyay, "Simulated annealing with time-varying strain in a dipole-coupled array of magnetosrictive nanomagnets," *J. Phys. D: Appl.*, *arXiv:1908.00893*.
[49] N. D'Souza *et al.*, "Energy-efficient switching of nanomagnets for computing: Straintronics and other methodologies," *Nanotechnology*, vol. 29, 2018, Art. no. 442001.

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