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Microwave Power Detection With Voltage-Gated Graphene

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ABSTRACT Commercially available, chemical vapor deposition grown, graphene has been used to realize voltage-gate tunable, microwave power detectors. Corbino disc structures with chrome/gold contacts have been fabricated on top of graphene deposited on P-type silicon substrates with silicon dioxide gate oxides. Devices of varying sizes were used to detect a 433.92 MHz signal. These test structures exhibited a peak power detection sensitivity of 3.25 mV/mW at 292 K and 5.43 mV/mW at 80 K. The improved graphene detectors exceed the sensitivity of previously reported graphene detectors, 0.86 mV/mW, as well as previously explored carbon nanotube bolometers, 0.36 mV/mW.

INDEX TERMS Graphene, detectors, microwave measurements, Corbino disc.

I. INTRODUCTION

Graphene, a single atom layer of carbon in a hexogonal lattice, is of great interest in radio frequency and microwave applications due to its high carrier mobility and DC transfer characteristic [1]. The chemical vapor deposition (CVD) technique for synthesizing graphene is relatively inexpensive, allows for large-scale production, and enables graphene to be transferred to a variety of microwave-compatible substrates. In this paper, we expand upon the previously reported power detection capabilities of graphene-loaded Corbino disc test structures [2] and present an improved microwave power detector based on aluminum-oxide passivated monolayer graphene. In prior published work, we have shown that the thermoelectric effect is the primary mechanism responsible for microwave power detection from nano-constrictions fabricated from this material system [3]. Incident microwave power locally heats the inner disc of the Corbino disc test structure while the outer annulus is held in thermal contact with probe station chassis. We also discuss the details involved in our simple, single-lithography-mask approach for making detectors that have a Corbino disc geometry [4] with a back-gate for modulating channel conductance [5]. We present the results from gated microwave power detection experiments at both room temperature (292 K) and liquid nitrogen cooled temperature (80 K) where the operating frequency was held at 433.92 MHz, the center of one of the unlicensed industrial, scientific, and medical (ISM) radio bands.

II. DEVICE FABRICATION

Work has been done in order to improve the previsouly reported device processing method [2]. Fig. 1 outlines the Corbino disc test structure fabrication process. The process starts by first cleaning commercially avaliable, CVD-grown monolayer graphene on silicon dioxide/silicon (SiO_2/Si) [6] with rapid thermal annealing (RTA) in forming gas (nitrogen with 4.5% hydrogen) atmosphere at 250 °C for 12 minutes. The RTA helps to reduce impurities absorbed by the graphene surface [6]. Then, a 5 nm sacrificial layer of aluminum was deposited over the entire substrate and allowed to form a native oxide passivation layer. This covering was used to protect the graphene during photolithographic processing. Negative photoresist (AZ nLOF 2020) was spun on, exposed, and then

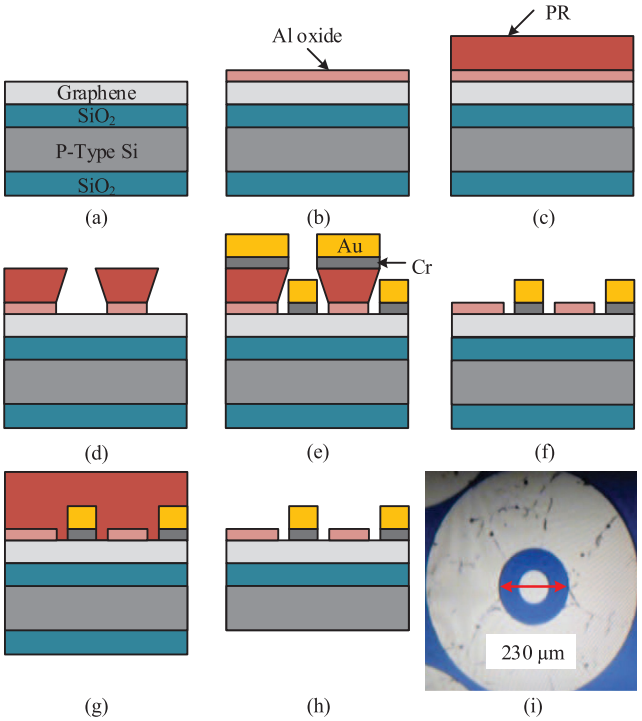

FIGURE 1. **(a) RTA cleaned graphene on Si substrate with SiO_2 thermal oxide. (b) Metallization of sacrificial aluminum layer. (c) Spin on photoresist for lithography. (d) Pattern with negative photomask. (e) Metallization of Cr/Au contact layer. (f) Lift-off excess photoresist and metal. (g) Spin on protective photoresist. (h) removal of back SiO_2 oxide with BOE. (i) Photo of finished Corbino disc test structure. The graphene layer has an average grain size of 20 μm and the finished device may span multiple grain boundaries.**

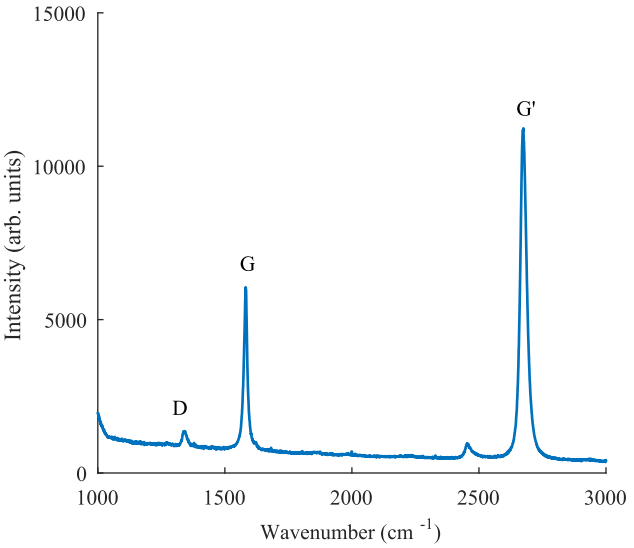

FIGURE 2. **Raman spectrum of the processed sample displaying G and G′ (2D) peaks as well as a small D peak resulting from disorder in the lattice due to device processing. The peak intensity ratios are: $I_{G'}/I_G = 1.85$ and $I_G/I_D = 4.43$.**

developed with AZ 300 MIF. The chosen developer not only patterned the photoresist but also selectively etched away the aluminum oxide layer [7]. A 3 nm layer of chromium (Cr) and 30 nm layer of gold (Au) was deposited via e-beam evaporation for electrical contact and a lift-off process was done to finalize the Corbino structure. Cr was chosen as the adhesion layer over Ti in order to more closely match the work function of graphene. The work function of graphene is approximately $\varphi = 4.56$ eV [8], [9]; that of Au is approximately 5.4 eV whereas those of Ti and Cr are 4.63 eV and 4.5 eV, respectively. Finally, a protective layer of positive photoresist was spun over the top of the sample, and it was immersed in a buffered oxide etchant (BOE) to remove the back layer of SiO_2, a necessary step to allow for contact to the back-gate. The Al-oxide passivation layer remained on top of the graphene within the disc structure preventing degradation of the graphene surface when exposed to potential contaminants. If desired, this oxide layer could be removed by a second immersion in photoresist developer, containing tetramethylammonium hydroxide (TMAH), subsequent to device processing. The fabrication step of capping the RTA cleaned sample with a passivation layer is necessary in order to protect the graphene layer during device processing and prevent exposure to ambient air. After device processing, the Raman spectrum was collected from a graphene annulus situated between an inner disc and outer ring. Although, the processing increased disorder within the polycrystalline graphene, as indicated by the D-band peak (~1350 cm^{-1}) [10]] shown in Fig. 2, the intensity ratios show that the overall Dirac characteristics remained intact [11].

III. DC CHARACTERIZATION

I-V traces of the graphene devices were collected to verify the electrical behavior expected of polycrystalline graphene. Device drain-source (inner disc-outer disc) current versus gate voltage for varying bias voltages was collected using a Keithley 4200 SCS. The data was used to show the point of minimum conductivity, Fig. 3, with conductivity given as

$$\sigma_{xx}(S \cdot \square) = \frac{G\, ln(r_2/r_1)}{2\pi}, \tag{1}$$

where r_1 and r_2 are the radius of the inner contact and outer contact, respectively [12]. The point of minimum conductivity, the charge neutrality point [13], is displayed between 2 V and 6 V as V_{DS} increases from 1–10 V. The shift in the charge neutrality point of the sample scales with the drain-source voltage (V_{DS}), Fig. 4. Higher values of V_{DS} create an effective gate voltage that causes the shift. In Fig. 5 we have plotted the conductivity, correcting for this effective gate voltage and find that the zero-bias Dirac voltage ($V_{G\,min}$) lies at 1.5 V.

The current-versus-voltage relationship of a traditional semiconductor MOSFET with a Corbino geometry [14] can be modeled in terms of three regimes of operation as

$$\frac{i_D}{k(V_{GS}) \cdot \frac{2\pi}{\ln(r_2/r_1)}} = \begin{cases} 0 & V_{OV} \le 0 \\ \frac{1}{2}V_{OV}^2(1 + \lambda V_{DS}) & 0 \le V_{OV} \le V_{DS} \\ (V_{OV} - \frac{1}{2}V_{DS})V_{DS} & V_{OV} > V_{DS} \end{cases} \tag{2}$$

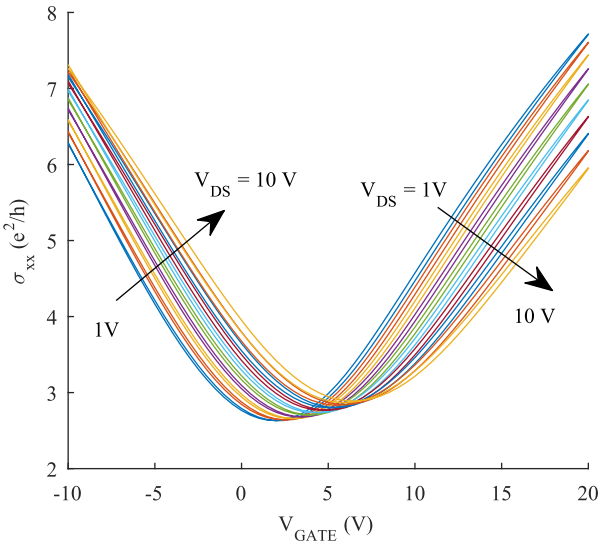

FIGURE 3. Conductivity vs gate voltage for V_{DS} varied between 1 V and 10 V and displaying a charge neutrality point between 2 V and 6 V.

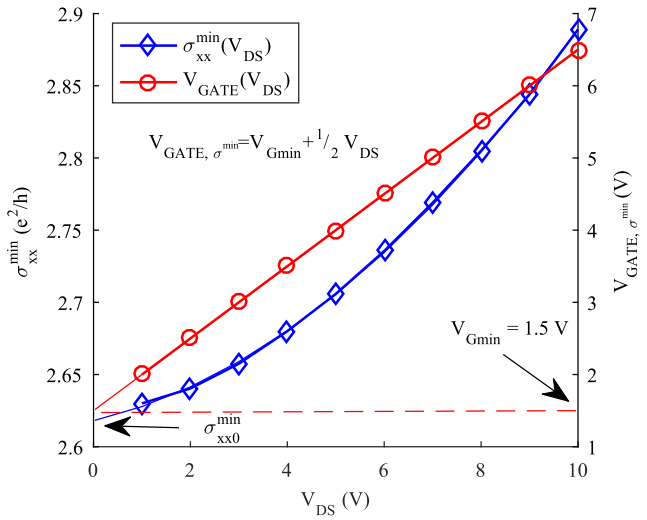

FIGURE 4. Minimum conductivity (left) and it's corresponding gate voltage (right) vs drain-source voltage.

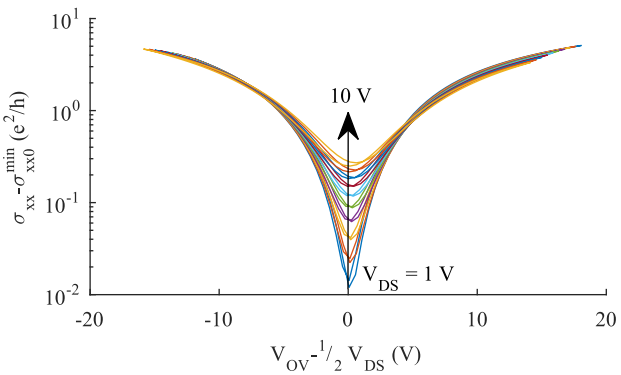

FIGURE 5. Conductivity vs effective gate voltage for V_{DS} varied between 1 V and 10 V, corrected for offset gate voltage.

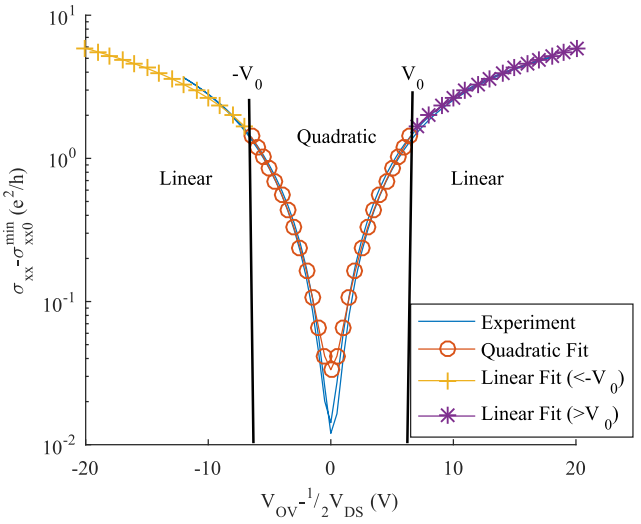

FIGURE 6. Conductivity vs effective gate voltage for $V_{DS} = 1$ V, showing quadratic and linear regions of operation.

where $k(V_{GS})$ is the product of the carrier mobility (with dependence on the gate-source-voltage difference) and the gate to channel capacitance per unit area, V_{OV} is the overdrive voltage given in terms of a threshold voltage V_t (such that $V_{OV} = V_{GS} - V_t$), and λ is the channel-length modulation effect parameter. Applying these expressions to Eqn. (2), one finds the corresponding large signal conductance to be:

$$\sigma_{xx} = \begin{cases} 0 & V_{OV} \leq 0 \\ \frac{1}{2}k(V_{GS}) \cdot (\lambda + \frac{1}{V_{DS}})V_{OV}^2 & 0 \leq V_{OV} \leq V_{DS} \\ k(V_{GS}) \cdot (V_{OV} - \frac{1}{2}V_{DS}) & V_{OV} > V_{DS}. \end{cases} \quad (3)$$

From inspection of Fig. 5, we observe that sheet conductance of the channel in our graphene device exhibits behavior of the form

$$\sigma_{xx} = A\sqrt{1 + \left(\frac{(V_{OV} - \frac{1}{2}V_{DS})^2}{V_0}\right)} + B, \quad (4)$$

with the empirical constants A, V_0 and B. Equation (4) can be broken into three regimes of operation analogous to the behavior of the MOSFET:

$$\sigma_{xx} = \begin{cases} \sigma_{xx}^{min} & |V_{OV} - \frac{1}{2}V_{DS}| = 0 \\ C(V_{OV} - \frac{1}{2}V_{DS})^2 + \sigma_{xx}^{min} & 0 \leq |V_{OV} - \frac{1}{2}V_{DS}| \leq V_0 \\ D(V_{OV} - \frac{1}{2}V_{DS}) + E & |V_{OV} - \frac{1}{2}V_{DS}| > V_0, \end{cases} \quad (5)$$

where C, D, and E are empirical constants. In this case, the equivalent overdrive voltage is expressed in terms of an experimentally observed gate-voltage offset such that $V_{OV} = V_{GATE} - V_{G\,min}$ and there is an added term σ_{xx}^{min}, which must be due to the minimum conductivity of graphene [15]. Fig. 6 shows the three regimes of operation for the case of operation $V_{DS} = 1$ V.

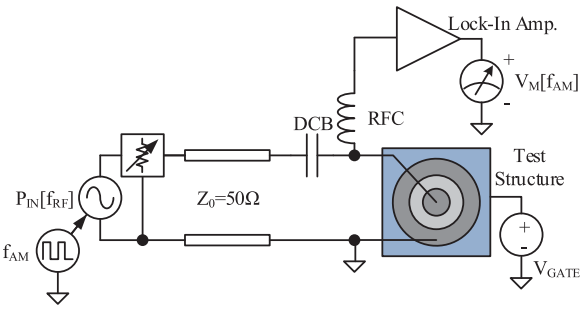

FIGURE 7. Schematic of the graphene power detection circuit.

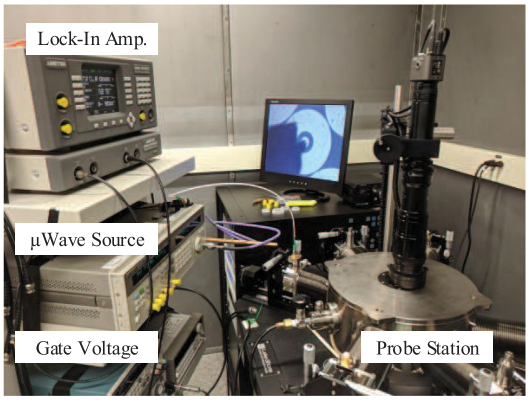

FIGURE 8. Photo of the graphene power detection experimental setup.

IV. POWER DETECTION

The graphene loaded Corbino disc test structures have been used to realize a microwave power detector operating at 433.92 MHz, in the ISM band. The gated graphene devices were fed with incident microwave power chopped at 1501.487 Hz. A voltage measurement was taken via lock-in detection at the chopping frequency on the device under test. An illustration of the experimental structure is shown in Fig. 7 and a photograph of the test setup is shown in Fig. 8.

Power detection was characterized at both room temperature and liquid nitrogen temperature under vacuum ($<10^{-4}$ Torr) using a Lakeshore Cryotronics CPX-VF probe station with GS-style probes having a ground-to-signal spacing of 250 μm. Power detection data was collected by sweeping the input power (P_{IN}) and measuring the detected signal (V_M) with the gate voltage (V_{GATE}) chosen to maximize sensitivity as shown in Fig. 9. The graphene Corbino disc detectors achieved a peak sensitivity (S_V) of approximately 3.25 mV/mW for a device with an annular area of 40,300 μm^2 at 292 K determined via a fit to the measured data with

$$V_M(\text{dBmV}) = b(\text{dB}) + 2P_{IN}(\text{dBm}), \tag{6}$$

where S_V (mV/mW) can be obtained from the log-log plot intercept b (dB) from the relation

$$S_V(\text{mV/mW}) = 10^{\frac{b(\text{dB})}{20\,\text{dB}}}\left(\frac{1\,\text{mW}}{1\,\text{mV}}\right). \tag{7}$$

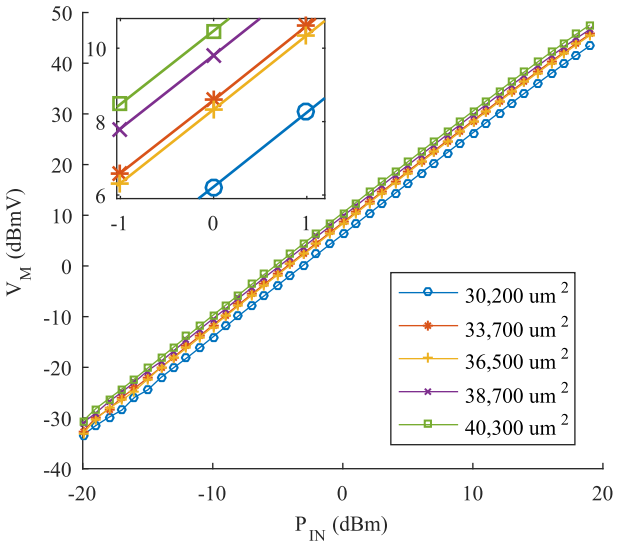

FIGURE 9. Measured voltage vs applied input power at 292 K for multiple disc annular areas (Inset shows zoom-in of plot for clarity).

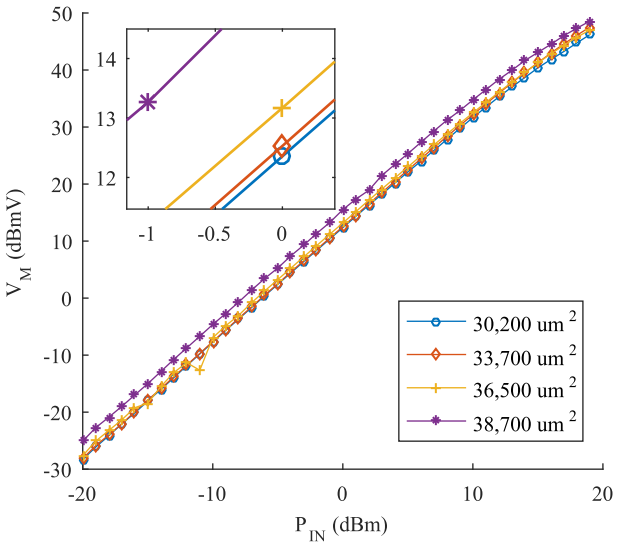

FIGURE 10. Measured voltage vs applied input power at 80 K for multiple disc annular areas (Inset shows zoom-in of plot for clarity).

The 1 dB compression point of the detectors occured beyond the range of the available microwave source (>20 dBm at the operating frequency). Power detection measurements done at 80 K improved the sensitivy by approximately 5 dB to peak sensitivity at 5.44 mV/mW for a device with an annular area equal to 38,720 μm^2, Fig. 10. The improved graphene detectors exceed the sensitivity of previously reported graphene detectors, 0.86 mV/mW [2], as well as previously explored carbon nanotube bolometers, 0.36 mV/mW, [16], [17]. We attribute microwave power detection in the material system under test primarily to the thermoelectric effect [3] with possible contributions of signal rectification due to the nonlinear conduction of the the voltage-gated graphene device.

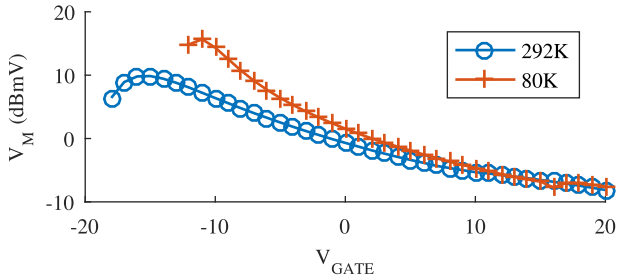

FIGURE 11. Measured voltage vs gate voltage at an incident power of 0 dBm at 433.92 MHz at temperatures of 292 K and 80 K.

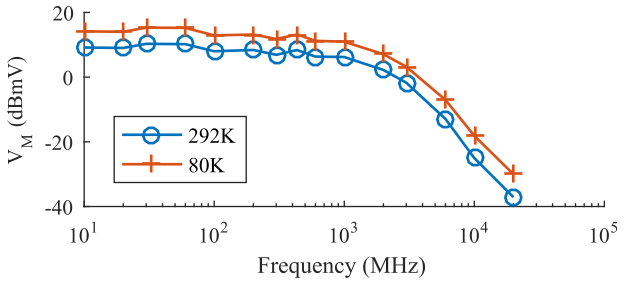

FIGURE 12. Frequency response of a detector showing measured voltage vs frequency at temperatures of 292 K and 80 K.

Measurements were done on devices of varying sizes, with annular areas ranging from 30,200 μm^2 to 40,300 μm^2, and displayed sensitivities from 2.02 μV/mW to 3.25 mV/mW at room temperature. The sensitivity of the devices increases with the annular area of the graphene within the discs. The gate voltage allows for tuning to achieve the maximum sensitivity of the device by altering the gate capacitance and carrier mobility [14] and biasing the material where the conductivity is most nonlinear. The maximum sensitivity was achieved near -17 V at 292 K and shifted down to -12 V at 80 K. The measured voltage response of a 433.92 MHz signal at 0 dBm to a changing gate voltage is shown in Fig. 11 for temperatures of both 292 K and 80 K. From inspection of Eqn. (5), we see that in the linear regime, the I-V characteristic can be expanded into the polynomial form of:

$$i_d = g_m V_{\mathrm{DS}} + \frac{1}{2} g'_m V_{\mathrm{DS}}^2. \tag{8}$$

The power detection sensitivity S can therefore be expressed as:

$$|S| = \frac{|g'_m|}{|g_m|} \propto \frac{1}{|V_{OV} + E/D|}. \tag{9}$$

This expression indicates that the power detection should fall-off with increasing gate voltage, which is in agreement with our observations shown in Fig. 11.

A frequency sweep across the detectors with an incident power of 0 dBm shows the bandwidth of the devices, Fig. 12. The detectors can operate up to approximately 1 GHz before there is 3 dB roll-off and power detection falls due to the gate capacitance.

V. CONCLUSION

Power detection measurements using graphene Corbino discs yielded a peak power sensitivity of 3.25 mV/mW at room temperature and 5.44 mV/mW at liquid nitrogen temperature. We expect that the performance can be improved through continued optimization of the fabrication process and device dimensions. A thicker metal layer will help to increase device yield and prevent damage due to probing as well improve the device reflection coefficient to improve power delivery to the device. Devices without back-gates could help to improve performance at higher frequencies by removing parasitic capacitances, at the loss of tunability via the back-gate voltage.

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