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Analysis and Design of FeFET Synapse With Stacked-Nanosheet Architecture Considering Cycle-to-Cycle Variations for Neuromorphic Applications

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ABSTRACT Using extensive Monte-Carlo simulations with a nucleation-limited-switching (NLS) ferroelectric model and considering cycle-to-cycle variations, this paper constructs and analyzes the intrinsic conductance (G_{DS}) response of stacked-nanosheet FeFET synapses with emphasis on the challenging identical-pulse stimulation. Our study indicates that the interlayer oxide thickness of the FeFET and the saturation polarization of the ferroelectric are crucial to the linearity and symmetry of the intrinsic G_{DS} response. With the stacked-nanosheet architecture, the maximum-to-minimum conductance ratio in the G_{DS} response can be boosted by increasing the number of channel tiers without footprint penalty. For a stacked-nanosheet FeFET synapse with an area ratio effect, the G_{DS} response can be further engineered by varying the tier number. In addition, the immunity to cycle-to-cycle variations and the noise margin for each state in the G_{DS} response can also be improved by increasing the number of tiers. Our study may provide insights for future FeFET synapse design for analog computing.

INDEX TERMS Stacked nanosheet, ferroelectric field-effect transistor (FeFET), analog synapse, neuromorphic computing.

I. INTRODUCTION

Neuromorphic computing, with its great capability in recognition and inference, has garnered substantial interest as a beyond von-Neumann computing [1], [2], [3], [4], [5], [6]. By using the analog-memory based crossbar array to perform matrix manipulations in parallel, the neuromorphic/analog computing can accelerate deep learning for energy efficiency [3], [6]. The synapse, a memory device with an incremental analog switching behavior, is crucial to the accuracy/performance of neuromorphic computing [4], [5], [6]. HfO_2-based ferroelectric FET (FeFET), with its CMOS compatibility, has become a promising nonvolatile memory (NVM) device candidate [7], [8]. Stemming from its multi-domain switching behavior, the FeFET is attractive for analog synapse applications because the gradual change of the ferroelectric polarization can continuously modulate the channel conductance of the FeFET to mimic the synaptic weight update [9].

The analog synapse has to exhibit a symmetrical and linear conductance response in addition to a large maximum-to-minimum conductance ratio (G_{max}/G_{min}), under potentiation and depression stimulations for weight update. Among all the gate pulse stimulations usually adopted (e.g., pulse-amplitude modulation, pulse-width modulation, etc. [6]), the identical-pulse stimulation is most attractive because it is simpler for more efficient on-chip implementations. However, it is very challenging to obtain a satisfactory conductance response for FeFET synapses under the identical gate pulse scheme. Stacked-nanosheet transistor [10] has the advantage of providing a large effective width and ON current with a small

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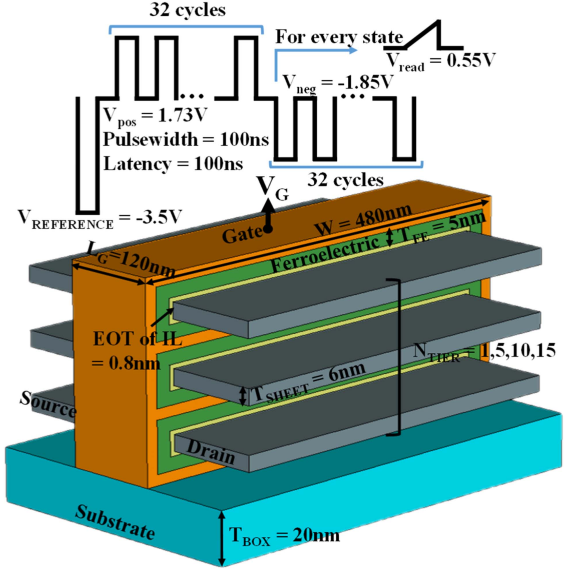

FIGURE 1. **Baseline stacked-nanosheet FeFET structure and pertinent device parameters considered in this work. Also shown is the baseline gate pulse scheme employed for the conductance response of the FeFET synapse.**

footprint. FeFET synapse with the stacked-nanosheet architecture (Fig. 1) is interesting because it may provide the ferroelectric domains necessary to suppress the impact of domain stochastic switching [11] on the conductance response with a small footprint. In this work, utilizing extensive Monte-Carlo (MC) simulations with a nucleation-limited-switching (NLS) ferroelectric model [12], [13] and considering cycle-to-cycle variations, we construct and analyze the intrinsic conductance response of stacked-nanosheet FeFET synapses with emphasis on the challenging identical-pulse stimulation (Fig. 1).

This paper is organized as follows. Section II describes the methodology used in this work. In Section III, the intrinsic conductance (G_{DS}) response of the stacked-nanosheet FeFET synapse (Fig. 1) under the stimulation of identical gate pulses is analyzed and optimized. In Section IV, we evaluate the G_{DS} response for a stacked-nanosheet FeFET synapse with an area ratio effect. In Section V, we investigate the impact of stochastic switching induced cycle-to-cycle variations on the G_{DS} response for the stacked-nanosheet FeFET synapse with various tier numbers. The conclusion is drawn in Section VI.

II. METHODOLOGY

Fig. 1 depicts the baseline MFIS (metal-ferroelectric-insulator-semiconductor) stacked-nanosheet FeFET synapse and baseline gate pulse scheme in this study. Unless otherwise specified, 5 nm ferroelectric thickness with saturation polarization P_S=28.6 μC/cm^2 and 0.8 nm equivalent oxide thickness (EOT) of interlayer oxide (IL) are considered. Fig. 2, with (1)–(3),

$$IF\ s^{(i)} * E_{FE} < 0$$

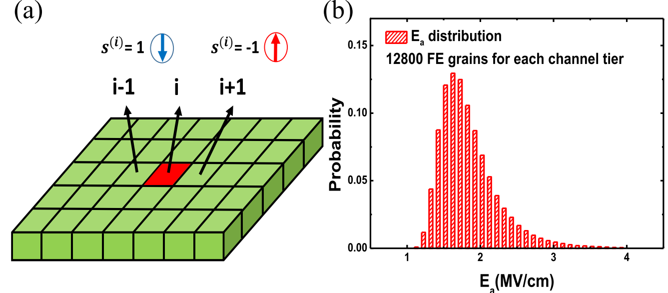

FIGURE 2. **(a) Schematic of the ferroelectric NLS model with "i" representing the grain/domain index. (b) The effective activation flied E_a distribution (based on [12]) used in this work.**

$$\tau^{(i)} = \tau_\infty * \exp\left(\left(\frac{E_a{}^{(i)}}{|E_{FE}|}\right)^\alpha\right) \tag{1}$$

$$h_{new}^{(i)} = h^{(i)} + \frac{\Delta t}{\tau^{(i)}} \tag{2}$$

$$P^{(i)} = 1 - \exp\left[\left(h^{(i)}\right)^\beta - \left(h_{new}^{(i)}\right)^\beta\right] \tag{3}$$

concisely describes the MC NLS ferroelectric model [12], [13], in which the ferroelectric is viewed as an ensemble of elementary regions (with index i) that switch independently. Each elementary region possesses a distinct domain switching time (see (1)) and its own effective activation field (E_a). Note that if the directions of domain ($s^{(i)}$) and electric field (E_{FE}) are opposite, the history parameter $h^{(i)}$ will increase with time (see (2)), and the accumulation of $h^{(i)}$ for each domain will raise the domain switching probability (see (3)). In other words, the domain-switching probability has an accumulation effect [14], and time-domain MC simulations are carried out to capture the accumulative switching behavior for the ferroelectric. In this work, related parameters (e.g., α, β, τ_∞) and E_a distribution (Fig. 2(b)) are based on the measured ferroelectric polarization-switching data in [12] with more-detailed calibration procedure shown in [13]. We self-consistently solve the NLS model with the transistor charge-voltage and current-voltage relationships to construct the intrinsic G_{DS} response of the stacked-nanosheet FeFET synapse.

III. ANALYSIS AND OPTIMIZATION OF CONDUCTANCE RESPONSE FOR STACKED-NANOSHEET FEFET SYNAPSE

Figs. 3(a) and 4(a) show our constructed conductance responses for 1-tier Nanosheet FeFET synapse under stimulations with identical pulses (see Fig. 3(b)) and pulse-amplitude modulation (see Fig. 4(b)), respectively. Also shown in Figs. 3(c) and 4(c) are our calculated ferroelectric field (E_{FE}) and polarization (P_{FE}) responses to the stimulations. It can be clearly seen that the identical-pulse stimulation leads to a poor linearity and symmetry in the conductance response (Fig. 3(a)), while the pulse-amplitude modulation can result in a satisfactory G_{DS} response (Fig. 4(a)).

To obtain a linear and symmetrical G_{DS} response for the FeFET synapse, it is crucial to have a linear and symmetrical

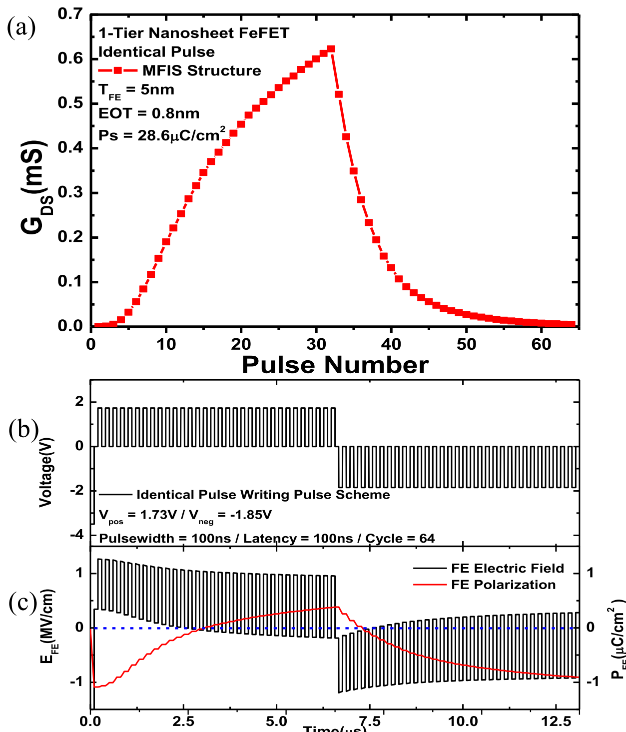

FIGURE 3. (a) Constructed G_{DS} response of a 1-tier Nanosheet FeFET synapse under the stimulation of identical pulses with voltage waveform shown in (b). (c) Responses of ferroelectric field, E_{FE}, and polarization, P_{FE}.

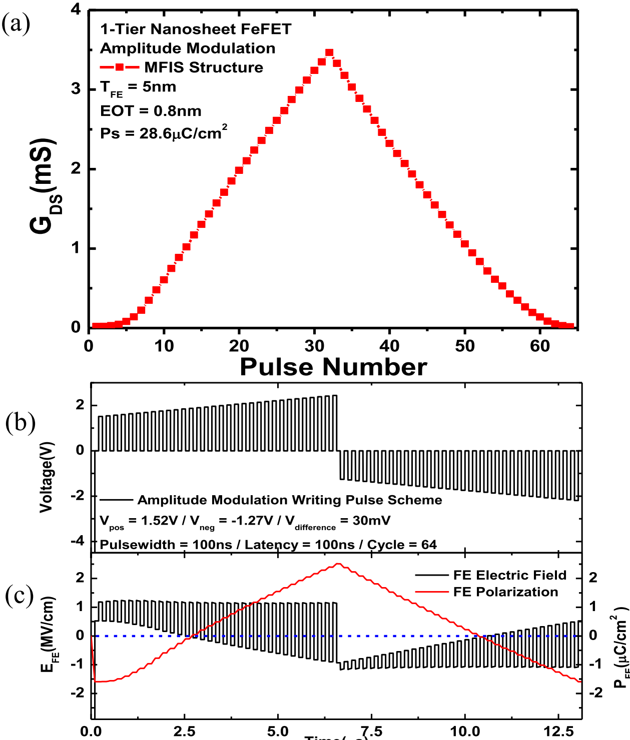

FIGURE 4. (a) Constructed G_{DS} response of a 1-tier Nanosheet FeFET synapse under the stimulation of pulse-amplitude modulation with voltage waveform shown in (b). (c) Responses of ferroelectric field, E_{FE}, and polarization, P_{FE}.

TABLE 1 Non-linearity (ideal $\alpha_{P,D}$ = 0) and Asymmetry (ideal $|\alpha_P-\alpha_D|$ = 0) for Each Conductance Response in Fig. 5. The extraction of the numbers is based on [19].

	Non-linearity α_P	Non-linearity α_D	Asymmetry $\lvert\alpha_P-\alpha_D\rvert$	G_{max}/G_{min}
Baseline EOT = 0.8nm & Ps = 28.6μC/cm²	1.79	–19.61	21.40	54.3
EOT = 0.6nm	0.88	–12.51	13.39	57
EOT = 0.4nm	0.41	–7.25	7.66	66.1
Ps = 22.9μC/cm²	0.98	–10.92	11.90	39.5
Ps = 17.2μC/cm²	0.40	–7.92	8.32	30.4
EOT = 0.4nm & Ps = 17.2μC/cm²	0.33	–4.45	4.78	51.6

response in the ferroelectric polarization P_{FE} [15]. Under the stimulation of pulse-amplitude modulation, Fig. 4(c) reveals that the during-write E_{FE} for each state can be kept constant, so the P_{FE} can have a linear and symmetrical response. However, under the identical-pulse scheme, Fig. 3(c) shows that the during-write E_{FE} changes with increasing pulse number, resulting in a poor P_{FE} response.

$$E_{FE\ During-wite} = \frac{1}{T_{FE}}\left(C_{MOS}\frac{V_G}{C_{MOS}+C_{FE}} - \frac{P_{FE}}{C_{MOS}+C_{FE}}\right) = \frac{1}{T_{FE}}\left(C_{MOS}\frac{V_G}{C_{MOS}+C_{FE}} - E_{dep}T_{FE}\right) = \frac{V_G}{T_{FE}}\frac{C_{MOS}}{C_{MOS}+C_{FE}} - E_{dep} \tag{4}$$

$$E_{FE\ After-wite} = E_{dep} = P_{FE}\left[\varepsilon_{FE}\left(\frac{C_{MOS}}{C_{FE}}+1\right)\right]^{-1} = \frac{P_{FE}}{T_{FE}\left(C_{MOS}+C_{FE}\right)} \tag{5}$$

The during-write E_{FE} is governed by (4), in which the first term is related to the voltage divider effect between the ferroelectric layer (with thickness T_{FE} and capacitance C_{FE}) and the underlying transistor (with capacitance C_{MOS}), while the second term is the depolarization field E_{dep} [16]. The pulse-amplitude modulation scheme, through varying the gate voltage V_G, can maintain a constant during-write E_{FE} for each writing pulse according to (4). For the identical-pulse scheme, the V_G cannot be changed and the during-write E_{FE} is impacted by the second term in (4), the E_{dep}. In other words, to improve the FeFET synapse response under the identical-pulse scheme, it is very important to reduce the E_{dep}.

The depolarization field E_{dep} is governed by (5), which suggests that, for a given T_{FE}, the E_{dep} can be reduced by lowering the EOT of IL [17] (through the C_{MOS} term) or lowering the saturation polarization P_S (through the P_{FE} term). Note that it has been reported in [18] that different dopant of HfO_2 can result in different P_S. It can be seen from Fig. 5 and Table 1 that, under the identical-pulse scheme, the linearity and symmetry in the G_{DS} response of the 1-tier Nanosheet FeFET synapse can indeed be improved (compared with the

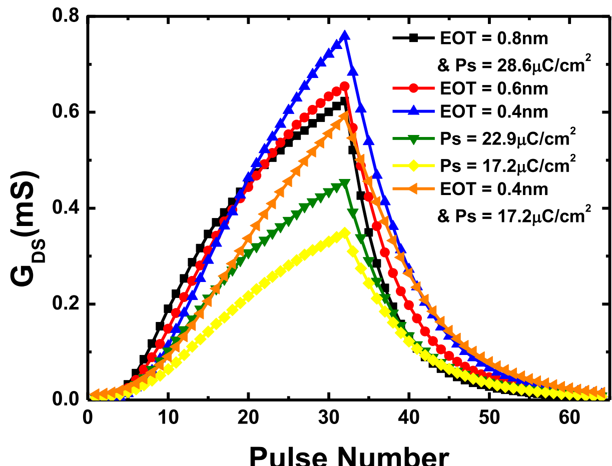

FIGURE 5. Compared with the baseline design (EOT = 0.8 nm, P_S = 28.6 μC/cm^2), lowering the IL EOT or lowering the saturation polarization P_S can improve the linearity and symmetry of the G_{DS} response for the 1-tier Nanosheet FeFET under the stimulation of identical pulses.

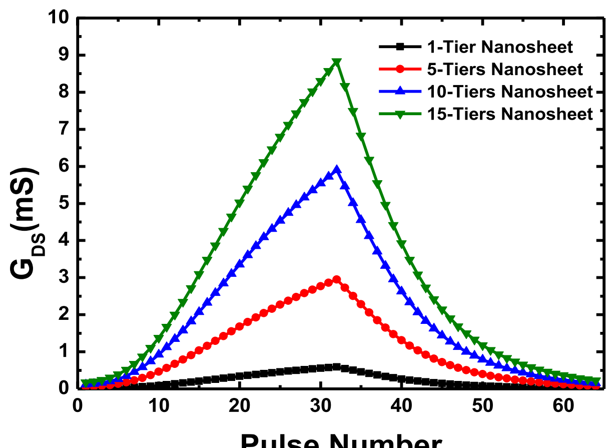

FIGURE 6. The G_{max}/G_{min} of the stacked-nanosheet FeFET synapse response can be greatly raised by increasing the number of tiers without footprint penalty.

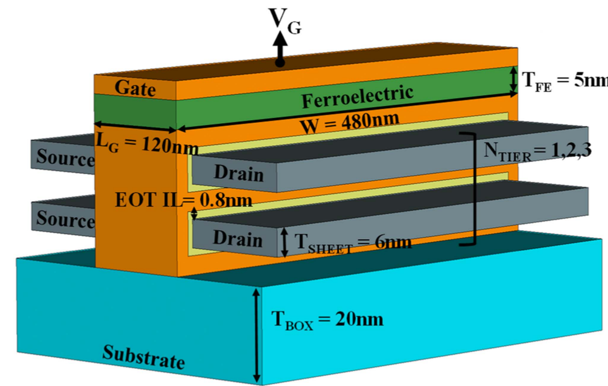

FIGURE 7. With a ferroelectric layer on top of a stacked-nanosheet FET, the FeFET has an area ratio AR = A_{FE}/A_{MOS} (A_{FE}: ferroelectric area. A_{MOS}: effective transistor area). The G_{DS} response for a stacked-nanosheet FeFET synapse with the structure can be engineered by varying the number of tiers (N_{TIER}).

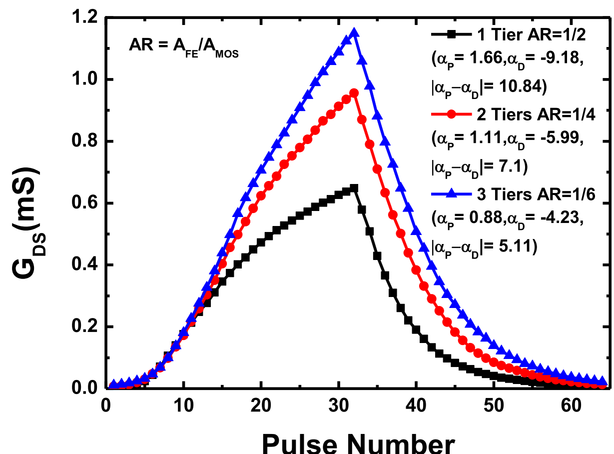

FIGURE 8. Impact of area ratio on the conductance response of stacked-nanosheet FeFET synapse with the MFMIS structure in Fig. 7 under the stimulation of identical pulses. The G_{DS} response for each case is optimized by using an optimum V_G.

baseline EOT=0.8 nm, P_S=28.6 μC/cm^2) by reducing the IL EOT or P_S. In fact, reducing both the EOT and P_S (e.g., EOT=0.4 nm, P_S=17.2 μC/cm^2) can provide the best linearity and symmetry for the G_{DS} response of the 1-tier FeFET synapse. Fig. 5 and Table 1 also show that lowering the IL EOT improves G_{max}/G_{min} while lowering P_S degrades the G_{max}/G_{min}. With the stacked-nanosheet architecture, nevertheless, Fig. 6 demonstrates that the G_{max}/G_{min} in the FeFET synapse response can be greatly increased by increasing the number of tiers without footprint penalty.

IV. CONDUCTANCE RESPONSE FOR STACKED-NANOSHEET FEFET SYNAPSE WITH AREA RATIO

In this section, under the identical-pulse scheme, we investigate the conductance response for stacked-nanosheet FeFET synapse with an area ratio effect. As shown in Fig. 7, with a ferroelectric on top of a stacked-nanosheet FET, the MFMIS (metal-ferroelectric-metal-insulator-semiconductor) stacked-nanosheet FeFET structure has an area ratio AR=A_{FE}/A_{MOS} depending on the number of tiers based on (6). This structure has been proposed in [20] to boost the memory window for NVM applications. Nevertheless, the conductance response for stacked-nanosheet FeFET synapse with this structure has rarely been known and merits examination.

$$A_{MOS} = 2*(number\ of\ tiers)*A_{FE} \tag{6}$$

$$E_{FE\ During-wite} = \frac{V_G}{T_{FE}}\frac{C_{MOS}*A_{MOS}}{C_{MOS}*A_{MOS}+C_{FE}*A_{FE}} - E_{dep} \tag{7}$$

$$E_{FE\ After-wite} = E_{dep} = \frac{P_{FE}*A_{FE}}{T_{FE}\left(C_{MOS}*A_{MOS}+C_{FE}*A_{FE}\right)} \tag{8}$$

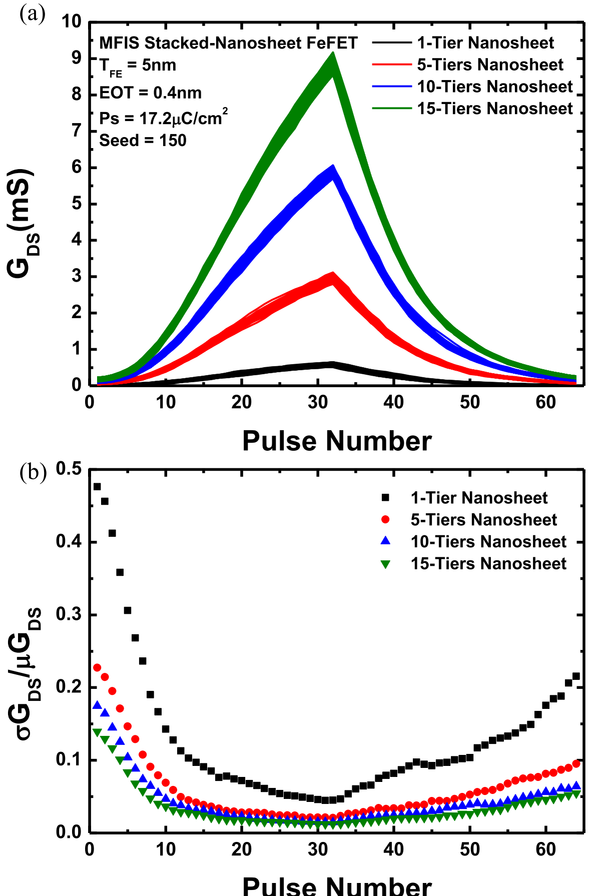

FIGURE 9. **(a) Dispersion in the G_{DS} response for stacked-nanosheet FeFET synapses (with the MFIS structure in Fig. 1) with various numbers of tiers. 150 samples are considered. (b) Increasing the number of tiers may result in a smaller $\sigma G_{DS}/\ \mu G_{DS}$.**

For a FeFET synapse with different ferroelectric area (A_{FE}) from the effective transistor area (A_{MOS}), the during-write E_{FE} and the depolarization field (E_{dep}) can be described by (7) and (8), respectively. To improve the FeFET synapse response under the stimulation of identical pulses, we have known from Section III that it is crucial to reduce the E_{dep}. This can be achieved by increasing the number of tiers (and thus A_{MOS}) as suggested by (8). Increasing the number of tiers can also help maintain a constant during-write E_{FE} for each state by increasing the first term in (7). It can be seen from Fig. 8 that, as the number of tiers increases (i.e., with decreasing area ratio), the linearity and symmetry in the G_{DS} response of the Nanosheet FeFET synapse with the MFMIS structure in Fig. 7 can indeed be improved in addition to a raised G_{max}/G_{min}.

V. FERROELECTRIC STOCHASTIC SWITCHING INDUCED CYCLE-TO-CYCLE VARIAIONS

FeFET synapse with a stacked-nanosheet architecture (see the baseline structure in Fig. 1) is interesting also because it may provide a large number of ferroelectric domains to suppress the cycle-to-cycle variation in the conductance response for

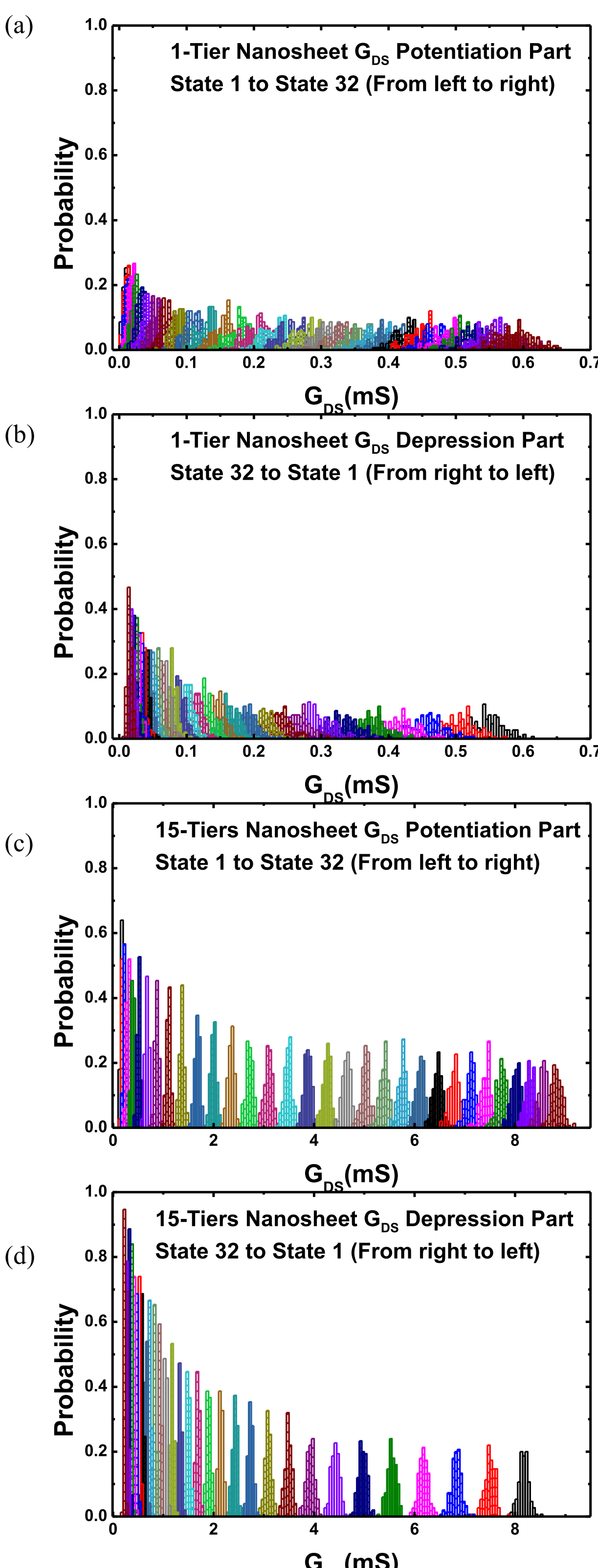

FIGURE 10. **Distributions of 32 G_{DS} states corresponding to potentiation and depression, respectively, in the conductance response for stacked-nanosheet FeFET synapses with 1-tier and 15-tiers design, respectively, showing the impact of tier number.**

a small footprint. The cycle-to-cycle variation stems from the ferroelectric stochastic switching nature [11]. Under short pulse time (small Δt in (2)), small applied voltage (small E_{FE} in (1)) and also a large number of operation states, the increased cycle-to-cycle variation may degrade the robustness of the neural network [21] and demands investigation. In this study, considering the MFIS stacked-nanosheet FeFET structure in Fig. 1, we use 150 samples for a given device design (EOT=0.4 nm, P_S=17.2 μC/cm^2) to evaluate the impact of cycle-to-cycle variations on the conductance response of the FeFET synapse. Fig. 9(a) shows the dispersion in the G_{DS} response for the stacked-nanosheet FeFET synapse with various numbers of tiers. Although the dispersion in Fig. 9(a) increases with increasing tier number, Fig. 9(b) shows that the $\sigma G_{DS}/\ \mu G_{DS}$ for each state actually decreases with increasing the number of tiers. (The σG_{DS} and the μG_{DS} represent the standard deviation of G_{DS} and the mean value of G_{DS}, respectively.) In other words, albeit the ferroelectric switching behavior of each tier is independent, the current of each tier will be collected at the drain, and the current averaging effect will mitigate the impact of domain stochastic switching. Therefore, the $\sigma G_{DS}/\ \mu G_{DS}$ reduces as the tier number increases.

A smaller $\sigma G_{DS}/\ \mu G_{DS}$ also infers a larger noise margin for each state. To examine the distribution for each G_{DS} state in more detail, Fig. 10(a) and (c) show the state distributions (32 states considered) corresponding to the potentiation process for the stacked-nanosheet FeFET synapse with 1-tier and 15-tiers design, respectively. While Fig. 10(b) and (d) show the state distributions corresponding to the depression process for the FeFET synapse with 1-tier and 15-tiers design, respectively. It can be clearly seen that, for stacked-nanosheet FeFET synapse, the immunity to cycle-to-cycle variations and the noise margin for each state can indeed be improved by increasing the number of tiers.

VI. CONCLUSION

We have constructed and analyzed the intrinsic conductance response for stacked-nanosheet FeFET synapses considering cycle-to-cycle variations with emphasis on the challenging identical-pulse stimulation. Our study indicates that a thinner EOT of interlayer oxide and a smaller P_S should be used to suppress the depolarization field and improve the linearity and symmetry of the G_{DS} response. With the stacked-nanosheet architecture, the G_{max}/G_{min} in the G_{DS} response can be boosted by increasing the number of channel tiers without footprint penalty. For a stacked-nanosheet FeFET synapse with an area ratio effect, the G_{DS} response can be further engineered by varying the tier number. Finally, our study shows that the immunity to cycle-to-cycle variations and the noise margin for each state in the G_{DS} response for the stacked-nanosheet FeFET synapse can be improved by increasing the number of tiers.

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