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Analysis of GAA Junction Less NS FET Towards Analog and RF Applications at 30 nm Regime

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ABSTRACT This research focuses on a quantum model created using an entirely novel nanosheet FET. The standard model describes the performance of a Gate-all-around (GAA) Junction-less (JL) nanosheet device with a gate dielectric of SiO_2 and HfO_2, each having a thickness of 1 nm. The performance of both the classical and quantum models of the GAA nanosheet device is evaluated using the visual TCAD tool, which measures the I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, threshold voltage, DIBL, gain parameters (g_m, g_d, A_v), gate capacitance, and cut-off frequency (f_T). The device is suited for applications needing rapid switching since it has a low gate capacitance of the order of 10^{-18}, according to the simulation results. A transconductance (g_m) value of 21 μS and an impressive cut-off frequency of 9.03 GHz are displayed during device analysis. A detailed investigation has also been done into the P-type device response for the same device. Finally, the proposed GAA nanosheet device is used in the inverter model. The NSFET-based inverter, although having higher gate capacitance, has the shortest propagation latency.

INDEX TERMS CMOS inverter, dielectrics, high-k, gate-all-around, quantum effects, transient analysis, vertical oxide stack.

I. INTRODUCTION

Due to its strong channel gate control and ability to scale to the 7 nm technology node, FinFET emerged as the architecture to watch at sub-22 nm nodes. Additionally, the FinFET made a significant contribution to high-performance (HP) applications.

According to the foundry papers (N7) [1], [2], FinFETs are still employed, albeit more often, at the 7 nm technological node. However, it is demonstrated that the FinFET cannot be further scaled down since it became difficult to maintain the device's electrostatic control in next technological nodes. A narrower fin is required for preserving good electrostatics. However, this results in decreased carrier mobility and fluctuating threshold voltage (V_{th}) [3], [4], [5]. To boost performance, the nanowire (NW) and nanosheet (NS) architectures emerged as promising contenders for sub-5 nm nodes [6], [7], [8], [9], [10], [11]. Therefore, it is crucial to evaluate the performance of these devices using physics-based 3D simulations. At nodes smaller than 5 nm, the GAA nanowire FET demonstrates greater electrostatic integrity.

The drive current in NWFETs is constrained by the smaller channel area, which limits their use in HP applications.

The building of stacked NSFETs, which performed better than FinFETs and stacked NWFETs, was proposed by IBM in 2017 [12]. NSFETs may have lower parasitic capacitance for a given active width, improving the effective capacitance-current (C_{eff}-I_{eff}) relationship. NSFET became a strong contender for scaling sub-5 nm technology nodes as a result [12]. Si NSFET has been developed in the meantime to enhance effective channel widths (W_{eff}) for greater current drivability while assuring ideal electrostatics through gate-all-around (GAA) design. Additionally, NSFETs regulate drive current by altering NS width, enabling designs that are compatible with CMOS layouts [3].

A key consideration for the semiconductor industry is transistor size reduction since it directly improves the speed of integrated circuits. The prime objective of design engineers in the chip industry is to design a smaller transistor with low power consumption and operating at high frequency. By redesigning the fin shapes to provide the desired performance, a device can be made smaller [13]. With drain expansion and the imposition of the dual-k dielectrics with underlap criterion for FinFET devices, performance characteristics in RF and analog have improved [14]. Utilizing high-k materials will reduce leakage current [15]. Because they can be scaled up with the same device area and still attain comparable device efficiency, stacked Nano sheet devices are preferable to FinFET and Nanowire devices [16]. The channel must undergo quantum adjustment due to its extreme quantum mechanical confinement, which significantly lowers the saturation current [17]. GAA Nanosheets and Nanowires provide enhanced and flexible performance optimization, and the device settings can be changed by the designer [18]. For quick transition and high I_{ON} upon I_{OFF} ratio, tri-gate junctionless FETs are made for digital circuits [19]. NSFETs with various thresholds can be employed in a variety of exceptionally well and ultra-powerful applications [20]. By offering a selective deposition strategy, RC latency was further improved [21]. The hetero gate dielectric oxide with GAA nanowire (GAANW) displays an improved I_{ON} upon I_{OFF} ratio, higher g_m, reduced DIBL, and perfect SS in comparison to DM devices [22]. The RC delay and the DC/AC performance are improved by adopting the process-induced variation [23]. It is possible to obtain the parameters for an RF-MOSFET with a small-signal model [24]. For drain overlap zones, vertical construction and surface treatment are used to reduce the detrimental effect of SCE impacts [25]. Surface roughness needs to be kept to a minimum for the device to function properly [26]. The thickness, channel orientation, and surface orientation of the silicon are all crucial parameters in FinFETs [27]. Improved short-channel effects and even better performance in both DC and AC studies are shown by multi-gate FET performance studies, proving it is suited for low-power applications [28], [29], [30], [31], [33], [34], [35], [36], [37]. With the aid of the review, the traditional tri-gate model is created using the same parameters [19] and implemented using a simulation platform to match the drain current. In addition, to improve performance, a fourth gate is added to the bottom of the tri-gate model to create a gate that surrounds the device (Quad gate model). One further feature—the effects of the quantum model on the classical model—has also been added to the device to make it suitable for use in analog and RF applications. To see the flexibility in the circuit environment, the 3D inverter model is designed using both the classical and quantum models. The Visual TCAD professional platform is used for the entire procedure.

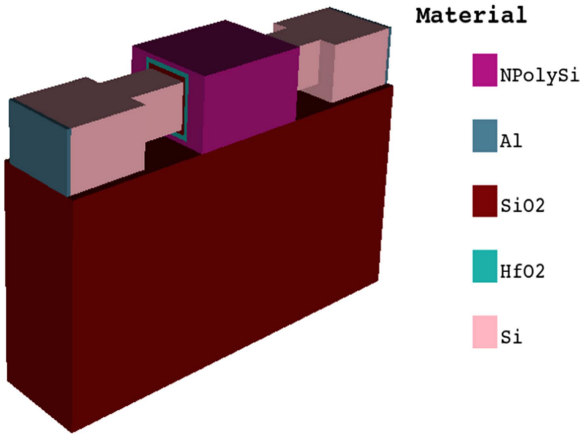

FIGURE 1. Proposed Nanosheet device (3D view).

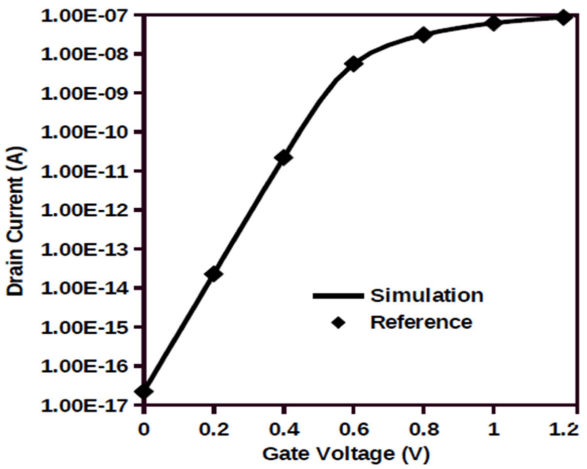

FIGURE 2. TCAD device calibration using experimental data at $V_{DS} = 0.1$ V.

II. PROPOSED DEVICE STRUCTURE AND SIMULATION METHODOLOGY

Fig. 1 depicts the quad gate containing multilayer gate oxide and a junction-free Nano-sheet device in three dimensions. We take into account the parameters using [19], [24], and [32]. To finish the changes by constructing gate all the way around, a gate is also built at the bottom. In addition, SiO_2 and HfO_2 gate oxides are stacked with the same gate oxide thickness to prevent gate leakage. Table 1 lists all the additional improvement parameters and shows their geometric properties. Uniform doping with an acceptor concentration of 1×10^{19} cm^{-3} is maintained throughout the channel region. The dielectric constants are set to be 3.9 (low-k) and 22

TABLE 1. Structure Parameters.

Structure Parameters	Dimension
Channel length (L_g)	30 nm
Channel Width (W)	10 nm
Channel Thickness (t_{Si})	10 nm
Channel Doping (N_a)	1×10^{19} cm^{-3}
Work function (Ø)	5.1 eV
Gate length/ Fin length	15
Low - k Oxide Layer Thickness	1
High - k Oxide Layer Thickness	1
Pad length of source and drain	20
Fin Width	10
Fin Height	10

(high-k). The operating voltage V_{DD} of 0.1 V and 1 V are considered during linear and saturation mode of operation respectively. Topological architecture for both classical and quantum components is shown in Table 1. The work function of N-type polysilicon and operating temperature are chosen as 5.2 eV and 300 K, respectively.

The carrier temperature, electric field, and voltage each affect the current across the proposed GAA device. By resolving several density-gradient drift-diffusion equations, a detailed simulation of a 3D quantum mechanically corrected device is performed. The Auger model is used to take carriers' lifetime and current density into account. Shockley-Read-Hall models are included to take into account generation and recombination effects. Schenk's model and Caughey-Thomas model are used to account for bandgap narrowing effects brought on by high doping as well as velocity saturation effects. The nonequilibrium Greens function approach is used to initially validate all of the device parameters. The thin-layer mobility model is used to take interface mobility degradation phenomena into account. The quantum drift-diffusion model (QDDM) from Visual TCAD is also used in the simulation, and it takes into account the quantum effects at lower nodes. The structure and their corresponding parameters are considered, as mentioned in Table 1, during simulation.

III. RESULTS & DISCUSSION

The GAA structure is designed and calibrated with experimentally fabricated device characteristics to validate the considered models during simulation [19]. The calibration shows that the simulated drain current (I_D) and experimental data have a reasonable degree of agreement, as shown in Fig. 2.

The same geometric characteristics as the fabricated device structure are used to generate a quad gate junctionless FET (QGJLFET) using a 3D visual TCAD device simulator. The DC transfer characteristics are obtained by obtaining drain current at a gate voltage range of 0 V to 1.2 V by keeping V_{DS} constant at 0.1 V. The findings of the overlapped QGJLFET

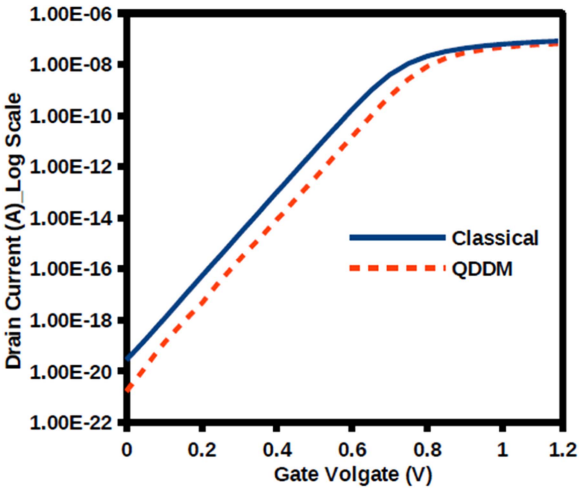

FIGURE 3. Transfer characteristic of the device at V_{DS} = 0.1 V for quantum and classical models.

TABLE 2. Comparison of Performance Parameters of Both the Models

Drain current Model	Operating mode	I_{off} (A)	I_{on} (A)	I_{on} to I_{off} ratio ($\times10^{13}$)
Classical	Linear	2.79×10^{-20}	8.6×10^{-8}	0.3
	Saturation	1.79×10^{-19}	3.7×10^{-7}	0.2
Quantum	Linear	1.65×10^{-21}	6.8×10^{-8}	4.11
	Saturation	2.36×10^{-19}	2.4×10^{-7}	0.1

simulation show a sizable leakage current. Using an underlap condition reduces the leakage current of a quad gate overlap configuration.

A. EFFECT OF QUANTUM MECHANICS FOR PROPOSED DEVICE

As the proposed device's channel length is 30 nm, the initial classical model is simulated using the same design parameters as those in [19] in a visual TCAD platform environment with gate voltage variations between 0 and 1.2 V at a constant VDS of 0.1 V in linear and 0.75 V in the saturation region. The quantum mechanical implications of the same model have also been considered and implemented under the same voltage conditions. In Fig. 3, the impact of both models' outcomes is examined and highlighted. The obtained threshold voltage by utilizing the quantum model is 0.067 V less than the classical drift-diffusion model. When the quantum correction model is employed during simulation, the off-state leakage current soars and the on-state current is also decreased. Tables 2 and 3 present the comparison results for the linear and saturation results for OFF current, ON current, and $I_{ON}/IOFF$ current for the classical and quantum models.

The I_{ON} of $8.692\times\ 10^{-8}$ A is obtained while operating the device in linear mode for the classical drain current

TABLE 3. DC Analysis Parameters for Classical and Quantum Analysis

Analysis	Threshold voltage (Volts)	DIBL (mV/dec)	SS (linear mode) (mV/dec)	SS (Saturation mode) (mV/dec)
Classical	0.651	8.66	61.31	61.03
Quantum	0.643	8.68	61.18	60.94

model, while I_{ON} is slightly smaller with the quantum model. Moreover, the linear model shows better I_{ON} compared to the quantum model due to better electron mobility. Whereas while device operating in saturation mode shows exactly the inverse. The I_{OFF} of 2.791×10^{-20} Amp and 1.795×10^{-19} amp are obtained while the device is operating in linear mode and saturation mode, respectively, for the classical drain current model. Similarly, I_{OFF} of 1.654×10^{-21} Amp and 2.378×10^{-19} amp are noticed while operating the device in linear mode and saturation mode, respectively, for the quantum drain current model. Hence, the highest I_{ON}/I_{OFF} ratio of 4.11×10^{13} is obtained for the quantum model during the linear operating mode of the device.

B. DEVICE PERFORMANCE AT RF

This section describes in detail the analog performance measurements used in the investigation. During simulation, physical models such as band-to-band tunneling (BBT), Lombardi mobility, drift-diffusion, and the carrier recombination mechanism have been considered. The Poisson-Schrodinger equation has not been solved as the density gradient model is used to deal with quantum confinement effects.

Transconductance (g_m) effectively converts voltage into current and is a measure of device amplification. It is the change in drain current towards fluctuation of voltage at gate (VGS) by keeping V_{DS} constant as per (1).

$$g_m = \frac{\partial I_d}{\partial V_g}. \tag{1}$$

Fig. 4 depicts the corresponding g_m plot with V_{GS} in the range 0 V to 1 V for the quantum and classical models at a constant V_{DS} of 0.1 V. The plot displays a peak g_m of 21 μS at V_{GS} of 0.8 V with the classical drain current model and a peak gm of 20 μS at VGS of 0.9 V with the quantum drain current model. Compared to QDDM, the classical model exhibits better g_m and ensures better gain and amplifying capabilities.

Output conductance (g_d) effectively converts voltage into current and is used to measure device efficiency. It is assessed as a change in the ratio of source voltage to a change in drain current at a specific value of V_g. It is written as in (2).

$$g_d = \frac{\partial I_d}{\partial V_d}. \tag{2}$$

The variation of g_d with V_{DS} for the quantum and conventional models is demonstrated in Fig. 5. The saturation zone

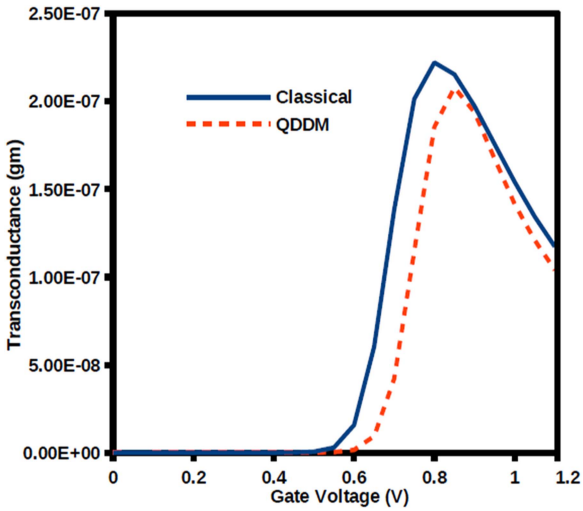

FIGURE 4. Transconductance plot for both the models at $V_{DS} = 0.1$ V.

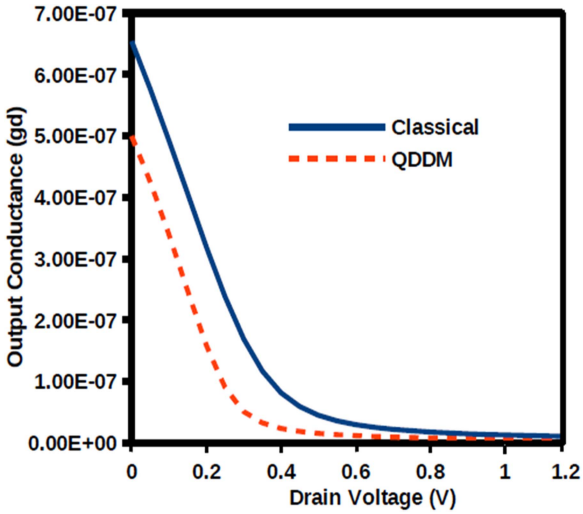

FIGURE 5. Output conductance plot for both the models.

has undergone a thorough AC investigation with a drain to source voltage (V_{DS}) set to 1 V. For analog applications, a low g_d value is desired since it enables better DIBL and channel length modulation by increasing the device's inherent gain. The outcome demonstrates that the quantum model's output conductance exhibits a better lower g_d value of 5E-07 than the classical model, which exhibits a higher g_d of 6.5E-07. The intrinsic voltage gain of a device is the maximum possible voltage gain of the device. Calculating intrinsic gain (Av) is the ratio of g_m and gd. Fig. 6 shows the variation in intrinsic gain with respect to gate voltage (V_{GS}), as seen in (3), with the drain bias held at saturation 1 V.

$$A_V = \frac{g_m}{g_d}. \tag{3}$$

In contrast to the classical model's gain value of 14, the quantum model's intrinsic gain displays a higher gain value of 27. The intrinsic gain is noticed almost double for the QDDM

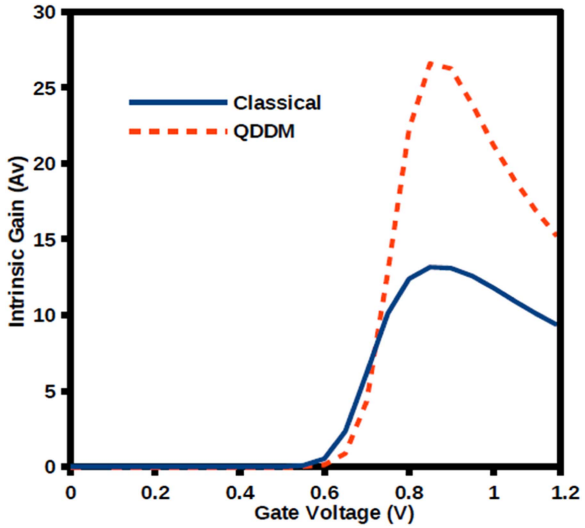

FIGURE 6. Intrinsic Gain plot for both the models.

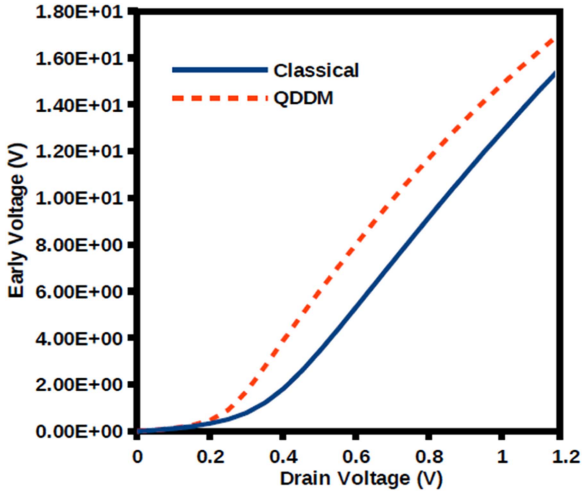

FIGURE 7. Early voltage comparison among both the models.

model, which clearly shows the efficiency of the proposed model. For both the quantum and classical models, the intrinsic gain plot is shown in Fig. 6. The intrinsic gain and early voltage (V_e) of analog circuits should be high, as given by (4), whereas the g_d should be low.

$$V_e = \frac{I_D}{g_d}. \tag{4}$$

The early voltage of the quantum model shows the higher voltage of 17 V than the classical model of 15.9 V with fixed VDS of 1 V and varying V_{GS} 0 V to 1.2 V. Fig. 7 displays the variation of Ve for the quantum and classical models.

C. POTENTIAL DISTRIBUTION IN CLASSICAL AND QUANTUM DEVICE

To ensure consistent charge carriers throughout the channel and prevent channel leakage current, it is crucial to forecast potential distributions over the channel and core. The potential

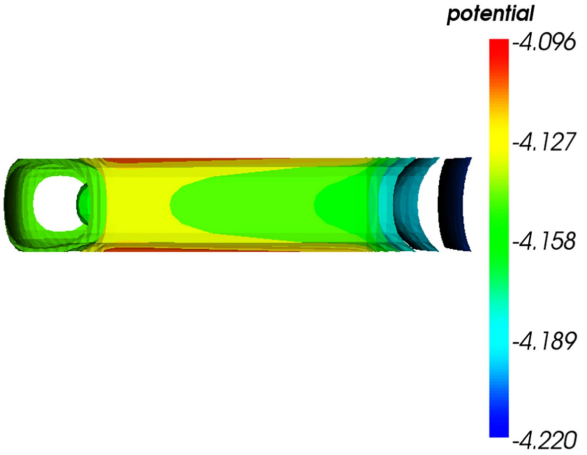

FIGURE 8. Potential distribution of the classical structure over the core and surface.

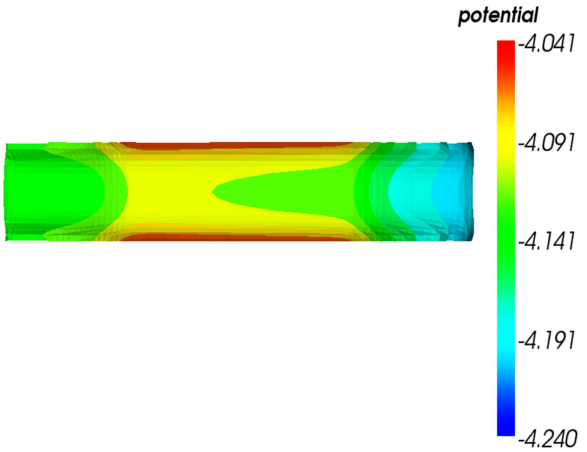

FIGURE 9. Distribution of quantum structure's potential over the core and surface.

distribution over a Quad gate quantum effect with gate oxide stack is illustrated in the following 3D view of both models. The Nano-sheet device structure is assessed by contrasting the quantum and classical results.

Figs. 8 and 9 display the potential distribution inside the channel for conventional quad gate nanosheets and QDDM quad gate oxide stacking nanosheets, respectively. Over the channel's surface and in the center, the potential is constant. Because of its link to vacuum potential, the potential redistribution in the channel has a negative value.

D. GATE CAPACITANCE (C_{GG})

The total gate intrinsic capacitance (C_{intr}) is the sum of the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}). The C_{gd} is miller capacitance or parasitic capacitance. The $C_{gg} = (C_{intr} + C_{para})$ and C_{gd} values are low for FinFET compared to Nanowire FET and NSFETs. Delay in switching results from a high capacitance value. A low value of C_{gg} is crucial for improved RF performance and a faster switch. The total gate capacitance is obtained during AC simulations with

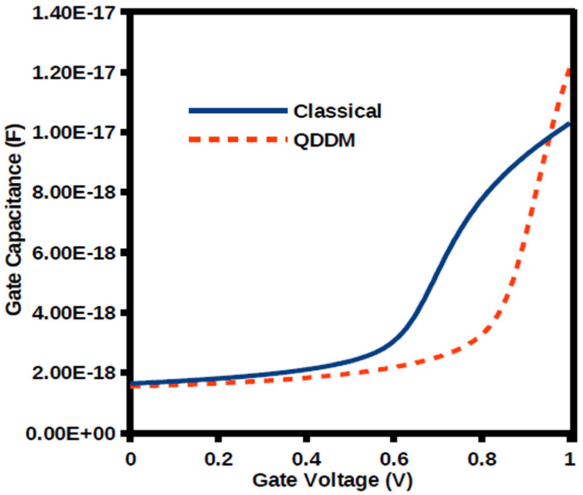

FIGURE 10. Comparison of Gate Capacitance (C_{gg}).

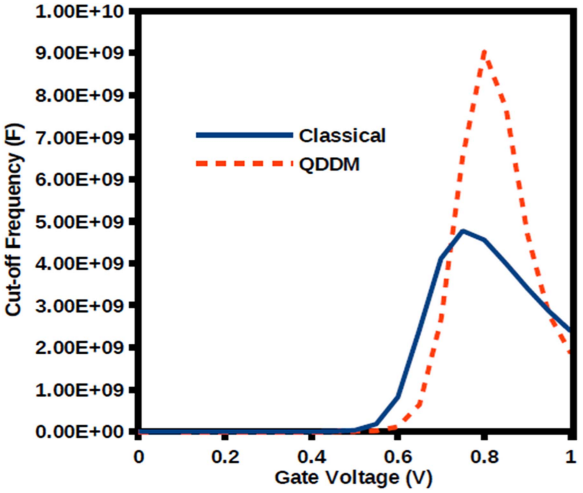

FIGURE 11. Variation of f_T with V_{GS}.

1MHz input frequency. According to Fig. 10, the C_{gg} value is shown to be in the range of 10^{-18} F.

D. CUT-OFF FREQUENCY (F_T)

The unity gain cutoff frequency, a critical RF design parameter based on transconductance and total gate capacitance, can be represented using (5).

$$f_T = \frac{g_m}{2\pi\ \left(C_{gs} + C_{gd}\right)}. \tag{5}$$

Higher peak frequencies and greater susceptibility to high-frequency impulses characterize devices that are well suited for frequency-switching circuitry. The analysis showed a maximum f_T of 9.03 GHz at $V_{GS} = 0.8$ V for the QDDM model, which is double that of the classical model, as shown in Fig. 11. The higher cut-off frequency helps the device to work in high-frequency device applications.

HfO_2 is now added to the gate oxide stack as a high-k material to emulate a quad gate using a gate oxide stack junction-less Nano-sheet P-type device. The thickness of

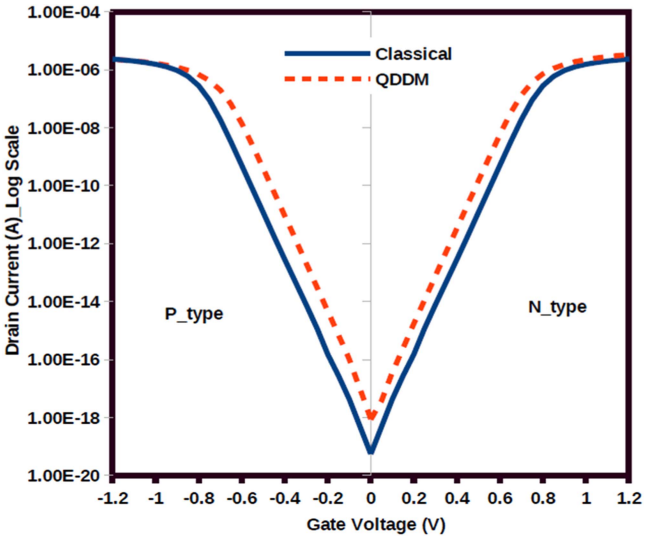

FIGURE 12. Transfer characteristics for classical and quantum N and P type devices at $V_{DS} = 0.1$ V.

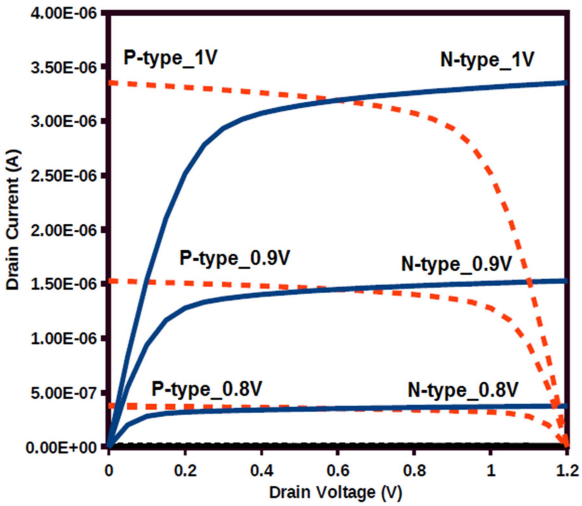

FIGURE 13. Output characteristics of N-type and P-type device using quantum model.

HfO_2 and SiO_2 are both 1 nm, while all other oxides have a thickness of 2 nm. For the effective oxide thickness (EOT), it is 1.156 nm. The transfer characteristics for both N-type and P-type devices with gate oxide stack Nano-sheets are displayed in Fig. 12 and matched with the precise origin and node. Using a gate oxide stack Nano-sheet, the output characteristics for N-type and P-type quad gates are simulated over a range of VGS, including 0.8 V, 0.9 V, and 1 V, and presented in Fig. 13.

Both N-type and P-type Gate stack Junction-less FETs are arranged as shown in Fig. 14 to be operated as a complimentary logic to test for inverter application. The inverter's structure and transient response have been examined using a logic pulse delivered to maintain V_{DS} at 1 volt. Fig. 15 displays the transient response of the classical Quad gate and QDDM Quad gate. During circuit simulation, the inclusion

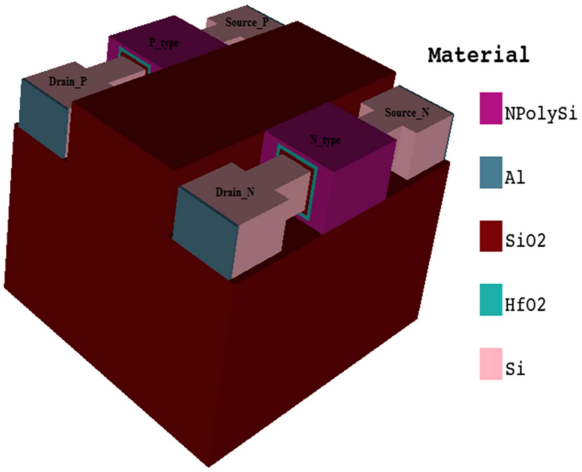

FIGURE 14. CMOS Inverter using Quad gate with gate oxide stack junction-less FET.

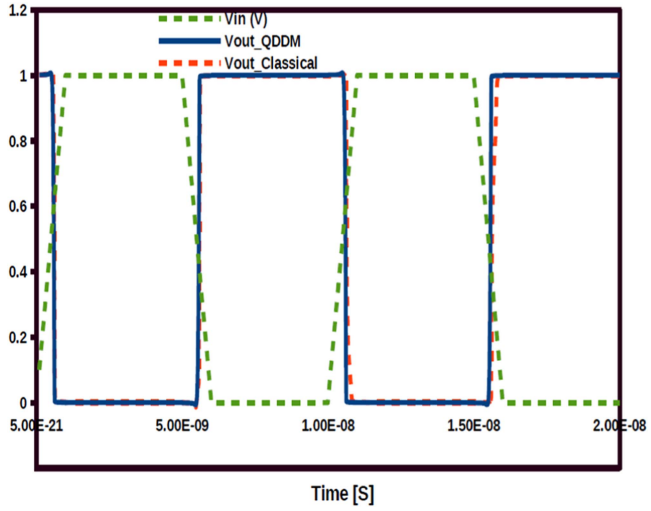

FIGURE 15. Transient response of Quad gate with classical and QDDM Inverter.

of both classical and quantum current models doesn't portray any difference in transient response due to seldom effect on delay.

IV. CONCLUSION

The applicability of the quad gate with gate oxide stack junction-less device in analog and RF domain applications is carefully investigated. High-temperature doping methods are not required because the device may be made much more easily and almost without any doping. Device performance is impacted by quantum mechanical processes. The device is demonstrated to be suitable for use in circuits for quick switching by the identification of its lowered output conductance and high unity current gain frequency. Additionally, the intrinsic gain is greater. It might be argued that the device's improved performance metrics make it appropriate for faster-switching analog/RF applications.

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