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Enhancing the Performance of E-Mode AlGaN/GaN HEMTs With Recessed Gates Through Low-Damage Neutral Beam Etching and Post-Metallization Annealing

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ABSTRACT This study investigated the electrical properties of AlGaN/GaN high-electron-mobility transistors (HEMTs) with varied recess depths under the gate electrode. We demonstrated a recess depth of approximately 6 nm, which was achieved through neutral beam etching (NBE) technique with a low etch rate of 1.8 nm/min, resulting in device enhancement-mode (E-mode) behavior with threshold voltage (V_{th}) of 0.49 V. The effects of post-metallization annealing (PMA) on the device performance were also examined. The results revealed that PMA treatment improves the DC characteristics of the devices, including maximum drain current (I_{DMAX}), transconductance (g_m), subthreshold swing (SS), on-off ratio, and off-state leakage current, with maximum enhancement percentage of 18.3% for I_{DMAX}, 3758% for on-off ratio, and 54.3% for SS. Moreover, this study compared the recess depths of metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) with the SiN dielectric layer. The results showed that MIS-HEMTs exhibit more negative V_{th} values, which can be attributed to the controlled surface states achieved through passivation.

INDEX TERMS AlGaN/GaN HEMTs, recess gate, neutral beam etching, post-metallization annealing.

I. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) are regarded as promising candidates for high-frequency and high-power applications for the next generations due to the natural two-dimensional electron gas (2DEG) channel near the AlGaN/GaN interface, allowing the device to function even in the negative gate bias (i.e., depletion mode (D-mode)). A Si MOSFET combined with GaN HEMT is commonly used to achieve the enhancement mode (E-mode). However, the additional Si driver circuit increases the system's cost and complexity while adding parasitic effects and delay. Thus, fabricating discrete normally-off GaN HEMTs is necessary. Some methods have been studied to achieve E-mode characteristics, including fluorine ion implantation [1], [2], p-GaN gate [3], and recess gate [4], [5]. Among them, recess gate is one of the simplest methods for accomplishing the normally-off characteristic. In this method, the AlGaN barrier layer under the gate region is thinned down to lift the energy band at the AlGaN/GaN interface, thus, causing V_{th} to move towards positive. However, there are some issues with recess gate

etching. First, controlling the etching depth is extremely difficult. Since the thickness of the AlGaN barrier layer is generally around 20 nm, controlling the etching depth is important to avoid etching out all the AlGaN barrier layer. Second, the maximum current density declines due to the thinning of the AlGaN barrier layer, reducing the polarization effect and the 2DEG density. Third, recess etching using plasma induces surface damage in the gate region, where electron mobility decreases; hence, decreasing the current density due to the surface roughness scattering effect [6].

Low-damage etching and the recovery of the electrical characteristic loss in exchange for E-mode operation are thus critical in engineering the V_{th} of HEMTs for recess etching. Neutral beam etching (NBE) and post-metallization annealing (PMA) were utilized to overcome this problem in this study. NBE has been demonstrated to have low etching damage on the substrates due to the blocking of the energetic ion bombardment and the ultraviolet/vacuum ultraviolet (UV/VUV) irradiation. Therefore, NBE could improve the performance of semiconductor devices [7], [8], [9], [10]. To control the defect generation associated with conventional plasma, we utilized the NBE technique for recess etching.

Several reports illustrated the annealing effect after gate metal deposition. Kim et al. proposed gate leakage and breakdown mechanisms before and after PMA [11]; Lee et al. demonstrated improved device uniformity and breakdown voltage after PMA by reducing the trapping centers on the AlGaN surface and/or GaN buffer layer [12]; Mazumder et al. investigated the mechanisms of the reduction of gate leakage in AlGaN/GaN MOS-HEMTs by optimizing the post-gate annealing treatment [13]; Lu et al. reported a two-step process combining PMA and O_2 plasma treatment reduced the device off-state leakage current [14]. However, most research on improving device characteristics requires a long-time (>10 min) annealing, or focuses solely on D-mode devices [13], [15], [16]. This study employed significantly shorter PMA treatment times, which led to notable improvements in the DC characteristics.

Metal-insulator-semiconductor HEMTs (MIS-HEMTs) have been well-known to enhance the device stability, long-term reliability, breakdown voltage, and current collapse, etc, compared with the conventional HEMTs due to its high-dielectric constant nature and the passivated surface states of III-V materials [10], [17], [18], [19], [20], [21], [22]. Furthermore, some research reported that the existence of the gate dielectric layer results in the V_{th} shift due to border traps and interface states [23], [24]. However, limited reports studied the influence of the gate dielectric layer on V_{th}. In this study, we demonstrated: (i) the electrical characteristics of both D-mode and E-mode AlGaN/GaN HEMT devices with varied recess depths using NBE before and after a 1-min PMA treatment. The enhancement of DC characteristics after PMA for I_{DMAX}, on-off-ratio, and SS is 18.3%, 3758%, and 54.3%, respectively. This study also examined (ii) how the existence of SiN dielectric influences the V_{th} adjustment with and without recess gate etching.

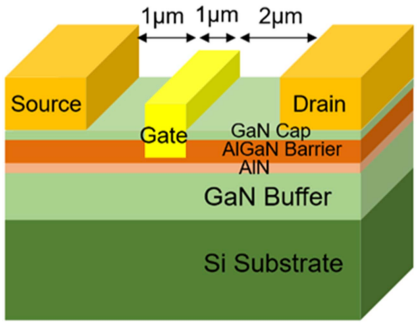

FIGURE 1. Cross-sectional schematic structure of a recessed AlGaN/GaN HEMT, where L_{sg} is 1 μm, L_{gd} is 2 μm, and L_g is 1 μm.

II. DEVICE FABRICATION

Fig. 1 illustrates the device structure used in this study. The GaN-on-Si epitaxial layers consist of the following: a 2 nm GaN capping layer, a 20 nm undoped AlGaN barrier layer, a 0.8 nm AlN, and a 3.7 um undoped GaN buffer layer on the Si substrate. The device structure started from the mesa area with an etching depth of ∼250 nm and was defined using neutral beam etching (NBE), followed by the Ohmic region patterning. Before the Ti/Al/Ni/Au (20/120/50/60 nm) metal stack was deposited, the sample was cleaned by an HCl (1:10) solution. The Ohmic contact was formed after 30 s of rapid thermal annealing at 850 °C in an N_2 ambient. The gate region was then patterned, and the recess etching was performed using NBE with different etching depths. Afterward, a gate metal stack of Ni/Au (20/100 nm) was deposited using E-gun. Lastly, a 1-min forming gas PMA at 400 °C in 95% N_2 and 5% H_2 ambient was performed. The fabrication process of the MIS-HEMTs was similar to that of the HEMTs, except that after mesa etching, a gate pattern was first formed and etched via NBE. Subsequently, a ∼17 nm SiN film was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) at 300°C. This was followed by the Ohmic contact patterning and SiN etching with NBE using fluorine-based dry etch. Then, Ohmic metal was deposited and the second gate lithography was performed as well as gate metal deposition.

The gate recess structure with four different depths was fabricated by NBE. The NB equipment is depicted in Fig. 2. A high-aspect-ratio carbon aperture electrode between the plasma chamber and the process chamber was used to neutralize the ions in the plasma. While passing through the carbon aperture, the charged particles were neutralized and became neutral atoms, blocking the UV/VUV radiation. As a result, a damage-free etching was achieved. A device without a recess gate was also fabricated. The source-to-gate distance, gate-to-drain distance, and gate length were 1 μm, 2 μm, and 1 μm, respectively.

III. RESULTS AND DISCUSSION

The etch rate of the AlGaN/GaN stack was determined at 1.8 nm/min using transmission electron microscopy (TEM). Fig. 3(a) shows the resulting relationship between the etch depth and etch time of GaN/AlGaN stack layers. As shown

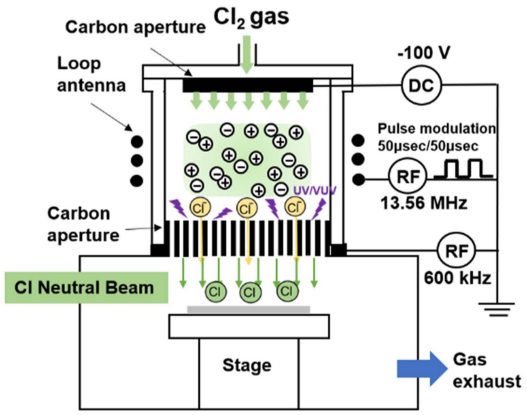

FIGURE 2. Schematic figure of the neutral beam system. The process chamber and plasma chamber are separated by a carbon aperture. A Cl neutral beam was formed after Cl^- ions passed through the aperture.

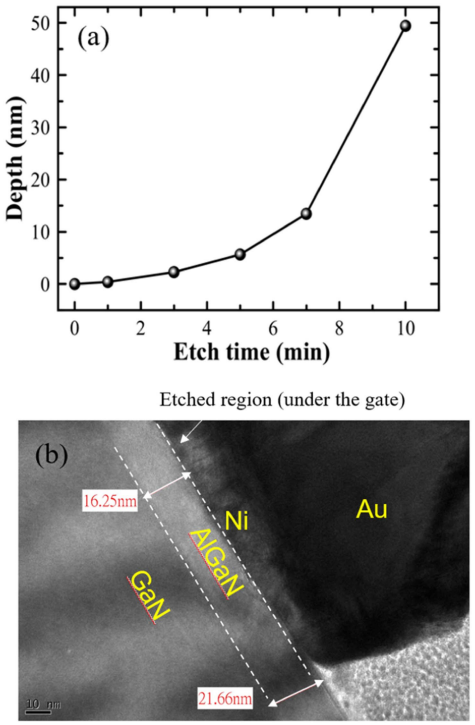

FIGURE 3. (a) Recess etch depth versus etch time measured by TEM, and (b) TEM image of the gate region for 5-minute recess time.

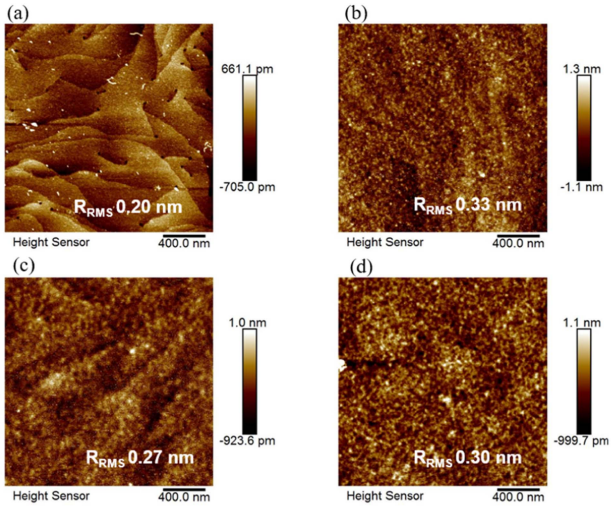

FIGURE 4. 2 μm x 2 μm surface roughness of samples (a) before etching and after NB etching for (b) 3 minutes, (c) 5 minutes, and (d) 7 minutes.

TABLE 1. Electrical Characteristics for Five Different Gate Recess Depths: 0, 2, 6, 13 nm.

Recess depth (nm)	No recess	2	6	13
V_{th} (V)	-2.66	-0.28	0.49	1.50
I_{DMAX} (mA/mm)	829	186	33.0	2.3
g_m (mS/mm)	251	130	43.8	3.8
SS (mV/dec)	123	380	205	347
On-off ratio	1.3×10^5	1.6×10^4	2.6×10^4	837
I_g (mA/mm)	0.06	9.4	56.0	72.9

in the figure, the etch depth and etch time did not show a linear relationship because the etching was performed on the same AlGaN/GaN structure used for the device fabrication. Since the AlGaN material has relatively higher hardness than GaN, etch time and depths observe a nonlinear relationship. Fig. 3(b) depicts a TEM image for a 5-min recess time, reducing the AlGaN barrier layer thickness under the gate. An atomic force microscope (AFM) was performed to examine the surface quality of the NB etching samples, as shown in Fig. 4. Before recess etching, the root-mean-square surface roughness of 2 μm $\times$ 2 μm scan size was 0.2 nm. The surface roughness did not increase significantly after recess etching via NB for 3, 5, and 7 min. Surface roughness typically observes a positive correlation with both etch time and depths. When samples are exposed to an etchant for a longer duration, they are more likely to encounter plasma instability and residual etching, which increases surface roughness. However, this study observed that despite the increasing etch depths, the surface roughness remains stable, suggesting that the reduction in I_{DMAX} with increasing etch depths is primarily attributed to the thinning of the AlGaN barrier, rather than surface roughness scattering caused by NB recess etching in this study.

The transfer characteristics measured at $V_{DS} = 6$ V of recessed HEMT devices are depicted in Fig. 5. Meanwhile, Table 1 lists the extraction of the DC characteristics for different recess depths, such as V_{th}, I_{DMAX}, g_m, SS, on-off ratio, and gate leakage current (I_G). Here, the V_{th} was calculated as the gate voltage at which the drain current equals 1 mA/mm.

The extracted V_{th} was -2.66 V for the device without recess etching, which was in a D-mode operation. When the recess depth reaches 6 nm, the device became an E-mode. However, the drain current reduces with increasing the recess

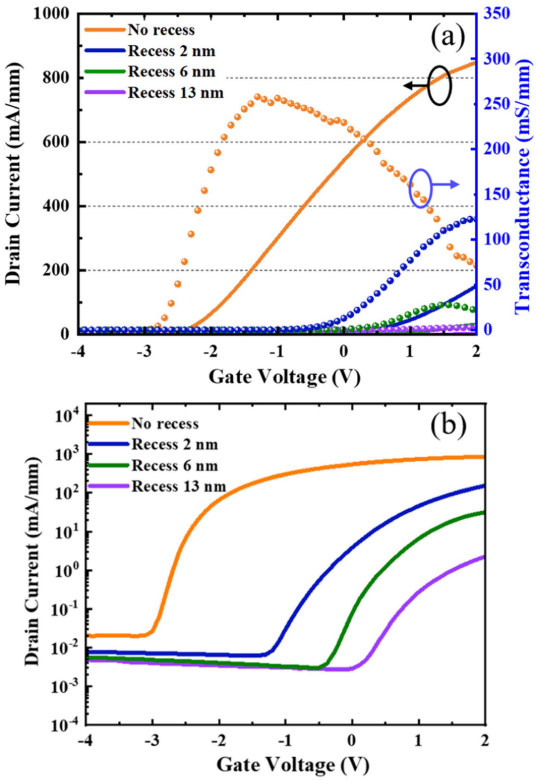

FIGURE 5. (a) Transfer characteristic curves in linear scale and transconductance curves, and (b) transfer characteristic curves in log scale of HEMTs devices with different recess etch depths.

depth due to the AlGaN barrier layer thinning, reducing the piezoelectric effect of AlGaN over GaN. The g_m has a similar trend as shown in Fig. 5(a). The on-off ratio decreases from 1.3×10^5 to 8.4×10^2 as the recess depth reaches 13 nm, which is inevitable because of the on-current reduction caused by the barrier layer thinning. Moreover, the electrons are easier to penetrate through the barrier layer to the surface, resulting in larger I_G.

Although there is a trade-off between obtaining the E-mode devices and losing some DC characteristics, there is a solution. Fig. 6(a) and (b) illustrate the transfer curves and the g_m before and after forming gas PMA treatment, respectively. The figures show that after forming gas PMA, almost all recess-depth samples demonstrated improvement in the DC characteristics, such as I_{DMAX}, g_m, on-off ratio, SS, and I_G. The V_{th} shifted towards positive after forming gas PMA. Table 2 compares the DC characteristics before and after the forming gas PMA treatment. Fig. 7 presents a bar chart illustrating the percentage difference in some DC characteristics for better comparison. The I_{DMAX} values increased for almost all samples with varied recess depths, except for the sample with a 13 nm recess, which may be attributed to the extremely thin barrier layer. The non-recess sample showed a maximum I_{DMAX} improvement of 18.3%. After the PMA treatment, there was a significant improvement in the device's on-off ratio, I_G, and SS with a maximum enhancement of 3758% in the on-off ratio, and 53.5% and 54.3% reduction

TABLE 2. Electrical Characteristics Before and After Forming Gas PMA (Separated by Slashes) for Four Different Gate Recess Depths

Recess depth (nm)	No recess	2	6	13
V_{th} (V)	-2.66/-2.78	-0.28/0.19	0.49/0.76	1.50/3.30
I_{DMAX} (mA/mm)	829/**980**	186/**189**	33.0/**33.6**	2.3/0.1
g_m (mS/mm)	251/**274**	130/**177**	43.8/**50.5**	3.8/0.3
SS (mV/dec)	123/**108**	380/**174**	205/**126**	347/**187**
On-off ratio	1.3×10^5 /$\mathbf{1.8\times10^6}$	1.6×10^4 /$\mathbf{6.3\times10^5}$	2.6×10^4 /$\mathbf{1.2\times10^5}$	837/$\mathbf{9.7\times10^3}$
I_g (mA/mm)	0.06/**0.03**	9.4/**7.1**	56.0/**50.4**	72.9/**52**

Bold font indicates better performance of forming gas PMA.

in I_G and SS, respectively. Moreover, the on-resistance also decreased from 119.0 Ω to 98.5 Ω, as shown in Fig. 6(c). These demonstrations reveal the effects of forming gas PMA. It is speculated that the defects and trapping centers are generated during the gate metal deposition, recess etching, and/or originally existed in the surface or bulk of the epitaxial layers [8], [25]. Those defects or traps act as positive charges. After the 1-minute forming gas PMA treatment, the positive charges can be reduced, allowing the gate to attract fewer electrons in 2DEG channel. Thus, the V_{th} can be positively shifted. Compared to other research [11], [12], [13], [14], [15], [16], [26], [27], this study can achieve significant improvement using short-time PMA. It is speculated that the low-damage NBE does not generate bond-breaking on the substrate surface caused by UV/VUV irradiations. Rather, it creates fewer deep traps than the conventional ICP etching, thereby requiring less time for the annealing to repair. The speculation is supported by previous research [7], [8], [9], [10], providing a strong hint for the NB advantage in gate recess etching for AlGaN/GaN HEMTs.

Fig. 8 illustrates the cross-sectional structure of the MIS-HEMT with a ∼17 nm SiN dielectric layer used in this study, and the DC characteristics of the MIS-HEMT devices are also investigated as shown in Fig. 9(a). The shift of the V_{th} with respect to the recess depth is not as much as the samples without the SiN dielectric layer. For the sample with a 4 nm recess, the shift of the V_{th} was around 6 V, which is much larger than that without the SiN dielectric layer, where the V_{th} shift of 3.1 V was exhibited even with a larger recess depth of 6 nm. Fig. 9(b) shows the transfer characteristics of the devices with and without the SiN dielectric layer. Both samples had no recess to address the influence of the SiN dielectric layer. With a SiN dielectric layer of 17 nm, the V_{th} was displaced 12.5 V to the negative. This is due to the reduced donor-like traps in the interface [28], [29]. The off-state drain current increased with the SiN dielectric layer. Previous research suggests similar results, which considered the damage induced during the SiN deposition by PECVD [10], [30], [31]. Hence, in order to fully leverage the benefits of the SiN dielectric layer, it is essential to carefully balance

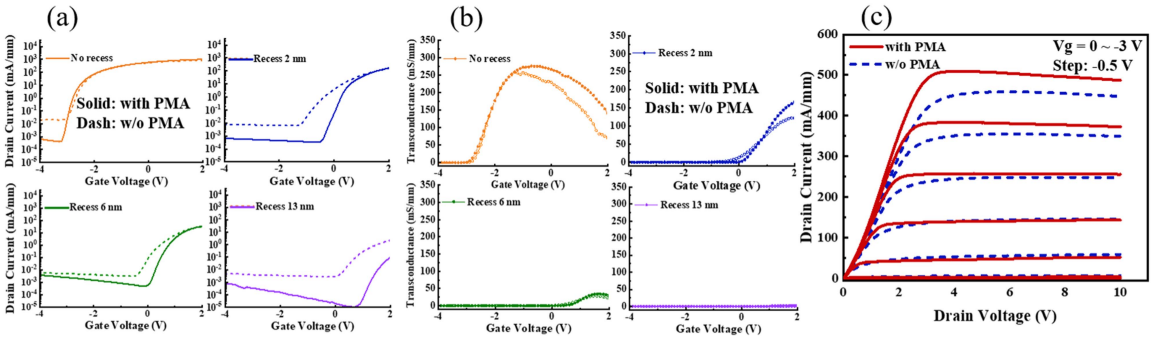

FIGURE 6. **(a) Transfer characteristic curves vs. gate voltage curves, (b) transconductance of HEMTs devices with different recess etch depths, and (c) output characteristic curves with and without forming gas PMA.**

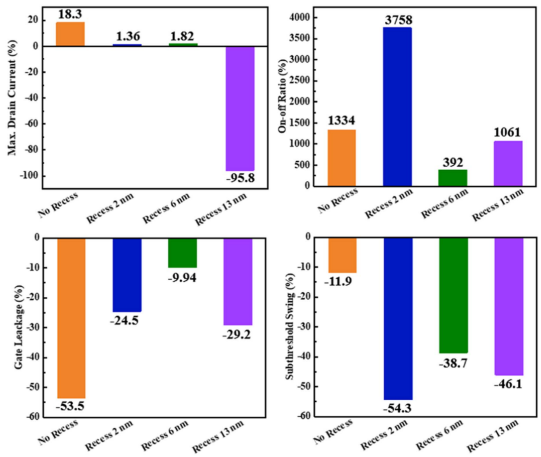

FIGURE 7. **Percentage difference of I_{DMAX}, on-off ratio, I_G, and SS for different recess depths.**

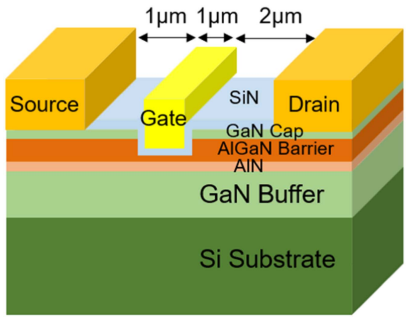

FIGURE 8. **Cross-sectional schematic of recessed AlGaN/GaN MIS-HEMT.**

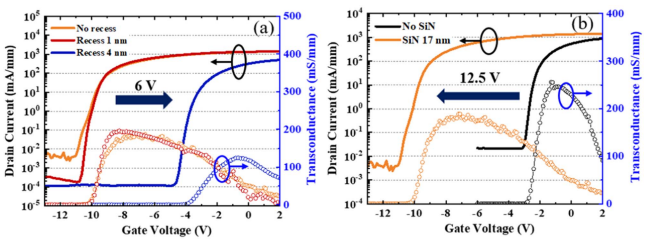

FIGURE 9. **Transfer characteristics of (a) ~17 nm SiN gated HEMTs with 2 different recess depths, and (b) different thickness of SiN gated HEMTs without recess.**

the trade-off between the improved I_{DMAX} and reliability, and the potential drawbacks such as reduced V_{th} tuning efficiency and some DC characteristics like off-state current, g_m, etc. These concerns could be mitigated by further optimization of the SiN film quality and the deposition environment.

IV. CONCLUSION

In this study, we investigated the electrical characteristics of the E-mode AlGaN/GaN HEMTs with varied recess depths by using NBE. The AFM results and previous reports confirmed NB's excellent etching performance. Increasing the recess depth beneath the gate electrode influenced the V_{th} to move positively, eventually leading to the E-mode behavior at a depth of 6 nm. PMA was performed on different recess-depth samples to repair the damage caused by the metal deposition and/or recess etching. Most electrical parameters, such as the on-off ratio, g_m, off-state leakage current, and SS, improved with a maximum enhancement percentage of 18.3% for I_{DMAX}, 3758% for the on-off ratio, 53.5% for I_G, and 54.3% for SS. Moreover, the V_{th} with smaller recess depths became more positive after the PMA due to the improved interface conditions. The results revealed that the short-time (1 min) PMA used in this study led to significant improvements compared to other reports which used longer-time PMA (>10 min). This improvement can be attributed to the low-damage NBE, as previous studies showed. Devices with SiN dielectric layer, which had more negative V_{th} values due to passivation-controlled surface states, were also compared. Therefore, to benefit from the device stability and long-term reliability of the SiN dielectric layer, the behavior of backward V_{th} should be considered as well.

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