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Modelling, Fabrication and Testing of RF Micro-Electro-Mechanical-Systems Switch

SRINIVASA RAO KARUMURI [1] (Member, IEEE), P. ASHOK KUMAR [2], GIRIJA SRAVANI KONDAVITEE [1] (Member, IEEE), AND AIME LAY-EKUAKILLE [3] (Member, IEEE)

[1]MEMS Research Center, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation Deemed to be University, Vijayawada 520002, India
[2]Department of Electronics and Communication Engineering, Chaitanya Bharathi Institute of Technology, Hyderabad 500075, India
[3]Department of Innovation Engineering, University of Salento, 73100 Lecce, Italy

CORRESPONDING AUTHOR: SRINIVASA RAO KARUMURI (e-mail: srinivasakarumuri@gmail.com)

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ABSTRACT This paper presents an approach to evaluate capacitance developed by perforated membrane of RF MEMS switch with high accuracy. An analytical model is developed for both upstate and downstate of switch by including parasitic and fringing field capacitance in parallel plate capacitance model. The proposed analytical model includes the ligament efficiency term directly in the formula which reduce the efforts to calculate it individually for various perforation sizes. The capacitance analysis has been carried out by varying the physical parameters to optimize the switch dimensions and these analytical results are compared with the simulation results carried out by 3D FEM tool COMSOL multiphysics for validation. The proposed analytical model results are then compared with benchmark models to understand the efficiency of proposed model in estimating the up and downstate capacitances. The proposed analytical model proved to be good with less error percentage of 2.13% at upstate and 2.59% at downstate whereas the other benchmark models gives greater than 5% error. The switch is then fabricated using 4-mask surface micromachining process and experimental evaluation of capacitance at both upstate and downstate is carried out by DC probe station. Experimentally, the upstate capacitance is obtained as 37.4 fF and downstate as 2.43 pF and the analytical models exhibited low error percentage of 3.95% at upstate and 2.05% at downstate condition for $\mu = 0.5$.

INDEX TERMS Analytical model, fringing field, ligament efficiency, 4-mask surface micromachining process parasitic, perforations.

I. INTRODUCTION

Now a days, electrostatic capacitive type Radio Frequency Micro-Electro-Mechanical System (RF MEMS) switches are the basic components in the microwave and millimeter wave communication systems [1]. These are largely utilized as a MEMS based capacitive sensors as they are involved variation of capacitance due to electrostatic actuation. These are used in robotic arms to detect the contact forces [2]. Since last two decades, significant research on fabrication and characterization of RF MEMS switches have been conducted and realized that most of the suspended beams in the switches contains perforations to release it during fabrication process [3], [4]. Analysis has been carried out on these type of perforated beam structures to reveal that perforated beam structures improves the switching time and reliability. But incorporating the perforations in the beam decrease the actuation and capacitive areas of switch which increases pull-in-voltage and decreases in up and down state capacitances. The s-parameters of switch are mainly depending on up and down state capacitance and a proper estimation of these capacitance values is a major assignment in developing RF MEMS Switches for high frequency applications [5], [6], [7].

Very few works on capacitance modelling have been reported till date. Among them, most of the analytical models deal with the capacitance development between parallel plate structures but none of them can be applicable for RF MEMS

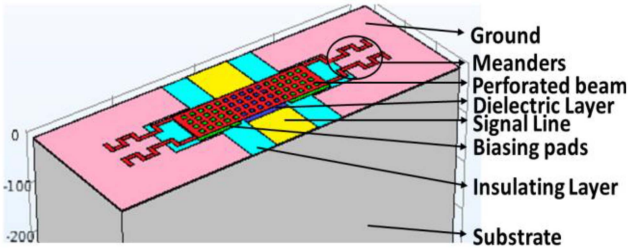

FIGURE 1. Proposed switch structure and its components.

switches due to the accommodation of dielectric layer between parallel plates. An hybrid model [8], [9] which is a combination of edge fringing field proposed by palmer [10] and fringing filed due to metal plate thickness proposed by yang [11] is reported but these models are failed to consider the perforations effect. Meji's [12] has proposed a model based on perforations in the beam but the effect of dielectric layer is not considered in this model. Later, K. G. Sravani & K. Guha et al., proposed modified versions of Meji's, Yang's and Palmer – Yang's capacitance models by including perforations, dielectric layer thickness, ligament efficiency and fringing field capacitance but these models has not considered the parasitic capacitance developed in the switch which leads to misinterpretation of capacitance with large error percentage [13].

In this paper, a modified analytical formula for capacitance of RF MEMS switch is developed by direct involvement of ligament efficiency (λ) parameter in it. The analytical formula includes the parallel plate, fringing field and parasitic capacitances. The proposed analytical formula contains the ligament efficiency term as one of the dimensional parameters and it helps to identify the overlapping area for capacitance contribution. The switch is then simulated by using finite element modelling (FEM) tool before fabrication to validate the proposed analytical models. The fabrication of switch is processed using surface micromachining technology and experimental values are compared with the modeled values for validation. The developed analytical models such as capacitance is compared with modified benchmark models to understand its efficiency in modelling of proposed RF MEMS switch.

II. DESIGN SPECIFICATIONS

The proposed design of RF MEMS switch in shunt configuration is shown in Fig. 1. The switch is constructed using the components such as substrate: a platform for monolithic fabrication of other layers on it; insulating layer: used to avoid contact between transmission line and substrate; CPW: acts as a transmission line for RF signal propagation; anchors: used to hold the suspended membrane with an airgap present between dielectric layer and membrane; meanders: used to restore the membrane when unactuated; membrane: used to develop capacitance; dielectric layer: avoid the metal contact between membrane and signal line of CPW and biasing electrodes:

TABLE 1. Dimensions for Proposed Structure

Component	Length (μm)	Breadth (μm)	Height (μm)	Material [14-16]
Substrate	820	620	450	Silicon
Membrane	320	80	0.5 - 1	Gold
Biasing Pads	100	80	1	Gold
Signal line	620	100	1	Gold
Dielectric layer	100	100	0.1 – 0.5	Si3N4
Insulating layer	820	620	1	SiO2
Anchor × 4	10	5	2.5	Gold
Airgap		2 – 3 μm		

μm = micrometers.

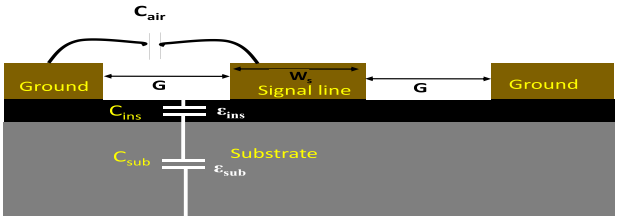

FIGURE 2. Schematic of parasitic capacitance components in switch.

used to actuate the membrane towards dielectric layer. The dimensions of each component are presented in Table 1.

III. MODELLING OF PROPOSED SWITCH

The basic parameters for designing RF MEMS switch are capacitance, pull – in voltage and switching time [17]. Among them, modelling of capacitance in the switch is primary assignment to evaluate performance of switch [18].

A. CAPACITANCE MODELLING FOR PROPOSED SWITCH

The proposed analytical formula for RF MEMS switch is expressed with three components, C_p: parasitic capacitance developed due to CPW transmission line, insulating layer and substrate; C_{pp}: parallel plate capacitance developed by surface area of suspended membrane; and C_{ff}: fringing field capacitance developed due to thickness of the membrane and edges of perforations. The total capacitance of the switch can be obtained as summation of all the three capacitance components.

$$C_{switch} = C_p + C_{pp} + C_{ff} \quad (1)$$

The first component in the capacitance model is parasitic capacitance developed by the substrate, insulating layer and CPW of the switch as shown in the Fig. 2. The parasitic capacitance of switch is developed in terms of femto farads and has much effect on upstate or onstate capacitance of switch. The total parasitic capacitance (C_p) formed by the transmission line is the sum of the capacitance developed by the signal line with ground lines (C_{air}) which are having air as a dielectric medium, capacitance developed by insulating layer (C_{ins}) and substrate (C_{sub}). Hence, the total parasitic capacitance is

given as

$$C_p = C_{air} + C_{ins} + C_{sub} \tag{2}$$

The conformal mapping technique is utilized to evaluate the capacitance developed by the CPW which involves in developing analytical expression for effective dielectric constant (ε_{eff}) of substrate - insulating layer combination and total characteristic impedance of switch (Z_0) [19]. The layers are assumed to be homogeneous to ensure quasi – TEM state and capacitance developed by signal line with ground lines where air acts a dielectric medium between them is given by

$$C_{air} = 4\varepsilon_0 \frac{K(k_0)}{K(k_0^{|})} \tag{3}$$

Where ε_0 is permittivity of free space such that

$$k_i = \frac{W_s}{W_s + 2G}, \text{i} = 0, 1, 2, 3 \ldots\ldots\ldots \tag{4}$$

Where W_S is signal line width and G is gap between signal line and ground lines.

$$k_i^{|} = K\left(\sqrt{1 - k_i^2}\right) \tag{5}$$

Where $K(k_i)$ and $K(k_i^{|})$ are elptical integrals of first kind and can be approximated as follows

$$K(k_i) = K(k_i^{|}) = \frac{\pi}{2}\left[1 + \left(\frac{1}{2}\right)^2 K^2 + \left(\frac{1.3}{2.4}\right)^2 K^4 + \ldots..\right] \tag{6}$$

The capacitance developed by the insulating layer having thickness (t_{ins}) with equivalent dielectric constant ($\varepsilon_{ins} - \varepsilon_{sub}$) is given by

$$C_{ins} = 2\varepsilon_0 \left(\varepsilon_{ins} - \varepsilon_{sub}\right) \frac{K(k_1)}{K(k_1^{|})} \tag{7}$$

Where, ε_{ins} and ε_{sub} are relative permittivity of insulating layer and substrate, respectively.

$$\text{Where} \quad k_1 = \frac{\sinh\left(\frac{\pi W_s}{4t_{ins}}\right)}{\sinh\left(\frac{\pi(W_s+2G)}{4t_{ins}}\right)} \tag{8}$$

Where, t_{ins} is thickness of insulating layer. Similarly, the capacitance developed by the substrate having thickness t_{sub} + t_{ins} with effective dielectric constant ($\varepsilon_{sub} - 1$) is given as

$$C_{sub} = 2\varepsilon_0 \left(\varepsilon_{sub} - 1\right) \frac{K(k_2)}{K(k_2^{|})} \tag{9}$$

$$\text{Where} \quad k_2 = \frac{\sinh\left(\frac{\pi w}{4(t_{ins}+t_{sub})}\right)}{\sinh\left(\frac{\pi(w+2G)}{4(t_{ins}+t_{sub})}\right)} \tag{10}$$

Therefore, the total parasitic capacitance of the switch is obtained by summation of (3), (7) and (9) and is given as

$$C_p = 4\varepsilon_{eff}\varepsilon_0 \frac{K(k_0)}{K(k_0^{|})} \tag{11}$$

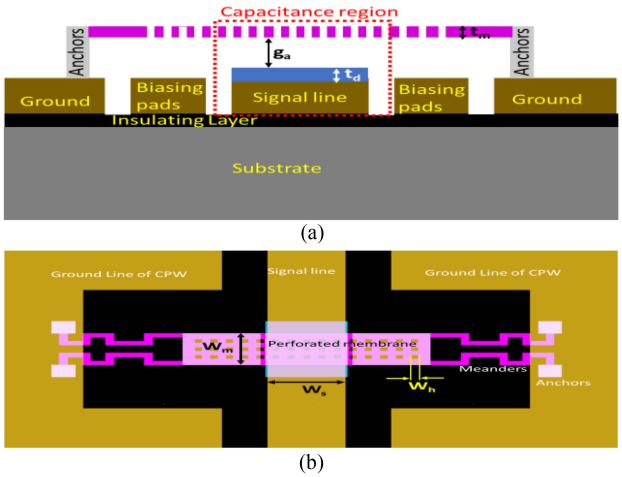

FIGURE 3. Schematic of switch at upstate: (a) Front view (b) Top view.

$$\text{Where} \quad \varepsilon_{eff} = 1 + q_1\left(\frac{\varepsilon_{ins} - \varepsilon_{sub}}{2}\right) + q_2\left(\frac{\varepsilon_{sub} - 1}{2}\right) \tag{12}$$

$$q_1 = \frac{K(k_1)K(k_0^{|})}{K(k_1^{|})K(k_0)} \tag{13}$$

$$q_2 = \frac{K(k_2)K(k_0^{|})}{K(k_2^{|})K(k_0)} \tag{14}$$

The second component in the analytical formula is parallel plate capacitance developed due to overlapping area between suspending membrane and lower electrodes. When no voltage is supplied to biasing pads and signal line is supplied with small RF voltage for signal transmission through CPW, the upstate capacitance is developed only between membrane and signal line having air and silicon nitride layer as a dielectric medium as shown in Fig. 3(a). Hence, parallel plate capacitance is majorly depends on width of the membrane (W_m) and signal line (W_s) represented in Fig. 3(b).

The membrane contains perforations hence, the total overlapping area varies with the ligament efficiency which is useful to trace the total number of perforations that can be accommodated in the membrane. The ligament efficiency varies with the size of the perforations, From the literature, the suitable size of the perforations to avoid air damping and residual stress is 10×10 μm [20]. Hence, 10×10 μm size perforations are adopted for the proposed switch design and later the size is varied for different ligament efficiency values for model validations.

The term ligament efficiency is associated with the perforations in the membrane as shown in Fig. 4. It is defined as the ratio of distance between edges of two consecutive perforations (l) and distance between centers of two consecutive perforations (pitch) [21]. Which is formulated as:

$$\mu = \frac{l}{pitch} \tag{15}$$

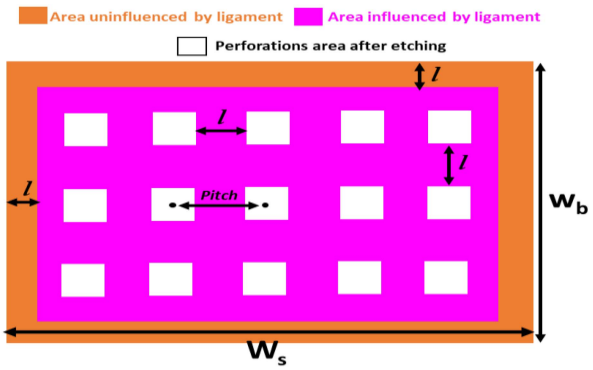

FIGURE 4. Categorization of overlapping areas.

This ligament efficiency is used to accommodate the perforations of the beam to reduce damping and stress development during actuation. Initially, when the signal line of CPW is supplied with RF signal having small voltage (≈1mV) develops an upstate capacitance between suspended membrane and signal line having air and dielectric layer as a dielectric medium. This upstate capacitance developed is in femto farads and is highly depends on ligament efficiency such that the total overlapping area in upstate is categorized into three types such as: (i) Overlapping area during formation of parallel plate capacitance (A_1); (ii) Overlapping area uninfluenced by ligament efficiency (A_2) and (iii) Overlapping area of perforated membrane influenced by ligament efficiency (A_3).

The first type in overlapping area does not contains the perforations on the beam and it is obtained from the parallel plate capacitance model. Hence the total overlapping area of membrane which contributes parallel plate capacitance of switch is formulated as

$$A_1 = (W_s \times W_m) \tag{16}$$

Where W_s: width of the signal line and W_m: width of the perforated membrane. The second term of overlapping area is the area uninfluenced by ligament efficiency (μ). Here, the width of the uninfluenced region is taken as same as the distance between edges of two consecutive perforations. Hence, the area uninfluenced by ligament efficiency of the switch can be obtained by subtracting the influenced region from total overlapping area of parallel plate capacitance model.

$$A_2 = (W_s \times W_m) - [(W_s - 2l)\,(W_m - 2l)] \tag{17}$$

The third term is based on the overlapping area on membrane after etching the perforations region on membrane. The percentage of area remained after including perforations on the membrane is formulated by using ligament efficiency value based on pitch and l values. It is given as

$$A_3 = (W_s - 2l)\,(W_m - 2l)\left[1 - (1-\mu)^2\right] \tag{18}$$

The total overlapping area to calculate upstate capacitance of the switch is obtained by adding the overlapping area uninfluenced by ligament efficiency and overlapping area influenced by ligament efficiency after etching holes which can be given as

$$A_{ov} = A_2 - A_3 \tag{19}$$

$$A_{ov} = \{(W_s \times W_m) - [(W_s - 2l)\,(W_m - 2l)]\} + \left\{(W_s - 2l)\,(W_m - 2l)\left[1 - (1-\mu)^2\right]\right\} \quad \ldots\ldots\ldots \tag{20}$$

Therefore, the total capacitance obtained by overlapping area of switch at upstate is given by

$$C_{pp\_U} = \frac{\varepsilon_0\left[(W_s \times W_m) - ((W_m - 2l) * (W_s - 2l)) + \left((W_m - 2l) \times (W_s - 2l) \times \left(1 - (1-\mu^2)\right)\right)\right]}{g + \frac{t_d}{\varepsilon_r}} \quad \ldots\ldots\ldots\ldots \tag{21}$$

Here the ligament efficiency is directly incorporated into the formula which is a novel methodology to calculate capacitance developed for perforated membrane structures accurately.

In downstate condition, the biasing pads are supplied with DC voltage to actuate the beam. Hence, additional capacitance develops between biasing pads and suspended membrane. Therefore, the first type overlapping area (A_1) can be represented as

$$A_1 = W_m \times (W_s + 2W_b) \tag{22}$$

Where, W_b is the width of the biasing pads. The second term of overlapping area becomes

$$A_2 = (W_m \times (W_s + 2W_b)) - [(W_s + 2W_b) - 2l)\,(W_m - 2l)] \quad \ldots\ldots\ldots\ldots \tag{23}$$

The third overlapping area is represented as

$$A_3 = [(W_s + 2W_b) - 2l)\,(W_m - 2l)]\left[1 - (1-\mu)^2\right] \tag{24}$$

The total overlapping area at downstate condition becomes

$$A_{ov} = \{(W_m \times (W_s + 2W_b)) - [(W_s + 2W_b) - 2l)\,(W_m - 2l)]\} + \left\{[(W_s + 2W_b) - 2l)\,(W_m - 2l)]\left[1 - (1-\mu)^2\right]\right\} \quad \ldots\ldots\ldots\ldots \tag{25}$$

Therefore, the total parallel plate capacitance developed in downstate condition is evaluated as (26) shown at the bottom of the next page

The third component in estimating the upstate capacitance of switch is fringing filed capacitance which is developed by the vertical edges of perforated membrane as shown in the Fig. 5. The fringing field capacitance of the switch is developed interms of femto farads and has major effect in upstate cpacitnace of switch. As the no.of perforations increases, the more no.of firnigning filed lines exists at the vertical edges of perforated membrane. The total count of perforations depends on the perforation size and ligament efficincy. The increase in

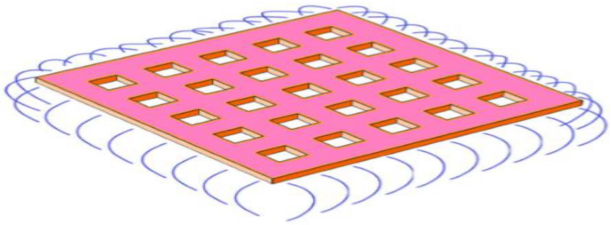

FIGURE 5. Fringing field by edges of perforated membrane.

perforation size decreases the ligament efficiency value such that it decreases the fringing filed effect due to decrease in vertical edges. The high ligament efficiency value decreases the hole size and increases the parallel plate capacitance. Hence, a proper selection of hole size and ligament efficency values are much need to develop capacitive RF MEMS switches.

The fringing field capacitance for perforated membrane is adopted by combining the modified palmer and yang's fringing field model which is given as

$$C_{ff} = \frac{2\varepsilon W}{\pi}\left[\ln\left(\frac{\pi w}{d+\frac{t_d}{\varepsilon_r}}\right)+\ln\left(1+\frac{2t_b}{d+\frac{t_d}{\varepsilon_r}}+2\sqrt{\left(\frac{t_b}{d+\frac{t_d}{\varepsilon_r}}+\frac{t_b^2}{\left(d+\frac{t_d}{\varepsilon_r}\right)^2}\right)}\right)\right] + n_l n_w w_h\left[0.77+1.06\left(\frac{w_h}{d+\frac{t_d}{\varepsilon_r}}\right)^{\frac{1}{2}}+1.06\left(\frac{t_b}{d+\frac{t_d}{\varepsilon_r}}\right)^{\frac{1}{2}}\right] \quad (27)$$

Where, C_{ff}: fringing field capacitance of switch, d: distance between perforated membrane and biasing pads (airgap), t_m; thickness of perforate membrane, t_d: thickness of dielectric layer, w_h: width of the perforations. n_l: no. of perforations along length of the membrane, n_w: no. of perforations along width of the membrane. By substituting the three capacitance components which are expressed in (11), (20) & (21) in (1). we obtain the total capacitance of switch for upstate and downstate conditions.

TABLE 2. Capacitance Component Analysis by Varying Airgap in Upstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.								
S. No	g (μm)	C_{pp} (fF)	C_{ff} (fF)	C_p (fF)	C_{switch} (fF)	% of C_{pp} in C_{switch}	% of C_{ff} in C_{switch}	% of C_p in C_{switch}
1	2	35.16	2.13	1.59	38.88	90.43	5.48	4.09
2	2.5	28.16	2.24	1.59	31.99	88.03	7.00	4.97
3	3	23.49	2.41	1.59	27.49	86.69	7.53	5.78

TABLE 3. Capacitance Component Analysis by Varying Dielectric Thickness in Upstate

When μ=0.5, g=2μm, t_m=0.5μm.								
S. No	t_d (μm)	C_{pp} (fF)	C_{ff} (fF)	C_p (fF)	C_{switch} (fF)	% of C_{pp} in C_{switch}	% of C_{ff} in C_{switch}	% of C_p in C_{switch}
1	0.1	35.16	2.13	1.59	38.88	90.43	5.48	4.09
2	0.2	34.93	2.145	1.59	38.665	90.34	5.54	4.12
3	0.3	34.7	2.151	1.59	38.441	90.28	5.59	4.13
4	0.4	34.48	2.156	1.59	38.226	90.21	5.64	4.15
5	0.5	34.25	2.16	1.59	38	90.13	5.69	4.18

IV. CAPACITANCE COMPONENT ANALYSIS OF PROPOSED ANALYTICAL MODEL

Finite element analysis is carried out to evaluate the analytical values of proposed capacitance components of switch. The total capacitance (C_{switch}) of switch is then calculated according to the (1). The parallel plate (C_{pp}), fringing field (C_{ff}) and parasitic (C_p) capacitances are analyzed to optimize switch dimensions by varying physical parameters of switch such as airgap (g), dielectric layer thickness (t_d), membrane thickness (t_m) and ligament efficiency (μ). Initially, the parasitic capacitance is evaluated using (11). The physical parameters varied has no impact on parasitic capacitance because, it depends on substrate, insulating layer of switch. From the (11), it is obtained as 1.59 fF. The proposed formula as presented in (1) is a generalized formula for both upstate and down state conditions of switch. In the upstate it is estimated that there will be an airgap between suspended membrane and lower electrodes and signal line is supplied with RF voltage. Hence the parallel plate and fringing field capacitances are developed according to the (21) & (22) and the variations with physical parameters are presented in the Tables 2, 3, 4 and 5 for upstate.

Intially, the physical parameters such as μ, t_m and t_d are kept at minimum values and capacitance is evaluated and

$$C_{pp\_D} = \frac{\varepsilon_0\left[((W_m\times(W_s+2W_b))-[(W_s+2W_b)-2l)(W_m-2l)])+[(W_s+2W_b)-2l)(W_m-2l)]\left[1-(1-\mu)^2\right]\right]}{g+\frac{t_d}{\varepsilon_r}} \quad (26)$$

TABLE 4. Capacitance Component Analysis by Varying Membrane Thickness in Upstate

When μ=0.5, g=2μm, t_d=0.1μm.								
S. No	t_m (μm)	C_{pp} (fF)	C_{ff} (fF)	C_p (fF)	C_{switch} (fF)	% of C_{pp} in C_{switch}	% of C_{ff} in C_{switch}	% of C_p in C_{switch}
1	0.5	35.16	2.13	1.59	38.88	90.43	5.48	4.09
2	1	35.16	2.26	1.59	39.01	90.13	5.79	4.07
3	2	35.16	2.42	1.59	39.17	89.76	6.18	4.06

TABLE 5. Capacitance Component Analysis by Varying Ligament Efficiency in Upstate

When g=2μm, t_m=0.5μm, t_d=0.1μm.							
μ	C_{pp} (fF)	C_{ff} (fF)	C_p (fF)	C_{switch} (fF)	% of C_{pp} in C_{switch}	% of C_{pp} in C_{switch}	% of Cpp in C_{switch}
0.3	30.05	1.97	1.59	33.61	89.41	5.86	4.73
0.5	35.16	2.13	1.59	38.87	90.45	5.46	4.09
0.7	37.28	2.21	1.59	41.08	90.74	5.37	3.89

presented in Table 2 for different airgaps ranging from 2-3μm. In this condition, the 86% – 91% of total capacitance is contributed by parallel plates, fringing filed contributes 5% – 8% whereas parasitic capacitance contributes 4% – 6%. At g=2μm, maximum capacitance of switch occurs as 38.88 fF with C_{pp}=35.16fF, C_{ff} = 2.13fF and C_p = 1.59fF. Hence, g = 2μm is the optimum gap required for switch to develop large capacitance values. By keeping airgap at 2μm and other physical parameters at minimum value, the thickness of dielectric layer is varied from 0.1μm – 0.5μm and model results presented in Table 3. In this analysis, the parallel plate contributes 90% of total capacitance whereas the fringing and parasitic capacitance contributes 6% and 4% respectively. The switch at t_d=0.1μm shows good capacitance value of 38.88 fF where it is a combination of C_{pp}=35.16fF, C_{ff}=2.13fF and C_p = 1.59fF. In both the case studies, the maximum contribution is incurred by the parallel plate capacitance which is obtained due to decrease in distance between suspended beam and signal line.

Airgap and dielectric thickness values of switch design are fixed to 2μm and 0.1μm respectively whereas other physical parameters are kept at minimum values and membrane thickness is varied from 0.5μm - 2μm and the model values are evaluated and presented in Table 4. In this case study, the parallel plate does not varies and shows a fixed value of 35.16 fF, this is due to fixed overlapping area in all the conditions. Here, the fringing filed capacitance only varies due to large accommodation of curved capacitance field lines between suspending beam edges and signal line. At this condition, the maximum capacitance of 39.17 fF occurs at the membrane thickness of 2μm but the contribution of parallel plate capacitance is only 89% whereas at t_m=0.5μm, parallel plates contributes 90.43% of total capacitance. By

TABLE 6. Capacitance Component Analysis by Varying Dielectric Thickness in Downstate

When μ=0.5, t_m=0.5μm.								
S. No	t_d (μm)	C_{pp} (pF)	C_{ff} (fF)	C_p (fF)	C_{switch} (pF)	% of C_{pp} in C_{switch}	% of C_{pp} in C_{switch}	% of Cpp in C_{switch}
1	0.1	2.38	2.72	1.59	2.38	99.82	0.11	0.07
2	0.2	1.19	2.24	1.59	1.19	99.68	0.19	0.13
3	0.3	0.79	2.38	1.59	0.79	99.50	0.30	0.20
4	0.4	0.59	2.09	1.59	0.59	99.38	0.35	0.27
5	0.5	0.47	1.79	1.59	0.47	99.29	0.38	0.34

TABLE 7. Capacitance Component Analysis by Varying Membrane Thickness in Downstate

When μ=0.5, g=2μm, t_d=0.1μm.								
S. No	t_m (μm)	C_{pp} (pF)	C_{ff} (fF)	C_p (fF)	C_{switch} (pF)	% of C_{pp} in C_{switch}	% of C_{pp} in C_{switch}	% of Cpp in C_{switch}
1	0.5	2.38	2.72	1.59	2.38	99.82	0.11	0.07
2	1	2.38	3.14	1.59	2.38	99.80	0.13	0.07
3	2	2.38	3.76	1.59	2.39	99.78	0.16	0.07

TABLE 8. Capacitance Component Analysis by Varying Ligament Efficiency in Downstate

When g=2μm, t_m=0.5μm, t_d=0.1μm.								
S. No	μ	C_{pp} (pF)	C_{ff} (fF)	C_p (fF)	C_{switch} (pF)	% of C_{pp} in C_{switch}	% of C_{ff} in C_{switch}	% of Cp in C_{switch}
1	0.3	1.92	2.46	1.59	1.92	99.79	0.13	0.08
2	0.5	2.38	2.72	1.59	2.38	99.82	0.11	0.07
3	0.7	2.44	2.83	1.59	2.44	99.82	0.12	0.07

having large membrane thickness, the pull-in-voltage increases hence, t_m=0.5μm is chosen as an optimum membrane thickness value for proposed switch design.

Therefore, by keeping all the physical parameters to a fixed value, the ligament efficiency is evaluated for different perforation sizes and model is evaluated and presented in Table 5. To obtain ligament efficiency (μ) value to 0.3, perforations are taken as 7μm×7μm size. For μ=0.5, the perforation size is 10μm×10μm and for μ=0.7, the perforation size is 3μm×3μm. Among these ligament efficiency values, μ=0.7 shows large capacitance value of 41.08fF but the perforation size of 5μm×5μm is not enough to overcome air damping effect on beam during actuation. Hence, the 10μm×10μm perforations reduces 25% of total area to reduce air damping and also produces good contribution of capacitance components (C_{pp}=35.16fF, C_{ff} = 2.13fF and C_p = 1.59fF). Hence μ=0.5 is the optimum value for proposed switch design.

In the downstate condition according the (26) and (27), the parallel plate and fringing filed capacitances develop between suspended membrane and baising pads along with signal line and are evaluated and presented in the Tables 6, 7, and 8. As the aig gap between the suspending beam and dielectric layer vanishes, the parallel capacitnace of the switch increases to

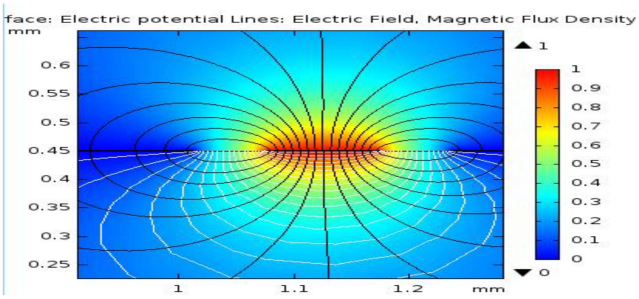

FIGURE 6. Simulated electromagnetic field associated with CPW.

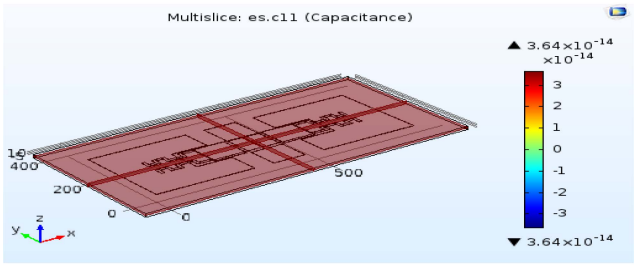

FIGURE 7. Simulated upstate capacitance of proposed switch.

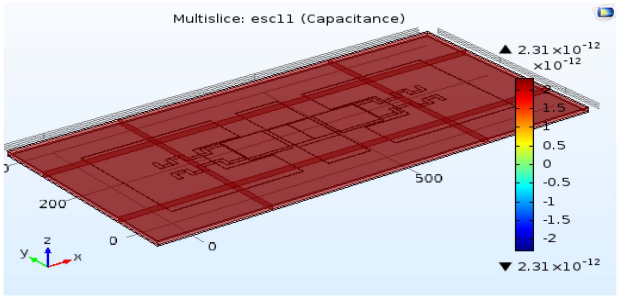

FIGURE 8. Simulated downstate capacitance of switch.

few pico farads. The fringing filed and parasitic capacitance values are always at femto farads and has very less contribution to the total capacitance of switch. Overall, 99.9% of total capacitance is offered by parallel plate and both fringing field and parasitic capacitanc combinely offers only 0.1%. This is due to exisitng of more no.of parallel lines than curved filed lines as air vanishes.

Here, the physical parameters such as ligament efficiency and membrane thickness are kept to minimum values and dielctric thickness varies from 0.1µm – 0.5µm. At t_d=0.1µm, the switch shows maximum capacitance of 2.38pF which is almost equal to parallel plate capacitance developed at that stage. As dielectric thickness increases, the total capacitance of the switch decreases whereas the fringing field capacitance increases as it increases the distance between parallel plates

The downstate capacitance of the switch increases as ligament effciency value increases. This is due to lowering the perforations area by increasing total no.of perfotations. The total no.of perforations decreases from µ=0.5 to 0.3 and 0.7 due to having large distance between perforations. In these cases, the parallel plate contributes 99.8% of total cpacitance whereas the fringing filed and parasitic capacitance offers only 0.2% of total capacitance in downstate condition. This low contribution is due to that the fringing and parasitc capacitances developes in femto fards and does not have much effect on downstate capacitance of switch.

V. MODEL VALIDATION

A. ERROR EVALUATION THROUGH SIMULATIONS

The parasitic capacitance is obtained by simulating the CPW transmission line in elecromegnetic physics environment. The CPW transmission line taken over SiO_2 layer and substrate is designed using COMSOL multiphysics tool. The materials are assigned according to the Table 1. Electromagnetics physics is applied to study the electromagnetic filed associated with CPW. A potential difference is applied on between signal line and gound line of CPW and stationary anlysis is carried out to extract the lumped parameters of CPW. The simulation of these electromagnetic filed lines are shown in the Fig. 6. These parameters contains the parasitic capacitance developed by the CPW and is obtained as 1.65 fF through simulation

Later, simulations have been carried out to obtain the fringing field capacitance and parallel plate capacitance values. The numerical simulations are carried out using COMSOL multiphysics software (FEM tool). The switch is designed in 3D environment where the materials are assigned to each physical component in the structure as prescribed in the Table 2. Later, electrostatics physics is applied having boundary conditions as: terminal voltage for signal line and biasing pads for downstate condition and only for signal line in upstate. In both the cases the suspending beam is always grounded. Stationary analysis is carried out to obtain the required capacitance values of switch. The obtained capacitance contains both fringing field and parallel plate capacitance because air is assigned for outer domain of switch.

The simulated upstate capacitance for all fixed physical parameters of switch is shown in the Fig. 7 is observed as 36.42 fF and for downstate which is represented in Fig. 8 is obtained as 2.31 pF.

The Simulations have been carried out by varying the physical parameters of switch to observe error percentage at both upstate and downstate conditions of switch.

The air gap will present only in upstate condition of switch and it vanishes at downstate. Hence the capacitance values are taken for switch at different height of suspended membrane and presented in Table 9. It is observed that the switch shows very low percentage error of +2.12% at g=2 µm. The positive symbol represents overestimation of capacitance by proposed analytical model than simulated results. Later, by keeping all physical constraints to the minimum value, the dielectric thickness is varied to observe capacitance variation in both upstate and downstate conditions of switch. From

TABLE 9. Error Analysis by Varying Airgap in Upstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	g (μm)	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Emperical-Simulated)/ Simulated]* 100
1	2	38.88	38.07	2.12%
2	2.5	31.99	30.81	3.82%
3	3	27.49	25.72	6.88%

TABLE 10. Error Analysis by Varying Dielectric Thickness in Upstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	t_d (μm)	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Analytical-Simulated)/ Simulated]* 100
1	0.1	38.88	38.07	2.12%
2	0.2	38.665	37.74	2.45%
3	0.3	38.441	37.49	2.53%
4	0.4	38.226	37.24	2.64%
5	0.5	38	36.93	2.81%

TABLE 11. Error Analysis by Varying Dielectric Thickness in Downstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	t_d (μm)	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Emperical-Simulated)/ Simulated]* 100
1	0.1	2.38	2.32	2.586%
2	0.2	1.19	1.04	14.42
3	0.3	0.79	0.68	16.17%
4	0.4	0.59	0.5	18%
5	0.5	0.47	0.39	20.51%

TABLE 12. Error Analysis by Varying Membrane Thickness in Upstate

When μ=0.5, t_m=0.5μm, t_d=0.1 μm.				
S. No	t_m (μm)	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Analytical-Simulated)/ Simulated]* 100
1	0.5	38.88	38.07	2.12%
2	1	39.01	38.26	1.96%
3	2	39.17	38.94	1.64%

the Tables 10–13 it is observed that the proposed analytical model shows low percentage error at td=0.1 μm. As the thickness of dielectric layer increases the capacitance value decreases thereby increasing the error percentage. Hence, dielectric layers having small thickness are efficient to develop high capacitance RF MEMS switches. In downstate condition

TABLE 13. Error Analysis by Varying Membrane Thickness in Downstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	t_m (μm)	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Analytical-Simulated)/ Simulated]* 100
1	0.5	2.38	2.32	2.586%
2	1	2.38	2.304	3.2986%
3	2	2.39	2.312	3.373%

TABLE 14. Error Analysis by Varying Ligament Efficiency in Upstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	μ	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Analytical-Simulated)/ Simulated]* 100
1	0.3	33.61	32.24	4.37%
2	0.5	38.87	38.07	2.12%
3	0.7	41.08	39.42	4.26%

TABLE 15. Error Analysis by Varying Ligament Efficiency in Downstate

When μ=0.5, t_m=0.5μm, t_d=0.1μm.				
S. No	μ	C_{switch} (fF)		Error Percentage
		Analytical Value (C_p+C_{pp}+C_{ff})	Simulated Value (C_p+C_{pp}+C_{ff})	[(Analytical-Simulated)/ Simulated]* 100
1	0.3	1.92	1.81	6.077%
2	0.5	2.38	2.32	2.586%
3	0.7	2.44	2.37	2.953%

the error percentage occurs greater than 10% due to absence of fringing field capacitance at downstate condition of switch.

The dielectric layer is fixed at 0.1μm and airgap at 2μm, other physical parameters to the minimum values and membrane thickness is varied from 0.5μm to 2μm for both upstate and downstate cases. The proposed analytical formula estimates the capacitance values with percentage error of +2.12% for upstate condition and +13.33% for downstate condition at t_m=0.5μm and the error value decreases as membrane thickness increases. This is due to increases in fringing field capacitance lines for large thickness beam. But increasing the membrane thickness may affects the pull – in voltage and other reliability issues of switch. Hence, t_m=0.5 μm is the best case for analytical formula to estimate capacitance of switch.

The error percentage of analytical model is evaluated for different ligament efficiency values for both upstate and downstate conditions which are present in the Tables 14 and 15 respectively. Here, for μ=0.3: a total no. of 126 perforations are present in the membrane; for μ=0.5: a total of 60 perforations will present and for μ=0.7: there are 126 perforations in the membrane. The analytical and simulated

capacitance of switch are very less for μ=0.3 because of having low capacitive area of suspended membrane due to perforations. The error percentage is very low for μ=0.5 (2.12%) than μ=0.3 and μ=0.7 because, the total area occupied by perforations is 25% of its total overlapping area of switch. Hence, the accommodation of fringing filed lines more efficient and parallel plate capacitance will be a dominant factor to develop capacitance. Whereas, in other two cases the fringing field lines are more due to formations of more perforation edges and they dominate the parallel plate capacitance in upstate. In downstate condition, the error percentage is less for μ=0.5 than μ=0.3 and μ=0.7 but it is in a very less margin because, the parallel plate capacitance (pF) is more dominant than the other two capacitance components which are in femto Farads. Therefore, the analytical model is good enough to estimate the simulation results of proposed switch with very less error percentage.

B. COMPARISON WITH BENCHMARK MODELS

Three benchmark models are proposed by Leus, Meji's and Palmer – Yang's combined model are utilized to compute the total capacitance between parallel plates including fringing field effect. Koushik Guha [22] proposed modified formulas for these benchmark models which can apply for RF MEMS Switches for calculation of total capacitance of switch effectively. Initially, the benchmark models are applicable to calculate capacitance without having perforation on the parallel plates. Later they are modified by incorporating perforations. The three modified models are

$$C_{\mathrm{mod\_mejis}} = \varepsilon_0 W \left[\frac{w}{d+\frac{t_d}{\varepsilon_r}} + 0.77 + 1.06\left(\frac{w}{d+\frac{t_d}{\varepsilon_r}}\right)^{1/4} + 1.06\left(\frac{t_b}{d+\frac{t_d}{\varepsilon_r}}\right)^{1/2}\right] - \frac{n_l n_w \varepsilon_0 w_h^2}{d+\frac{t_d}{\varepsilon_r}} + n_l n_w \varepsilon_0 w_h \times \left[0.77 + 1.06\left(\frac{w_h}{d+\frac{t_d}{\varepsilon_r}}\right)^{1/4} + 1.06\left(\frac{t_b}{d+\frac{t_d}{\varepsilon_r}}\right)^{1/2}\right] \tag{28}$$

$$C_{\mathrm{mod\_yang}} = \frac{\varepsilon w W}{d+\frac{t_d}{\varepsilon_r}} + \frac{2\varepsilon W}{\pi}\left[\ln\left(\frac{2\pi w}{d+\frac{t_d}{\varepsilon_r}}\right)\right] + \ln\left(1+\frac{2t_b}{d+\frac{t_d}{\varepsilon_r}}+2\sqrt{\frac{t_d}{d+\frac{t_d}{\varepsilon_r}}+\frac{t_b^2}{\left(d+\frac{t_d}{\varepsilon_r}\right)^2}}\right)$$

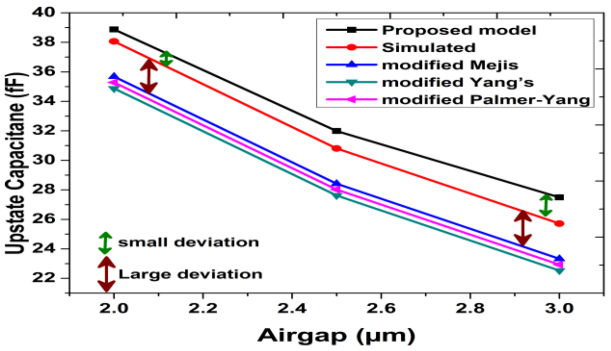

FIGURE 9. Upstate capacitance analysis by varying airgap.

$$- \frac{n_l n_w \varepsilon w_h^2}{d+\frac{t_d}{\varepsilon_r}} + \frac{2 n_l n_w \varepsilon_0 w_h}{\pi}\left[\ln\left(\frac{\pi w_h}{d+\frac{t_d}{\varepsilon_r}}\right) + \ln\left(1+\frac{2t_b}{d+\frac{t_d}{\varepsilon_r}}+2\sqrt{\frac{t_b}{d+\frac{t_d}{\varepsilon_r}}+\frac{t_b^2}{\left(d+\frac{t_d}{\varepsilon_r}\right)^2}}\right)\right] \tag{29}$$

$$C_{pal-yang} = \frac{\varepsilon_0 w W}{d+\frac{t_d}{\varepsilon_r}} + \frac{\varepsilon_0 w}{\pi}\left[1+\ln\left(\frac{2\pi w}{d+\frac{t_d}{\varepsilon_r}}\right) + \ln\left(1+\frac{2t_b}{d+\frac{t_d}{\varepsilon_r}}+2\sqrt{\frac{t_d}{d+\frac{t_d}{\varepsilon_r}}+\frac{t_b^2}{\left(d+\frac{t_d}{\varepsilon_r}\right)^2}}\right)\right] - \frac{n_l n_w \varepsilon_0 w_h^2}{d+\frac{t_d}{\varepsilon_r}} + \frac{n_l n_w \varepsilon_0 w_h}{\pi}\left[1+\ln\left(\frac{2\pi w}{d+\frac{t_d}{\varepsilon_r}}\right) + \ln\left(1+\frac{2t_b}{d+\frac{t_d}{\varepsilon_r}}+2\sqrt{\frac{t_d}{d+\frac{t_d}{\varepsilon_r}}+\frac{t_b^2}{\left(d+\frac{t_d}{\varepsilon_r}\right)^2}}\right)\right] \tag{30}$$

The upstate capacitance values are evaluated for proposed analytical and benchmark models and the calibration is carried out along with simulation results as presented in Fig. 9 for different airgaps. It is observed that the analytical model has close approximation than the benchmark models which is due to that the benchmark models does not includes parasitic capacitance whereas the analytical model accounts it which is developed between transmission line, insulating layer and substrate. As airgap increases the deviation between the simulation results and proposed models increases due to decrease in parallel plate capacitance and increase in fringing field effect. Hence, it can be say that the fringing field capacitance is a dominant factor during physical parameters variation in upstate. The error percentage is calculated and presented in

TABLE 16. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Airgap in Upstate

d (μm)	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
2	2.13	-6.28	-8.38	-7.33
2.5	3.83	-7.76	-10.35	-9.06
3	6.88	-9.29	-12.40	-10.85
Mean error	**4.28**	**-7.78**	**-10.38**	**-9.08**

TABLE 17. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Dielectric Thickness in Upstate

t_d (μm)	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.1	2.13	-6.28	-8.38	-7.33
0.2	2.45	-6.33	-8.45	-7.39
0.3	2.54	-6.38	-8.51	-7.44
0.4	2.65	-6.42	-8.57	-7.49
0.5	2.90	-6.47	-8.64	-7.55
Mean error	**1.62**	**-3.85**	**-5.14**	**-4.50**

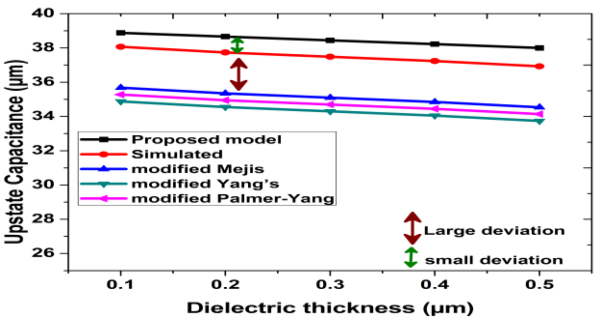

FIGURE 10. Upstate capacitance analysis by varying dielectric thickness.

the Tables 16 and 17. The mean error for proposed analytical model is observed as +4.28 which is less than 5% error whereas the benchmark models shows high mean error values (>5%). At 2μm airgap the proposed analytical model shows very less error percentage of +2.13% than the other values, therefore the airgap 2μm is an optimized value for proposed switch design. The proposed analytical model shows positive error which describes that it overestimates the simulated value whereas the benchmark models underestimates it but the error percentages is low for proposed analytical model which shows the efficiency in estimating the upstate capacitance of switch.

The upstate capacitance values are observed for analytical models by varying different dielectric thickness values and compared with the simulated results to observe the error deviation. From the Fig. 10, the proposed model is validated by observing less deviation from simulated results when compared to the benchmark models. The error percentage values

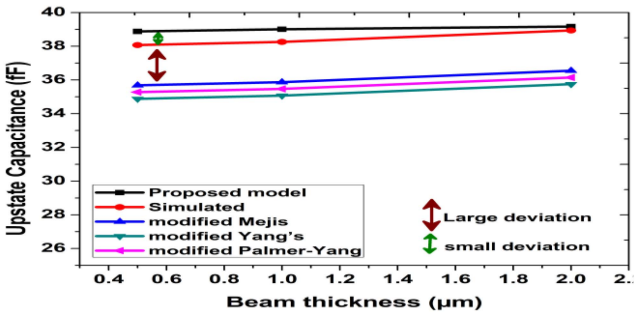

FIGURE 11. Upstate capacitance analysis by varying beam thickness.

TABLE 18. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Membrane Thickness in Down State

t_m (μm)	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.5	2.13	-5.17	-5.82	-5.50
1	1.98	-5.21	-5.86	-5.53
2	1.37	-5.19	-5.84	-5.51
Mean error	**1.82**	**-5.19**	**-5.84**	**-5.51**

are evaluated and observed that the proposed model shows very less mean error of +1.62 whereas the other benchmark models shows larger than that of it. The proposed analytical model diminishes the error percentage by including the parasitic capacitance term whereas the benchmark model neglected it in approximation. In this case, the proposed model overestimates with less error percentage of +2.13 at 2μm whereas the benchmark models underestimate the simulated value with greater than 5% error percentage.

The mathematical evaluation of upstate capacitance has been carried out by varying suspended membrane thickness of switch. From the Fig. 11, It is observed that the benchmark models are largely deviated from the simulated results than the proposed analytical model due to neglecting the parasitic capacitance of switch. As the membrane thickness increases, the deviation of analytical model reduces due to increase in fringing field effect associated with the edge formed by membrane thickness. But increasing the membrane thickness is not a good practice for low pull-in voltage RF MEMS switches. The difference in error percentage of analytical model at t_m=2μm and t_m=0.5μm is observed to be 0.76% which is very less in comparison, hence increasing the membrane thickness for small enhancement in capacitance does not serves good for low pull-in voltage RF MEMS switches. Therefore, t_m=0.5μm is chosen as an optimum value for switch membrane and the analytical model overestimates simulated values with less mean error of 1.82% than the other underestimating benchmark models (>5%). Hence, by observing the values presented in Table 18, the proposed analytical model is proved to be good in estimating upstate capacitance of switch.

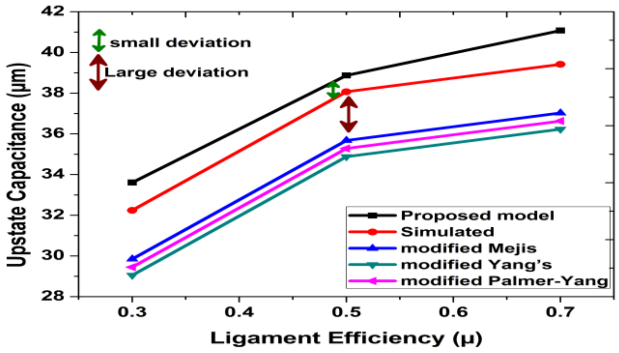

FIGURE 12. Upstate capacitance analysis by varying ligament efficiency.

TABLE 19. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Ligament Efficiency in Upstate

μ	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.3	4.25	-7.41	-9.89	-8.65
0.5	2.13	-6.28	-8.38	-7.33
0.7	4.21	-6.06	-8.09	-7.08
Mean error	**3.52**	**-6.58**	**-8.79**	**-7.69**

The upstate capacitance is calculated for proposed analytical and benchmark models and the variation for different ligament efficiency values are plotted with reference to the simulated values in the Fig. 12 such that large variation occurs between simulated values and benchmarks models than the proposed analytical model. These curves in Fig. 12 describes that the proposed analytical model is closely approximated to simulated value due to including the parasitic capacitance of the switch where the benchmark models have neglected it. The ligament efficiency value of μ=0.5 is observed to be good to estimate the upstate capacitance with minimum deviation in error as presented in Table 19. The benchmark models underestimated the capacitance of switch with large error percentages (>5%) whereas the proposed analytical model overestimates the upstate capacitance with less mean error percentage of 3.52 showing very less error percentage of 2.1% at μ=0.5. Hence, 10μm × 10μm size perforations are efficient to develop efficient RF MEMS switch for RF applications with high reliable characteristics.

The upstate capacitance is calculated for proposed analytical and benchmark models and the variation for different ligament efficiency values are plotted with reference to the simulated values in the Fig. 12 such that large variation occurs between simulated values and benchmarks models than the proposed analytical model. These curves in Fig. 12 describes that the proposed analytical model is closely approximated to simulated value due to including the parasitic capacitance of the switch where the benchmark models have neglected it. The

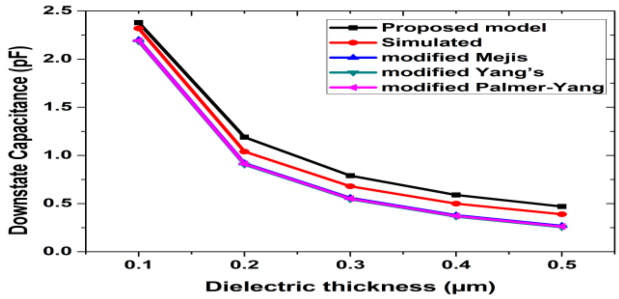

FIGURE 13. Downstate capacitance analysis by varying dielectric thickness.

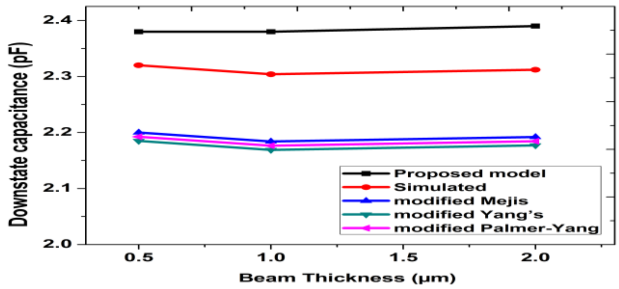

FIGURE 14. Downstate capacitance analysis by varying membrane thickness.

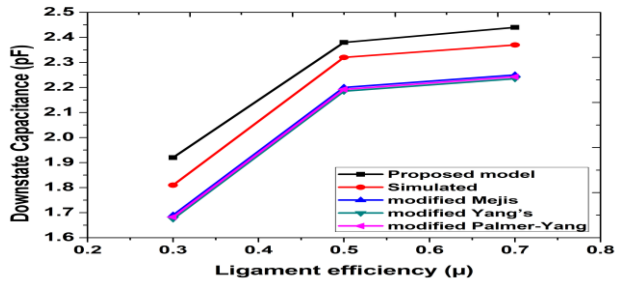

FIGURE 15. Downstate capacitance analysis by varying ligament efficiency.

ligament efficiency value of μ=0.5 is observed to be good to estimate the upstate capacitance with minimum deviation in error as presented in Table 19. The benchmark models underestimated the capacitance of switch with large error percentages (>5%) whereas the proposed analytical model overestimates the upstate capacitance with less mean error percentage of 3.52 showing very less error percentage of 2.1% at μ=0.5. Hence, 10μm × 10μm size perforations are efficient to develop efficient RF MEMS switch for RF applications with high reliable characteristics.

The downstate capacitance of switch is then evaluated by using the analytical models and compared with the simulation results as in the same manner carried out in upstate (varying the physical parameters of switch). In each case the simulated and analytical values are plotted to observe the close approximated of proposed analytical model. Fig. 13 represents the variation of downstate capacitance with respect to different

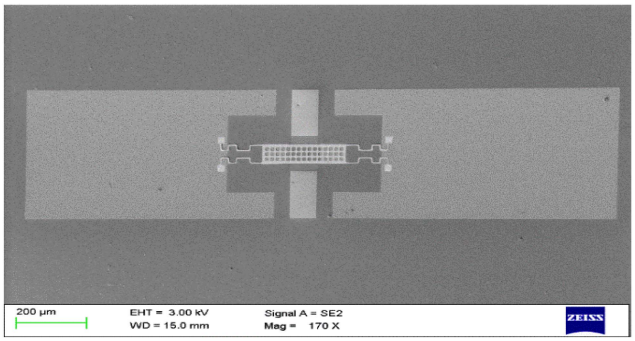

FIGURE 16. SEM picture of fabricated switch with perforations.

TABLE 20. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Dielectric Thickness in Downstate

t_d (µm)	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.1	2.59	-5.17	-5.82	-5.50
0.2	14.42	-11.54	-12.98	-12.26
0.3	16.18	-17.65	-19.85	-18.75
0.4	18.00	-24.00	-27.00	-25.50
0.5	20.51	-30.77	-34.62	-32.69
Mean error	**14.34**	**-17.83**	**-20.05**	**-18.94**

dielectric thickness values. From the Table 20, the proposed analytical shows very close approximation at t_d=0.1µm when compared to the other cases with a less percentage error of 2.59% and the mean error for proposed model is 14.34% which is less than the other benchmark models (>15%). The large deviation (>10%) in analytical and simulated values in downstate condition of switch is due to negligible influence of fringing field and parasitic capacitance terms (fF) on parallel plate capacitance (pF).

The downstate capacitance is evaluated for analytical models by varying membrane thickness of switch and plotted with simulated results for validation. The proposed analytical model overestimates the downstate capacitance with mean error of 1.56% whereas the benchmark models underestimates it with high error percentage (>5%). The error percentages of each model along with proposed model are presented in Table 21. This shows that the proposed analytical model is efficient than the models in literature to estimate the capacitance of switch.

The analysis is carried out by varying the ligament efficiency of switch at downstate condition. At µ=0.5, the analytical model estimates the downstate capacitance with 2.59% error which is very less when compared to benchmark models (>5%). The low mean error of analytical model (=3.87%) exhibits the efficiency of proposed analytical model than the benchmark models (5%). The positive and negative

TABLE 21. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Membrane Thickness in Downstate

t_m (µm)	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.5	2.13	-6.28	-8.38	-7.33
1	1.96	-6.25	-8.34	-7.29
2	0.59	-6.14	-8.19	-7.16
Mean error	**1.56**	**-6.22**	**-8.30**	**-7.26**

TABLE 22. Comparison of Error Percentage of Proposed Analytical Model With Benchmark Models by Varying Ligament Efficiency in Downstate

µ	% error of Modified proposed	% error of modified Mejis Fokkema model	% error of Yang's model	% error of modified Palmer-Yang combined model
0.3	6.08	-6.63	-7.46	-7.04
0.5	2.59	-5.17	-5.82	-5.50
0.7	2.95	-5.06	-5.70	-5.38
Mean error	**3.87**	**-5.62**	**-6.32**	**-5.97**

symbol for error percentage values represents the overestimation and underestimation of analytical models over simulated results.

VI. FABRICATION & CHARACTERIZATION SETUP

A four - mask process is utilised for fabrication of proposed RF MEMS switch with optimised dimensions prescribed for it. Initially, silicon wafer is chosen as a substrate due to high resistivity (>10 KΩ-cm) and also for possibility in monolithic integration. The first step in the process is the development of 1µm oxide layer over Silicon surface by thermal oxidation process carried out at 975°C. LOR and positive photoresist material (AZ5214) is deposited over the insulating layer. Photolithography process is carried out using mask-1 (defined for CPW and Biasing pads) and the exposed region of LOR and PPR is etched off to form trenches for CPW and biasing pads. Cr/Au/Cr stack with the thickness 50nm/400nm/50nm is deposited over the pattern surface by DC sputtering technique. Later the LOR and PPR is lifted of such that Cr/Au/Cr stack present over it also lifted off hence the desired structure of CPW and biasing pads are formed in this step. Later a thin layer of Silicon nitrate having thickness 0.1µm is deposited by using by PECVD method over top of the switch surface. Mask-2 (defined for dielectric layer) is used in photolithography to define the region for dielectric layer. The region where the dielectric layer should present is taken as dark filed in the mask-2 and other region is exposed to UV-rays in photolithography process. The exposed reason is then etched off to form required thin dielectric layer over signal line of CPW. Sacrificial layer made up of positive photoresist is grown up to 2µm height which is useful to form suspended

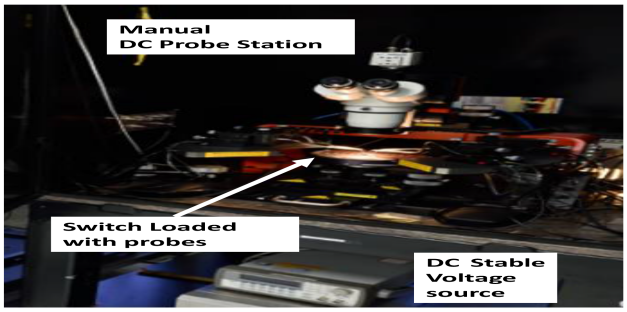

FIGURE 17. Experimental set – up to evaluate C – V characteristics.

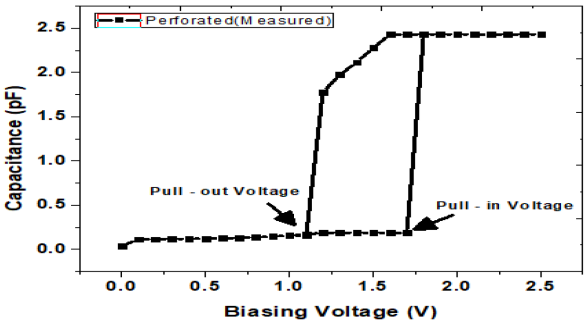

FIGURE 18. C – V characteristics of proposed fabricated switch design.

structure of membrane. Photolithography process is carried out using mask-3 (anchors) and the trenches are formed for anchors. Later, gold metal is deposited with a thickness of 0.5µm using DC sputtering technique at room temperature. Again photolithography process is carried out using mask-4 (defined for meanders and membrane) and undefined region for anchors meanders and perforated membrane is etched off using wet etching process ($KI:I_2:H_2O$). Later, the membrane is released by washing away the sacrificial layer with IPA, distilled water and H_2SO_4 solutions and then released switch is placed in a critical point dryer to remove the moisture on the surface of a switch to avoid stiction problems.

The fabricated switch with 10×10 µm perforations in the membrane is loaded on DC – probe station [Agilent Device Analyzer B1500A, PM5 with thermal chuck with pulsed source 5MHz] as shown in the Fig. 17 and the capacitance is measured by observing the hysteresis of switch as presented in the Fig. 18.

By, observing the calibration values obtained from DC probe station, it can be said that the switch produces a high downstate capacitance of 2.43pF along with upstate capacitance of 37.4fF during actuation.

VII. RESULTS AND DISCUSSIONS

The capacitance values at upstate and downstate condition are presented in the Tables 23 and 24 respectively and the deviation of analytical results with both simulation and experimental results are analyzed for Validation of the proposed model.

TABLE 23. Error Analysis by Varying Membrane Thickness in Upstate

C_{switch} (fF)When µ=0.5, t_m=0.5µm, t_d=0.1µm.	
Analytical Value (C_p+C_{pp}+C_{ff})	38.88
Simulated Value (C_p+C_{pp}+C_{ff})	38.07
Experimental Value	37.4
Error percentage of analytical value from simulated value	2.12%
Error percentage of analytical value from Experimental value	3.95

TABLE 24. Error Analysis by Varying Membrane Thickness in Downstate

C_{switch} (fF)When µ=0.5, t_m=0.5µm, t_d=0.1µm.	
Analytical Value (C_p+C_{pp}+C_{ff})	2.38
Simulated Value (C_p+C_{pp}+C_{ff})	2.32
Experimental Value	2.43
Error percentage of analytical value from simulated value	2.586%
Error percentage of analytical value from Experimental value	-2.05%

The proposed analytical model results in low percentage error of 3.95% with the experimental results obtained at upstate capacitance of switch. The deviation between experimental and analytical model values (3.95%) is larger than the simulated and analytical values (2.12%). It is due to small geometrical variations at edges of the fabricated switch formed during deposition and etching process steps. In downstate condition, the deviation of analytical model from experimental value (-2.43%) less than the deviation occurred with the simulated results (2.586%). The analytical model underestimated the experimental downstate capacitance value but exhibited low error percentage than the other benchmark models. Hence the proposed analytical models show its efficiency in estimating the capacitance of switch which is a combination of parallel plate, fringing field and parasitic capacitance and is validated through simulations and testing experimentally.

VIII. CONCLUSION

In this paper, an analytical model is developed to calculate the capacitance of RF MEMS switch including parasitic capacitance and fringing field effect along with parallel plate capacitance. The proposed analytical formula is based on ligament efficiency term directly involved in the formula which reduces the large computational time for capacitance evaluation. At t_m=0.5µm, d=2µm, t_d=0.1µm and µ=0.5, the parallel plate capacitance almost contributes 90% of total capacitance whereas the parasitic capacitance and fringing field contributes 4% and 6% respectively in upstate. In downstate the parallel plate capacitance which is in pico-Farads is a dominant factor with 99% contribution of total capacitance due to development of fringing and parasitic capacitance in femto Farads. The proposed model exhibits low percentage error of 2.13% in upstate and 2.586% in downstate condition with

simulated results. The analytical values are compared with the benchmark models along with simulated results obtained from 3D FEM simulation tool with a wide range of parametric variations. The proposed analytical model acquires low percentage error (<5%) than the benchmark models (>5%) and is validated with simulations. The fabrication of proposed switch is carried out by surface micromachining technology and is tested with DC probe station in clean room facility. The experimental capacitance of switch is observed to be 37.4 fF in upstate and 2.43 pF in downstate condition and proposed model shows 3.95% error in upstate and 2.05% error in downstate condition. The proposed analytical model has a correlation with simulation and experimental values and can be applicable for capacitive type perforated RF MEMS shunt switch having dielectric layer over the signal line of CPW.

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