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A Reconfigurable Power-Efficient Quantized Analog RF Front-End With Smart Calibration

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ABSTRACT A power-scalable RF front-end using quantized analog signal processing is presented. The front-end is based on a voltage-mode power-scalable approach which allows the power dissipation to be scaled upon the operative scenario and to perform an agile calibration for mismatch impairments. Power and input dynamic range can be scaled upon the desired 1-dB compression point (1dBCP) (from −15.3 to 0.5 dBm) while keeping the same sensitivity with 2.5-dB NF. Signal path power can vary between 3.3 and 6.4 mW while clock generation and distribution power can vary between 1.6 and 18.5 mW/GHz, with a phase noise as low as −171.2 dBc/Hz. After calibration, IM2 and IM3 improved up to 33 dB while 1dBCP improved by 1 dB, which resulted in achieving an IIP3 of 26.1 dBm and IIP2 of 71 dBm at 0-dBm 1dBCP.

INDEX TERMS Digital calibration, dynamic range (DR), high linearity, low power, nonuniform quantization, power scalable, quantized analog (QA), surface acoustic wave (SAW)-less, voltage-mode.

I. INTRODUCTION

THE REMOVAL of surface acoustic wave (SAW) filters on the modern RF front-end has become a popular trend to reduce the overall cost and save precious real-estate on the device [1], [2], [3], [4], [5], [6]. However, lack of high-Q filters demands high dynamic range (DR) from the RF front-end as well as requiring low noise floor even when large blockers are present (which generally is the case for SAW-less receivers). Large power consumption in both signal and local oscillator (LO) paths are needed to meet these stringent requirements. In modern RF front-ends, the gain in the signal path is limited by using the current-mode approach to increase input 1-dB compression point (1dBCP). This solution however requires a transimpedance amplifier (TIA) in the baseband, whose power can grow significantly when low input-referred noise and high compression point are demanded. In the LO path, the phase noise (PN) must be limited to reduce the impact of reciprocal mixing when large blockers are present. This can only be achieved by increasing the clock buffer sizes and consume significantly more power (e.g., 33 mW/GHz to get a PN as low as −170 dBc/Hz [7]).

A. STATE-OF-THE-ART SAW-LESS RF RECEIVERS REVIEW

Voltage-mode circuits have been widely implemented in RF front-end in the past. However, after the introduction of current passive mixers, which are technology-scaling friendly and are more compatible with modern low-voltage supplies [8], current-mode approaches have become the de-facto standard, especially in SAW-less applications. As mentioned previously, one of the major advantages of using the current-mode approach is minimization of the output swing which, in turn, increases the upper limit of the DR. Nevertheless, current-mode front-ends need power hungry TIAs with stringent noise requirements due to the inherent lack of RF gain in front of them. Fig. 2 provides state-of-the-art RF receivers as well as an overview of their performance and power dissipation breakdown (power consumption is reported for a common operative carrier at 2 GHz). While the majority of

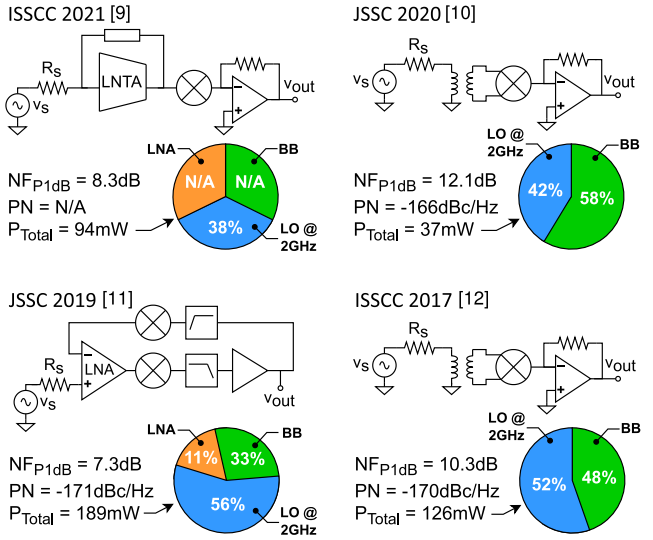

FIGURE 1. Modern state-of-the-art RF receiver comparison with their respective specs (simplified schemes have been used) [9], [10], [11], [12].

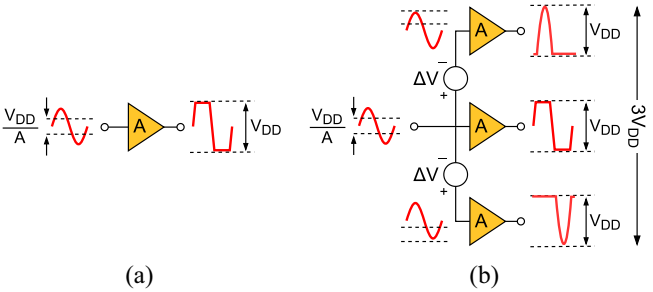

FIGURE 2. (a) Regular amplifier and (b) QA amplifier with three slices, where all amplifiers have the same voltage gain, *A*.

the receivers are current-mode [9], [10], [12], a voltage-mode receiver is proposed in [11]. Such an approach needs to use multiple mixer stages with filters and a feedback circuit for rejecting the blockers in order to meet comparable specs as current-mode receivers. However, the additional circuitry adds complexity and, in turn, requires significantly more power (e.g., 189 mW) than the rest of the current-mode receivers. PN is another major requirement in SAW-less RF receivers due to reciprocal mixing phenomena and this is evident from the total power consumed by the LO generators and the PN specs.

The power consumption of these state-of-the-art receivers are in the order of 100–200 mW at 2 GHz with the only exception of [10]. However, in [10], the performance is sacrificed in favor of a long-lasting battery life with having the highest PN (−166 dBc/Hz) and NF with 1dBCP blocker (12.1 dB). With the aim to outperform already such good designs, this article will explore the potentialities of the quantized analog (QA) signal processing in a voltage-mode fashion and will exploit the inherent QA benefit of the high level of reconfigurability to account for mismatch impairments and lead to a power-scalable design.

B. STRATEGIES FOR LOWERING POWER CONSUMPTION

From the previous observations of the state-of-the-art RF receivers, one strategy to employ in order to reduce overall power consumption should be to maintain a high RF gain for lowering noise and remove power-hungry circuits such as TIAs. This leads us to reconsider the use of a voltage-mode approach which suffers from poor DR when a low-voltage supply is used. To circumvent this DR problem, the QA signal processing was adopted. In a QA system, the signal is sliced in amplitude into multiple paths, where each path (slice) is dedicated amplifying only a single portion of the input signal (Fig. 2). In this way, a low-voltage supply no longer limits the upper bound of the DR performance of a voltage-mode RF amplifier. With the use of multiple paths for processing the input signal, the opportunity to scale the power of the receiver arises when little to no blockers exists (i.e., small input amplitude) and only a single path needs to be active for the receiver. As it will be shown, the entire RF front-end of this work has been sliced into multiple subunits along with the LO distribution so that the LO path power can also be scaled based on the incoming blocker power of the receiver which results in a significant reduction of the power consumption.

C. QUANTIZED ANALOG APPROACH

The QA signal processing was originally introduced by Musayev and Liscidini [13]. The basic concept can be understood by analyzing Fig. 2 where a regular amplifier and a QA amplifier with three slices are compared. In this example, all the amplifiers have the same voltage gain (A), while the overall current of the regular amplifier is equally distributed among the three units of the QA amplifier to keep the same total power dissipation. The QA approach exploits the presence of voltage offsets at the input of each amplifier to slice and amplify different portions of the input signal. As seen from the QA example, the input range is virtually increased beyond the operative voltage supply of the amplifier by a factor of 3 (i.e., total number of slices). Another key advantage of the QA approach is that no noise is contributed at the output and no power is consumed for CMOS implementation when the amplifier is saturated to V_{DD} or ground [14]. This is extremely beneficial since ideally only a single slice is active (i.e., unsaturated) at any given time instance and rest of the slices are inactive (i.e., saturated).

There are additional benefits from implementing the QA approach. First, the overall SNR for a given power will increase in the QA circuit when compared to a single (regular) amplifier as explained in [14]. Another benefit of the QA approach is reducing the impact of mismatches and nonlinearities by adjusting the individual voltage offsets between each slices (i.e., predistorting the voltage offsets) as shown in [15]. Finally, the DR of the QA receiver can be reconfigured based on the value of the voltage offsets between each slice as demonstrated in the QA prototype from [16].

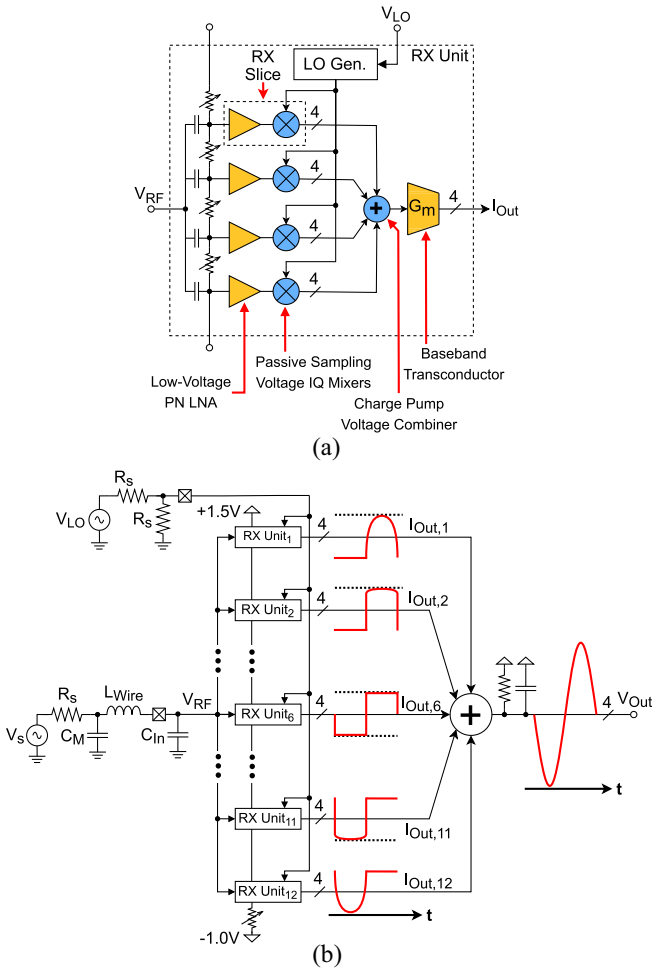

FIGURE 3. Simplified diagram of the proposed QA receiver with (a) 1 RX unit with differential I & Q outputs and (b) complete front-end with 12 RX units.

II. PROPOSED QA RECEIVER

As shown in Fig. 3(a), the proposed voltage-mode power-scalable QA RF front-end was designed starting from a single RX unit quantized into four paths. Each of the four RX slices is composed of an low-noise amplifier and differential I & Q mixers where the four slices of signals are merged together using a passive signal recombiner followed by a transconductor. In order to increase the input range of a single RX unit, up to 12 RX units were stacked vertically where it increased 1dBCP from −15.3 to 0.5 dBm [Fig. 3(b)]. The output signals of the differential I & Q transconductors of each RX unit are eventually combined together in current for the signal reconstruction. The required offsets between the slices were realized using a resistive ladder by ac-coupling the RF input signal as done in [14]. The RX unit is completed by an LO generator that synthesizes the four phases required for the differential I & Q mixers using an external clock signal. Lastly, a pi-matching network was implemented using the inductance of the bondwire, the input parasitic capacitance of the receiver, and an external capacitor, C_M.

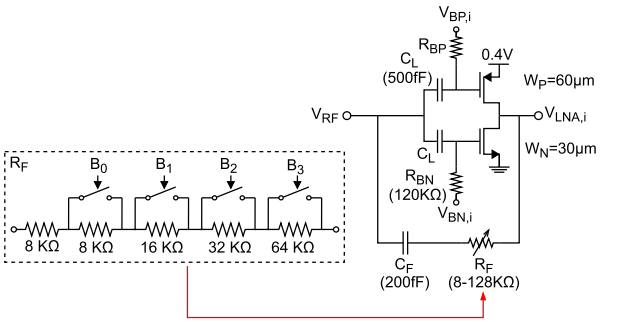

FIGURE 4. Single PN (pMOS/nMOS) LNA slice with variable feedback matching resistor.

In this section, each building block on the RF signal path of the RX unit will be presented in detail, and ending with an insight on the generation of the clock phases required by the differential I & Q mixers.

A. HIGH-SWING LOW-SUPPLY VOLTAGE-MODE LNA

As shown in Fig. 4, the topology chosen for the low-noise amplifier (LNA) is a CMOS push–pull amplifier with a resistive feedback to provide the required input matching [17]. Thanks to the use of the QA approach, the four LNAs of the RX unit can have an overall output swing virtually larger than the voltage supply. This feature allows the use of only a 0.4-V supply without compromising the 1dBCP of the RX unit. To be able to operate with such a low-voltage supply, the nMOS and pMOS gates were independently biased.

The feedback resistor used for matching purposes, R_F, is 4-bit adjustable in order to accommodate for different ΔV values between each LNA. As explained in [16], as more LNA slices operate in parallel by using a smaller ΔV, the overall QA amplifier input impedance decreases. Note that due to the LC matching pi-network, the source resistance to match by the QA receiver on the IC side is higher than 50 Ω because of passive impedance transformation.

As shown in [16], the total noise factor of the QA LNA, nf_{LNA}, can be calculated as a function of the transistor noise parameter γ and total effective QA LNA transconductance $G_{m,\text{LNA}}$ as follows:

$$nf_{\text{LNA}} = 1 + \underbrace{\frac{\gamma}{G_{m,\text{LNA}} \cdot R_s \cdot A_{\text{LC}}^2}}_{\text{LNA}} \tag{1}$$

where R_s is the source resistance value of 50 Ω and A_{LC} is the voltage gain of the LC matching pi-network. For this QA prototype, the target NF of the QA LNA was less than 2 dB (at sensitivity) which can be achieved with $G_{m,\text{LNA}}$ value of approximately 12 mA/V and LC matching pi-network voltage gain of 1.6 V/V.

Note that the dc bias resistors, R_{BN} and R_{BP}, were sized large enough to have negligible noise contribution at the output of the receiver. For the feedback resistors, R_F, the noise contribution can be considered negligible thanks to

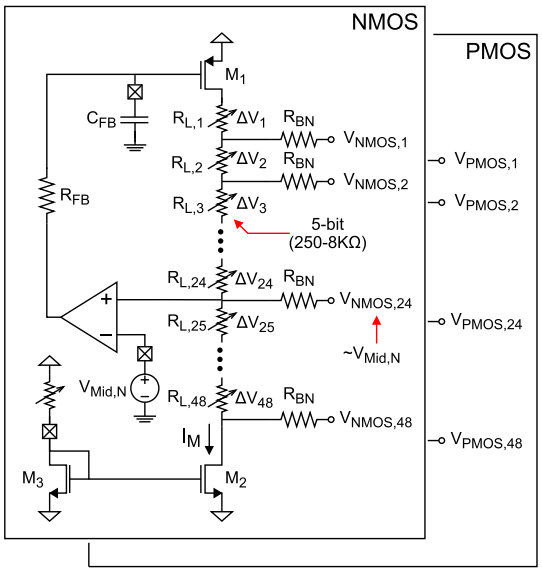

FIGURE 5. QA dc offset generators for individual nMOS and pMOS gates.

the presence of an adequate voltage gain of the amplifier stage (e.g., approximately 15 dB per RX slice) [16].

B. DC OFFSET DISTRIBUTION AND GENERATIONS

In [16], it has been shown that a variation in the value of the dc offset (ΔV) among the slices can be used to reconfigure the system DR to accommodate for different scenarios. In contrast, the proposed QA receiver kept the same distribution for all scenarios, evaluated through an optimization algorithm. The strategy was to find the proper offset for each slice by performing an agile calibration of the mismatch impairments and a correction of distortion of the overall RX, as theoretically suggested in [15]. Hence, the generation of the dc offset was carefully designed to be capable of a more flexible choice of the offsets compared to [16].

The nMOS and pMOS dc bias voltages of each LNA are created using two dc offset generators as shown in Fig. 5. The generator circuit consists of a resistive ladder where an op-amp in feedback controls the mid-node voltage of the ladder. The voltage offset value itself is set using a controllable current passing through the resistive ladder as well as the 5-bit variable resistor ranging from 250 to 8 kΩ. The individual adjustability of the resistors and, in turn, the ΔV values, allows predistortion of the receiver gain characteristic and accounts for mismatches. This results in a higher linearity performance and is further explained in the later section along with the explanation of the automated calibration system.

The entire dc offset generator circuit, including the op-amp, was designed with thick-oxide transistors in order to handle bias voltage of up to 2.5 V (i.e., AV_{DD} and AV_{SS} of 1.5 and −1.0 V, respectively) and consumes 52 μA. Note that in the final implementation of the QA receiver, a charge pump circuit can be used to generate the 1.5 and −1.0 V supplies internally but with approximately 50% efficiency [18].

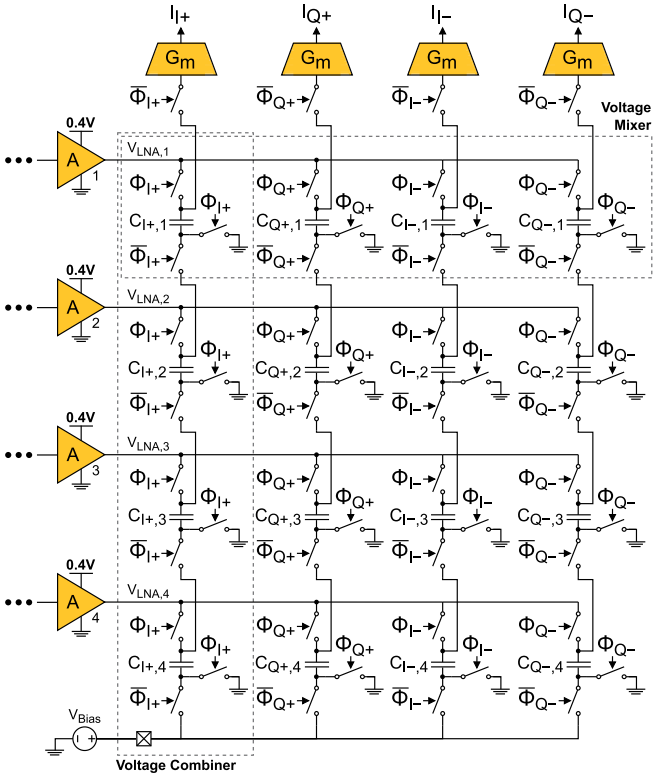

FIGURE 6. Passive voltage-mode sampling differential I & Q mixers and voltage combiners along with baseband transconductors.

Even with such low efficiency of the circuit, the power consumption of the entire dc offset generator can be considered negligible because of the low current consumption of 52 μA. The op-amp used in the feedback circuit is based on the telescopic amplifier and was designed to have over 50 dB of dc loop gain and a phase margin of approximately 85°.

C. HIGH-SWING PASSIVE VOLTAGE-MODE I & Q MIXERS AND PASSIVE VOLTAGE COMBINER

The use of a QA approach is the key to solve the linearity issue of voltage passive mixers since the signal swing of the single RX slice can be relatively small without compromising the overall input range of the front-end. Furthermore, a slight overlap among the slices can compensate the compression occurring at the switch in the same way as compensating the gain roll-off of the LNA, when using the QA approach [16].

The voltage mixer adopted for this design is an I & Q sampling topology using sampling capacitors. Such capacitors are also used to recombine the signals coming from the four LNAs in each RX unit by creating a matrix of switches and capacitors as shown Fig. 6. Each row of the matrix represents the I & Q mixers connected to each of the four LNAs of the RX unit ladder while each column is the signal recombiner for the four QA slices.

As shown in Fig. 6, the LNA output in each row is sampled by the four I & Q LO phases. Since the maximum signal swing at the output of the LNA is 0.4 V (i.e., the LNA supply), a single 2 μm-width nMOS switch (driven by

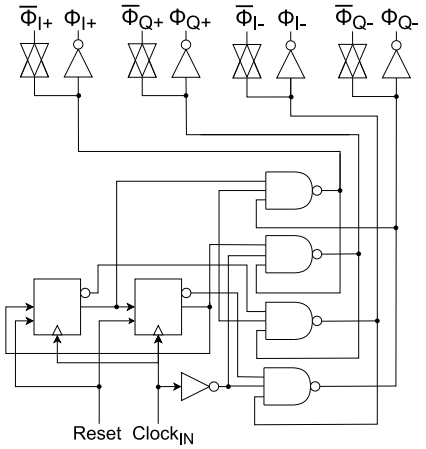

FIGURE 7. Nonoverlapping divide by two LO generators.

a 1.2-V signal) can be used instead of a transmission gate. This reduces the gate capacitance of the mixer switches significantly when compared to passive current-mode mixer switches and relaxes the requirements of the LO generator buffers [19].

Once the voltage signal from the LNA has been downconverted by the differential I & Q mixers, the voltage signal of each phase from multiple slices (up to four slices) are summed together using the voltage combiner (formed by each column of the matrix). The combination occurs during the opposite phase of the corresponding phase of the mixer (e.g., in ϕ_{I-} for the I+ mixer). The partial recombination occurring in each RX unit allows the reduction of the total number of baseband transconductors needed. Unlike the mixer switches, the charge pump circuit switches of the combiner are designed with transmission gates to handle signal swing up to 1.2 V where the nMOS and pMOS widths are 1.3 and 2.6 μm, respectively.

D. BASEBAND TRANSCONDUCTOR

The baseband transconductors were implemented to sum all of the 12 RX unit signals (i.e., 12 of the four differential I & Q signals) together for measurement purposes only. Each signal from the four differential I & Q signals are shorted together in open-drain structure where it connects to an external resistor load to convert to voltage for measurement. Each transconductor can digitally be turned off (along with the corresponding local LO generator) to save power when it is not needed.

E. LO GENERATOR

The LO generator is a divide-by-two circuit with CMOS buffers driving the mixer and voltage combiner switches, which is a modified circuit from [20]. The modification include the NAND gates of the LO generator being routed to prevent overlap from occurring for the 25% duty-cycle signals provided to the differential I & Q mixer switches (Fig. 7).

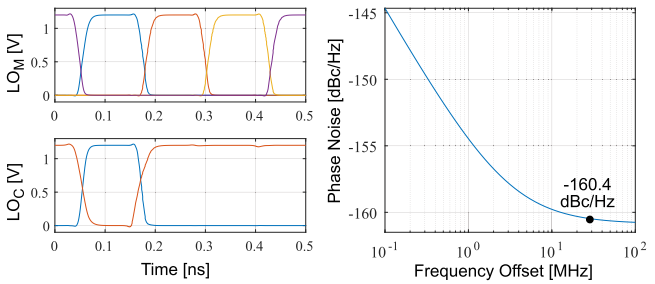

FIGURE 8. LO generator 4-phase mixer and combiner (+I-phase is shown only in this figure) signals, and PN of a single LO generator from post-layout simulation at 2 GHz.

Note that there are multiple LO generators that can individually be turned off digitally to scale the power consumption of the RF receiver and, in turn, scale the PN of the receiver. There is a total of 12 LO generators where each one locally provides the 4-phase clock signals to four differential I & Q mixers (i.e., for a total of four slices per LO). A reset feature was implemented where it sets the phase of all 12 LO generators to a known state. The required PN, $L(\Delta f)$, of the entire combined LO generators can be calculated with the following equation based on the desired NF contributed from reciprocal mixing with the blocker noted as NF_{RM}, the expected blocker power value as P_{Blocker}, and Δf is the frequency offset of interest

$$\mathrm{NF_{RM}} = P_{\mathrm{Blocker}} + L(\Delta f) + 174\ \mathrm{dBm/Hz}. \tag{2}$$

The buffer sizes and power consumption of each LO generator were chosen based on an example LTE scenario where the target NF due to reciprocal mixing with blocker is approximately 4 dB and expected blocker power is -9 dBm at a frequency offset of approximately 28 MHz. Noting that the NF target specs for the QA receiver at sensitivity is less than 3dB, the required PN of all 12 LO generators combined is less than -169 dBc/Hz. Thus, the required PN of each LO generator is approximately -158 dBc/Hz. As shown in Fig. 8, a single LO generator was designed to achieve -160.4 dBc/Hz PN which is approximately 2-dB lower than the required specs. This is noise of the clock divider (excluding the VCO), which is dominated by flicker noise.

III. AUTOMATED MISMATCH CALIBRATION SYSTEM

In order to exploit the adjustability of the dc offset generators for calibration purposes, a test setup was designed and implemented that allowed mismatches of the QA receiver to be calibrated in an automated fashion.

A. SYSTEM OVERVIEW

The test setup for the QA receiver consisted of three main subsystems: 1) motherboard/daughterboard with the microcontroller/test chip; 2) the measurement instruments; and 3) the host PC (Fig. 9). The microcontroller is populated on the motherboard which has several voltage sources along

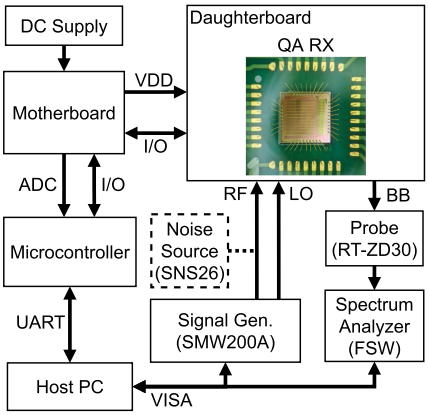

FIGURE 9. Overview of the automated calibration system.

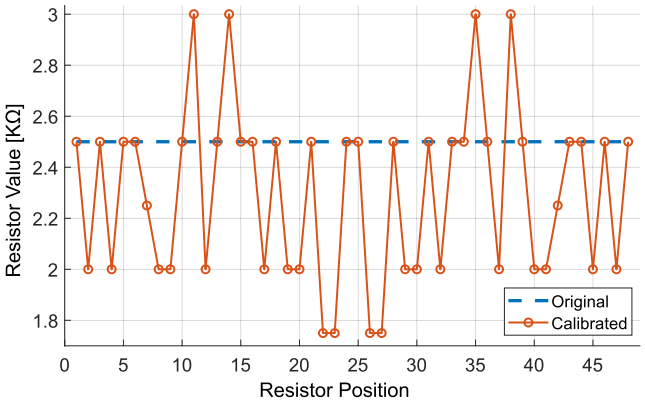

FIGURE 10. dc offset generator variable resistor values (both nMOS and pMOS) after calibration.

with the voltage/current sensors and communicates with the host PC via universal asynchronous receiver–transmitter (UART). The measurement instruments consist of signal generators providing high-frequency RF and LO signals into the test chip via SMA cables, a smart noise source for measuring NF, and a spectrum analyzer connected to the test chip via active differential probe to measure downconverted differential I & Q baseband signals. The measurement instruments communicate with the host PC via virtual instrument software architecture (VISA). The host PC is running MATLAB where it executes automated test scripts that monitors, controls, and calibrates the QA receiver with the use of UART and VISA wrappers.

B. DAUGHTERBOARD AND MOTHERBOARD

The hardware portion of the test setup consists of two main PCBs: 1) daughterboard and 2) motherboard. The daughterboard has the QA test chip populated (wire-bonded) with several decoupling capacitors for the voltage supplies and references. It also has two SMA connectors for the high frequency RF and LO input signals as well as male header pins for providing access to the downconverted differential I & Q outputs. The daughterboard connects to the motherboard via male/female header pins and this was done to enable modularity where the motherboard can easily be modified and upgraded if needed. The motherboard consists of several adjustable low-dropout regulators (LDOs), digital-to-analog converters (DACs), and sensors for voltage/current monitoring.

C. INTEGRAL-BASED CALIBRATION METHOD

To calibrate for mismatches in the QA receiver, an integral-based calibration method was devised. This calibration method first provides a small input signal (e.g., −35 dBm or approximately 11 mV) to the QA receiver where it would only explore the center two resistors in the resistive ladder of the dc offset generator. The gain is recorded with the small input signal by measuring the downconverted output signal at baseband and this recorded gain is set as the main reference gain throughout the entire calibration process. After, a larger input power is provided to explore the next upper/lower resistors on the resistive ladder where it will explore up to four resistors (i.e., one upper and one lower resistors from the previous center two resistors). Then, the two new 5-bit variable resistor values on the resistive ladder are adjusted with all possible combinations with this new input power and the configuration which provided the closest gain to the reference gain is kept. This process is repeated where the input power is slowly and linearly incremented, and the next set of resistors are explored and adjusted until all 48 sets of variable resistors have been explored and optimized. Note that the authors are aware that the proposed algorithm based on a foreground calibration cannot address, as it is, the issues related to voltage and temperature variations. However, the goal of the proposed analysis was to present and verify the feasibility of the corrections of the mismatches and distortions through a nonuniform distribution of the offsets.

Fig. 10 shows the resistor values on the dc offset generator resistive ladders (for both nMOS and pMOS) after the integral-based calibration method was completed. As shown in the plot, the default resistor value for each variable resistor was 2.5 kΩ when no calibration took place. Once the calibration was completed, the resistor values were adjusted where it ranged from 1.75 to 3 kΩ.

IV. QA RX PROTOTYPE AND MEASUREMENT RESULTS

The QA RF front-end prototype was manufactured on the TSMC 65-nm CMOS technology. Fig. 11 shows the prototype with the 12 RX units that consist of 48 voltage-mode LNAs, 48 passive sampling differential I & Q mixers and combiners, 12 LO generators, and 12 baseband transconductors. The total active area with 12 RX units is 0.33 mm^2. The test chip was wire bonded to a PCB which connected to various LDOs, DACs, as well as current and voltage sensors that were all controlled and monitored from a microcontroller. As mentioned previously, the microcontroller communicated with the host PC via UART.

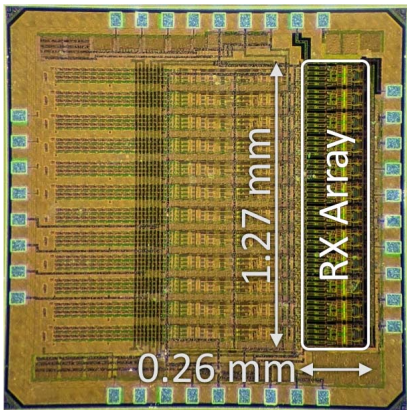

FIGURE 11. QA RF front-end prototype with 12 RX units (active area of 0.33 mm^2).

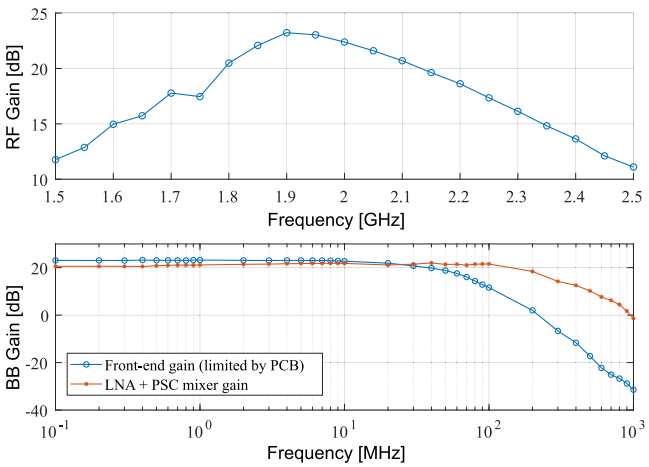

FIGURE 12. RF Gain with 300-MHz BW near 2 GHz and baseband gain after the transconductor and before (i.e., after downconversion) the transconductor.

A. RF AND BASEBAND GAIN

The RF gain of 23.2 dB was measured near 2 GHz with 3-dB bandwidth of approximately 300 MHz, as shown in Fig. 12. For the baseband measurements, there were two separate measurements completed due to parasitic capacitance causing issues at the output of the transconductor with the daughterboard PCB. The expected baseband bandwidth from post layout simulation was over 200 MHz but only 40-MHz bandwidth was measured at the output of the transconductors. The baseband transconductor external load was adjusted to change the gain closer to the RF gain value and to account for the PCB parasitics. After, the measurements were completed again which showed closer bandwidth to the expected value from post-layout simulation of approximately 200 MHz.

B. 1DB COMPRESSION POINT AND NOISE FIGURE

The 1dBCP was measured using an in-band blocker where the blocker power was increased until a significant gain drop was observed as shown in Fig. 13, where it provides the results of the noncalibrated and calibrated QA amplifier using the adjustable dc offset generator. With the calibration, the QA receiver achieved 1-dB higher 1dBCP and reduced

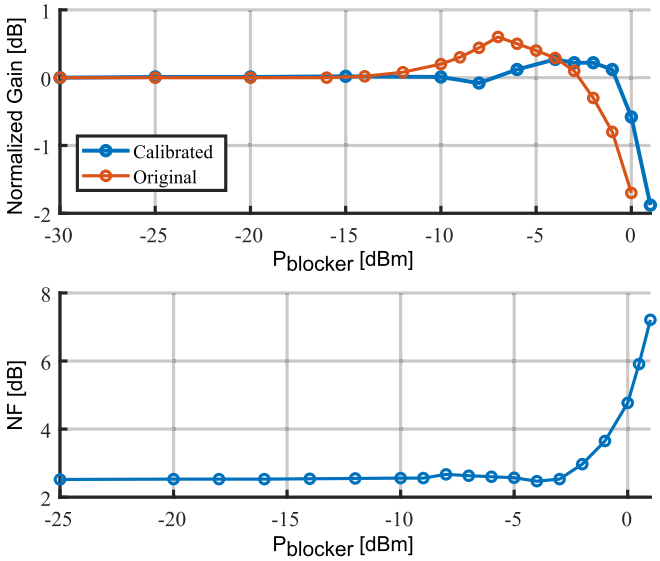

FIGURE 13. In-band gain (normalized) for calibrated and original configurations as well as NF versus blocker power placed at 80 MHz from the carrier.

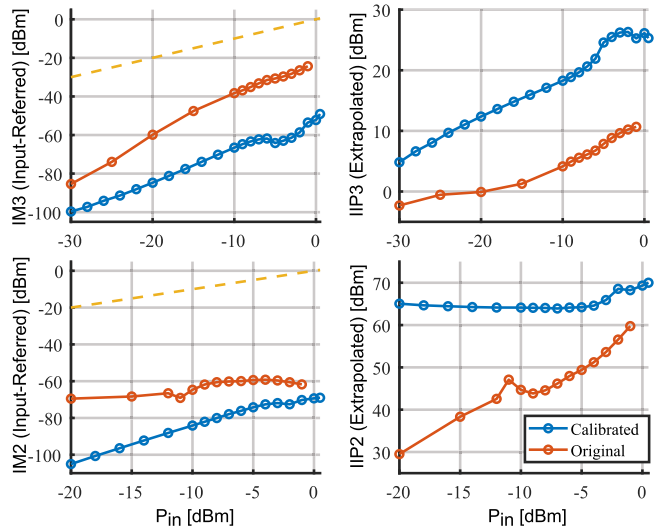

FIGURE 14. IM3 and IM2 measurement results with extrapolated IIP3 and IIP2 where $\Delta f_{IM3} = 120$ MHz and $\Delta f_{IM2} = 200$ MHz.

the peak of the normalized gain by making it more linear near the 1dBCP.

NF at sensitivity was measured at 2.5 dB. With the 1dBCP blocker present, the NF was measured at 2.6 and 5.9 dB for only 1 RX unit enabled and 12 RX units enabled, respectively. As expected, the NF increases with larger blocker power (i.e., with all 12 RX units are enabled) and the effects of reciprocal mixing are observed as shown in Fig. 13.

C. LINEARITY PERFORMANCE: IIP3 AND IIP2

Intermodulation measurements were completed using two tone tests for IM3 and IM2 with varying blocker powers as shown in Fig. 14, where it again provides results with and without calibration. Due to the inherent linearization effect

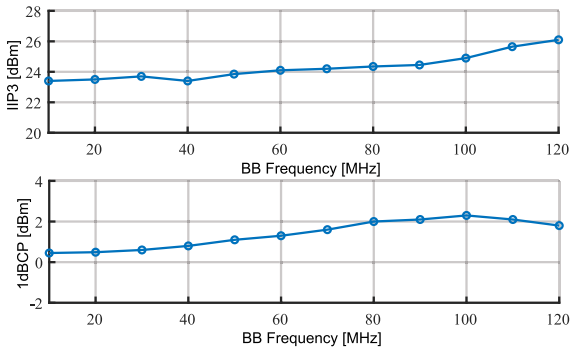

FIGURE 15. IIP3 and 1dBCP measurement results at different frequencies in baseband.

of the QA amplifier as discussed in [14], the IIP3 changes (and grows) with input power (i.e., linearity performance improves with larger blocker power) and must be extrapolated as shown in Fig. 14. With $\Delta f_{\mathrm{IM3}} = 120$ MHz, the QA receiver was able to achieve IIP3 of 26.1 dBm with 12 RX units enabled and 14.9 dBm with only 1 RX unit. For IM2, similar behavior seen from IIP3 was observed with IIP2, where IIP2 generally improved as blocker power increased. With $\Delta f_{\mathrm{IM2}} = 200$ MHz, the QA receiver was able to achieve 71.0 dBm with 12 RX units enabled and 64.6 dBm with 1 RX unit. The calibration was able to improve the IM performance by up to 33 dB. Note that the reported IIP3 and IIP2 are dominated by the transconductors since the frequencies of the IM products (i.e., $\Delta f_{\mathrm{IM3}}/\mathrm{BW} = 0.6$ and $\Delta f_{\mathrm{IM2}}/\mathrm{BW} = 1$) are within the 3-dB BW of the downconverter (i.e., before the transconductors). Fig. 15 provides measurement results of the extrapolated IIP3 from different two tone frequency offsets as well as 1dBCP against varying frequency offsets of the blocker.

D. POWER CONSUMPTION

Power consumption measurements of different RX blocks enabled for varying achievable 1dBCP (i.e., from 1 to 12 RX units enabled) as well as the clock divider with 12 RX units enabled operating at various frequencies are provided in Fig. 16. When 1 RX unit is enabled, approximately half of the power is consumed by the signal path and half of the power is consumed by the LO generator, with total power consumption of 6.5 mW at 2 GHz. However, as additional RX units are enabled to handle larger blockers and increase 1dBCP, the LO generator quickly becomes the largest power consuming circuit block. When all 12 RX units are enabled to handle 0.5-dBm blocker, the total power consumption at 2 GHz is 43.4 mW where 85% of power is consumed by the LO generator alone and signal path only consumes 6.5 mW (i.e., 3.7 mW for LNA, 2.7 mW for baseband, and 0.13 mW for dc offset generators). As mentioned previously, the large LO generator power is needed to reduce reciprocal mixing when large blockers are present which most likely is the case when all 12 RX units are enabled.

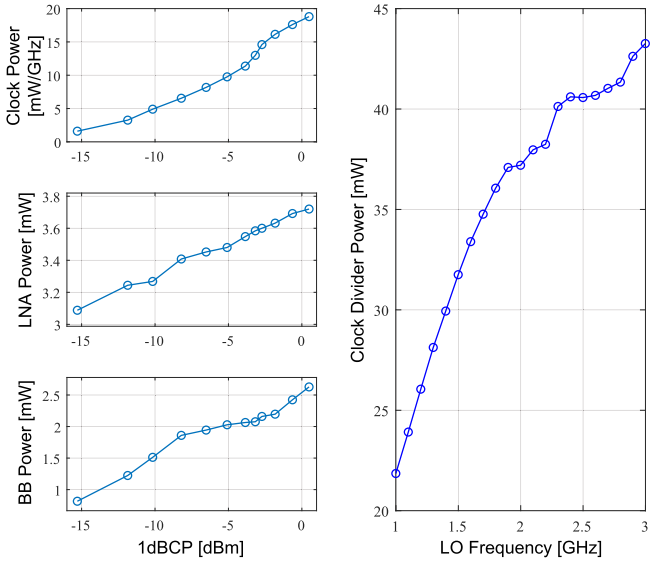

FIGURE 16. Power consumption measurements of different RX blocks versus achievable 1dBCP and the clock divider (12 RX units enabled) versus frequency.

The total active LNA slices at any time instance are approximately 4 and the other 44 slices are saturated and inactive for any amplitude of the input signal. That is, the QA LNA power consumption is self-regulated and only the individual LO generator and baseband transconductor need to be turned off digitally to implement the power scalability feature. The LO power can scale from 1.6 mW/GHz when the required 1dBCP is less than −15.3 dBm (1 RX unit enabled) to 18.5 mW/GHz (12 RX units enabled) when the required 1dBCP is as large as 0.5 dBm.

E. COMPARISON WITH STATE-OF-THE-ART SAW-LESS RECEIVERS

When comparing with state-of-the-art SAW-less RF front-end, this work has the lowest signal path power consumption thanks to the voltage-mode circuits and using the QA approach, despite using one of the oldest technology node (Table 1). Although at 2 GHz, this work is not the lowest power consuming receiver when handling the largest blocker power possible (i.e., all 12 RX units enabled). In fact, [10] consumes the least amount of overall power at 2 GHz. However, [10] has the highest PN of −166.5 dBc/Hz and suffers heavily from reciprocal mixing. This is evident from its NF of 12.1 dB when the 1dBCP blocker is present, which is the highest in the comparison. When comparing the upper DR limit of these receivers, [12] has the highest 1dBCP in the comparison measured at 13 dBm, but suffers from high NF in sensitivity. As mentioned previously, the input blockers for the IM3 and IM2 two tone tests for this work are within the 3-dB BW of the downconverter (i.e., $\Delta f_{\mathrm{IM3}}/\mathrm{BW} = 0.6$ and $\Delta f_{\mathrm{IM2}}/\mathrm{BW} = 1$) and should be considered in-band as opposed to out-of-band measurements reported by all other RF receivers in the comparison.

TABLE 1. Comparison with state-of-the-art SAW-less RF receivers.

Architecture	This Work		ISSCC 2021 [9]	JSSC 2020 [10]	JSSC 2019 [11]	JSSC 2019 [16]		ISSCC 2017 [12]
	QA (Voltage-Mode)		LNTA Based	Mixer First	Voltage-Mode	QA (Current-Mode)		Mixer First
	1 RX ΔV=12mV	12 RX ΔV=12mV				100 RX ΔV=0mV	100 RX ΔV=10mV	
Technology	65nm		40nm	28nm	180nm	65nm		28nm
Max Freq. [GHz]	2.2		3.2	2.0	5.8	1.4		2.0
f_{3dB} [MHz]	40 (200[1])		80	130	150	15		13
RF Gain [dB]	23.2		40.0	32.4	33.2 - 48.3	36.8	20.8	16.0
$NF_{Sensitivity}$ [dB]	2.5		2.7 - 3.6	5.5	3.9 - 5.2	1.9	14.6	6.3
NF_{P1dB} [dB]	2.6	5.9	8.3	12.1	6.0 - 7.3	6.6	-	10.3
P_{1dB} [dBm]	-15.3	0.5	-5.0	3.0	3.0	-8.5	10.5	13.0
IIP3 [dBm] (Δf [MHz])	14.9 (120)	26.1 (120)	13.0 (400)	21.0 (390)	23.0 (200)	-	20.5 (2)	44.0 (80)
IIP2 [dBm] (Δf [MHz])	64.6 (200)	71.0 (200)	70.0 (-)	70.0 (390)	-	-	75.0 (100)	90.0 (80)
PN [dBc/Hz]	-160.4	-171.2	-	-166.5	-171.0	-167.0		-170.0
$P_{Sig.\ Path}$ [mW]	3.3	6.4	58.5	21.6	83.0	14.0	13.8	60.0
P_{LO} [mW/GHz]	1.6	18.5	17.6	7.8	38.0[4]	37.2		33.0
P_{Total} @ 2GHz [mW]	6.5	43.4	93.7	37.2	189.0	-		126.0
Supply [V]	0.4[2], 1.2, 2.5[3]		1.2, 1.3	1.2, 1.8	1.8	0.8, 1.0, 1.2		1.0, 1.2
Area [mm^2]	0.33		0.60	0.16	1.26	0.25		0.49

[1]After mixer down-conversion, [2]supply for LNA, [3]supply for DC offset generators, [4]plus 30mW base power.

Note that there are major differences between this QA receiver and the previous QA receiver from [16]. The previous work used current-mode approach with a TIA and consumed more than twice as much power in the signal path. Furthermore, the buffers for the current-mode mixer switches required significantly more power than voltage-mode mixer switches of this work. Also, there is no power-scalability feature in the previous work where it always has 100 RX units enabled. Note that the previous work has low-noise and high-linearity modes where the ΔV value needs to be adjusted from 0 to 10 mV whereas this work has a fixed nominal 12 mV for all configurations. Another major difference is that the nMOS and pMOS LNA gates of this work are individually ac coupled (as opposed to the two gates tied together) which allows the use of low supply voltage of 0.4 V. Finally, the resistive ladder in the dc offset generator in the previous work were not adjustable and could not calibrate for mismatches.

V. CONCLUSION

A power-scalable RF front-end using the QA approach was presented with being the lowest power consuming receiver when considering both NF and PN, despite using one of the oldest technology nodes. Voltage-mode was implemented to avoid the use of power hungry circuits such as TIAs without sacrificing linearity performance thanks to the QA structure. The power-scalability feature was also presented in this work where both the power consumption and input DR can be scaled based on the required 1dBCP while keeping the same NF at sensitivity. An automated calibration system was also presented where it predistorts the gain characteristics of the QA amplifier to account for mismatches and significantly increased linearity performance of the receiver (i.e., IM3, IM2, and 1dBCP). For the first time, to the best of our knowledge, a voltage-mode RF receiver (with the use of QA structure) is able achieve comparable specs to the state-of-the-art current-mode RF receivers.

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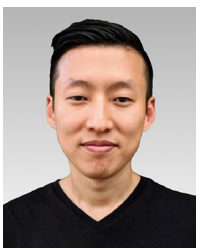

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