IEEE Open Journal of the
Solid-State Circuits Society

Received 8 August 2022; revised 23 September 2022; accepted 14 October 2022. Date of publication 25 October 2022; date of current version 9 November 2022.

Digital Object Identifier 10.1109/OJSSCS.2022.3217019

A 3-GS/s RF Track-and-Hold Amplifier Utilizing Body-Biasing With >55-dBFS SNR and >67-dBc SFDR Up To 3 GHz in 22-nm CMOS SOI

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This work was supported in part by the German Research Foundation (DFG) under Grant ScaledRX 397976366, Grant INST 131/785-1 FUGG, and Grant INST 131/786-1 FUGG; and in part by BMBF under Grant 03ZZ05X04.

ABSTRACT In this article, a 3-GS/s time-interleaved (TI) RF track-and-hold (TaH) amplifier designed in a 22-nm SOI technology is presented. The TaH amplifier is designed to drive an ADC, which can be either two pipeline-ADCs or two rows of SAR-ADCs. Both TI TaH are driven by a single RF-matched wide-band bulk-controlled front-end (FE) buffer. The measured TaH amplifier has an SFDR beyond 70 dBc up to 2.5 GHz and remains above 67 dBc till 3 GHz enabling subsampling. An overall system bandwidth of 4.5 GHz is achieved with an SNR above 55 dBFS. The ultralow-jitter clock regeneration has only 45 fs rms jitter not limiting the SNR up to 3 GHz. Two-tone and multitone measurements reveal a third intermodulation and interband nonlinearity with >72 and >82 dBFS, respectively. Off-chip calibration of offset/gain mismatch and time-skew between both TaH-lanes reduce interleaving spurs >75 dBFS utilizing a 37-tap fractional delay FIR filter. The efficient body-bias control of the technology is used to dynamically body-bias the TaH sample-switch increasing bandwidth by 10% improving settling performance while at the same time the leakage decreases. Static body-biasing is also applied to the common-mode feedback by using the bulk as a control node. The TaH amplifier including the clock generation consumes only 178 mW from a triple 2 V/0.9 V/−0.8 V supply.

INDEX TERMS Body-biasing, common-mode feedback (CMFB), FD-SOI, front-end (FE), RF, time interleaving (TI), track and hold (TaH).

I. INTRODUCTION

FUTURE wireless communication standards such as 6G demand high data rates of several Gbit/s. Thus, ultrawide-band, high-linear, and low-noise RF-ADCs are in the focus of research to support such rates [1], [2], [3]. However, not only the throughput is of importance but also a small footprint is of interest for a low-cost single-chip CMOS solution enabling the elimination of several RF components of the traditional receiver chain to save power and silicon area. This trend is supported by a rapidly shrinking CMOS feature size enabling high transit frequencies above 400 GHz [4] as well as low-phase noise performance [5].

Directly sampling the RF signal, made possible by moving the ADC toward the antenna, has the benefit that the number of mixers can be decreased and the noise figure as well as the flexibility and area efficiency are improved. However, to achieve data rates above 10 Gbit/s, RF sampling requires ADC sample rates in the GS/s regime [2], a high input bandwidth as well as a low phase noise clock. The former can be fulfilled by time interleaving (TI) the ADC resulting in a row of multiplexed sub-ADCs where each sub-ADC operates with a lower sampling frequency as done in [1] and [3]. Furthermore, Ali et al. [2] proposed to use a front-end (FE) sampler to relax the settling requirements

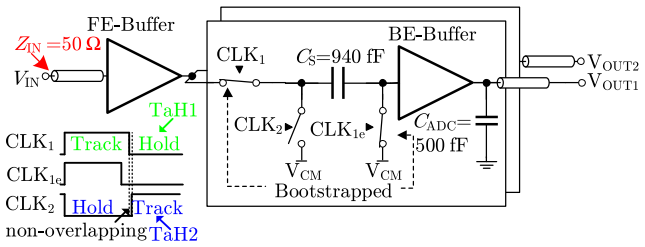

FIGURE 1. Proposed single-ended schematic of the TaH.

of the sub-ADCs saving power and to reduce the number of TI errors. Both approaches require an FE-buffer as in a Nyquist-rate ADC a large sample capacitance is required if a resolution above 9 bit is targeted as less noise is accumulated from C_S. Thus, a matched FE-buffer is typically applied at the input to drive the ADC, achieving both a large input bandwidth and isolating the FE-sampler reducing kickback effects. As a result, the FE buffer together with the FE sampler are one of the most critical building blocks defining the ADC performance in terms of noise and linearity.

Open-loop FE-buffers, as shown in Fig. 1, are the first choice [1], [2], [3] due to their improved power efficiency and bandwidth but with a tradeoff in linearity compared to closed-loop architectures.

This article is an expanded version of the RFIC paper [6] including an introduction to the used 22-nm CMOS SOI technology and a more in-depth circuit analysis of the 3-GS/s low-power high-linear open-loop pseudo-differential FE buffer together with the highly linear TI track and hold (TaH). The proposed TaH amplifier employs both static as well as dynamic body-biasing to control the common mode, reduce the power, and increase the linearity of the FE-sampler. New measurements depict the linearity and noise performance as a function of the input amplitude, sample speed, and supply voltage. Two-tone and multitone measurements are added to show the TaH amplifier linearity with multiple carrier frequencies.

II. 22-NM CMOS SOI TECHNOLOGY

The core circuits inside the TaH amplifier utilize the efficient body-biasing technique of the used SOI process. Therefore, the key technology benefits will be reviewed in this section. 22-nm CMOS SOI has an advanced threshold voltage controllability in forward direction compared to common bulk CMOS. This is achieved by using flipped-well devices enabled by the buried oxide (BOX) layer as highlighted in Fig. 2(a). Hence, an nMOS can be placed above an n-well and a pMOS above a p-well allowing forward body-biasing (FBB). Fig. 2(b) shows the V_{TH} controllability, by applying voltages up to 3 V to the body of the nMOS (−3 V for the pMOS) altering the threshold voltage by 83 mV/V. This benefit is used for dynamic as well as static body-biasing as reported in [6], [7], and [8].

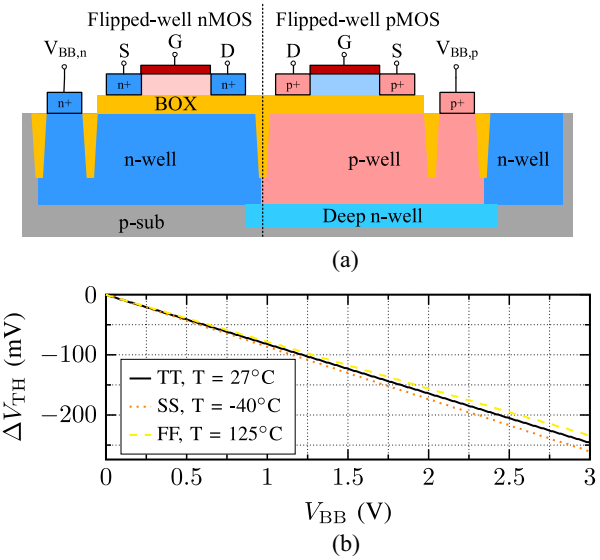

FIGURE 2. (a) Cross section of flipped-well devices [9]. (b) ΔV_{TH} of a flipped well super low-threshold nMOS transistor as a function of the body-bias voltage across PVT [7].

III. CIRCUIT DESIGN

Fig. 1 depicts the schematic of the TaH amplifier. For simplicity, the single-ended design is shown in contrast to the integration, where it is fully differential. The input is differentially terminated to 100 Ω for adequate return loss (RL), while a single wide-band FE buffer drives the two 1.5 GS/s TaHs. Both TaHs operate in a ping-pong fashion, i.e., one TaH is sampling while the other is in the hold mode. Bottom-plate sampling is utilized to achieve high linearity, eliminating signal-dependent charge from the sample directly flowing into the FE buffer due to the high impedance node on the sampler side. Three different clock phases are required per TaH for the sampling operation, where CLK_1 and CLK_{1e} establish the sampling phase connecting the sample capacitance C_S to the output of the FE-buffer. The input signal is sampled with respect to common-mode voltage. Therefore, the common mode is buffered by a 2-stage closed-loop amplifier. In the following phase, the early clock CLK_{1e} opens slightly before the top-plate switch. In the hold mode, CLK_2 connects the top plate to the common mode V_{CM} (Fig. 1) and driving the charge to the back-end (BE) buffer. Typically a row of SAR ADCs or a pipeline ADC would convert the sampled and buffered output voltage into the digital domain, however, in this design, the ADC resampling capacitance is modeled with a statically connected 500-fF MOM capacitance C_{ADC} as shown in Fig. 1. Transmission lines connect the output to the pads.

The FE-buffer is depicted in Fig. 3(a), where a pseudo-differential push–pull architecture with bootstrapped drain nodes is used [1], [6], [10]. With this architecture, the FE-buffer output resistance is minimized. The output resistance R_{BUFF} can be evaluated by

$$R_{BUFF} \approx \frac{1}{g_{M3} + g_{M4} + g_{DS3} + g_{DS4} + g_{MB3} + g_{MB4}} \quad (1)$$

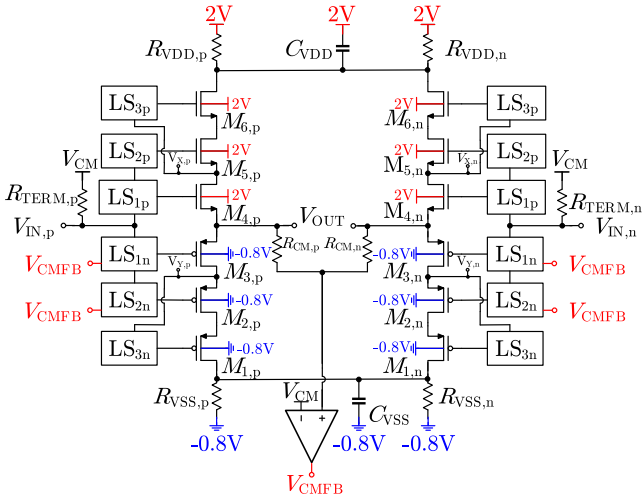

FIGURE 3. Schematic of the (a) pseudo-differential buffer with CMFB and FBB and (b) corresponding LS.

with

$$g_{DS} = \frac{\delta i_D}{\delta v_{DS}} = I_D \cdot \lambda(v_{DS}). \tag{2}$$

Hereby, g_M is the transistors transconductance, g_{DS} is the output conductance, and g_{MB} is the bulk transconductance. Here, both g_M's are utilized in the pMOS and nMOS branches, effectively doubling the g_M/I_D of the buffer. The dc gain is evaluated by

$$\frac{V_{OUT}}{V_{IN}} \approx (g_{M3} + g_{M4}) \cdot R_{BUFF}. \tag{3}$$

The transconductance in combination with second-order effects are defining the linearity of the FE-buffer, thus, a high g_M is preferred to decrease its variation [11]. However, increasing g_M is limited by the input bandwidth, which depends on the total width of the input devices, or by the power consumption, which increases $V_{GS,eff}$ the effective gate-to-source voltage and hence I_D. Therefore, the main source-follower M_3 and M_4 each have a g_M of approximately 100 mS allowing an output impedance of approximately 5 Ω total, which is an optimum tradeoff between input and output bandwidth, linearity, suppression of kick-back effects between both TI lanes, settling, and power consumption. The FE-buffer branch current is set by M_3 and M_4 to about 10 mA for a fast slewing. Both source-follower stages suffer, from a low drain-to-source resistance, due to the large signal swing, degrading the linearity of the buffer as highlighted in (1) and (2). Increasing the channel length will improve the g_{DS}, however, this degrades the input bandwidth and thus the overall performance. Another option to improve the g_{DS} is to decrease the variation of V_{DS} by bootstrapping the drains of M_3 and M_4. Therefore, two-level of cascoded source-followers are added improving g_{DS} and hence the linearity of the source-follower buffer stage [12]. Two additional supplies are necessary to provide sufficient voltage headroom for all source-followers and their cascodes enabling a 1.2-V full-scale (FS) signal swing. Thus, the additional power supplies of 2 and −0.8 V increase the linearity and noise performance of the entire FE at a cost of raised power consumption. All stacked source-follower transistors demand a dc shift of a V_{GS} to bias them in the desired operating point. Thus, all gates of M_2–M_5 are connected to the input via the level shifters (LSs). Therefore, the chosen input common mode of 600 mV is shifted by a $\pm V_{GS}$ for M_3 and M_4. The gates of M_2 and M_5 require a higher dc shift compared to M_3 and M_4 to account for the drain-to-source voltage of M_3 and M_4, which is higher than their $V_{GS,eff}$ to have a safe operating condition across process corner. M_1 and M_6 get their gate voltages from the level-shifted nodes V_X and V_Y to reduce the parasitic gate capacitance seen from the input. Hence, the dc levels require a shift of a $\pm V_{GS}$ plus the drain-to-source voltage of M_2 and M_5. All transistors M_1–M_6 exploit the body-biasing effect by FBB them to reduce the required dc level shift due to a reduced threshold voltage improving the voltage headroom for the LS circuits and enabling a shared supply. Table 1 summarizes the minimum required gate voltages for M_1–M_6.

TABLE 1. Required gate voltages for all source-followers and cascodes.

Device	Minimum $V_{BIAS,i}$	$V_{BIAS,i}$
M_1	$V_Y - (V_{GS,eff,M1} + V_{TH,1} + V_{GS,eff,M2})$	-0.42 V
M_2	$V_{IN} - (V_{GS,eff,M2} + V_{TH,2} + V_{GS,eff,M3})$	-0.06 V
M_3	$V_{IN} - (V_{GS,eff,M3} + V_{TH,3})$	0.22 V
M_4	$V_{IN} + (V_{GS,eff,M4} + V_{TH,4})$	0.92 V
M_5	$V_{IN} + (V_{GS,eff,M5} + V_{TH,5} + V_{GS,eff,M4})$	1.25 V
M_6	$V_X + (V_{GS,eff,M6} + V_{TH,6} + V_{GS,eff,M5})$	1.62 V

The LSs that generate the dc shifts are depicted in Fig. 3(b). Here, two current sources provide a constant current of 100 μA to control the IR drop over the resistor R_{BIAS}. An ac path is added in parallel by the 1-pF feed-forward capacitance C_{FEED}. R_{BIAS} and C_{FEED} introduce a

pole/zero doubled generating a flat frequency response above 100 MHz.

Cascoded current sources are also used in LS_1 and LS_2 to reduce the channel length modulation stabilizing the bias current improving the overall source-follower linearity. A reliable operating condition across FS input signal swing is given by using thick gate oxide transistors as cascodes, where the voltage exceeds 0.9-V signal swing. The upper current source of LS_{3p} and lower current source of LS_{3n} have a reduced minimum voltage headroom of approximately 100 mV, due to the required signal swing and the needed gate voltage of M_1 and M_6. Thus, only a single CS without a cascode is used, not limiting the linearity as proven by simulations. The reference current is externally controlled and mirrored to all CS inside the LS, to tune the bias points and thus the FE-buffer current across process corners.

The input impedance is differential matched to 100 Ω and externally ac-coupled. Thus, the input common mode is set by the level-shifting network requiring a control loop to regulate the output common mode. Contrary to [1], the proposed common-mode feedback (CMFB) uses the transistors bulk, inside LS_{1n} and LS_{2n}, as an input as shown in Fig. 3(b). Therefore, the CMFB senses the output common mode with a 50-kΩ resistor and compares it with the desired common mode of 0.6 V via a differential amplifier. The difference is fed back regulating the current source transistor of LS_{1n} [Fig. 3(b)] and LS_{2n} threshold voltages. Here, the CMFB regulates both current sources from LS_{1n} and LS_{2n} to maximize the loop gain. As a result, the FE-buffer and hence the TaH amplifier can be directly driven without the need of a bias-T (no dc level required) on the source side. However, the proposed solution exploits the body-bias feature and can be thus only integrated in an SOI technology.

Both supplies of 2 and −0.8 V are reused inside the LS to reduce the pad count and to save power. This leads to a challenging small voltage headroom for the upper current source of LS_{3p} and lower current source for LS_{3n} due to the biasing. The high dc shift at the gates of M_1 and M_6 is twofold: first, the transistors M_2 and M_5 require a higher drain-to-source voltage compared to their effective gate-to-source voltage to have a safe operating condition across process corner; second, the drain-to-source voltage of M_1 and M_6 is limited to 900 mV across FS signal swing to keep them in reliable operating conditions. Therefore, M_1 and M_6 have a decreased $V_{GS,eff}$ leaving more headroom for the current sources. Furthermore, a small degeneration resistor of $R_{VSS} = R_{VDD} = 10\ \Omega$ is added to the drains of M_1 and M_6 to reduce the drain-to-source voltage of the transistors for a reliable operating condition. The voltage drop over both degeneration resistors is stabilized by connecting both drain nodes with their pseudo-differential counterpart forming a virtual ground. The virtual ground is stabilized by the capacitance C_V to filter any noise degrading the linearity of the overall FE-buffer. In addition, an overall simulated FE-buffer input capacitance of only 215 fF dominated by the source-follower M_2–M_5 is achieved.

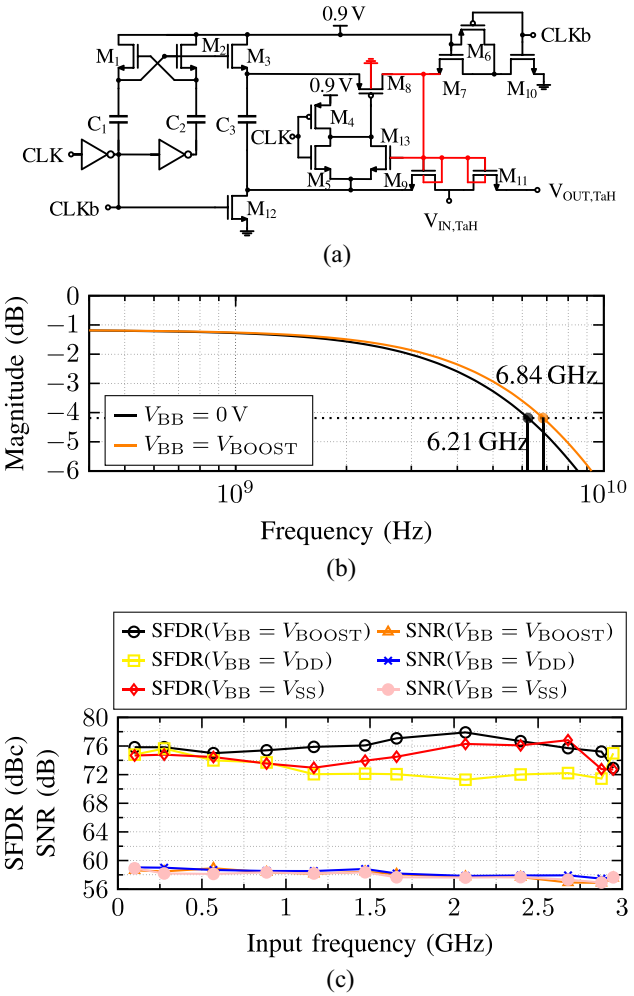

FIGURE 4. (a) Schematic of the modified bootstrap, (b) simulated TaH tracking bandwidth benefit, and (c) SFDR/SNR results over the input frequency and different body-biasing options.

In order to achieve high linearity and a high bandwidth the top- and bottom-plate switches are implemented as bootstrapped switches shown in Fig. 4(a) [13]. Here, M_3 and M_{12} charge the bootstrap capacitance C_3, while M_4 pulls up the gate of M_8 and thus disconnects the bootstrap capacitance from the sample switch M_{11} during the charging process. CLKb triggers M_7 and M_{10}, which initiate the hold phase of the sampler by discharging the gate of M_9, M_{11}, and M_{13}. The track-phase starts when CLK is high and thus M_5 pulls down the gate of M_8 applying a constant gate-to-source voltage of approximately 0.9 V_{DD} to M_{11}. M_6 ensures that the floating node between M_7 and M_{10} is biased to V_{DD} to reduce the leakage in the track phase.

Thanks to 22-nm CMOS SOI static body-biasing, as well as dynamic body-biasing can be applied inside the bootstrap circuit enabling multiple performance enhancements compared to the traditional bootstrap. The body of M_8 is zero-body-biased (ZBB) to GND to separate the well capacitance from the signal path resulting in a lower parasitic capacitance and a lower sample switch V_{GS} variation.

Typically this would introduce latch-up issues, however, the SOI prevents those due to the separated wells from the drain and source region [9]. Thus, M_8 is ZBB in the hold phase and FBB in the track phase, since all G/D/S nodes are shifted by approximately $0.9V_{DD}$, reducing the transistors on-resistance while the off-resistance is unchanged. The effect can be mathematically shown by the on-resistance model of the nMOS in a linear region

$$R_{ON,n} = \frac{1}{\mu C'_{OX}\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH,n}(V_{BB}) - \frac{V_{DS}}{2}\right)}. \quad (4)$$

V_{BB} changes the transistor's threshold voltage and thus the current leading to an increased on-resistance in the ZBB state as well as a decreased on-resistance in the FBB state. However, as FBB reduces the switch on-resistance the off-resistance decreases resulting in leakage effects in the hold phase if FBB is applied to the sample switch M_{11}, degrading the linearity, especially at hot temperatures. Lallement et al. [14] proposed to apply dynamic body-biasing to reduce the leakage in the off-state. Alike [14], M_9 and M_{11} are FBB during the track phase and ZBB in the hold phase. Therefore, the boosted clock is used to drive both the gate and the well of both transistors to reduce the on-resistance and its variation, which improve the linearity and maximize the bandwidth. Simulations of the TaH connected to the FE-buffer show a tracking bandwidth improvement of >10% compared to ZBB as depicted in Fig. 4(b). Note that the −1.2-dB drop at low frequencies is due to the FE-buffers bulk transconductance g_{MB} as highlighted in (1) and the LSs. Simulations reveal also a reduction of the hold-mode leakage by a factor of 6 compared to a static FBB at the FF 125 °C corner. The bandwidth depends on the sum of the buffer output impedance, the impedance of the switches, and the load capacitance and can be calculated by

$$f_{3dB} = \frac{1}{2\pi \cdot (C_S + C_{PAR})(R_{BUFF} + R_{SWITCHES}(V_{BB}))}$$

where R_{BUFF} is ∼5 Ω and C_{PAR} is negligible compared to the 940-fF sample capacitance. From the simulated 6.21-GHz bandwidth [Fig. 4(b)], $R_{SWITCHES}(V_{BB} = 0\ V)$ can be estimated as ∼22.3 Ω. With dynamic body-biasing the bandwidth increases to 6.84 GHz, leading to an estimate of $R_{SWITCHES}(V_{BOOST})$ of 19.8 Ω, showing a decrease in impedance of 2.5 Ω. In addition, the well capacitance of M_9 and M_{11} reduce the gate-to-source voltage in the tracking phase due to the capacitive divider between C_3 and C_{PAR} compared to the traditional bootstrap. However, if a static ZBB design is targeted the sample switches have to increase to maintain the same tracking bandwidth as the proposed sampler leading to an increased C_{PAR} which also reduces the gate-to-source voltage. Simulations of the TaH amplifier with different body-bias options reveal that dynamic body-biasing the sample switch improves the overall linearity, while the SNR is in the same range, compared to a static body-biasing approach as depicted in Fig. 4(c).

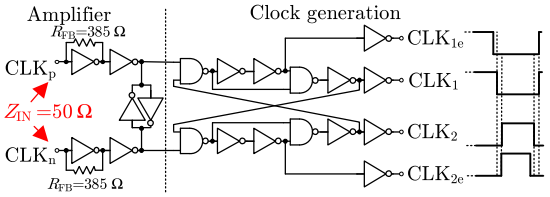

FIGURE 5. Clock amplification and generation.

The TaH amplifier receives the clock signal externally and generates all four clock phases on-chip. Therefore, the differential clock is externally ac-coupled and connected to the clock generator, depicted in Fig. 5, via transmission lines. A self-biased inverter amplifies the clock with a gain of approximately 17 dB with a low jitter performance as demonstrated in [15] and [16]. The feedback resistor R_{FB} does not only set the gain of the amplifier it also defines the input impedance since the input sees roughly the feedback resistor divided by the gain of the amplifier. Thus, the feedback resistor has a value of 385 Ω resulting in a well-matched 50-Ω input for a low RL. The ratio of the transistors inside the self-biased inverter is designed so that the input and output levels are V_{DD} half. A cross-coupled inverter ensures a 180° phase difference between both amplified and buffered clocks. The clock generation provides the nonoverlapping clocks CLK_1 and CLK_2 as well as the corresponding early clocks.

Jitter plays a dominant role since it degrades the high-frequency input SNR performance. Thus, a low jitter clock is required for CLK_{1e} and CLK_{2e} as they are the jitter contributors. Therefore, the clock generation is adjusted to have a sharp falling edge, after one inverter in the bootstrap circuit, resulting in a sharp rising edge at M_{10} [Fig. 4(a)], which opens the sample switch M_{11} and introduces the hold phase. As a result, a simulated clock jitter of 45 fs rms was extracted, which does not limit the SNR up to a 3 GHz input. Timing mismatch between both clocks occurs due to process variation degrading the SFDR performance by unwanted TI tones. However, in this design, the sample-phase mismatch will be calibrated off-chip with a fractional delay FIR filter.

In the hold phase, the held signal is buffered by the BE buffer, which is a replica of the FE buffer. Hence, the parasitic capacitance at the input of the BE buffer ($C_{PAR,BE}$) reduces the signal power due to the capacitive divider between C_S and $C_{PAR,BE}$ resulting in a loss of −4.5 dB including the transfer characteristic of the buffer itself. Furthermore, the BE buffer has to drive the 500 fF modeled ADC input capacitance as well as the 50-Ω impedance from the measurement device decreasing the signal power by −1 dB.

IV. EXPERIMENTAL RESULTS

The fabricated 3-GS/s time-interleaved (TI) RF TaH amplifier in 22-nm CMOS SOI is shown in Fig. 6(a). A total area of 650 × 1000 μm^2 is required mainly due to the probe spacing requirements. The TaH core only occupies an area of 50 × 35 μm^2, while the FE buffer requires 68 × 230 μm^2.

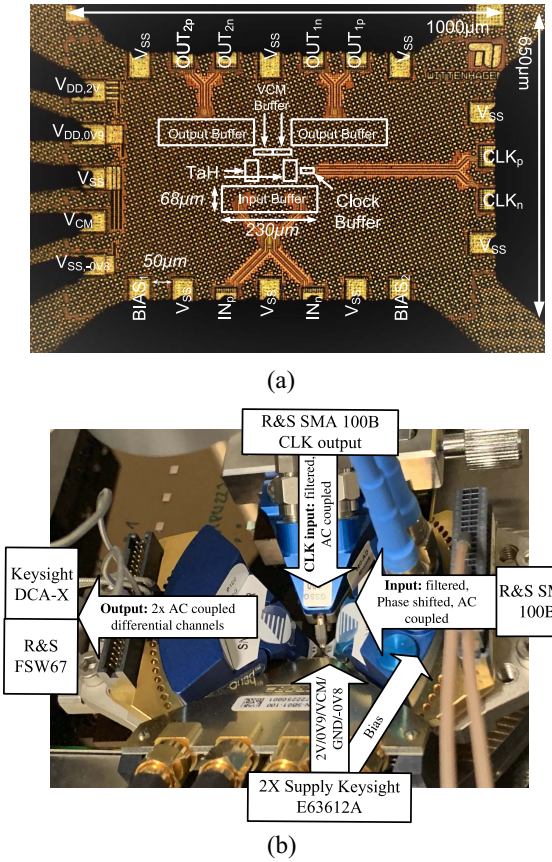

FIGURE 6. (a) Die micrograph and (b) measurement setup.

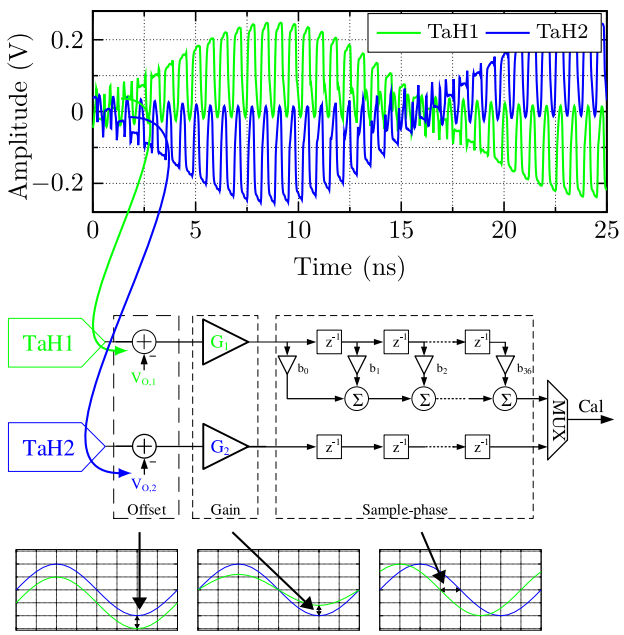

FIGURE 7. Measured time-domain output with the off-chip signal processing.

Fig. 6(b) depicts the measurement setup including all utilized external components. The TaH is measured using a wafer probing station, where input and clock signals are generated by the ultralow jitter signal generator R&S SMA100B.

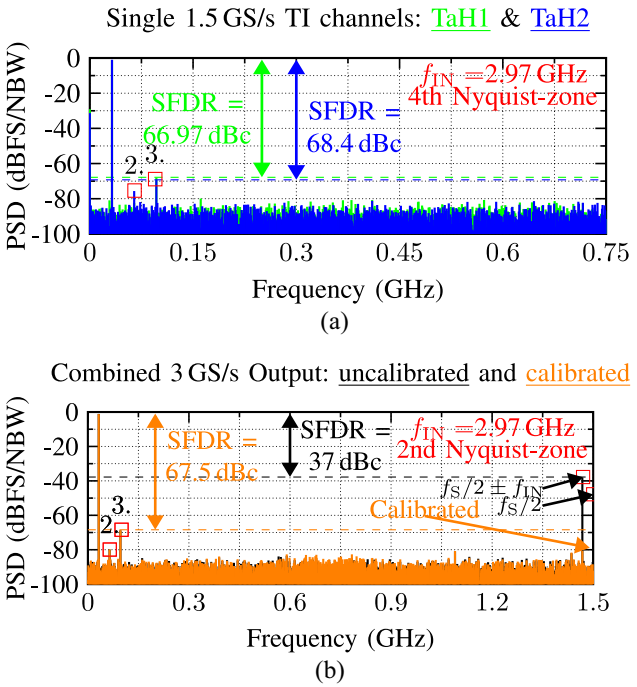

FIGURE 8. (a) Magnitude response of the four times averaged single and (b) uncalibrated and calibrated output at 0 dBFS with an RBW of 732 kHz.

Phase shifters are used at the input to tune the phase imbalance introduced by the balanced–unbalanced converter and cables.

Fig. 7 depicts the time-domain waveform of both differential TI channels measured with the sampling scope Keysight DCA-X. Here, a 2.97-GHz 1.2-V FS sinusoidal input is down-folded from the 4th Nyquist zone to 32 MHz due to subsampling. The frequency spectrum is analyzed by taking one sample point of the DCA-X at the end of each hold phase and subsequently performing a 2048 point FFT. Fig. 8(a) shows the resulting FFT of both TaH channels obtaining an SFDR of 68.4 and 67 dBc, respectively. To measure such high linearity, the repetitive input waveform was averaged four times to lower the noise floor of the DCA-X. By combining both channels in Fig. 8(b), the SFDR drops to 37 dBc due to TI spurs. Offset, gain, and sample-phase mismatch between both samplers lead to unwanted frequency spurs at $f_S/2$ and $\pm f_{IN} + f_S/2$ significantly degrading the overall linearity of the sampling system. The spurs at $f_S/2$ are caused by dc-offset mismatch while the latter spurs arise due to a combination of gain, sample-phase, and bandwidth mismatch. Fig. 7 highlights the off-chip calibration steps utilizing MATLAB. The offset error is digitally corrected by calculating the mean offset V_O per channel and digitally subtracting it. The gain error is also digitally corrected by detecting the rms signal power of each channel and applying a gain scaling coefficient G. Furthermore, the sample-phase mismatch is digitally detected and corrected by applying a fractional delay FIR filter. The number of taps is 37 which is set to achieve a sufficient high bandwidth with

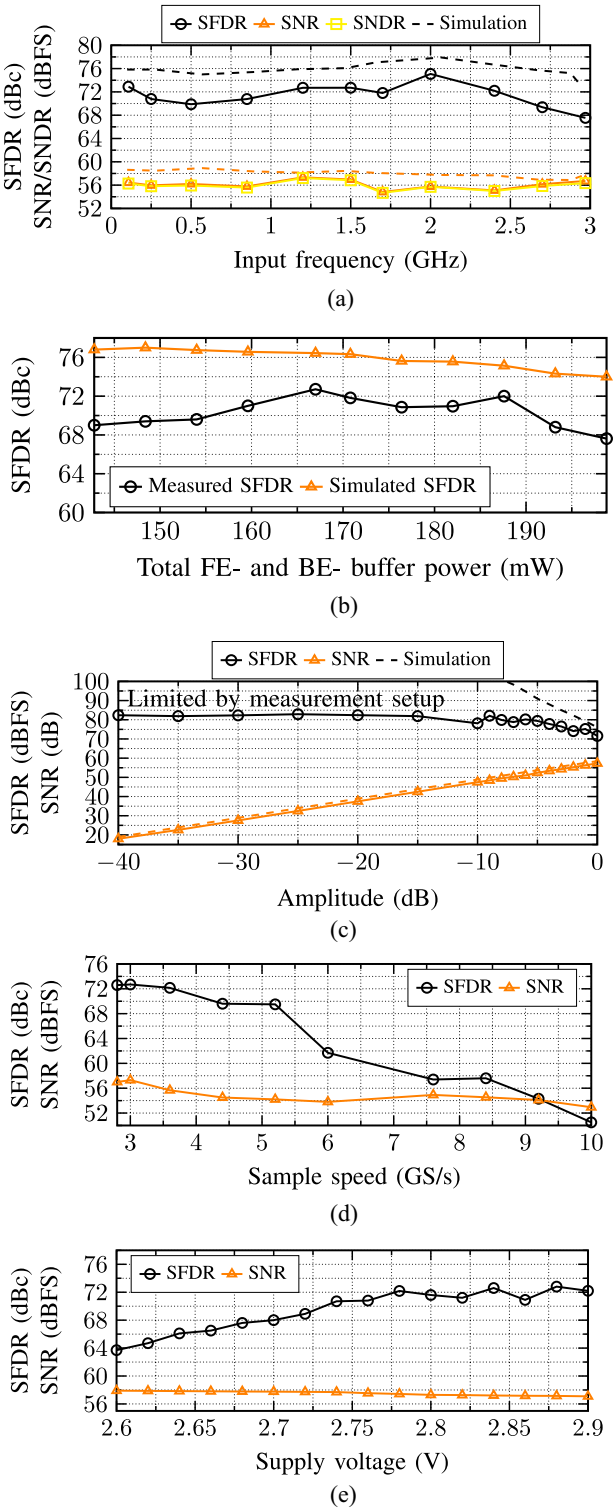

FIGURE 9. Measured and simulated TI SFDR and single-channel SNR/SNDR (a) over the input frequency and for 1.47-GHz input frequency over (b) total FE- and BE-buffer power, (c) input amplitude, (d) sample speed, and (e) supply voltage.

constant group delay. The required correction accuracy can be calculated by

$$\mathrm{SFDR} = \frac{1}{\pi^2 \cdot \Delta T^2 \cdot f_{\mathrm{IN}}^2}$$

leading to a ΔT below 30 fs for a TI spur smaller than 70 dBc at the maximum input frequency of 3 GHz [17]. Finally, the combined and calibrated output in Fig. 8(b) obtains an SFDR of 67.5 dBc for a 2.97-GHz input, while the TI mismatch spurs are below 75 dBFS.

The spectrum analyzer R&S FSW67 is used for the SNR measurements since the DCA-X has only a limited SNR of 47 dB. Thus, SNR measurements are performed on a single channel. Note that the TI calibration does not add noise to the combined signal. Fig. 9(a) depicts the SNR over the input frequency together with the combined and calibrated SFDR. An SFDR above 70 dBc is obtained up to 2.5 GHz and remains above 67 dBc till 3 GHz, while an overall SNR/SNDR of above 55 dBFS is achieved. Furthermore, simulation results are added showing an SFDR difference about 3–5 dB which is caused by mismatch and the limited linearity of the sampling scope. The SNR difference is 0.5–2.5 dB and is caused by the total integration of the tracking and hold phase of the TaH sampler while measuring with the spectrum analyzer. Additionally, the SFDR across the total buffer power at a 1.47-GHz Nyquist input is measured and simulated by varying the external reference current and is depicted in Fig. 9(b). The SFDR is above 67 dBc and the optimum power linearity ratio is at 167 mW which is used for all measurements. Fig. 9(c) shows the measured and simulated TaH amplifier performance for a 1.47-GHz Nyquist input with a varying input amplitude. The SNR behaves as expected and increases for a raising input amplitudes, while the SFDR is above 70 dBFS and is limited to 80 dBFS below −15 dB due to the sampling scope resolution.

Fig. 9(d) depicts the SFDR and SNR for a 1.47-GHz FS sine-wave input with a varying sample speed. The SFDR remains above 69 dBc up to 5.2 GS/s and decreases for higher sample speeds since there is not enough settling time while SNR slightly decreases due to the same effect. In order to analyze the effect of a nonideal supply source, the total supply voltage, which is the sum of the lower −0.8 V and upper 2 V [Fig. 3(a)], is swept from originally 2.8 V to 2.9 V and 2.6 V. As a result, Fig. 9(e) shows the SFDR and SNR for a 1.47-GHz input, where the SFDR is greater than 70 dBc above 2.73 V supply. By reducing the supply, the current decreases and thus the SFDR decreases due to less tracking bandwidth, while the SNR increases since less noise is accumulated.

A subsampled calibrated two-tone spectrum is shown in Fig. 10(a) with a 34-MHz band around 2.7 GHz where both inputs have an input amplitude of −6 dBFS. The TaH is IM_3 limited and achieves a linearity of 72.3 dBFS. In order to test an OFDM environment, multiple tones representing multiple carrier frequencies at 1.47 GHz with a 16-MHz spacing are connected to the TaH amplifier and the output is measured. Furthermore, to see the in-band intermodulations, one of the carrier tones is removed and the intermodulation is measured at that tone. As a result, Fig. 10(b) shows an in-band linearity of 82.4 dBFS where the sample-phase mismatch spurs are visible around dc.

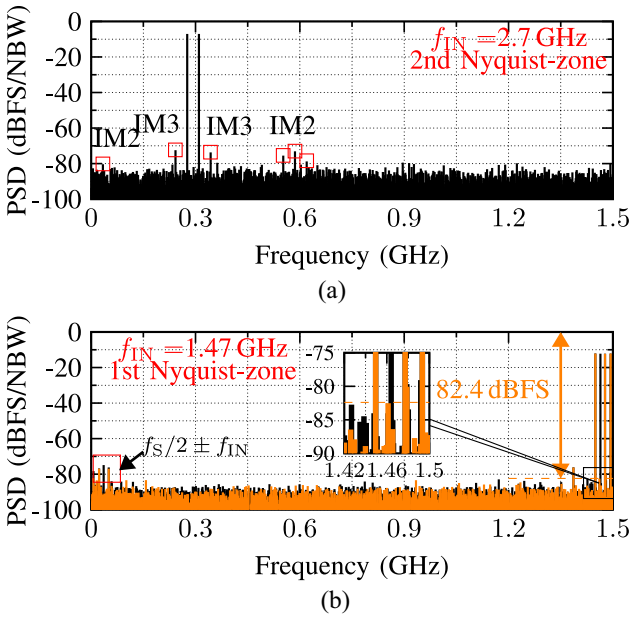

FIGURE 10. Measured (a) two-tone spectrum with f_{IN} = 2.7 GHz and f_{BAND} = 34 MHz and (b) multitone test to show the in-band intermodulation with f_{IN} = 1.47 GHz and f_{BAND} = 16 MHz, both with an RBW of 732 kHz.

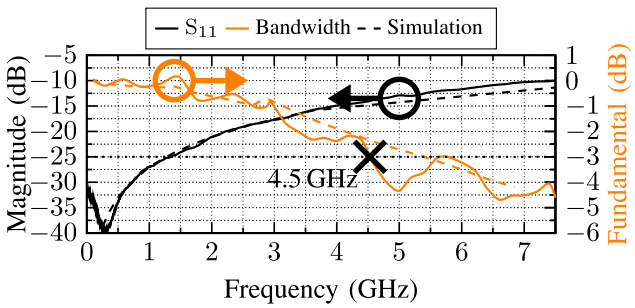

FIGURE 11. Measured and simulated input matching and bandwidth.

In order to evaluate the large signal bandwidth a low-frequency FS sine-wave input is measured as a reference point. Followed by measuring an input frequency sweep with the same source amplitude. Finally, the input route up to the probe connection is measured with a VNA and the result is embedded with the measured TaH amplifier output. As a result, an overall large-signal system bandwidth of 4.5 GHz is achieved with an overall loss of only 4.5 dB up to 7.5 GHz as shown in Fig. 11, which also includes the simulation results. Furthermore, the input is measured with the Keysight VNA obtaining an RL below −10 dB till 7.5 GHz. The TaH amplifier requires a power of only 178 mW where 11 mW is needed for the clock generation and the bootstrap circuit, 55.7 mW for the FE-buffer, and 111.4 mW for the BE-buffers. All performance parameters are summarized in Table 2 and are compared with state-of-the-art TaH FEs.

V. CONCLUSION

In this article, a high-linear 3-GS/s RF TaH amplifier exploiting the strong body-bias feature of 22-nm CMOS SOI was presented. The pseudo-differential FE buffer utilizes stacked source-followers biased by LSs to maximize the linearity. FBB all source-followers inside the buffers reduces the power consumption, since only 2.8 V are required for 6 stacked source-follower for a 1.2-V input swing. A degeneration resistor ensures the reliability of the outer cascode transistors within the buffer by forming a virtual ground node. Furthermore, also the CMFB employs static body-biasing by building a loop using the current source body as an input. Dynamic body-bias inside the TaH increase the bandwidth by more than 10% while leakage current is reduced by a factor of six. In summary, the TaH amplifier achieves a high linearity of better than 70 dBc up to 2.5 GHz while remaining above 67 dBc till the end of the second Nyquist zone with an SNR above 55 dBFS. The TaH amplifier remains above 69 dBc up to 5.2 GS/s for a 1.47-GHz FS sine-wave input. Two-tone and multitone measurements were performed revealing an IM3 of 72 dBFS and interband linearity of 82 dBFS. An overall bandwidth of 4.5 GHz supports a wide range of input frequencies where all RF inputs are well matched below −10 dB up to 7.5 GHz. The TaH amplifier draws only 178 mW from a triple supply including the ultralow jitter clock generation.

TABLE 2. Comparison table with state-of-the-art TaH.

	ISSCC 2017 [1]	ISSCC 2017 [3]	ISSCC 2020 [2]	**this work**
Technology	28 nm	16 nm FinFET	16 nm FinFET	**22 nm FD-SOI**
Sample-rate (GS/s)	10	4	12	**3**
Bandwidth (GHz)	7.4	-	18	**4.5**
f_{IN} (GHz)	4	2	4	**3**
SFDR at f_{IN} (dBc)	65.5	67	61	**67.5**
SNDR at f_{IN} (dB)	55	57.3	53	**56.3**
FE-Power (mW)	400	282	220	**178**
Power supplies	3	-	2	**3**

ACKNOWLEDGMENT

The authors would like to thank Mentor Siemens for AFS as well as Globalfoundries for providing 22FDX MPW support and fabrication of the chips.

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