

A 3.7-mW 12.5-MHz 81-dB SNDR 4th-Order Continuous-Time DSM With Single-OTA and 2nd-Order Noise-Shaping SAR

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ABSTRACT This article presents a hybrid 4th-order delta–sigma modulator (DSM). It combines a continuous-time (CT) loop filter and a discrete-time (DT) passive 2nd-order noise-shaping SAR (NS-SAR). Since the 2nd-order NS-SAR is robust against PVT variation, the stability of this 4th-order DSM is similar to that of a 2nd-order CT-DSM. The CT loop filter is based on single-amplifier–biquad (SAB) structure. As a result, only one OTA is used to achieve 4th-order noise shaping, leading to a high power efficiency. Moreover, this work implements both excess-loop delay (ELD) compensation and an input feedforward path inside the NS-SAR in the charge domain, further reducing the circuit complexity and the OTA power. Overall, this work achieves 81-dB SNDR over 12.5 MHz with 3.7-mW power, leading to a Schreier FoM of 176 dB.

INDEX TERMS Delta–sigma modulator (DSM), extra loop delay compensation, hybrid, noise-shaping SAR (NS-SAR).

I. INTRODUCTION

THE CONTINUOUS-TIME (CT) delta–sigma modulator (DSM) is a popular choice in wide-band analog-to-digital converters (ADCs), especially for wireless transceivers. The loop filter of CT DSM processes the signal before sampling, achieving both noise shaping and anti-alias filtering. The settling requirement is obviated, owing to the CT-domain operation. Therefore, lower dynamic requirements for the loop filter, the inherent anti-aliasing filtering, and an easy-to-drive front-end are the major advantages that CTDSM has over its discrete-time (DT) counterpart.

A low oversampling ratio (OSR) is needed if an energy-efficient CT DSM with high bandwidth and high resolution is desired. A high-order noise transfer function (NTF) is usually applied to achieve the target resolution. However,

several challenges are posed to the high-order CT DSMs due to the nonidealities of practical implementations. First, the CT loop filter is sensitive to the process variation [8]. The loop-filter coefficients primarily depend on the resistors and capacitors whose values vary across PVT variations. Consequently, extra tuning circuitry is needed. Second, conventional high-order loop filters have a large number of OTAs. Multiple cascaded OTAs cause phase shifts, leading to instability. Third, excess-loop delay (ELD) in the CT DSM alters the NTF. The price paid to compensate the ELD is high in high-order designs. Extra circuit complexity and power consumption deteriorate the power efficiency.

In this work, we present a 4th-order hybrid CT-DT DSM that combines a 2nd-order single-amplifier–biquad (SAB)-based CT filter with a 2nd-order passive noise-shaping SAR

(NS-SAR). With the DT noise shaping immune from the PVT variation, the hybrid DSM obtains a better robustness. Compared to the conventional design, the combination of SAB and passive NS-SAR reduces the number of OTAs from many to one. The power is saved because of removing many power-hungry OTAs and the relaxed bandwidth requirement. Moreover, the ELD compensation (ELDC) is embedded into the charge domain. There is minimal extra power and circuitry cost for the ELDC since it is implemented with the small CDAC of the NS-SAR.

This article is an extension of [28] and organized as follows. Section II reviews the prior high-order CTDSM designs and introduces the proposed hybrid 4th-order DSM. Section III discusses the ELDC techniques and introduces the proposed charge-domain ELDC with both feedforward and feedback paths. Section IV describes the design of the prototype ADC and discusses implementation details. Section V presents measurement results. Section VI concludes this article.

II. PROPOSED 4TH-ORDER HYBRID CT-DT DSM

A. PRIOR HIGH-ORDER CT DSMs

There is extensive research on tackling the challenges in high-order CTDSM designs. The NTF sensitivity to the RC time constant variation causes the performance degradation and instability. Leaving the design margin for variation is a feasible solution, which essentially trades noise-shaping (NS) performance for better robustness [15], [17], [18]. An alternative solution is a corner-adaptive tuning circuit or off-chip calibration [1]. The loop-filter implementation is a determinant for the power efficiency. Gm-C and VCO integrators are proposed as a low-power alternative for the power-hungry feedback integrators [5], [6]. However, their linearity is limited. To reduce the total delay of the multiple cascaded OTAs, higher power budget has to be assigned to meet the stringent OTA bandwidth requirement. OTA bandwidth requirements can be relaxed by the ELD over compensation [38], but there are still four OTAs for a 4th-order DSM. One way to improve the power efficiency is to reduce the sheer number of OTAs. SAB has been studied and used in the CT DSM [18], [19], [21]. However, unsatisfactory loop-filter robustness still remains as an issue.

Lowering the CT noise shaping order by adding the DT order can be a strategy to improve both the robustness and power efficiency. A CT front-end is applied to the DSM, followed by switched-capacitor-based filters [23]. The large sampling capacitor is avoided by using a first-order RC integrator. The precise positioning of poles and zeros in the NTF is guaranteed by the following third-order DT filter. However, the DT filter still needs OTA. Thus, the total number of OTAs in the DSM is unchanged. An effective way to incorporate the DT shaping order is to embed an NS quantizer into the DSM loop. Emerging passive NS-SARs are attractive because they are OTA-free, PVT robust, and energy efficient [39], [41]. An RC integrator and a 2nd-order passive NS-SAR are proposed in [22]. Third-order shaping

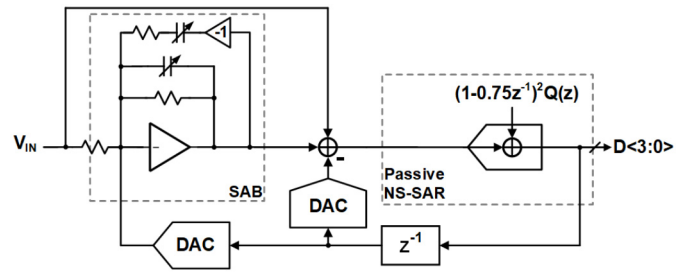


FIGURE 1. Proposed hybrid DSM with SAB filter and passive NS-SAR quantizer.

is achieved by a single OTA. However, the passive NS-SAR input-referred noise cannot be sufficiently suppressed by the 1st-order CT filter. Even worse, the NS-SAR noise is amplified by four times because of the direct feedback ELDC, which will be discussed in Section III. Therefore, the resolution is limited to 70-dB SNDR. The work of Xing et al. [40] adopts a SAB-based filter as front-end and the 1st-order NS-SAR as the backend quantizer. However, the NS-SAR NTF is limited to the first order, and the current domain ELDC is more costly than charge-domain operations. A 1st-order NS-SAR is used with a 1st-order RC integrator in [39]. The high resolution relies on the 12-cycle NS-SAR. Nevertheless, the 12-cycle NS-SAR costs extra delay and area.

B. HYBRID DSM ARCHITECTURE

To address the high-order CT DSM design challenges mentioned above, we propose a 4th-order hybrid CT-DT DSM. Fig. 1 shows the architecture of the proposed hybrid DSM with a 2nd-order CT SAB filter and a passive 2nd-order DT NS-SAR. The NS-SAR NTF coefficients are set by capacitor and transistor device ratios [22]. Therefore, the 2nd-order shaping from the passive NS-SAR is immune from PVT variations, which improves the robustness of the proposed 4th-order DSM. The extra thermal noise from the passive NS-SAR prevents it from achieving a high resolution as a standalone quantizer. In the proposed DSM, the high gain provided by the SAB filter suppresses the noise of the passive NS-SAR. Consequently, the power and area of the NS-SAR can be made very small. In the meantime, the 4th-order shaping is achieved by only one OTA. The power is saved from the elimination of multiple power-hungry OTAs and the bandwidth relaxation. Moreover, the ELDC is implemented in the charge domain with minimal circuitry and power overhead.

C. COEFFICIENT SENSITIVITY

Hybridizing the DT noise shaping and CT noise shaping can mitigate the issue of variation-sensitive poles and zeros in the pure CT DSM. We compare a conventional CT DSM structure and the proposed hybrid structure in Fig. 2. Both DSMs have an NTF with two optimized zeros and same out-of-band gain. Assuming all the CT NS orders are determined by RC products, Fig. 2(a) shows a conventional 4th-order CTDSM. Compared to the conventional design, Fig. 2(b)

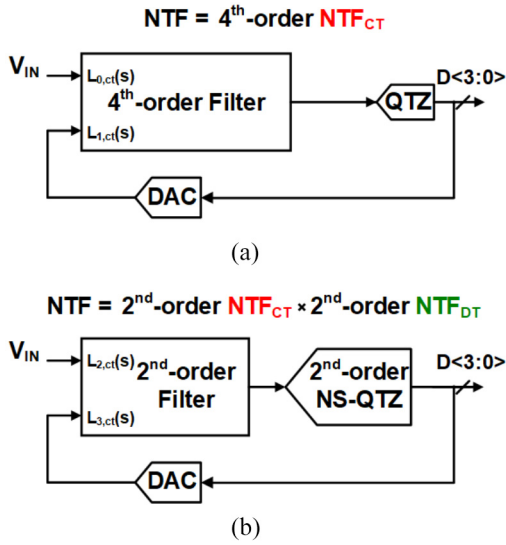


FIGURE 2. (a) Conventional 4th-order CT DSM. (b) Proposed 4th-order hybrid CT-DT DSM.

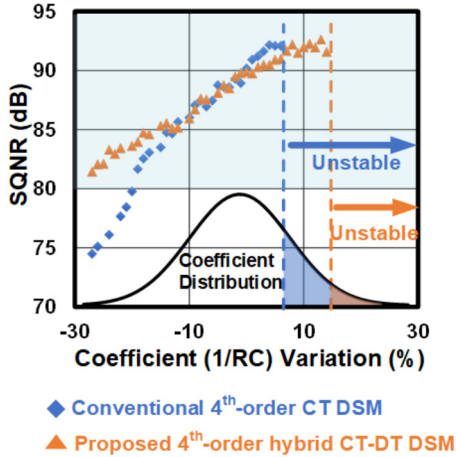


FIGURE 3. Coefficient sensitivity comparison between a conventional and the proposed 4th-order hybrid CT-DT DSM.

shows a structure with a nested NS quantizer. Since the NTF of the NS-quantizer is in the discrete domain, the poles and zeros are immune from PVT variations. The resulting compound NTF of the DSM obtains more robustness. The sensitivity of the conventional and proposed DSM to the RC time constant variation is shown in Fig. 3.

It can be clearly seen that conventional 4th-order CTDSMs are highly sensitive to RC time constant variations. It becomes unstable when the variation in the coefficients ($1/RC$) goes beyond $+8\%$. In the meantime, its SQNR drops significantly as the coefficients decrease. In contrast, the proposed DSM remains stable as long as the coefficient variation is less than $+15\%$, and the slope of the SQNR variation is also milder (e.g., SQNR > 80 dB with -30% coefficient variation). The improved robustness leads to the area and complexity reduction of the tuning circuits.

Fig. 4 shows the simulated SQNRs of the CT-DT DSM versus process corners and the temperature variations, under

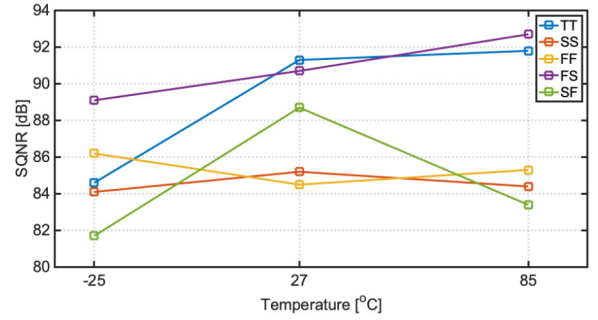


FIGURE 4. Simulated SQNRs of the CT-DT DSM with temperature and process corner variations.

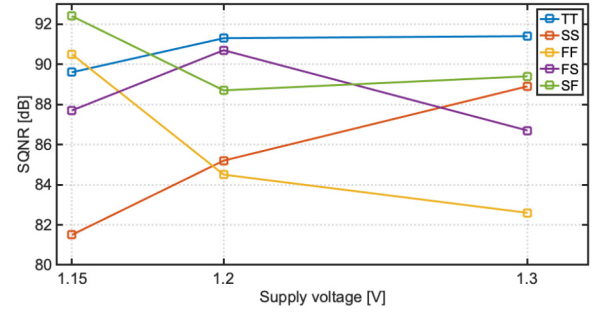


FIGURE 5. Simulated SQNRs of the CT-DT DSM with supply voltage and process corner variations.

the supply voltage of 1.2 V. It shows that the SQNRs are between 82 and 92 dB with the five process corners and the temperature range from -25 °C and 85 °C. Fig. 5 shows the simulated SQNRs of the CT-DT DSM versus process corners and supply voltage variations, under the temperature of 27 °C. It shows that the SQNRs are all above 81 dB across the process corners and the supply voltage range from 1.15 to 1.3 V.

D. FINITE UGB EFFECTS

The finite UGB of the OTA degrades the stability of the feedback loop. To investigate how the proposed DSM performs under different BW_0 , we incorporate the OTA UGB into our DSM modeling. The SAB transfer function is

$$H(s) = \frac{k_1 s + k_2}{s^2 + k_3 s + \omega_p^2} \quad (1)$$

where ω_p , k_1 , k_2 , and k_3 are determined by the RC products. The transfer function has two conjugate complex poles at ω_p .

We model the OTA as a single-pole system with a finite DC gain A_{DC} and a pole frequency ω_0 . Correspondingly, the UGB is $A_{DC}\omega_0$. In order to achieve an ideal SAB filter response, k_3 is set to zero by choosing proper RC values. Therefore, the SAB transfer function with the finite OTA UGB becomes

$$H'(s) = \frac{k_1 s + k_2}{s^2 + \omega_p^2 + \left(\frac{s}{UGB} + \frac{1}{A_{DC}}\right)(s^2 + k_1 s + k_2 + \omega_p^2)} \quad (2)$$

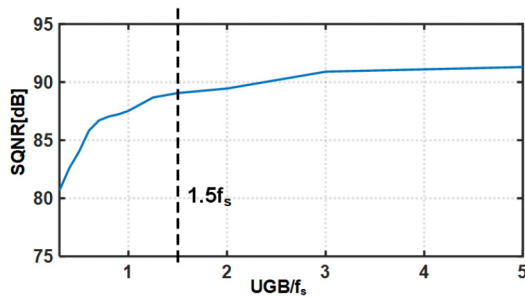


FIGURE 6. Proposed hybrid CT-DT DSM SQNR with different OTA UGBs.

Fig. 6 shows the SQNR over different UGB of the single OTA. From $0.5f_s$ to $1.5f_s$, the SQNR improvement is around 10 dB while there is only 2–3-dB improvement from $1.5f_s$ to $5f_s$. Thus, $1.5f_s$ is chosen as our OTA bandwidth. In contrast, a recent 4th-order CTDSM design with multiple OTAs requires 3–4 f_s OTA bandwidth to make the loop stable [16]. The relaxation of the OTA bandwidth and the decreased number of OTAs result in significantly reduced power.

III. PROPOSED ELD COMPENSATION SCHEME

A. BRIEF REVIEW OF ELD COMPENSATION

ELD is a key problem in the CT DSM design. Such delay is bound to degrade modulator stability and change NTF. ELDC techniques can be used to restore the loop stability and the desired NTF. However, the price for ELDC is high in high-order and high-speed CT DSM designs. The high cost consists of two parts. First, it adds the extra circuitry into the DSM. In the conventional designs, a direct feedback path around the quantizer dictates an extra DAC [1]. Second, the tuning of the filter coefficients is needed. To compensate for the delay, we have to increase the coefficients of lower-order paths in the loop filter. The required filter UGB is then increased. The OTA bandwidths have to be increased proportionally to maintain the desired filter response. Therefore, the ELDC incurs a significant increase in both circuitry complexity and power consumption. Prior works have dedicated significant efforts to address the high cost of ELDC. The direct feedback path can be embedded into the flash quantizer [38]. However, the feedback path complicates the flash quantizer design. If the quantizer is SAR, the feedback path implementation can be simplified because of the inherent CDAC [20], [22], [25], [37]. However, the direct feedback path around the quantizer increases the loop-filter swing. The larger swing degrades the OTA linearity or even exceeds the power supply range. A dynamic range (DR) scaling has to be performed by changing the loop-filter and quantizer gain. With a reduced filter gain, the noise is amplified. A residual ELDC can avoid the large filter output swing by not feeding the signal component to the filter output [15], [16]. However, they are implemented in the current domain. The ELDC is affected by the finite UGB of the OTA. Alternatively, the compensation can also be implemented in

the phase domain in a VCO-based design [36]. Nevertheless, it consumes almost a 1.5-fold power of the whole loop filter.

B. PROPOSED CHARGE-DOMAIN ELD COMPENSATION

We propose an efficient charge-domain ELDC shown in Fig. 7. The high efficiency stems from two reasons. First, the compensation is implemented by the small CDAC of NS-SAR. The passive capacitor-based ELDC adds no extra burden on the OTA. In the meantime, the additional circuitry on the CDAC is minimal. An extra feedback DAC is not needed. Second, it implements the residual ELDC by combining a feedforward and a feedback path. Therefore, no DR scaling is needed. The noise performance degradation is avoided. Fig. 7(a) shows the signal diagram of the ELDC. Fig. 7(b) shows the detailed charge domain operations and Fig. 7(c) shows the timing diagram. The feedback path and feedforward path are implemented by a sub-DAC, C_{ELDC} . The feedback path output is fed into the bottom plate of C_{ELDC} . The feedforward path output is sampled onto the top plate of C_{ELDC} . Note the feedforward signal is also sampled onto the C_{SAR} . This helps to reduce the SAB output swing further, leading to the linearity enhancement. The timing of the ELDC is as follows. During the sampling phase, the bottom plates of C_{ELDC} and C_{SAR} are connected to $D[n-1]$ and the inverse of the SAB output $-V_L$, respectively. Their top plates are both connected to the DSM input, V_{IN} . At the sampling frequency of 500 MHz, all sampling operations need to finish within 200 ps under 40-nm LP technology. Fortunately, they do not need to be absolutely accurate, as any sampling error is 2nd-order shaped by the front-end SAB. As the SAR conversion phase begins, their top plates are disconnected from V_{IN} . Shortly after that, the bottom plates of C_{ELDC} and C_{SAR} are reset to V_{cm} . Consequently, both feedback and feedforward functions are implemented. Then, the SAR conversion is performed on C_{SAR} . After the conversion, NS-SAR continues to perform passive integration, which is detailed in Fig. 11.

It is worth noting that lowering the number of CT NS order can significantly save the power of ELDC. Compared with a 4th-order loop filter, a 2nd-order filter is easier to stabilize. To compensate for the same ELD, the UGB increase of the conventional 4th-order filter is significantly larger than that of the 2nd-order SAB filter, as shown in Fig. 8. Assuming the loop filters are active RC filters, the filter transfer functions with higher UGBs need OTAs with higher bandwidths, leading to more power consumption. Note the frequency response plots in Fig. 8 are normalized to f_s . It is more challenging to push UGB even further at a higher f_s . Consequently, DSMs of a higher f_s benefit more from lower-order CT shaping because of the reduced ELD cost.

C. FEEDFORWARD PATH AND STF

In the high-order CTDSM with multiple OTAs, the full output swing is handled by the last integrator. The resulting

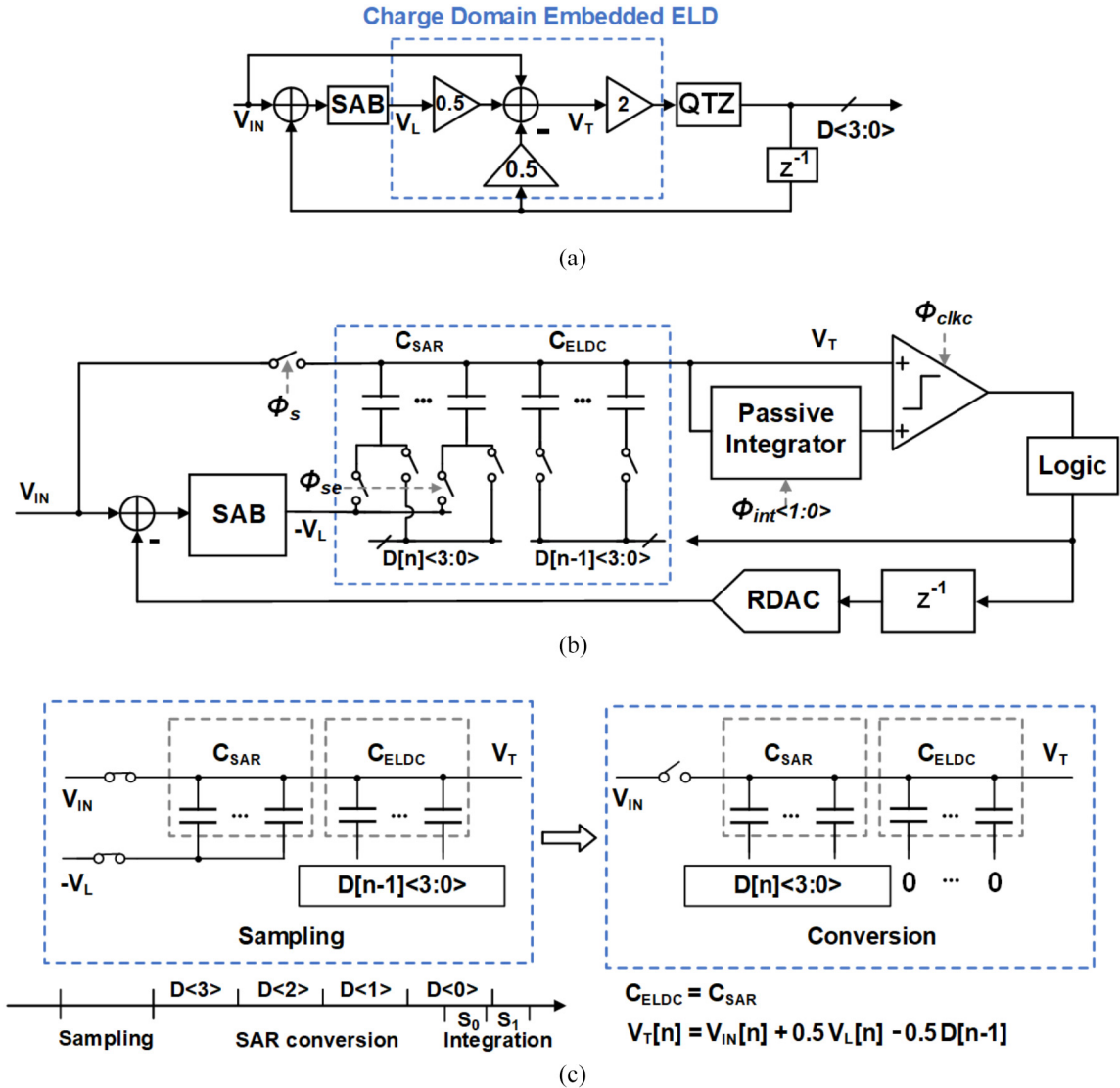


FIGURE 7. (a) Signal flow and schematic of proposed charge domain embedded ELDC. (b) Detailed structure of ELDC. (c) Timing diagram of ELDC operations on CDAC.

distortion due to the large output swing is suppressed by the prior stage gain. However, SAB has an inferior linearity because the single OTA has to handle the full swing and provides less loop gain to suppress the distortion. The non-linearity becomes an issue when the target resolution is high (SNDR >80 dB). In this work, the feedforward path with a gain of k_{ELD} and direct feedback DAC form a residual ELDC in Fig. 9(a). We rearrange the signal diagram, as shown in Fig. 9(b), to better analyze the STF. Besides the feedforward signal for ELDC purpose, the extra signal is fedforward to enhance the filter linearity. The feedforward component with a gain of k_{FF} and the residual ELDC component with a gain of k_{ELDC} will modify the STF of the CT DSM. Since STF of the NS-SAR is unity, we only need to study the STF of second-order CT outer loop. We can further rearrange the signal flow model to separate the CT and DT transfer functions [1]. Fig. 9(c) shows the final signal diagram to derive the STF.

After the rearrangement, it can be easily shown that the STF is

$$STF(s) = (LF_1(s) + k_{FF}) \cdot NTF_2(e^{sT_s}) \quad (3)$$

where $LF_1(s)$ is the loop-filter transfer function with ELDC and NTF_2 is the corresponding 2nd-order NTF created by the outer CT loop. STF(s) from this mathematical modeling and circuit simulation results are shown in Fig. 10. The simulation results match well with the modeling, including the peaking and notch of our STF. $LF_1(s)$ is low-pass. Since NTF_2 creates notches at multiples of sampling frequency, STF(s) maintains the anti-aliasing feature. The cost is a peaking of 10 dB due to the direct feedforward path.

IV. CIRCUIT IMPLEMENTATIONS

A. SYSTEM ARCHITECTURE

Fig. 11 shows the schematic of the entire DSM. The 2nd-order CT front-end is implemented by an SAB. To realize

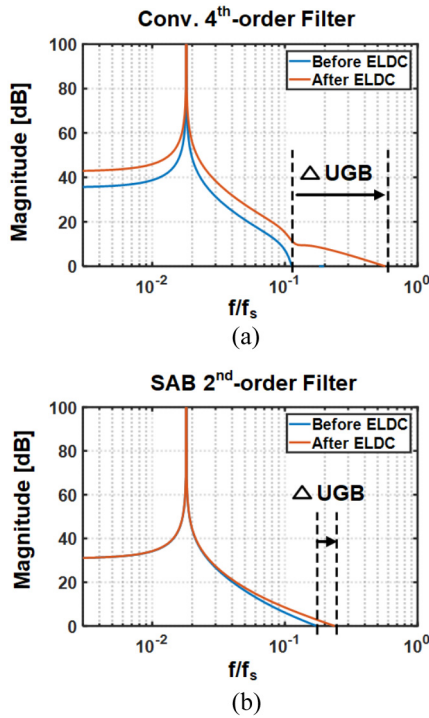


FIGURE 8. (a) UGB increase of the conventional 4th-order filter after ELDC. (b) UGB increase of the SAB 2nd-order filter after ELDC.

the desired biquad response, the OTA outputs are cross-coupled to its inputs via R_1 and C_1 . Negative feedback paths are formed by R_2 and C_2 . C_1 and C_2 are made by adjustable capacitor banks to further enhance the DSM stability against process variations. The passive NS-SAR achieves a 2nd-order NTF by capacitor merging and the multi-input comparator ratio. The OTA output and one-cycle delayed quantizer output are sampled onto the CDAC bottom plates. ADC input is sampled onto the CDAC top plates. kT/C noise and capacitor mismatch errors in the NS-SAR CDAC are significantly attenuated by the 2nd-order shaping provided by the SAB. Thus, capacitors in the CDAC can be made very small. The differential CDAC is used for both sampling and conversion. Each half is only 30 fF. The small CDAC facilitates the high-speed operations in the NS-SAR, including signal sampling, SAR conversion, and capacitor-merging-based residue integration. The power that CDAC draws from the reference is only 0.04 mW, which is 1% of the total ADC power.

B. SAB DESIGN

The coefficients of (1) are determined by several RC products. The detailed equations can be found in the Appendix. The formula of C_1 is derived from the condition $k_3 = 0$. Arbitrary combinations of a second-order and a first-order path can be achieved. However, there is a lack of a zero-order path in the SAB filter transfer function. The zero-order path has to be implemented by other circuitry in the CT DSM. The input resistor R_{IN} is 1 k Ω , R_1 is 2.7 k Ω , and

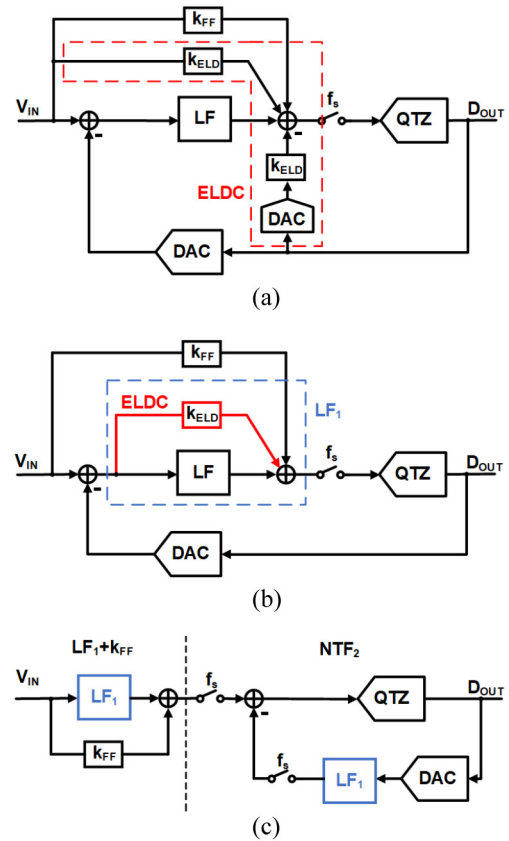


FIGURE 9. (a) Original CT DSM model. (b) Equivalent residual ELDC model. (c) Rearranged model to separate CT and DT domain.

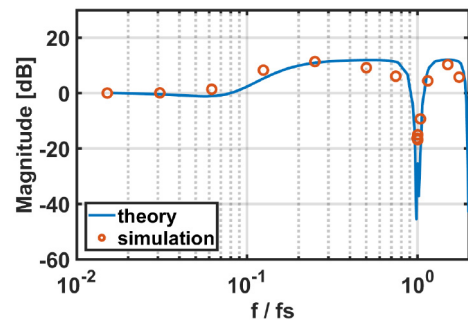


FIGURE 10. STF curve of mathematical modeling and circuit simulation results.

R_2 is 49 k Ω . The capacitors C_1 is 1.55 pF and C_2 is 1.48 pF.

The single OTA is a key circuit block in our DSM design. Thanks to the system design of the proposed DSM, the tight BW requirement is significantly relaxed to only $1.5f_s$. Therefore, a simple two-stage feedforward compensated OTA is adopted in the SAB filter. Fig. 12 shows the OTA schematic. The cascade of M_{1-4} and M_8 provides a slow but high dc gain path. M_7 creates a fast feedforward path between the input and the output to stabilize the OTA. The input common-mode voltage of second stage is determined by the output common-mode voltage of the first stage. Therefore, the current

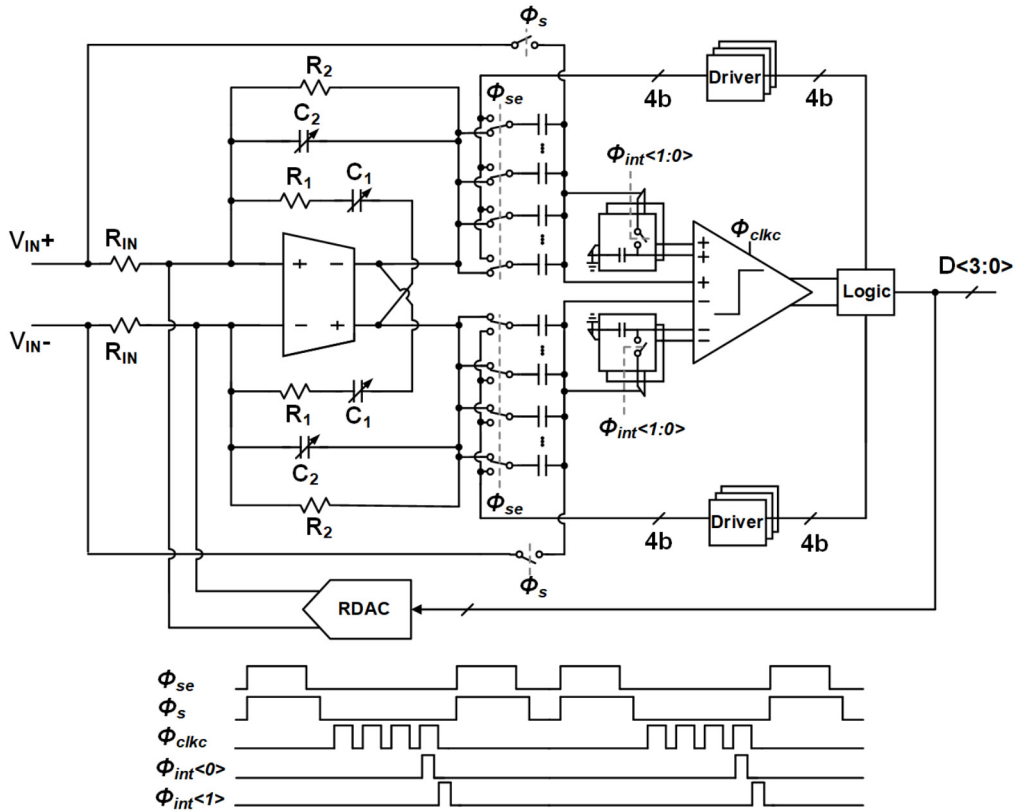


FIGURE 11. Schematic and timing diagram of proposed hybrid DSM.

of the second stage tracks that of the first stage under PVT variations. The constant current ratio leads to a constant g_m ratio between the first and second stage, hence a high stability. The first stage adopts the current reuse technique in [35], which nearly doubles the g_m/I_d . The first stage CMFB loop is implemented by an output resistor divider. The second stage CMFB includes an extra error amplifier. Overall, this OTA consumes 2 mW under the 1.2-V power supply, which takes 54% of the total power.

C. 2ND-ORDER NS-SAR DESIGN

The passive NS-SAR is an emerging quantizer architecture. It can achieve a high resolution by the noise shaping capability while inheriting the high power efficiency from the SAR architecture. They leverage the charge sharing between capacitors to implement the integration. The passive NS-SAR variants have different ways to implement the gain block. Two methods are capacitor stacking [30], [31] and multi-input comparator [22], [41]. Capacitor-stacking helps to reduce the comparator noise [30], [31]. However, those NS-SARs have only 1st-order noise shaping. Therefore, we choose multi-input comparator-based NS-SARs, which achieves 2nd-order noise shaping and avoids adding circuit complexity.

Fig. 11 shows the architecture of NS-SAR. In our design, 4-bit conversion is finished during ϕ_{clk} , followed by two

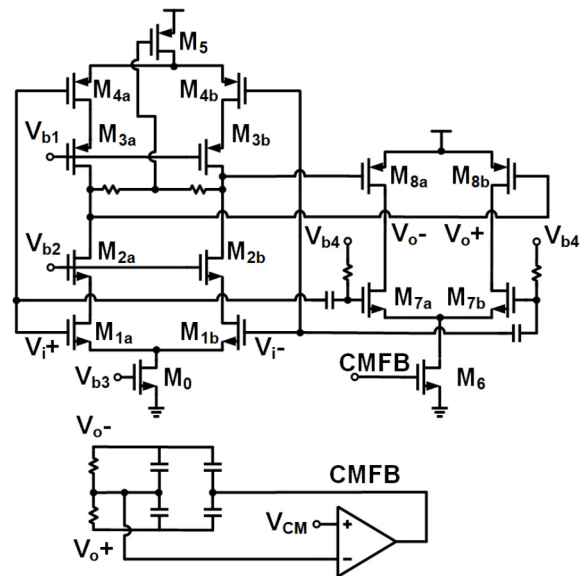
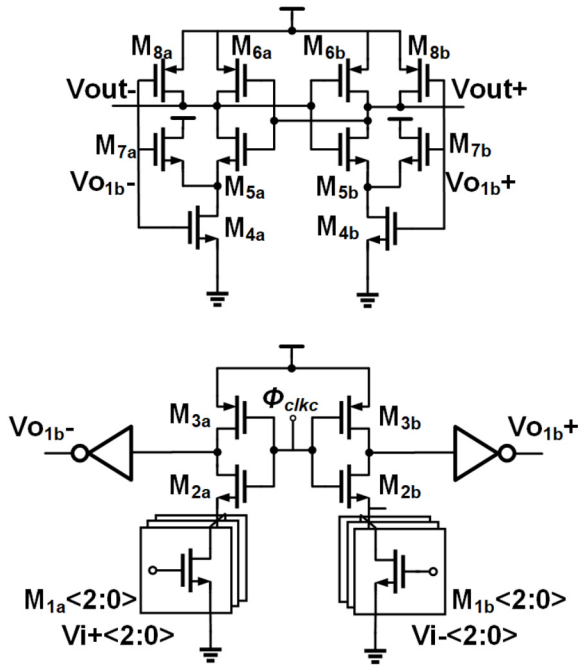
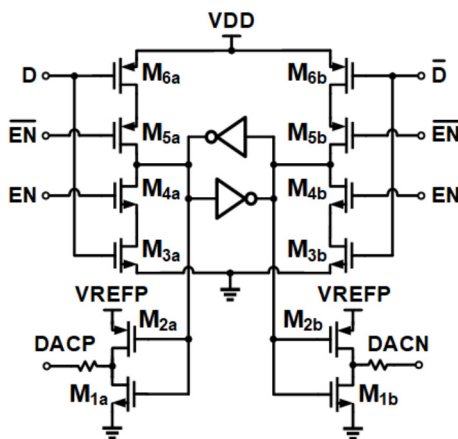


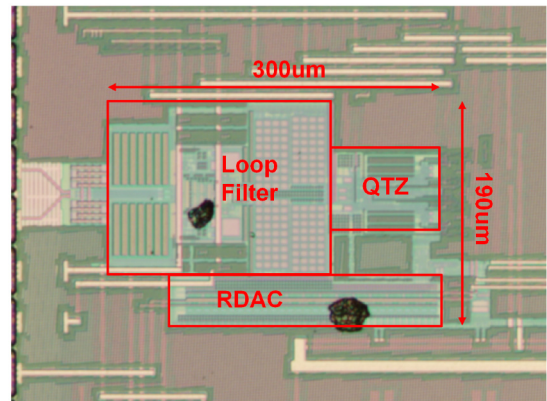
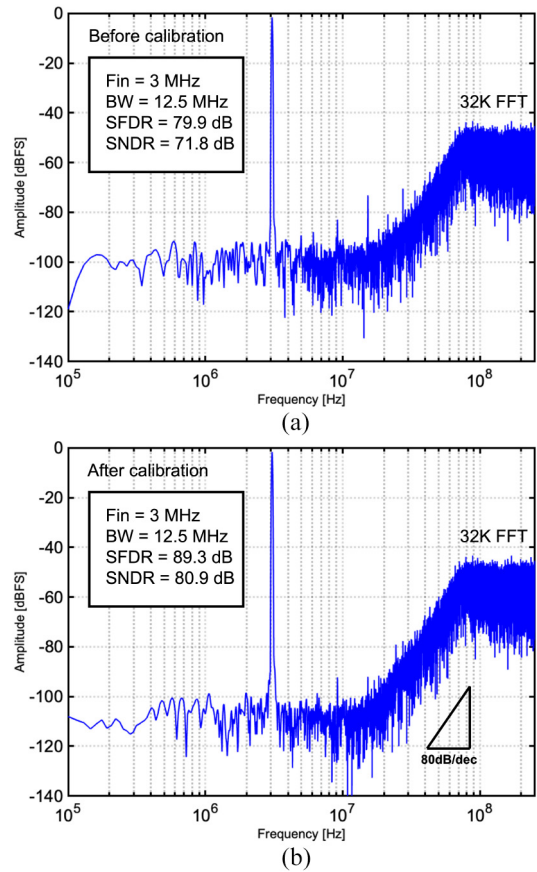
FIGURE 12. Two-stage feedforward-compensated OTA design.

integration phases $\phi_{int(0)}$ and $\phi_{int(1)}$. The 1st integration phase $\phi_{int(0)}$ is merged with the SAR LSB conversion. Therefore, only the 2nd integration phase $\phi_{int(1)}$ takes the extra time [22]. Overall, the timing budget of this 4-b NS-SAR is equivalent to that of the standard 5-b SAR, but


FIGURE 13. Comparator design.

FIGURE 14. Schematic of the RDAC unit cell.

can provide an effective 8-b resolution at the OSR of 20 thanks to its 2nd-order noise shaping.

The robust passive gains are crucial to the NS-SAR NTF, which are determined by relative gain ratios of the comparator input transistor [22]. The ratios depend on the transistor dimensions to the first order. Still, they are affected by the common-mode input voltage V_{cm} variations in the bi-directional DAC switching [22]. To minimize the V_{cm} variation during the SAR conversion, V_{cm} switching of [9] is used in our NS-SAR. The comparator schematic is shown in Fig. 13. The width ratios of the three input pairs are set to 1:3:12. Input pairs sense the differential inputs and determine the relative gains. The two inverters connecting to VO_{1b-} and VO_{1b+} act as dynamic amplifiers and provide extra gain. Since the inverter outputs VO_{1b-} and


FIGURE 15. Die micrograph.

FIGURE 16. Measured single-tone spectrum (a) before and (b) after calibration.

VO_{1b+} are both clock and input signals to the latch, the next stage can only be triggered by the previous stage outputs. The sequential operations guarantee a consistent preamplification gain; hence, a robust noise performance against variations.

D. RDAC

Compared to the current source DAC, RDAC is chosen because of better noise and linearity performance. Fig. 14

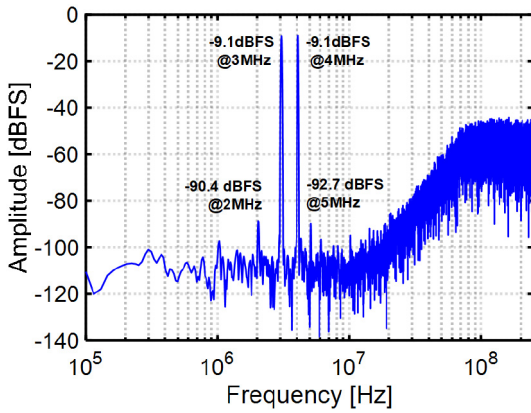


FIGURE 17. Measured two-tone spectrum.

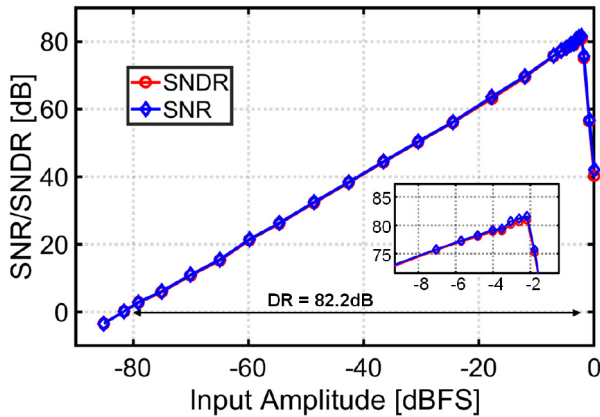


FIGURE 18. Measured SNDR/SNR versus different input amplitudes.

shows the schematic of a unit cell of the 4-bit feedback DAC. D is the digital input and DACP(N) are analog outputs. The retiming latch consists of a pair of cross-coupled inverters and access transistors. For simplicity, DEM is not used. The off-chip foreground digital calibration is applied to this prototype ADC to address nonlinearities. Static error and intersymbol interference (ISI) are calibrated together. To correct ISI errors, we need four extra tuning coefficients [2]. During the calibration, the sinusoidal test signal has to excite all the bits. The least-square regression is used to find the optimal element weights which yield the lowest distortion [3], [26]. We freeze the optimal set of weights and apply it to subsequent measurements.

V. MEASUREMENT RESULTS

A prototype of the proposed 4th-order hybrid CT-DT DSM is fabricated in a 40-nm LP CMOS process. Fig. 15 shows the die photograph. The active area is 0.057 mm^2 . The SAB filter occupies the largest area of 0.035 mm^2 . The quantizer is 0.0078 mm^2 and RDAC is 0.0065 mm^2 .

Fig. 16 shows the measured output spectrum with a 3-MHz input signal, showing 4th-order shaping. With the bandwidth of 12.5 MHz, this DSM achieves SNDR, SNR,

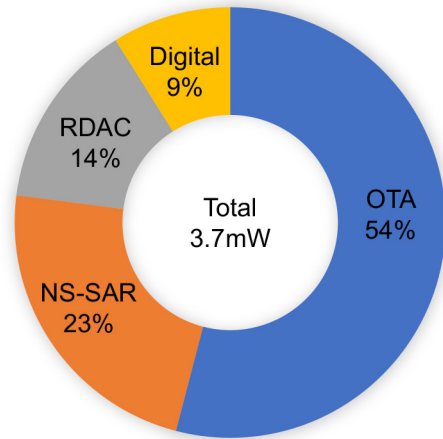


FIGURE 19. Proposed DSM power breakdown.

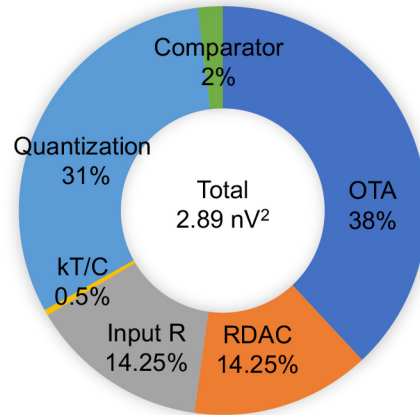


FIGURE 20. Proposed DSM noise breakdown.

and SFDR of 80.9, 81.7, and 89.3 dB, respectively. The RDAC mismatch is addressed by an off-chip calibration. The two-tone test in Fig. 17 shows the IMD3 of -81.3 dB . Fig. 18 shows the measured SNDR and SNR versus the input amplitude. The DR is 82.2 dB.

The prototype CT-DT DSM consumes 3.7 mW of power with a 1.2-V supply. The sampling frequency is 500 MHz. The OTA consumes the largest portion of total power, which is 2 mW. NS-SAR consumes 0.85-mW power. RDAC consumes 0.52 mW. The digital circuit power is 0.33 mW. The measured power breakdown is shown in Fig. 19. The calculated in-band input-referred noise breakdown is shown in Fig. 20. The total in-band noise is 2.89 nV^2 . The input resistor and the RDAC contribute in total 25% of noise. The noise contributions of OTA, quantization error, kT/C , and comparator take up 38%, 31%, 0.5%, and 2%, respectively. Table 1 summarizes the measurement results and compares them with the state-of-the-art single-loop CTDSMs. There are also other multiloop designs that achieve competitive FoMs [43], but we focus on single-loop design tradeoffs here. Compared to the prior works, our work achieves the highest SNDR of 80.9 dB. This work is the only 4th-order

TABLE 1. Comparison with the state-of-the-art single-loop CT DSMs.

	ISSCC-13 Shu [38]	ISSCC-17 Kim [42]	ISSCC-19 Lo [39]	VLSI-18 Liu [22]	VLSI-19 Weng [27]	VLSI-20 Xing [40]	JSSC-21 Baluni [24]	This work
Order	4	4	2	3	3	3	4	4
# OTA	4	2	1	1	3	1	4	1
Quantizer	Flash	DNSQ	1st-order NS-SAR	2nd-order NS-SAR	1st-order NS-SAR	1st-order NS-SAR	1-bit Quantizer	2nd-order NS-SAR
Process [nm]	28	130	7	40	12	28	65	40
F _s [MHz]	640	640	400	500	832	1500	2560	500
BW [MHz]	18	15	25	12.5	30	50	20	12.5
Area [mm ²]	0.08	0.17	0.056	0.029	0.058	0.024	0.37	0.057
Power [mW]	3.9	11.4	3.8	1.16	3.2	10.4	11.3	3.7
DR [dB]	78.1	82.9	79.4	73	74.5	80.6	85	82.2
SNDR [dB]	73.6	80.4	74	70.4	71.4	74.4	82.1	80.9
FoMs* [dB]	170.2	171.6	172.2	170.7	171	171.2	174.1	176.1

* FoMs = SNDR + 10log₁₀(BW/Power).

DSM with a single OTA. Owing to the reduced number of OTAs and charge domain ELDC, our high-order DSM also achieves the best Schreier FoM of 176.1 dB. Overall, this article presents a compact, high-resolution, and energy-efficient DSM.

VI. CONCLUSION

This article presented a 4th-order hybrid DSM with a CT SAB-based 2nd-order loop filter and a passive 2nd-order passive NS-SAR. It combines the merits of a CTDSM (anti-aliasing filtering and relaxed OTA settling) and DTDSM (PVT robustness and accurate NTF). The robustness against PVT variations was improved. The multiple cascaded OTAs are reduced to a single OTA to achieve 4th-order shaping. Moreover, the ELDC and the input feedforward path were implemented in the charge domain. Therefore, the power efficiency and area consumption were improved. The proposed CT-DT DSM was well suited for applications demanding low power, low design complexity, and high robustness.

APPENDIX

In our work, the coefficients in (1) are

$$\begin{cases} k_1 = \frac{1}{R_{IN}C_2} \\ k_2 = \frac{1}{R_{IN}R_1C_1C_2} \\ k_3 = \frac{1}{R_1C_1} + \frac{1}{R_2C_2} - \frac{1}{R_1C_2} \\ \omega_p^2 = \frac{1}{R_1R_2C_1C_2} \end{cases} \quad (4)$$

Assuming R_{IN} is bounded by thermal noise constraints, the resulting component values are

$$\begin{cases} R_2 = \frac{k_2}{\omega_p} R_{IN} \\ R_1 = \frac{R_2}{1 + \left(\frac{k_2}{k_1}\right)^2 \frac{1}{\omega_0^2}} \\ C_1 = \frac{k_1}{k_2 R_1} \\ C_2 = \frac{\left(\frac{k_2}{k_1}\right)^2}{\left(\frac{k_2}{k_1}\right)^2 + \omega_p^2} C_1 \end{cases} \quad (5)$$

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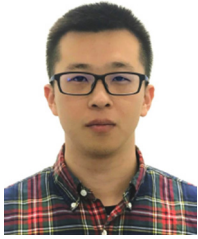


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