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An Overview of Noise-Shaping SAR ADC: From Fundamentals to the Frontier

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ABSTRACT The Noise-Shaping (NS) SAR is an attractive new ADC architecture that emerged in the last decade. It combines the advantages of the SAR and the DSM architectures. NS SAR shows excellent potential for high efficiency and low cost, and is highly suited to process scaling. This paper gives an overview of the history of NS-SAR, reviews the fundamentals challenges, and summarizes the latest developments, including advanced loop filtering techniques, DAC mismatch mitigation, kT/C mitigation, and bandwidth boosting. A comprehensive comparison of the state-of-the-art NS-SAR ADCs is provided, and conclusions are derived.

INDEX TERMS ADC, DSM, oversampling, Noise-shaping, successive approximation, SAR.

I. INTRODUCTION

ANALOG to Digital Converters (ADCs) are essential in modern electronic systems. However, because ADCs are often performance bottlenecks in the signal chain, ADC requirements continue to increase, pushing the boundaries of what we once thought was impossible. For example, current mobile devices require ADCs with over 100MHz bandwidth (BW) and 70dB dynamic range (DR) while consuming only a few milliwatts. In addition, IoT sensor nodes must be very low-cost and low-power, with ADCs providing over 100dB Signal-to-Noise Ratio (SNR) without any complicated calibration. Conventional architectures, such as Flash, Successive Approximation Register (SAR), Pipeline, and Delta-Sigma Modulation (DSM), are challenged by these specifications due to inherent tradeoffs. These challenges have encouraged research in hybrid architectures that have led to performance breakthroughs.

The Noise-Shaping SAR (NS-SAR) is one of the most promising hybrid architectures to have emerged during this decade. NS-SAR combines the SAR and the DSM architectures and benefits from the advantages of both: NS SAR is power efficient and low cost like SAR, and at the same time, it provides a high SNR comparable to conventional DSM ADCs. NS-SAR is also very amenable to process scaling, which makes it very promising for long-term development. Fig. 1 compares NS-SAR and conventional architectures in terms of power and area [1]. The efficiency and cost advantages of NS-SAR over DT-DSM are clear.

The rest of this paper is arranged into five sections. Section II briefly reviews the history of NS-SAR and some milestone innovations. Section III gives a system-level perspective of NS-SAR, discussing its fundamental framework and advantages. Section IV goes through the main challenges in NS-SAR and reviews the solutions. Section V reviews and discusses the stage-of-the-art NS-SAR designs. And finally,

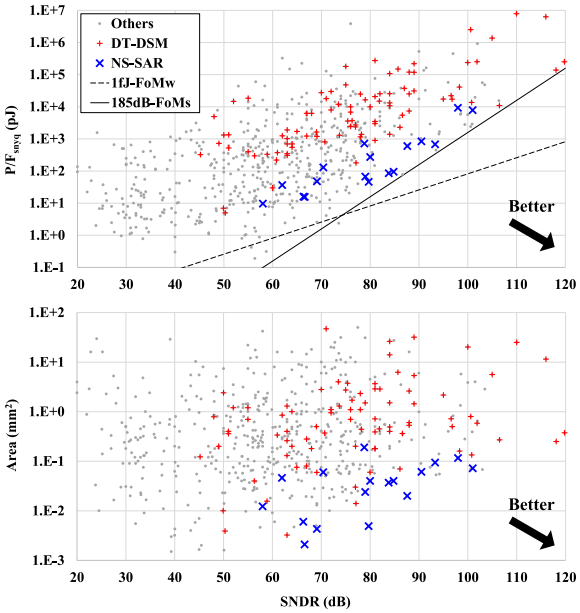

FIGURE 1. Comparison between NS-SAR and conventional architectures.

Section VI presents conclusions and offers some predictions for the future of NS-SAR.

II. A BRIEF HISTORY

Although both the SAR and the Delta-Sigma ADCs architectures can be traced back to the 1950s [2], there were no apparent attempts to combine these two architectures before the twenty-first century. This may be because SAR ADCs are conventionally considered as "slow" converters, while Delta-Sigma ADCs need a fast quantizer (traditionally a Flash ADC) to accomplish over-sampling. However, the development of CMOS technology significantly improved the speed of SAR ADCs, making the combination feasible. **In the early 2000s**, [3] proposed using a SAR ADC in a DSM to overcome the difficulty of implementing a multi-bit quantizer with a low supply voltage. At this stage, the SAR architecture was considered an alternative to Flash, which did not make full use of the properties of the SAR ADC. Later **in 2010**, a simulation work [4] presented the idea of a SAR-DSM by exploiting the residue in a SAR ADC, which is indeed a key concept in modern NS-SARs ([5]–[40]).

Eventually, **in 2012**, Fredenburg and Flynn proposed the first modern NS-SAR and also coined the term "Noise-Shaping SAR" for the first time [5]. This first practical NS-SAR is a *Cascaded Integrator Feed-Forward* (CIFF) structure and needs a slightly complicated loop filter. Reference [5] considers the efficiency of the loop filter as essential in NS-SAR, and thus uses a single-stage, low-gain opamp to efficiently implement the loop filter.

Recognizing that the loop filter is the key to energy efficiency, **in 2015**, [7] proposed a passive loop filter to further improve the efficiency of NS-SAR. The idea was soon followed and improved [9], [15]. From 2016, the number of publications on NS-SAR grows steeply. Some milestone works include:

In 2016, [8] introduced the *Passive Gain* technique to NS-SAR, providing a high-efficiency amplification solution for later works, including [29]. Reference [10] introduced the *Mismatch-Error-Shaping* method to NS-SAR, addressing the SAR DAC mismatch challenge in NS-SAR. Reference [12] implemented a 1st-order *Error-Feedback* (EF) NS-SAR similar to the EF idea in [4]. Reference [41] embedded an NS-SAR into a Discrete-Time DSM.

In 2017, *Dynamic Amplifiers* were introduced to NS-SAR [13], [14]. Reference [13] also adopted the sub-ranging and prediction techniques. Reference [15] introduce the voting technique to NS-SAR. The first FinFET NS-SAR [16] was reported.

In 2018, [18] demonstrated a 2nd-order EF-NS-SAR with complex zeros and introduced *Charge-Sharing Summation*, which later became a common approach for EF-NS-SAR design. Reference [42] merged NS-SAR and CT-DSM, forming a now popular structure for CT-DSM. Reference [43] explored embedding NS-SAR into a pipelined architecture for bandwidth expansion, paving the way for other later improvements.

In 2019, [22] realized feedback summation through *Capacitor-Stacking*. This low-cost but high-precision summing scheme is the foundation of many later structures [27]–[29], [36], [37]. Reference [23] pioneered the *Time-Interleaved-NS-SAR* with an EF-based architecture for higher bandwidth. CIFF-based time-interleaving later followed [30], [38]. *Buffer Embedding* was also transplanted to NS-SAR at this time [24].

In 2020, [27] proposed a *Cascaded-NS-SAR* framework for robust high-order noise-shaping, and was later improved by [37]. Reference [28] introduced a *Dynamic Closed-Loop Amplifier*, for nearly optimum loop-filter performance.

In 2021, [36] applied kT/C noise-cancellation to reduce the sampling capacitance in NS-SAR. Reference [39] combined N-path filter and NS-SAR. More novel NS-SAR designs can be expected in the near future.

III. SYSTEM VIEW

A. BASIC FRAMEWORK

In a SAR ADC, a comparator and a feedback DAC sample and quantize the input signal, as shown in black in Fig. 2(a). Logic circuitry, usually a Successive Approximation Register (SAR), uses the comparator output to successively decide the bits of D_{OUT} and converge the DAC output (V_{DAC}) and the sampled input signal (V_{IN}). Since the resolution of D_{OUT} (i.e., V_{DAC}) is limited, at the end of the conversion, there remains a small difference between V_{IN} and V_{DAC}, which is called the *residue* or *quantization error* (V_{RES}). Thus, the conversion residue in SAR ADC presents naturally, and the essence of the NS-SAR architecture is to exploit this residue.

NS-SAR essentially builds on the SAR ADC framework (Fig. 2(a)). Thus, despite various implementations, from a system view, an NS-SAR consists of three parts:

1) A SAR ADC that performs quantization and extracts the residue. In most designs, this is a CDAC-based SAR

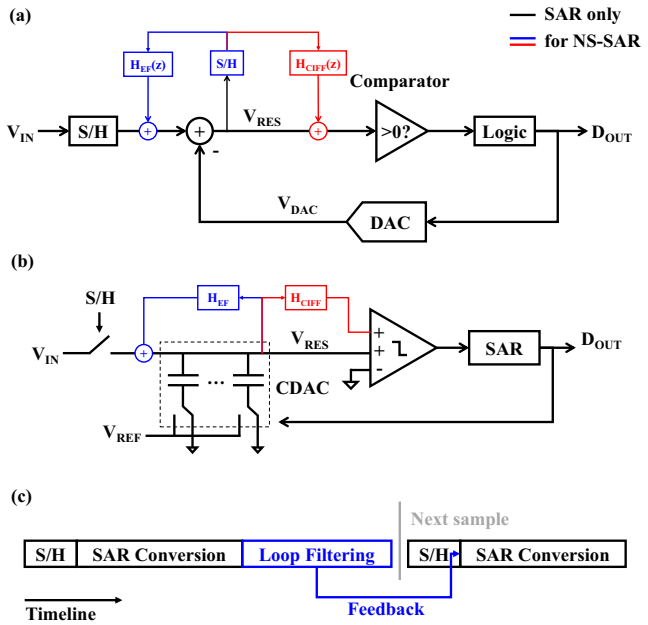

FIGURE 2. a) The basic framework of SAR and NS-SAR, b) a common implementation of NS-SAR and c) its operation timing.

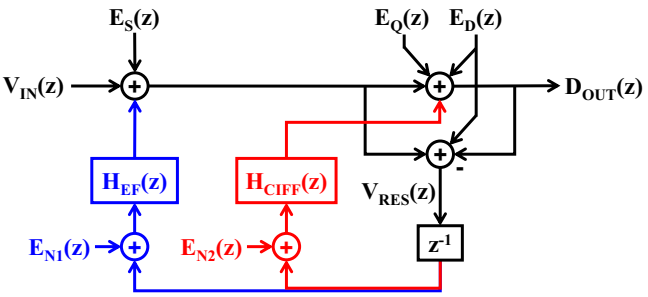

FIGURE 3. A generalized model of NS-SAR.

ADC, where the residue presents on the CDAC as a voltage (V_{RES}) at the end of conversion (Fig. 2(b)).

2) Loop filters (H_{EF} and or H_{CIFF}) that sample and process the residue after the SAR conversion. These loop filters should be highly efficient and scaling-friendly. H_{EF} and H_{CIFF} are for different NS-SAR configurations and are explained in the next section.

3) A signal summation mechanism that feeds the filtered residue back to the SAR ADC. Similarly, these summers should also be efficient and low-cost. In one approach, charge-sharing implements the summer to the CDAC (i.e., after H_{EF}) [18]. In another approach, a multi-input comparator implements the summer [5]. Sometimes the filter in 2) and the summer in 3) can also be implemented together for simplicity (e.g., [6], [22]).

B. SYSTEM MODEL

Fig. 3. shows a generalized signal model corresponding to the NS-SAR framework in Fig. 2. Here, E_S models the errors and noise during sampling, such as kT/C noise. E_Q represents the quantization error but also includes comparator noise and DAC settling error during SAR conversion. E_D models DAC errors from nonlinearity and mismatch.

H_{EF} and H_{CIFF} are the loop filters for different NS-SAR configurations. Specifically, the feedback path, containing loop filter H_{EF}, forms the *Error-Feedback* (EF) structure [4]. In contrast, the other path with loop filter, H_{CIFF}, forms the *Cascaded-Integrator Feed-Forward* (CIFF) structure as in [5]. E_{N1} and E_{N2} represent the input-referred noise of these filters. The delay (z^{-1}) models the minimal delay from the loop filters (the S/H block before the loop filters in Fig. 2(a) also models this delay).

To understand the CIFF path in this model, we notice that the CIFF feedback signal (V_{RES} H_{CIFF} z^{-1}) is summed by the comparator and not summed to the CDAC (Fig. 2(b)). Intuitively, this feedback signal is like an offset to the comparator, and offset is treated as quantization error (E_Q) in the SAR signal model. Thus, in the model, the CIFF feedback should connect to the same summer as E_Q.

The model in Fig. 3 leads to an all-pass Signal Transfer Function (STF) that processes the input signal. The following Noise Transfer Functions (NTFs) process the errors E_S, E_Q, E_D, and $E_{N1,2}$:

$$STF(z) = \frac{D_{OUT}(z)}{V_{IN}(z)} = 1 \tag{1}$$

$$NTF_S(z) = \frac{D_{OUT}(z)}{E_S(z)} = 1 \tag{2}$$

$$NTF_D(z) = \frac{D_{OUT}(z)}{E_D(z)} = 1 \tag{3}$$

$$NTF_Q(z) = \frac{D_{OUT}(z)}{E_Q(z)} = \frac{1 - H_{EF}(z)z^{-1}}{1 + H_{CIFF}(z)z^{-1}} \tag{4}$$

$$NTF_{N1}(z) = \frac{D_{OUT}(z)}{E_{N1}(z)} = H_{EF}(z) \tag{5}$$

$$NTF_{N2} = \frac{D_{OUT}(z)}{E_{N2}(z)} = \frac{H_{CIFF}(z)}{1 + H_{CIFF}(z)z^{-1}}\left(1 - H_{EF}(z)z^{-1}\right) \tag{6}$$

According to (2) and (3), E_D and E_S are not suppressed (i.e., "shaped") in NS-SAR. At the same time, since we aim to suppress the quantization error (E_Q), the in-band NTF_Q is designed to be nearly zero, requiring $H_{EF} \to 1$ or $H_{CIFF} \to \infty$. This choice makes NTF_{N1} approximately unity-gain in-band, and therefore E_{N1} is not suppressed. NTF_{N2} is not suppressed by the CIFF loop, but it can be shaped by the EF loop, which is an advantage in some CIFF-EF mixed designs [36], [40].

We notice from Eq. (4) that H_{EF} is on the numerator of the NTF. This location for H_{EF} implies that a simple FIR filter can implement the zeros in NTF and suppress E_Q. In contrast, H_{CIFF} is on the denominator of the NTF, and it needs high gain (i.e., integrators or IIR filters) to suppress E_Q. However, a drawback is that EF-NS-SAR is more sensitive to filter-gain variation, as in-band H_{EF} must be precisely 1. Despite its higher complexity, CIFF-NS-SAR generally is more tolerant to gain variation as H_{CIFF} only needs to be sufficiently large. Fortunately, as we will discuss in Section IV-A, *Cascaded Noise-Shaping* can mitigate the sensitivity of EF-NS-SAR.

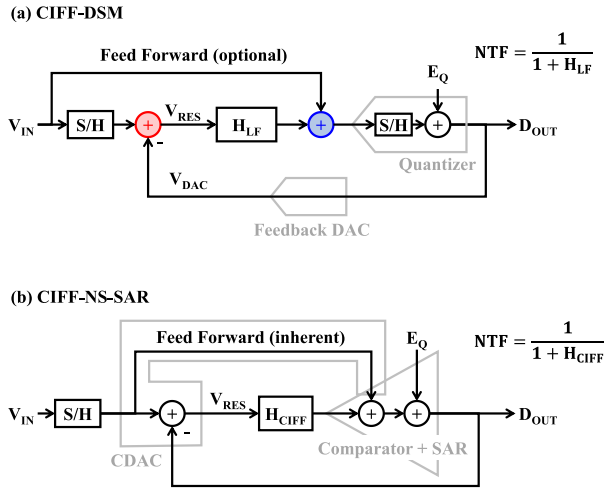

FIGURE 4. Comparison between conventional CIFF-DSM and CIFF-NS-SAR.

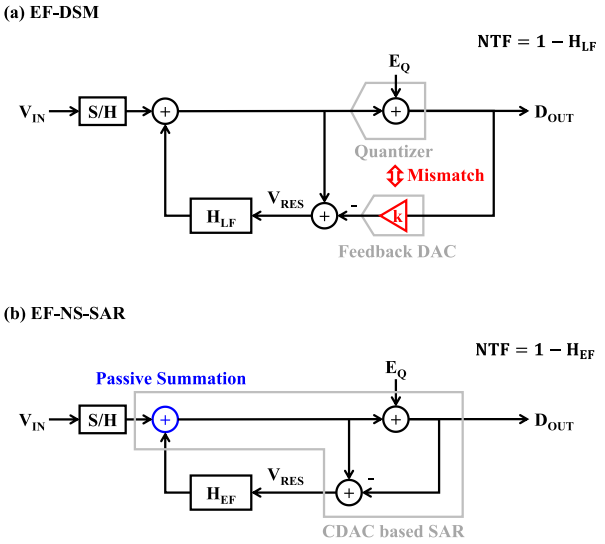

FIGURE 5. Comparison between conventional EF-DSM and EF-NS-SAR.

C. COMPARISON TO CONVENTIONAL DSM

The signal model of NS-SAR is essentially similar to that of a conventional DSM, but there are three key differences:

1) An NS-SAR (Fig. 4(b)) directly samples and quantizes the input signal. The loop filter only processes a small residue, and therefore no active, linear block processes large signals. However, in a conventional DSM (Fig. 4(a)), a summer (shown in red) sees the input signal and subtracts the feedback DAC output, to generate a shaped residue ($V_{RES} = -E_Q NTF$). The loop filter has to amplify this residue to almost full-scale before sending it to the quantizer. All of these operations involve large-signal processing, and thus opamps are typically required for linearity. An optional feedforward path can reduce the output swing of the loop filter, but this feedforward adder (shown in blue) still processes large signals. A passive feedforward adder can provide better linearity, but is still less flexible compared to the small-signal adders in NS-SAR.

2) An essential advantage of NS-SAR is that it precisely extracts the residue, making the EF structure practical. This advantage is because the DAC that generates the residue in NS-SAR is also used in quantization. This feature eliminates the possible mismatch between the quantizer and the feedback DAC in conventional EF-DSM (Fig. 5). Reusing the CDAC as the feedback DAC also lowers the overall cost.

3) It is hard to make a high-resolution quantizer (i.e., Flash ADC) in a conventional DSM, and therefore, typically, the quantizer resolution is below 6-bits. However, the SAR core in an NS-SAR can readily provide more than 8-bits of resolution. A high-resolution quantizer further relaxes the loop-filter requirements, including gain, linearity, and swing. Therefore, the loop filter in NS-SAR can be more efficient and compact. Moreover, the stability requirement of the noise-shaping loop is greatly relaxed by the high-resolution quantizer. Indeed, NS-SARs are usually unconditionally stable even with a noise-shaping order as high as 4^{th} order [27]. Although using a SAR quantizer in a conventional DSM can also achieve higher resolution, again, it needs an extra feedback DAC and is less elegant.

Due to the reasons above, NS-SAR can be a good substitute for a conventional discrete-time DSM. Indeed, as we can see from Fig. 1, the performance of NS-SAR already matches that of most DT-DSMs, but with lower power and area cost.

IV. CHALLENGES AND SOLUTIONS

Despite the advantages over DSM, NS-SAR also has various challenges, which are the main focus of current research. This section discusses the challenges in loop filtering, DAC mismatch, bandwidth limitations, and kT/C noise. We also discuss existing solutions.

A. LOOP FILTER

The loop filter is one of the critical blocks in NS-SAR. It is the only analog-like block in NS-SAR, and usually, it dominates the SNR and power efficiency. As mentioned, the loop filter in NS-SAR can be much simpler than one in DT-DSM, mainly because the loop filter only processes a small residue. In recent NS-SARs, the loop filter is usually opamp-free and sometimes entirely passive.

A loop filter generally provides three functions: **1**) It provides filtering of the residue, which is essentially an LTI system; **2**) It provides loop gain, meaning that it can amplify the residue at some specific frequencies. **3**) It sums its output back to the SAR. The first function is often implemented by classic switched-capacitor (SC) circuits, either in FIR or IIR forms. There are various strategies for the implementation of the latter two functions, and these are critical for loop filter performance.

1) PASSIVE STRATEGIES

Passive signal processing (i.e., filtering and summing) is popular in recent NS-SAR designs and requires only passive

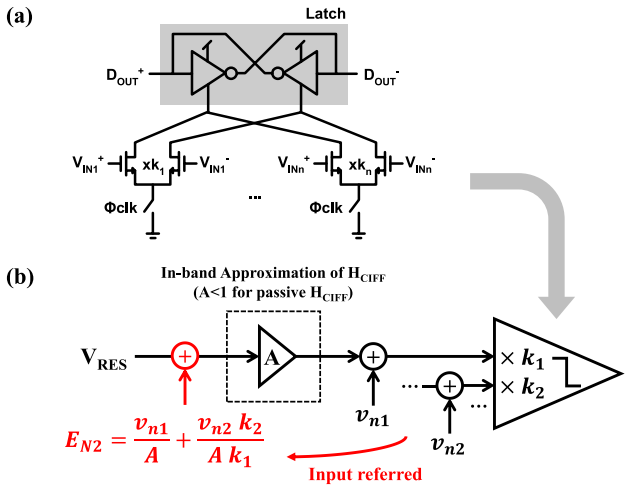

FIGURE 6. a) Realizing summation and gain with a multi-input comparator, b) and its noise inefficiency.

components, such as switches and capacitors. It is simple, linear, PVT robust, and scaling-friendly. Passive filters are also inherently dynamic. Thus, they are usually more energy-efficient than active ones that consume static power. The biggest challenge in passive filtering is its insufficient gain. Due to energy conservation, there is no power gain in a passive filter, and thus high gain is either not achievable, or a high gain simply has no driving ability. There are currently two strategies to deploy passive filters in NS-SAR: **1**) using an implicit active amplifier and summer, or **2**) using capacitor stacking.

The first strategy mainly applies to multi-input comparators, as proposed in the first CIFF-NS-SAR [5]. Fig. 6(a) gives an illustration. In this class of NS-SAR, there are multiple different-pair comparator inputs, each with different sizing. Summing the output currents of these input pairs simultaneously realizes signal amplification and summation in the comparator input stage. This configuration can only implement the CIFF structure.

A multi-input comparator is not entirely passive, and the first stage of a dynamic comparator is essentially a dynamic amplifier. However, this approach is simple and fully dynamic, and therefore some recent NS-SAR designs still use this method. Compared to "true active" methods, however, a multi-input comparator is noise inefficient. This inefficiency is in part because the extra input pairs generate additional noise. Furthermore, the comparator is behind the passive filter (H_{CIFF}). Thus the kT/C noise of the passive filter is not suppressed by the comparator gain, and any loss in the passive filter increases the input-referred noise of the loop filter, as shown in Fig. 6(b). This drawback is insignificant in low SNR designs, but it is hard to make a high SNR NS-SAR that solely relies on a multi-input comparator.

Another promising strategy for passive loop filtering is capacitor stacking. The basic idea originates from the voltage doubler in power electronics, and [44] introduces this idea to provide gain in a pipeline ADC. Fig. 7. shows the basic

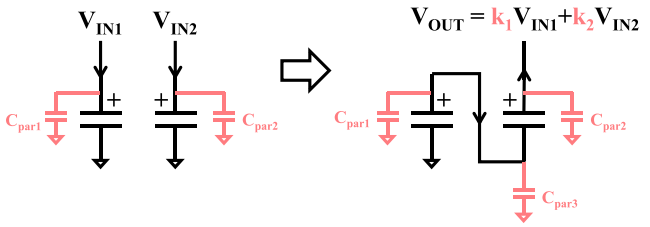

FIGURE 7. Capacitor stacking realizing amplification or summation.

concept of capacitor stacking, where we simply charge two capacitors and then connect them in series. From KVL, we know that the voltage across the two capacitors is the sum of voltages on each of the capacitors. Therefore, this passive SC circuit can realize signal summation or amplification if we charge both capacitors with the same signal voltage (i.e., $V_{IN1} = V_{IN2}$).

Unlike the first passive gain strategy, capacitor stacking is truly passive and can provide integer gain and/or signal summation with high linearity. This method became popular after being introduced to NS-SAR by [8] and [22] and also enables the Cascaded-NS-SAR [27], [37]. An advantage is that the input-referred noise (kT/C_{tot}) of a capacitor stacking amplifier is only related to its total capacitance (C_{tot}) regardless of the number of stackings. This is because the kT/C noise induced during capacitor splitting is eventually canceled out after stacking [29]. Furthermore, differential capacitor stacking can provide an extra 2x gain and remove common-mode [22]. A limitation of capacitor stacking is its poor output driving ability, but this can be mitigated by following with an active amplifier or buffer [37]. Another problem is the high sensitivity to parasitic capacitances. The parasitics (C_{par}) in Fig. 7 are from both the capacitor plates and the switches. These parasitic introduces gain errors (k_1 and k_2) and distortions if C_{par} is nonlinear, degrading the overall accuracy. The sensitivity to parasitics quickly increases as the number of stacked capacitors increases, making a high stacking number (i.e., high gain) impractical. Thus, the highest capacitor stacking number reported for NS-SAR is only 2, providing a passive gain of roughly 4 [29].

2) ACTIVE STRATEGIES

In contrast to passive strategies, active loop filtering is more flexible and better developed. This is because active amplifiers provide the gain in an active filter. This gain can be high if there is sufficient power and area. Essentially, active amplifiers introduce an extra degree of freedom in the loop-filter design. Thus, an active NS-SAR can cover a more extensive specification range. The main concern for the active strategy is the extra power consumption. Intuitively, active circuits burn power for biasing, but as we will see later, active methods can still achieve surprisingly high efficiency with proper design.

There are many methods for implementing active loop filters in NS-SAR. Early designs used (simplified)

TABLE 1. DT amplifier comparison.

Techniques	Gain	Linearity	Robustness		Efficiency	
			PVT[1]	Timing[2]	Noise[3]	Bias[4]
Opamp (closed-loop)	High	Good	Good	Good	Poor	Poor
Multi-input Comparator[5] [9]	Medium[6]	-	Fair	Good	Worst	Good
DA [13] (conventional)	Medium	Fair	Poor	Poor	Best	Good
DA [18] (regenerative)	High	Fair	Poor	Worst	Fair	Good
DA [28] (closed-loop)	Medium	Good	Good	Good	Good	Good
Gm-R [27]	Medium	Fair	Poor	Good	Poor	Fair
Gm-R [31] (power-gated)	Medium	Fair	Poor	Good	Poor	Good
Cap-Stacking + Follower [37]	Low	Good	Good	Good	Good	Good
Ring Amp [45] (closed-loop)	High	Good	Fair	Good	Good	Fair

[1] Stability of the gain under PVT variation.
[2] How the gain changes under timing variations, such as skew and jitter.
[3] Efficiency the amplifier thermal noise suppression in terms of power consumption.
[4] How efficiently the amplifier biases its circuitry. Static biasing and multi-stage topology are regarded as inefficient while dynamic operation and current reuse are regarded as efficient.
[5] Strictly, a comparator is not an amplifier as it does not provide analog outputs. This is for CIFF-NS-SAR scenario only.
[6] Refers to relative gain. A comparator's absolute gain is extremely high.

opamp-based switched-capacitor filters [5], [10], [11], which are robust but not the most efficient. Later work introduced dynamic gm-C amplifiers [13] and open-loop gm-R amplifiers [23] to NS-SAR. These new designs are lower power and easier to scale than opamps. However, these designs are highly sensitive to PVT and timing. Indeed, opamps and dynamic open-loop amplifiers are two extreme cases in the performance-robustness trade space. Recent active NS-SARs achieve a better balance between performance and robustness by exploring new DT amplifier and loop filter designs, pushing the FoMs of active NS-SAR to over 180dB under PVT [28], [36], [37] – this efficiency is better than that of most passive NS-SARs.

To conclude, Table 1 gives a qualitative evaluation of mainstream DT amplifiers. The Closed-loop Dynamic Amplifier [28] is a promising choice as it has a large closed-loop gain for high robustness. In addition to being dynamic for high biasing efficiency, the closed-loop DA is not sensitive to timing because of its natural settling behavior. Furthermore, similar to the Ring Amplifier [45], its bandwidth shrinks during settling, which improves noise efficiency. Finally, although the achievable gain of a closed-loop DA is a little lower than with an opamp, this can be easily compensated by cascading more stages.

3) CASCADED NOISE-SHAPING

The amplifiers in an NS-SAR usually sacrifice gain accuracy for efficiency and process-scaling concerns. This causes coefficient variation in the loop filter and makes high-order filter implementation challenging. As analyzed in [27], a conventional NS-SAR (Fig. 3) is hard to be implemented with an aggressive NTF above 2nd-order because the performance degrades too much in the presence of circuit variations.

To solve this, [27] proposes the Cascaded NS-SAR, which places NS-SAR in a nested structure. Fig. 8 illustrates this idea and shows a practical implementation with capacitor stacking. There are multiple decoupled feedback stages in

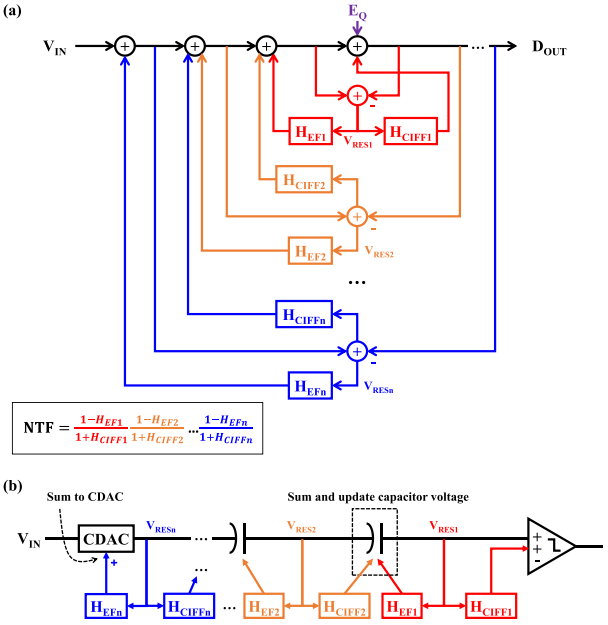

FIGURE 8. a) Generalized Cascaded NS-SAR and b) an implementation based on cap-stacking.

a Cascaded NS-SAR. Each stage receives the shaped noise from its previous stage, applies a new round of shaping on the noise, and then passes it to the next stage. In this way, a cascaded NTF is naturally formed. Cascaded NS-SAR can independently place each zero-pole pair and has much better tolerance to variations, especially for a high order NTF. Besides, it relaxes the noise requirements of the former stages as their noise is filtered by the latter stages. This method enables the first 4th-order (2x 2nd-order) NS-SAR [27], and later [37] demonstrate a 4x 1st-order Cascaded NS-SAR with a robust 94dB SNR and a 182dB FoMS. Reference [36] is also implemented in the same framework with both CIFF and EF path enabled.

B. DAC MISMATCH

DAC mismatch is another significant error source in an NS-SAR. It introduces a signal-dependent error at the DAC output. This error is modeled as additive noise, E_D in Fig. 4, but it is essentially a nonlinear behavior and causes harmonic distortion of the signal. Furthermore, it also increases the in-band noise floor due to intermodulation of the out-of-band noise. Conventional SAR ADCs have the same issue, and some solutions already exist. However, the oversampling of NS-SAR enables a family of Mismatch-Shaping techniques that more elegantly solve this problem.

1) CONVENTIONAL SOLUTIONS

A brute-force way to reduce DAC mismatch is to increase the DAC area. Roughly, every 4x increase in the area reduces the normalized standard deviation of DAC elements by 2x. This strategy goes against the low-cost goal of NS-SAR, and it is rarely practical.

A more commonly used method is digital post-calibration, which uses digital algorithms to cancel out the DAC

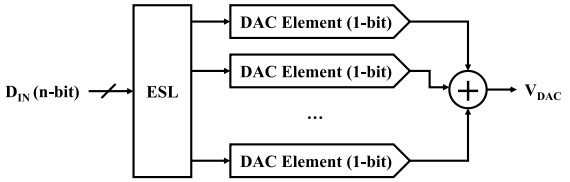

FIGURE 9. Digital MS (a basic form without segmented).

mismatch at the digital output. This is feasible because mismatch errors are deterministic. In most cases, it is theoretically possible to recover the "original version" of the signal by digital post-processing (redundancy is usually needed). The key to calibration is an accurate estimation of the DAC mismatch, and two types of strategies exist: foreground and background. Foreground calibration is usually simpler in implementation; thus, many reported NS-SAR designs apply foreground calibration and can achieve as high as 105dB SFDR [37]. The drawbacks are that foreground calibration needs an extra calibration phase,[1] and it cannot track variations during normal conversion. Background calibration can track variations in real-time, but it is more complicated and converges slower. In NS-SAR, background calibration is not very attractive[2] compared to the Mismatch-Shaping methods, discussed below.

2) DIGITAL MISMATCH-SHAPING

Mismatch-Shaping (MS) is an attractive mismatch solution for oversampled ADCs such as NS-SAR. Similar to noise-shaping, MS only suppresses the in-band mismatch error, but it does not require any prior knowledge or estimation of the mismatch. There are two types of MS techniques: digital MS and analog MS.

Digital Mismatch-Shaping is also known as Dynamic Element Matching (DEM). It is based on element-wise DAC operation (Fig. 9). An Element Selection Logic (ESL) block chooses the elements, so that the mismatch error is less dependent on the DAC code, and the in-band error reduces. Some simple but popular ESL techniques, such as random selection and code-dependent rotation (i.e., Data Weighted Averaging, DWA [46]), shuffle and 1st-order shape the mismatch error respectively. Furthermore, advanced ESL techniques [47] can achieve higher-order shaping but at the cost of more complicated logic. Indeed, logic complexity and the related long delay are the main drawbacks of digital MS; therefore, digital MS higher than 2nd-order is rare in practice.

Another drawback of digital MS is the element-wise operation requirement. The scale of the DAC control logic grows exponentially as the DAC resolution increases. This complexity makes it impractical for high-resolution quantizers, such as NS-SAR ADCs. To solve this, most NS-SAR designs apply digital MS to only a few MSBs, so that the scale of ESL is acceptable. But then the errors from LSBs are not suppressed. Binary-operated DEM [14] reduces ESL complexity but offers limited error suppression. Segmented DEM [48] is another technique to reduce ESL complexity, but suffers from some limitations in signal swing and has not yet been applied to NS-SAR. Reference [11] achieves 112dB SFDR with digital MS, which is the highest among NS-SAR. But it is limited in bandwidth (2kHz) due to its complicated ESL.

1. In commercial products this is usually done in the post-fabrication testing. An e-fuse ROM stores the calibration code (trim code). This kind of foreground calibration is also called "trimming".

2. We are not aware of any reported use of background calibration in an NS-SAR.

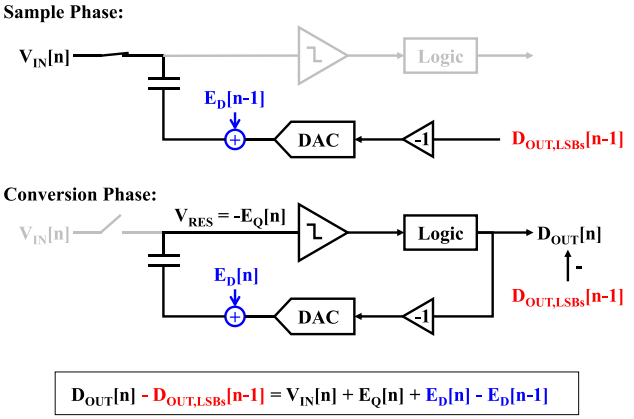

FIGURE 10. Analog MS (1st-order example).

3) ANALOG MISMATCH-SHAPING

Analog Mismatch-Shaping is also known as Mismatch Error Shaping (MES) [10]. The basic idea is to capture the mismatch error in analog form and feed it back for noise-shaping. Fig. 10 shows the framework of analog MS, where the key is to preset the CDAC's LSBs in NS-SAR before sampling, such that the mismatch error from previous conversions is captured during sampling. Note that the MSB is not fed back as it is assumed to be an accurate reference. The preset LSBs from the previous conversion are later subtracted from the current D_{OUT}.

Unlike digital MS, analog MS is relatively simple in implementation and does not need element-wise operations. Moreover, it can still achieve similar performance (105dB SFDR in [10]). The main challenge in analog MES is that the presetting of the CDAC not only feeds back the mismatch error but also feeds back the previous input signal. Thereby, the feedback signal occupies a large portion of the input signal range and reduces the maximum input range. To mitigate this problem, [10] proposed applying analog MES on only some LSBs and still using DWA for the MSBs, greatly reducing the input range loss. Reference [29] introduced a predictor to compensate the input signal and recover the input range to full scale. Reference [29] also implements 2nd-order MES. Higher-order MES is also possible with reasonable hardware costs [49].

C. BANDWIDTH LIMITATION AND INTERLEAVING

An inherent disadvantage of oversampled ADCs, including NS-SAR, is their limited bandwidth. The fastest

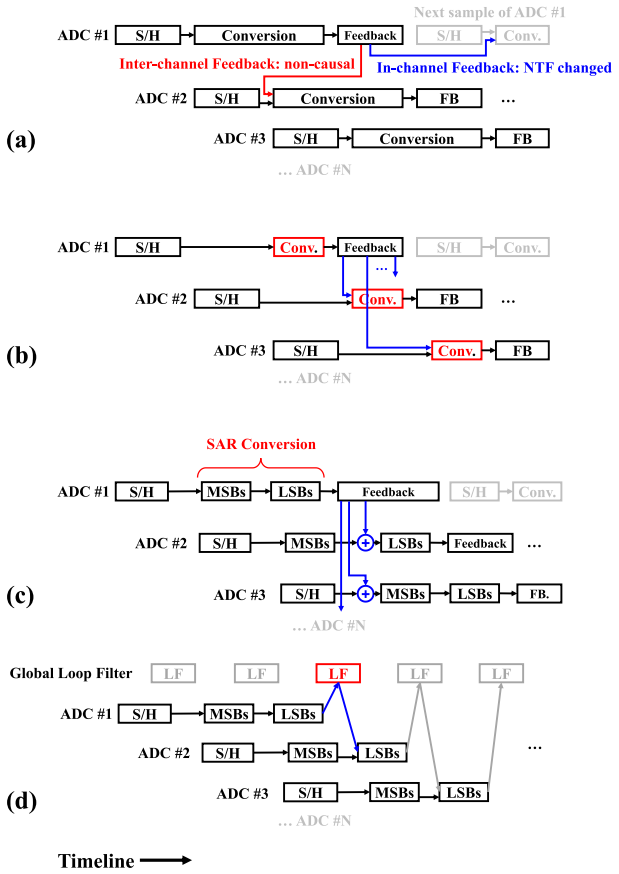

FIGURE 11. Time-interleaving NS-ADCs. a) The challenges, b) conventional TI-DSM, c) EF-based TI-NS-SAR, and d) CIFF-based TI-NS-SAR.

single-channel NS-SAR [22] is implemented in a 14nm FinFET process and has a 40MHz bandwidth with 67dB SNR. However, this bandwidth and DR are insufficient for many applications. The limitation is caused by oversampling and the multi-cycle nature of SAR conversion.

Time-Interleaving (TI) is a simple but effective technique to boost the sampling rate. The basic idea of time-interleaving is to operate multiple ADC channels in turn and overlap their conversions, as shown in Fig. 11(a). Directly applying time-interleaving to NS ADCs does not work because the feedback delays become N-times longer, and thus the NTF form is not preserved (applied with z to z^N transformation). On the other hand, feeding signals between adjacent channels is not causal (physically impossible) because the residue is generated after the start of the next channel (Fig. 11(a)). Therefore there are two requirements for interleaving of NS-ADC: 1) inter-channel feedback to avoid the z to z^N transformation,[3] and 2) a mechanism to receive the inter-channel feedback.

Some early examples of interleaving with conventional DSMs [50] pass the residue between channels, but the residue

3. In some special cases we can accept a z to z^N transformed NTF, and then inter-channel feedback is not necessary. An example is a bandpass DSM, where interleaving two lowpass DSM implements a bandpass DSM by natural z to z^2 transformation.

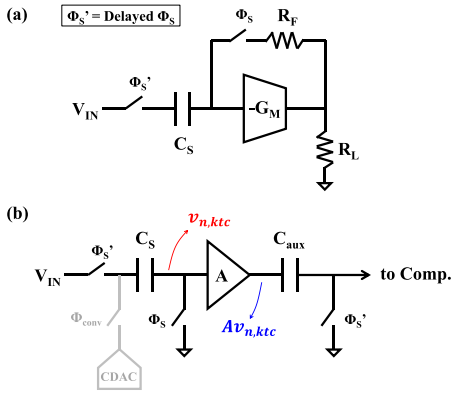

FIGURE 12. kT/C reduction techniques, a) through feedback and b) by active cancelation.

arrives before the quantizer converts (Fig. 11(b)). In other words, the quantizers still have to run at full rate. Besides, each loop filter in these TI-DSMs requires inter-channel feedback (also called "noise cross-coupling"), and thus the wiring is quite complicated. For this reason, many of these DSM designs are only 2x interleaved and suffer considerable efficiency and area penalties. In contrast, NS-SAR is a better candidate for time interleaving because the SAR process is naturally multi-phase, and with sufficient redundancy, it can accept feedback signals during the conversion process. In this way, a TI-NS-SAR does not need to run its SAR core faster, and the efficiency advantage is preserved.

TI-NS-SARs can be built with both EF structure [23] and the CIFF structure [30], [38]. An EF-based TI-NS-SAR directly feeds the residue from one channel to the others, and each channel samples and sums the feed-in signal with an analog adder (Fig. 11(c)). Since only one channel in an EF TI-NS-SAR is generating a residue at any moment, a single shared wire (i.e., the analog bus in [23]) is enough to carry all the inter-channel feedbacks. A significant advantage is that an EF-based TI NS-SAR is very flexible in terms of NTF. It is easy to adjust the coefficients simply by changing the weights of the adders. However, the implementation of the analog adder is challenging, and this limits the power efficiency of this kind of TI-NS-SAR. In contrast, CIFF-based TI-NS-SAR shares a global integrator between channels (Fig. 11(d)). Thus the loop filter in CIFF-TI-NS-SAR is actually not interleaved, but usually, it is passive and can run at the full rate [30], [38]. Interleaving the SAR core in a CIFF-based TI-NS-SAR is still beneficial in overall speed and efficiency.

So far, the fastest lowpass TI-NS-SAR (in a CIFF structure) demonstrates 80MHz bandwidth with 66dB SNDR [38]. Bandpass TI-NS-SAR can deliver even more bandwidth (e.g., 100MHz in [51]) but may have limited application.

Lastly, it is worth mentioning that TI-NS-ADCs with an OSR larger than the number of channels benefit from reduced sensitivity to channel mismatch. This resiliency is because most errors from channel mismatch are at high frequency

and are out-of-band.[4] This is an advantage compared to time-interleaved Nyquist-rate ADCs, where channel mismatch calibration is a big challenge.

D. DRIVING THE INPUT AND KT/C NOISE

Another common challenge in high-resolution SAR ADCs is the sampler. Typically, the input signal samples onto a CDAC (whose total capacitance is C), and inevitably, thermal noise with a total power of kT/C is also sampled. Thus a large CDAC capacitance is regarded as necessary to make a high-resolution sampler. However, such a large capacitance places a considerable burden on the signal source. A well-known solution is to insert an input buffer to relax the load on the input source. Some advanced designs [52] embed this buffer in the SAR loop for higher linearity. However, a drawback is that these buffers often consume more power than the ADC core.

In an NS-SAR, oversampling reduces kT/C noise power by the OSR, so that the sampling capacitor can be OSR-times smaller. But since the sampling frequency increases, the input buffer has to charge the capacitor faster, and thus the buffer's burden is not fully relaxed. For example, [24] introduced an embedded buffer in an NS-SAR with a FoMs of 163dB. In [24], the buffer leads to a 4dB FoM penalty.

Reference [53] proposes two techniques to reduce the kT/C noise in the sampling phase. The first technique uses a feedback circuit to decouple the noise source impedance and the noise bandwidth (Fig. 12(a)). In the optimal case ($R_L{}^2 = R_F/G_M$), this method can reduce kT/C noise roughly by $R_F/R_L/2$. Reference [54] implements this technique in a Nyquist SAR ADC for a 3.5x kT/C noise reduction. The second technique uses an extra amplifier and a sampler to capture the kT/C noise and then cancel it out in a later phase (Fig. 12(b)). Although the second sampler (C_{aux}) introduces extra kT/C noise, this noise is suppressed by the amplifier gain and theoretically can become negligible. In an ideal case, this technique can completely remove kT/C noise, but it introduces extra amplifier noise and thus requires careful tradeoffs. Furthermore, this method places a bandwidth limitation on the input signal. If V_{IN} is changing too quickly, then the noise-capturing amplifier will overload. Reference [36] applies this technique to an NS-SAR for an 87dB DR with only a 0.8pF sampling capacitance. In a sense, both techniques trade sampling capacitance for amplifier cost, which seems not much different from using a buffer. However, the amplifiers in these techniques need only to process small signals and thus can be simpler. The signal BW limitation of these methods also makes them more suitable for NS-SAR.

V. COMPARISON OF PUBLISHED DESIGNS

We compare NS-SAR ADCs from some academic publications (till June, 2021) to gain insight. Table 2 summarizes the main specifications and design strategies (only those with silicon results are included). Fig. 13 provides scatter plots of some critical specifications for better understanding. We draw several conclusions.

1) The overall performance of NS-SAR is slowly improving. Roughly, FoMs increases by 6.4dB, and BW increases by 8.4x per decade.
2) The performance of NS-SAR strongly benefits from process, especially for FoMs, BW, and area. The designs in the advanced processes (14nm and 22nm) are the smallest in area. So far, designs in 28∼65nm planar CMOS processes have the highest FoMs.
3) Although CIFF designs outnumber the EF ones (i.e., 26 out of 36), there is no clear performance difference between CIFF- and EF-NS-SARs. However, robustness may be a potential difference and deserves further examination.
4) Capacitor-stacking is beneficial in many respects. The designs with the highest FoMs, the highest BW, and the smallest area all use cap-stacking.
5) Dynamic amplifiers are helpful for high efficiency, but so far they are not used high BW (>10MHz) NSSAR ADCs.
6) By itself, a multi-input comparator (e.g. [7], [9], [15]) is inefficient, and these ADCs cannot achieve high SNDR and FoM.
7) An opamp is still beneficial for superior SNDR, although these ADCs are at low speed.
8) SNDR is limited to ∼70dB with natural DAC matching.
9) Foreground calibration is the mainstream solution for DAC mismatch. However, publications usually do not consider the power and area cost of foreground calibration.
10) Both analog and digital MS can enable high SNDR and FoM.

In conclusion, we make the following recommendations for NS-SAR ADC design: **1**) Use the most advanced process node available; **2**) Consider advanced loop filtering techniques, such as capacitor-stacking and closed-loop dynamic-amplifiers; **3**) Consider mismatch-shaping and cascading for high resolution; and **4**) Consider passive filtering and interleaving for high bandwidth.

VI. FUTURE TRENDS

A. HIGHER SPEED

Even with interleaving, the highest BW for an NS-SAR reported is only 80MHz (100MHz in bandpass case [51]). The main speed limitation is the multi-cycle SAR conversion and the loop filtering. There are two promising approaches to improve BW: **1**) improve conversion speed by adopting some existing SAR ADC techniques, such as multi-bit-per-cycle conversion [55], loop-unrolling [56], and ping-pong comparator operation. **2**) Speed up the loop filter with advanced filtering techniques, such as CT loop filtering.

4. Out-of-band blockers may be down-mixed into the signal band. In this case a pre-filter can be used to suppress the blockers. Note that this filter is simpler than the anti-aliasing filter in a Nyquist rate ADC, as the modulation by channel mismatch is relatively weak.

TABLE 2. Comparison table[3].

Year	Publication	Process (nm)	Area (mm^2)	BW (MHz)	OSR	Power (μW)	SNDR (dB)	FoM_S (dB)	Structure	Gain Type[1]	DAC Mismatch Mitigation[2]	Legacy
2012	[5] Fredenburg	65	0.03	11	4	800	62.1	163.5	CIFF	OPA+MIC	-	First silicon CIFF-NS-SAR
2013	[6] Park	500	0.689	3.125	10	38	67.7	176.9	EF	-	Calibrated	First silicon (weak) EF-NS-SAR
2015	[7] Chen	65	0.012	6.25	4	100	58	166.0	CIFF+EF	MIC	-	Passive filtering
2016	[8] Chen	65	0.01	8	4	253	64.9	169.9	CIFF	CS+MIC	-	Passive gain
	[9] Guo	130	0.13	0.125	8	61	74	167.1	CIFF	MIC	Calibrated	Comparator input sizing
	[10] Shu	55	0.07	0.001	500	16	**101**	178.9	CIFF	OPA+MIC	DWA+MES	Highest SNDR, analog MES
	[11] Obata	28	0.12	0.002	25	37	98	175.3	CIFF	OPA+MIC	DWA	
	[12] Saisundar	180	0.28	$40*10^{-6}$	64	20	88	151.0	EF	OPA	DEM	EF with strong 1st-order NTF
2017	[13] C.C. Liu	28	0.005	5	13.2	460	79.8	180.2	CIFF	DA+MIC	DWA	DA, sub-ranging, prediction
	[14] Miyahara	65	0.08	0.25	20	258	83.4	173.3	CIFF	DA+MIC	DEM	Large F_S scalability, binary DEM
	[15] Guo	40	0.04	0.262	16	143	78.4	171.0	CIFF	MIC	Calibrated	Voting
	[16] Y. Lin	14	0.004	25	6	2400	69.1	169.3	CIFF	MIC	-	First FinFET design, Vref neutralization
	[17] Garvik	28	0.016	1.75	8	71	68.1	172.0	CIFF	OPA+MIC	Calibrated	LSE-based foreground calibration
2018	[18] Li	40	0.024	0.625	8	84	79	177.7	EF	DA	Calibrated	EF with complex 2nd-order NTF
	[19] Dai	65	0.082	3.76	5.7	460	68.5	167.6	CIFF	MIC	-	
	[20] Hwang	28	0.058	0.05	16	60	72	161.2	CIFF	MIC	DEM	
	[21] Shi	180	0.25	0.002	32	74	78.8	153.1	EF	OPA	-	Using a cyclic-based quantizer
2019	[22] Y. Lin	14	0.002	40	4	1250	66.6	171.7	CIFF	CS	-	Fastest single ch., cap stacking summing
	[23] Jie	40	0.061	50	4	13000	70.4	166.3	TI-EF	GMR	DEM	Time-interleaving (EF)
	[24] Kim	65	0.081	2	20	2130	73.8	163.5	CIFF	MIC	DWA+MES	Buffer embedded
	[25] Gravik	28	0.023	5	4	108	68.2	174.9	CIFF	OPA+MIC	Calibrated	Compiled layout
	[26] Yoon	65	0.072	0.625	8	130	71	167.8	EF	DA	Calibrated	
2020	[27] Jie	28	0.02	0.1	10	120	87.6	176.8	Cas.-EF	CS+GMR	Calibrated	Cascaded-NS-SAR
	[28] Tang	40	0.037	0.625	8	107	83.8	181.5	CIFF	CS+DA	Calibrated	Closed-loop DA
	[29] J. Liu	40	0.061	0.04	25	67	90.5	178.2	CIFF	CS	DWA+MES	2nd-order analog MES
	[30] Zhuang	40	0.125	50	6	8500	69.1	166.8	TI-CIFF	MIC	-	Time-interleaving (CIFF, passive)
	[31] Jiao	65	0.03	0.625	8	70	74.6	174.1	EF	GMR	Calibrated	Bandpass, configurable NTF
	[32] Y. Zhang	65	0.483	3.125	16	1240	77	171.0	CIFF	DA+MIC	Calibrated	
	[33] Shi	130	0.2	0.002	32	41	82.6	159.5	EF	OPA	-	(same architecture as [21])
	[34] Oh	65	0.013	18.8	4	500	68	173.8	CIFF	MIC	Calibrated	
	[35] Hu	180	0.12	$625*10^{-6}$	8	0.09	65	163.4	CIFF	MIC	-	
2021	[36] Wang	65	0.04	0.625	8	119	84.8	**182.0**	CIFF+EF	CS+DA	Calibrated	Highest FoMs, kT/C cancellation
	[37] J. Liu	40	0.094	0.25	10	340	93.3	**182.0**	Cas.-EF	CS+SF	Calibrated	Highest FoMs
	[38] C.Y. Lin	22	0.006	**80**	4	2560	66.3	171.2	TI-CIFF	CS	-	Highest BW
	[39] Shen	40	0.19	3.5	64	5000	78.7	167.2	CIFF	DA	Calibrated	With N-path filter
	[40] Q. Zhang	130	0.153	0.125	8	96	79.6	170.7	CIFF+EF	OPA+MIC	Calibrated	

[1] OPA = opamp, MIC = multi-input comparator, CS = cap stacking, DA = dynamic amplifier, GMR = gm-R amplifier, SF = source follower
[2] All calibration is foreground. MES refers to analog MS. DEM and DWA are digital MS.
[3] Blue marks for the top five in a column.

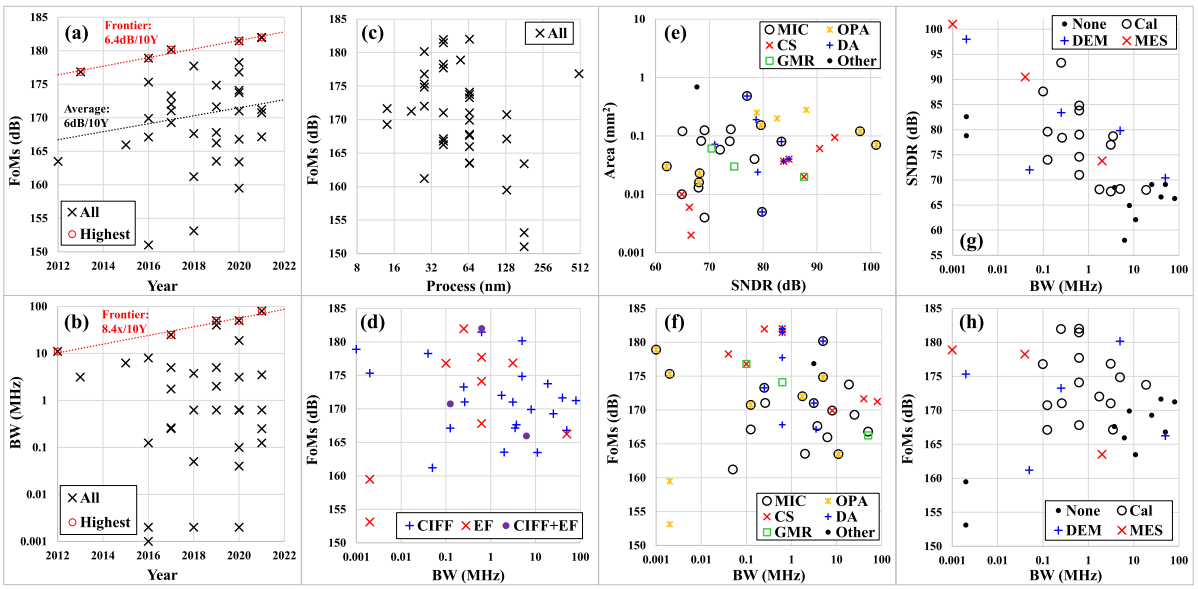

FIGURE 13. Comparison scatter plots. a) and b) plot FoM and BW over years. c) plots FoM over process. d) compares different structures. e) and f) compare different loop filter strategies. g) and h) compare different DAC mismatch solutions (DEM includes DWA).

B. HIGHER RESOLUTION

The only deficiency of NS-SAR compared to DT-DSM is the maximum SNDR. So far, few published NS-SARs have demonstrated >100dB SNDR, but this SNDR is relatively common for DSMs. Audio NS-SAR with ~120dB DR might be the next goal. More advanced

mismatch-shaping or low-cost background calibration is essential.

C. REFERENCE VOLTAGE

A well-known challenge in SAR ADCs, and especially in high-speed SAR ADCs, is to provide a stable reference voltage. In NS-SAR, this topic is rarely discussed, and most work simply relies on massive reference decoupling capacitors. Reference [16] introduces a charge neutralization technique to stabilize the reference, but this technique is limited to medium SNR. kT/C cancellation reduces CDAC size and eases the reference problem, but this method limits the signal bandwidth. A possible approach is to apply reference ripple cancellation [57] in an NS-SAR. Another possibility is to co-design a reference buffer optimized for NS-SAR. Note that this buffer might be more straightforward than the one in SAR, as an NS-SAR emphasize an accurate residue at the end of conversion, and it has a higher tolerance to the reference error during conversion.

D. FURTHER HYBRIDIZATION

Another possible trend is further architecture hybridizing. An NS-pipeline-SAR [43] and CT-DSM with NS-SAR [42] are two good examples. As the main advantages of NS-SAR are high efficiency and low cost, it is reasonable to improve it by hybridizing with available high-speed or high-SNR architectures. Possible choices are the Incremental and Zoom architectures, as both offer high resolution but are not very scalable. Another possibility is to further optimize NS-SAR with CT-ADCs. So far, the NS-SAR only serves as a quantizer in CT-DSM, and there are good opportunities for a deeper hybridization.

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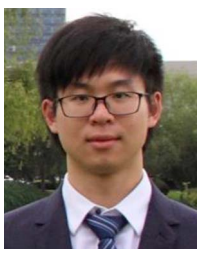

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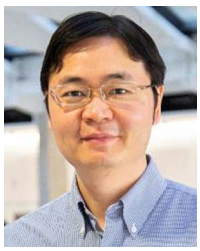

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