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Recent Advances in High-Resolution Hybrid Discrete-Time Noise-Shaping ADCs

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ABSTRACT High precision data acquisition requires very-high-resolution Analog-to-digital converters (ADC) for kHz speed or to keep a relatively high resolution for wider bandwidth (BW) around the MHz range. Although widely used, noise-shaping (NS) in ADCs offers a high-resolution characteristic, but obtaining good power efficiency and compact die area is still challenging. Recent literature showed promising progress by utilizing hybrid Discrete-Time (DT) NS-ADCs with measured silicon results. This paper focuses its analysis and discussion on two important trending classes: hybrid Incremental ADCs (I-ADC) and hybrid Time-interleaved (TI) NS-ADCs. Furthermore, this paper presents a review and addresses the benefits of those hybrid architectures.

INDEX TERMS ADC, analog-to-digital converter, DAC, digital-to-analog-converter, hybrid ADC, incremental ADC (I-ADC), delta-sigma modulator, time-Interleaving, extrapolating, noise shaping, successive approximation register, SAR.

I. INTRODUCTION

HIGH resolution ADCs are crucial building blocks in consumer electronics, especially for high precision sensors in the Internet of everything (IoE), audio codecs, and wearable healthcare applications. Such ADCs usually process signals around tens of kHz [1]. However, with the rapid development of modern industry, some wide bandwidth applications also raise the need for high-precision ADCs, including ultrasound imaging systems, radars, and emerging communications [2], [3].

The combination of oversampling and noise-shaping (NS) techniques is traditionally a promising approach to implement high-resolution ADCs. Based on the circuit characteristics, designers could divide NS-ADCs into two main types: continuous-time (CT) or discrete-time (DT). As the names suggest, the CT structure takes a continuous-time loop filter, whereas the DT structure operates based on switched capacitor circuits.

If high resolution is the primary consideration, Fig. 1 lists a detailed comparison between CT/DT NS-ADCs. The CT structure generally operates faster than the DT, leading to a possible larger oversampling ratio (OSR). Besides, the CT structure simplifies the analog front end by bringing along the inherent alias rejection property and providing an easy-driven resistive input. In this way, lower BW, smaller slew rate amplifiers can be the interface between the frontier stages and a CT-ADC. Similarly, the CT case doesn't need a reference buffer to fight against the large switching current in the DT. However, the CT case limits the linearity. Since CT's DACs' outputs error is directly injected into the loop in continuous time without the help of any noise shaping, the CT structure suffers from

	❑ CT NS-ADC	❑ DT NS-ADC
Pros	• Implicit anti-aliasing filtering • Higher sampling frequency • Resistive input stage	• Low sensitivity to clock jitter/DAC waveforms • Accurately defined integrator gains and transfer functions
Cons	• PVT problem • Tuning circuit (Capacitor bank) • ISI error • Sensitive to jitter/DAC waveforms	• The lack of anti-aliasing filtering • Lower sampling frequency • Inefficient op-amp design • Capacitive input stage

FIGURE 1. Pros/cons comparisons between CT/DT NS-ADCs.

all the DAC non-idealities [4], including the clock jitter. Moreover, the CT structure is sensitive to the process, supply, and temperature (PVT) variations as well as inter-symbol interference (ISI) errors [5], [6]. Furthermore, the CT NS-ADCs require auxiliary tuning circuits, which usually contain a large capacitor bank to ensure an accurate RC time constant in the integrator [7]. From another perspective, it is well known that the DT structure is robust and less sensitive to clock jitter and DAC waveform shapes [4]. Besides, in DT, we use well-matched capacitor ratios to define the integrator gains rather than resistor-capacitor (RC) products in CT; hence we can obtain an accurate noise transfer function (NTF) in DT. In summary, it is straightforward that DT NS-ADC responds more efficiently to high-resolution demands. Therefore, this paper focuses on the discussion of the recent trends in DT NS-ADCs.

Designers are always hunting for higher energy efficiency in the design of NS-ADCs, while simultaneously satisfying high-resolution or linearity requirements. Traditional DT NS-ADCs could be tailed or mixed with other advanced architectures, leading to hybrid ADCs. In this paper, we review two classes of hybrid high-resolution NS-ADC architectures: 1) for sub-MHz frequency, incremental ADC (I-ADC) has been widely used for ultra-high-resolution designs [8]–[16]. This paper takes a close look into the hybrid subsets, such as the zoom I-ADC [9], [10], the linear-exponential I-ADCs [11]–[13], and the sliced I-ADC [14], [15]; 2) to further extend the signal bandwidth into the MHz ranges, a good approach is the integration of Time-interleaved (TI) circuits with NS-ADCs. This paper lists several works of hybrid TI NS-ADC structures, including the N-paths filter type [17], the cross-coupling type [18], [19], and the extrapolating type [20], [21]. We discuss their pros and cons in detail.

The organization of the paper is as follows: Section II reveals the fundamental knowledge of I-ADCs, and then presents an overview of various hybrid I-ADCs. Section III discusses why and how the TI circuits can hybridize with NS-ADCs, and highlights recent solutions that led to breakthroughs. Section IV concludes the whole paper.

II. HYBRID I-ADCS

A. FUNDAMENTALS OF I-ADCS

Fig. 2 (top) shows the typical block diagram of a continuously running Delta-Sigma Modulator (DSM). The

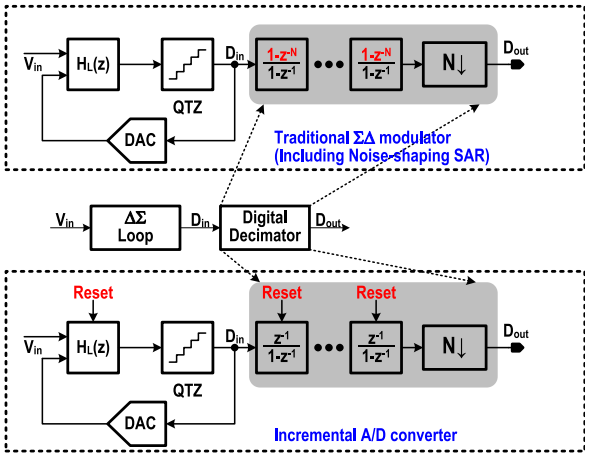

FIGURE 2. Continuously running delta sigma modulator (DSM) (top) vs. its incremental counterpart (bottom).

architecture involves three major imperative components: a DT loop filter, a quantizer, and a feedback DAC [22]. The modulator oversamples the moving analog input signal, and then the loop filter integrates the residue errors between this input and the estimated output (from the DAC). After the loop filter, the quantizer digitizes the processed signal and provides the information through a feedback DAC. The DSM continuously runs without resetting the memory in the analog integrator, resulting in shaped quantization noise. Consequently, filtering the out-of-band quantization noise and holding the in-band signal power with a lowpass digital decimation filter guarantees high in-band signal-to-quantization-noise ratio (SQNR). Furthermore, a higher loop's order shapes more quantization noise out of the band, resulting in a high-resolution performance.

Fig. 2 (bottom) shows that the I-ADC clears the memory periodically by resetting the analog modulator and the digital filter. In the I-ADC, the resetting operation breaks the loop's continuity but also brings the following advantages:

1) *Simpler Decimator:* The decimation filters of I-ADCs exhibit simple structures (counter or cascaded counters).
2) *Lower Latency:* The complex digital filters necessary for the decimation [1] significantly increase the DSM's latency.
3) *Easier for Multiplexing:* The I-ADCs do not contain memory effects since they reset the memory after a complete conversion. Therefore, they can easily share the digital outputs among channels.
4) *No Idle Tones:* The idle tones are periodic sequences generated by rational dc inputs [22]. Since the I-ADCs reset the memory periodically, therefore prevent the occurrence of those idle tones.
5) *Nyquist Rate Output:* Though the I-ADCs operate in an oversampling manner, its digital output only depends on the input samples during the Nyquist conversion interval.

However, I-ADCs still suffer from some drawbacks. In the first-order I-ADC, the required number of clock cycles is 2^N for an N-bit resolution. First-order structures are slow

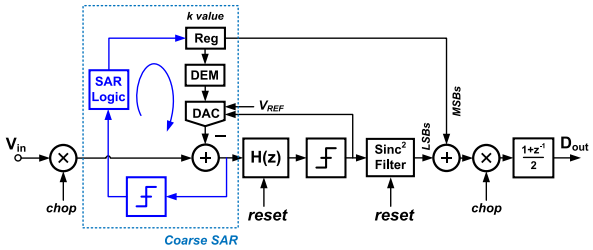

FIGURE 3. Block diagram of a zoom I-ADC proposed in [9].

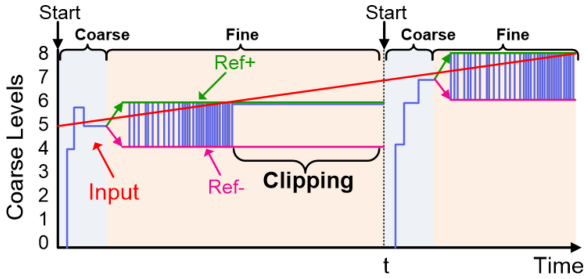

FIGURE 4. Time domain illustration of an input-clipping problem in zoom I-ADCs.

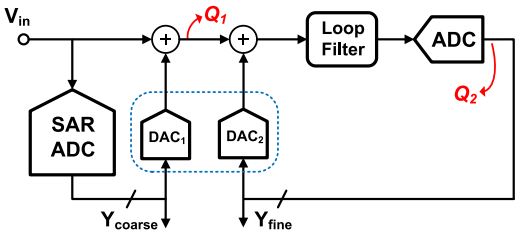

FIGURE 5. Block diagram of the coarse-fine operation in a zoom ADC.

due to the large required number of clock cycles. On the other hand, a high-order structure can significantly reduce the number of clock cycles. But, a high-order structure causes monotonic decreasing sample weightings and results in an input-referred thermal noise penalty as follows [13], [23]:

$$\frac{V_{n.total}^2}{M^2} = \frac{2kT}{C_s} \frac{\sum_{i=1}^{N} W(i)^2}{\left[\sum_{i=1}^{N} W(i)\right]^2}. \tag{1}$$

Here C_s is the total sampling capacitance, $V_{n.total}^2$ is the total output noise, M is the total gain of the input signal accumulation, and $W(i)$ are the weights for each of the samples i. The above penalty similarly applies to the average effectiveness of the dynamic element matching (DEM) performance for multi-bit DACs. The calculated penalty factors are 1.3/1.8/2.3 for 2^{nd}/3^{rd}/4^{th}-order I-ADCs [13]. Based on the above discussions, the I-ADCs attracted attention from Nyquist rate applications for their low-latency and easy multiplexing properties. As a trade-off, the noise/DAC linearity penalty is severe for higher-order I-ADCs, limiting their usage in wide bandwidth applications.

In the context of CT I-ADCs, the use of finite impulse response (FIR) feedback is a popular solution to reduce its jitter sensitivity, reduce the quantization noise being processed by the integrators, and relax the slew rate requirement of the opamps [24]–[27]. The FIR feedback can also appear in the DT incremental ADC with the latter two benefits stated above, especially for the single-bit quantizer.

B. THE ZOOM I-ADC

The zoom ADC, first introduced in [9], combines the I-ADC and the SAR ADC. The SAR ADC exhibits an excellent energy efficiency, but it is relatively weak to obtain high resolution. A subranging architecture can address such a challenge in a zoom I-ADC. Fig. 3 shows a 6-bit SAR followed by a fine 15-bit I-ADC. The SAR phase initially makes a coarse conversion and determines the approximate zoom range. Subsequently, the feedback of such preliminary digitalized codes adjusts the reference of the fine I-ADC, allowing the enhancement of the final resolution to 20-bit. This work [10], designed in a 160nm CMOS process, achieves 119.8-dB SNDR and 107.5-dB SNR in a 13 Hz bandwidth. It dissipates 6.3μW under a 1.8V voltage supply, which leads to a Schreier figure of merit (FoMs) of 182.7-dB.

However, this architecture suffers from an input-clipping problem, as illustrated in Fig. 4. When the input signal moves at a faster rate, the adjusted reference of the I-ADC cannot track the input signal well. To avoid it, an over-design of the fine ADC is usually necessary to provide at least ±1 LSB of over-range [28], which leads to waste. Meanwhile, such a 2^{nd}-order I-ADC inherently suffers from a thermal noise penalty with a factor of 1.3 (as discussed before).

Recent zoom ADCs also explored the DSM as the fine stage [28]–[30] (Fig. 5). Similar to the subranging ADC, such zoom ADCs suffer from an interstage gain mismatch between coarse and fine stages:

$$Y_{coarse} = X - Q_1 \tag{2}$$

$$Y_{fine} = Q_1 \cdot STF + Q_2 \cdot NTF. \tag{3}$$

Equations (2) and (3) give the final digital output as:

$$Y = X + Q_2 \cdot NTF + Q_1 \cdot (STF - 1). \tag{4}$$

The STF varies from unity when the ADC operates at high frequencies. Thereby, a noise leakage of Q_1 in (4) results in high-frequency spurs or interferers, which deteriorate in-band performance and further overload the system [28]. Some filtering techniques realized in the digital or analog domains can solve this issue. For example, [28] adopts a digital matched STF filter to compensate for such mismatches. While in the analog domain, [30] proposes a residue feedforward method to eliminate such STF peaking.

C. THE LINEAR-EXPONENTIAL I-ADC

Several works [11]–[13] proposed and implemented hybrid two-step linear-exponential conversion in the I-ADC, to further reduce the thermal noise and mismatch penalty while retaining an efficient accumulation. Fig. 6 (left) depicts the basic two-phase switching principle:

In phase one, the I-ADC operates in a 1^{st}-order linear mode with uniform weightings. Though uniform weighting

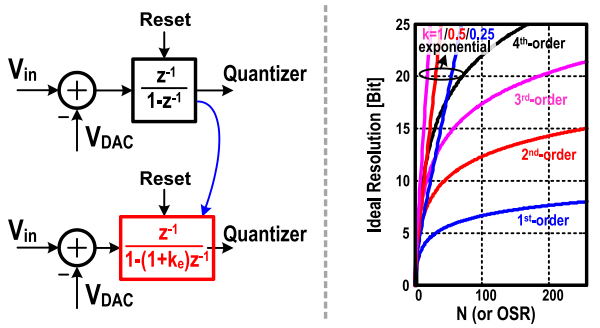

FIGURE 6. The linear and exponential transformation in I-ADCs (left) and the theoretical resolution of an exponential I-ADC and traditional order-based I-ADC versus OSR (right).

has a slower accumulation, it can fully utilize the OSR on in-band thermal noise suppression [16]. In phase two, the I-ADC operates in an exponential mode to boost the SQNR. The theoretical resolution leads to:

$$R \approx \log_2\left(\frac{(1+k_e)^N}{k_e}\right) + \log_2(L-1) - 1). \qquad (5)$$

Based on (5), Fig. 6 (right) demonstrates the relationship between resolution, the accumulation coefficient k_e and the oversampling ratio N (assuming a one-bit quantizer). Compared with the traditional order-based I-ADCs, the exponential scheme digitizes the signal faster and can achieve higher resolution within fewer clock cycles.

Fig. 7 (a) illustrates the I-ADC's exponential mode with its corresponding digital reconstruction filter. In terms of circuits implementation, there are two topologies to realize the exponential accumulation in the analog part. Reference [11] adopts a traditional integrator with an additional positive feedback path to generate the exponential transfer function. Usually, such an implementation of positive feedback requires a different capacitor-injection path into the integrator's virtual ground, as shown in Fig. 7 (b). However, we can reuse the feedback DAC to obtain the exponential integrator, when the modulator separates the sampling capacitor and the feedback DAC to avoid the detrimental reference noise caused by the signal-dependent loading of the reference driver [27]. The circuit presented in [11], fabricated in 65nm CMOS technology, achieves an SNDR of 86.02-dB with 500kHz BW. The power consumption is 20mW under a 1.2V supply.

On the other hand, [12], [13] apply the noise coupling (NC) technique to achieve exponential accumulation equivalently. From Fig. 7 (c). we can observe that the DAC output subtracts the internal ADC's input to obtain the quantization noise ε_q in the analog domain. Later, ε_q is amplified by $1+k_e$, and then feedback to the ADC's input node with one cycle delay. Accordingly, the noise transfer function is $(1-(1+k_e)z^{-1})\varepsilon_q$, as desired. Compared to the previous positive feedback case, this scheme has less penalty since the extra NC capacitors and adder are in the backend and consume less power and area. With the same 65nm CMOS process and 1.2V supply, the ADC in [13] achieves an

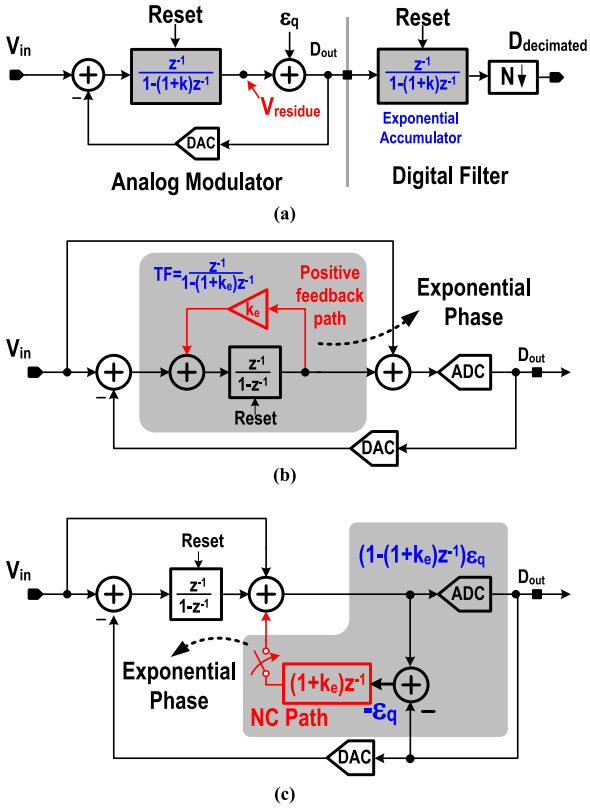

FIGURE 7. Diagrams of (a) an exponential I-ADC and its two possible analog part realizations: (b) positive feedback structure proposed in [11] and (c) noise coupling structure proposed in [12], [13].

SNDR of 100.8-dB with 20kHz BW, and dissipates 550μW, resulting in an FoMs of 176.4-dB.

D. THE SLICED I-ADC

In most I-ADCs, the first integrator needs to drive a thermal-noise-determined capacitor and fulfills a fast operational amplifier's (OTA) settling. In that way, the first integrator (and possibly the adder, for some architectures) [32] consumes most of the power. For the last stages, the gain of the preceding stages relaxes their performance; thus, the sampling capacitors can have smaller sizes. Therefore, the OTAs in the back-end consume less power. With a traditional 3rd-order I-ADC in [14] as an example, the 1st integrator consumes 80% while the 2nd/3rd-stage integrators occupy 10% and 7% of total power, respectively.

To reduce the power consumption of the first integrator, the 'split' concept is introduced into all transistors inside the first OTA and the feedback/sampling capacitors. With the first OTA's input/output nodes still connected, such hybrid architecture leads to the proposed sliced I-ADC in [15], dynamically reconfiguring the input loop filter stage with a slight signal power weakening.

Fig. 8 depicts the simplified schematic of the 3rd-order sliced I-ADC by utilizing the property of the input weighting function. As the figure illustrates, it has the first integrator split into four identical slices independently activated. Each slice, realized as a standalone switched-capacitor (SC)

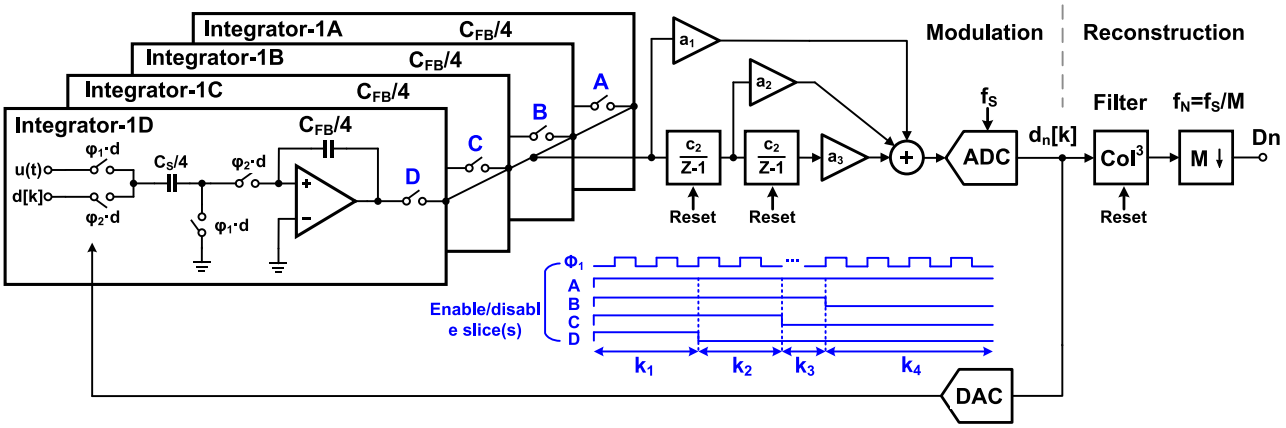

FIGURE 8. Simplified schematic of the 3rd-order I-ADC in [15] with the slicing 1st integrator.

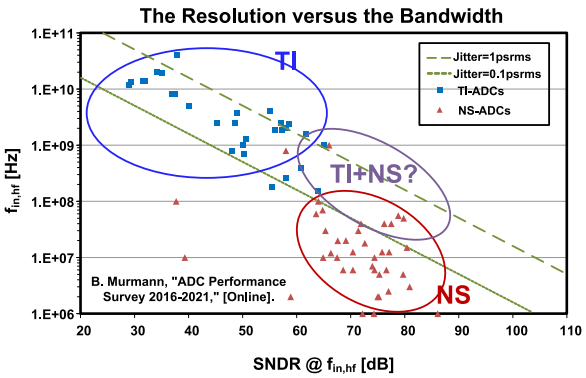

FIGURE 9. Scatter plot of the SNDR versus the input frequency for recent publications in ISSCC and VLSI (2016-2021).

integrator, employs bottom-plate sampling and uses bootstrapped switches. The four slices operate during k_0 clock cycles, three slices in k_1, two slices in k_2, and one slice operates in k_3 cycles. With the optimized clock cycle parameters ($k_{0,1,2,3} = 40, 30, 10, 70$), this prototype consumes 1.65-mW/1.098-mW without/with the slicing technique from a 3V supply, which results in only 0.7dB/0.8dB loss in SNR/SNDR, respectively. This ADC, fabricated in 180nm CMOS, has a peak SNDR of 86.6dB in a 100kHz BW, achieving a FoMs of 171.1 dB.

However, there is a trade-off between the first integrator power and the input signal power. Specifically, the effectiveness of the integrator slicing technique depends on the signal weighting function. Moreover, this work has to use a single-bit quantizer to keep the linearity. Otherwise, if the quantizer is multi-bit, it will induce DAC mismatch errors that are difficult to handle due to the square-decreasing weighting function. Consequently, the first stage must contain a power-hungry opamp architecture for a large output swing.

III. HYBRID TI NS-ADCS

Fig. 9 illustrates a comparison of SNDR vs. input frequency for recently published state-of-the-arts ADCs [33], with TI-ADC in blue squares and NS-ADC works in red triangles. We can find that: NS-ADCs dominate the high-resolution region of the plot. However, for high input frequency cases, the data points for NS-ADCs quickly diminish while the TI-ADCs points almost dominate the whole area. Such distribution leaves a blank area spanning medium SNDR (70-90dB) with moderate bandwidth (10-100MHz), near the green contour line denoted jitter=0.1ps_rms. Considering such observation, those data points suggest that it is possible to create a hybrid TI NS-ADC architecture to extend further the sampling frequency of the lower speed single channel NS-ADC. The purple circle in Fig. 9 indicates such a target area.

A. FUNDAMENTALS OF TI NS-ADCS

As mentioned above, TI architecture is the most common solution for wideband applications. For time-interleaved ADCs, we need to use multiple ADCs to sample the input signal and handle multi-phase clock relationships. A fundamental principle is that the effective sampling rate can increase by a factor of M with M ADCs.

The most significant drawback of TI is the mismatch between channels. Those mismatches are complicated and will generate interleaving spurs. Typically, there are four kinds of mismatches in TI circuits: 1) Offset, 2) Gain, 3) Timing-skew [34], and 4) Bandwidth [35] mismatches. The frequency locations of the mismatch-induced artifacts are determined by the sampling frequency f_s of the ADC system, the number of channels M, and the input signal frequency f_{in}. Here, we list all possible mismatch artifacts based on [36]:

$$f_{offset\_spurs} = k \times \frac{f_s}{N} \tag{6}$$

$$f_{timing,\ bandwidth\ \&\ gain\_spurs} = \pm f_{in} + k \times \frac{f_s}{N} \tag{7}$$

where $k = 1, 2, 3 \ldots N-1$. Consequently, for TI Nyquist ADCs, those mismatch spurs would be harmful and usually need extra calibration [37]. On the other hand, for a TI-DSM, it is only important to care about the performance inside the interesting band, due to the OSR. This means that if we place those mismatch tones outside the bandwidth, we will finally filter them out, thus not hurting the SFDR and the total

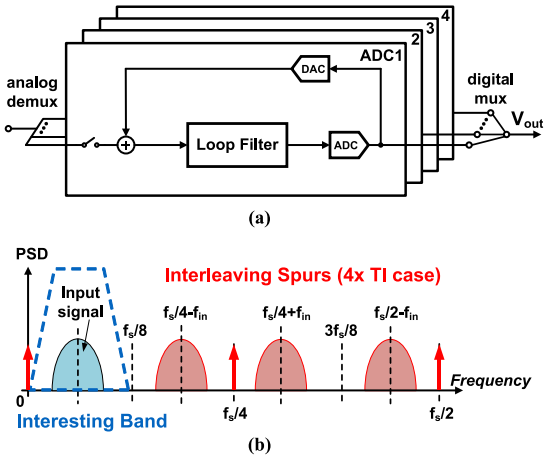

FIGURE 10. (a) 4-channel TI-DSM, and (b) its Power density spectrum with all TI spurs inside Fs/2 (color in red).

SNDR performance. However, as a trade-off, we still have to consider that those spurs limit the overall tuning range.

Fig. 10 (a) depicts an example with details. Once we operate interleaving at the circuit level (here we set M = 4), the total sampling speed increases 4 times. According to (6)-(7), it generates offset tones as well as gain, timing, and bandwidth mismatch images in Fig. 10 (b). Still, as we control the bandwidth in a specific narrow range, all those TI mismatch spurs would fall outside the BW. Specifically, if the signal range covers from DC to BW, the closet spur will be at f_s/N-BW. Therefore, we can deduce the constraint condition which makes all the artifacts fall out of band [19]:

$$OSR = \frac{f_S}{2BW} > M. \tag{8}$$

In this way, TI NS-ADCs can be immune to the inherent mismatch problems of TI Nyquist ADCs. It is an excellent benefit with such a hybrid architecture since a TI NS-ADC does not need power-hungry and complicated calibration circuits to alleviate the channel mismatches. Recent works [17]–[21] based on TI NS-ADCs utilized such characteristics to develop fast and high-performance ADC circuits. Fig. 11 summarizes three kinds of NS-ADCs, which we will discuss in the following few sections.

Similarly, the FIR feedback is also a popular solution in recently developed CT NS-ADCs. The CT implementations in [38]–[41] utilized TI FIR feedbacks for their TI quantizers, with the CT front-end stages. Although the application of such techniques are in CT, they are also applicable in the DT counterpart, with the benefits of reducing the high-frequency quantization noise in the integrators, relax the opamp's slew rate requirement, and also the distribution of the FIR filter tap coefficients along different interleaving paths.

B. TI NS-ADC BASED ON AN N-PATH FILTER

It is well known that the TI paralleling in N paths allows a z to z^N transformation of the NTF in a NS-ADC. An example is: if a single path's loop filter is $H_P(z) = 1 - z^{-1}$, then the N-path transfer function intrinsically develops as:

$$H_{Modified} = H_P\left(z^N\right) = 1 - z^N. \tag{9}$$

The NTF brings a noticeable band-stop feature when we apply a larger number of paths. Naturally, [17] presents an N-path (N = 8) Bandpass (BP) TI NS-ADC for wideband base station receivers. This ADC can achieve 78.9-dB SNDR in a 3.5-MHz BW with 5.04-mW power consumption. Each of the eight channels operates at 56.25 MHz; thus, the effective sampling frequency f_s equals 450 MHz for the whole ADC. The used CMOS technology is 40nm, and the operating voltage is 1.2V.

A BP-ADC is usually more effective when placed at the intermediate frequency (IF) in RF systems, which turns out to be an excellent trail to simplify the signal chain [42]. This design mainly solves two challenges: 1) We can easily achieve the required shaped NTF with an N-path filter, 2) Traditional closed-loop BP solutions need power-hungry amplifiers to cover the IF frequency [43], as a substitute, this TI NS-ADC adopts dynamic-amplifier (DA) based NS-SAR, leading to excellent power efficiency.

Fig. 12 illustrates a systematic block diagram of [17]. The N-path TI structure up-modulates the NTF to the IF frequency. This ADC can achieve multiple pass/stop bands: the STF is selective while the NTF is sharp and friendly scaled between channels. In the circuit implementation, a good combination is the re-utilization of the sampling capacitor of the N-path filter as the SAR's CDAC. This innovation not only reduces the total capacitance but also avoids the input signal attenuation. The 10b SAR in Fig. 12 adopts top-plate sampling. To ensure accuracy, the floating inverter-based amplifier (FIA) provides relatively high voltage gain [44] and reduces the size of the subsequent multi-input comparator.

Overall, [17] presents a BP 8X TI NS-ADC, which hybridizes the N-path filter and the NS-SAR, eases the design of analog blocks, including the front-end sample-and-hold circuits and operational amplifiers. Due to these characteristics, this BP architecture is an advanced solution for simplifying the receiver chain in many RF systems. But, this N-path TI NS-ADC only suits BP designs. The duplicated hardware is another issue, which leads to a total area of $700 \times 270\ \mu m^2$.

C. CROSS-COUPLING TI NS-ADC

The previously mentioned z to z^N transformation in the TI BP NS-ADC spreads the NTF zeros to DC locations and the multiples of fs/N. To reconstruct the NTF for Lowpass (LP) designs, it is better to move all the NTF zeros to DC by the cross-coupling technique, which has been introduced into TI NS-ADCs through polyphase decomposition [45], [46]. Nevertheless, when we implement those coupling feedback paths between channels, the major problem is the causality restrictions or the delay-free paths [47]. This situation occurs when one TI NS-ADC channel needs the adjacent previous

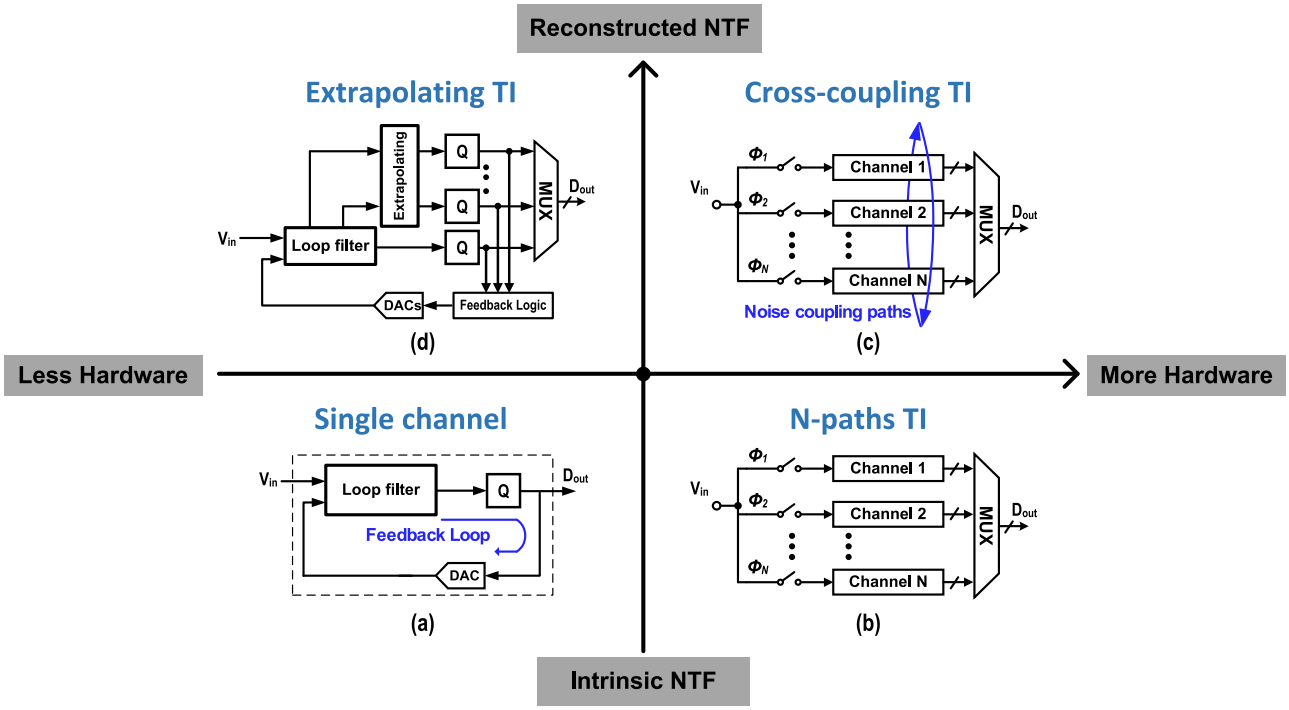

FIGURE 11. Hybrid TI NS-ADCs classifications (a) Traditional single channel (b) N-path filter TI (c) Cross-coupling TI (d) Extrapolating TI.

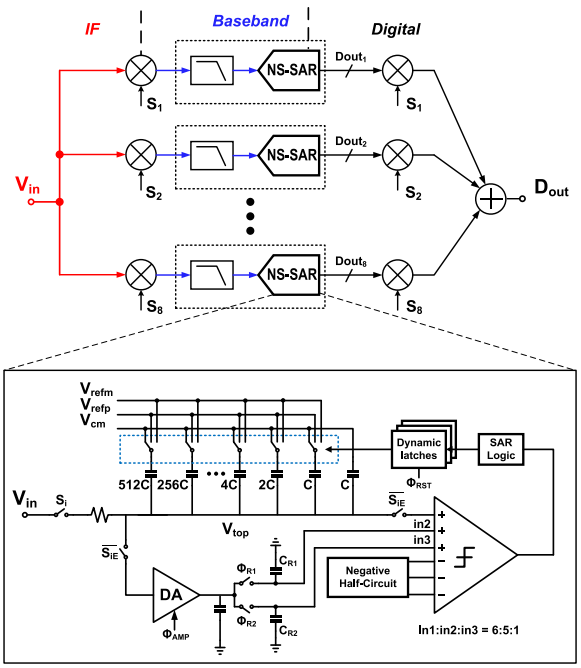

FIGURE 12. System overview of the N-paths filter TI NS-ADC in [17] (top), with its detailed NS-SAR Implementation (bottom).

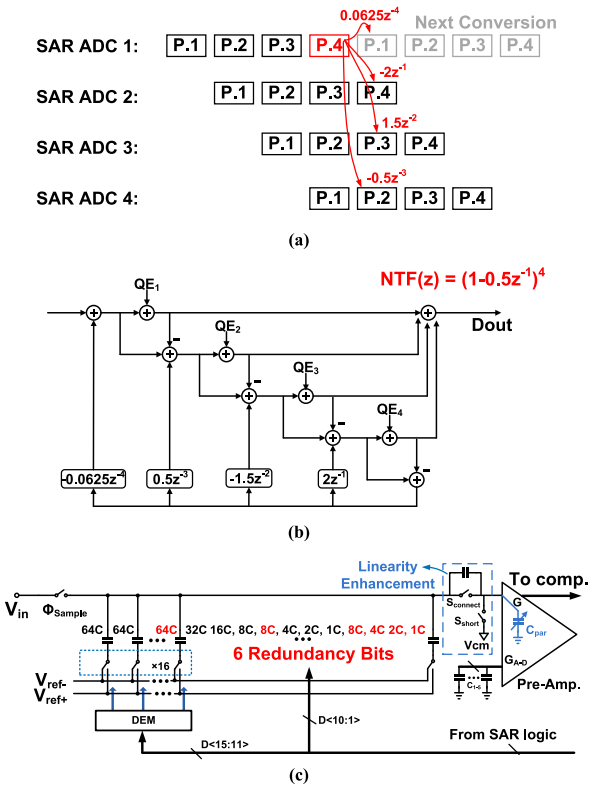

FIGURE 13. A 4-path cross-coupling TI NS-SAR proposed in [19] with its (a) timing sequence (b) signal flow chart model (c) and circuit details.

channel's output. Such traveling is impossible since the previous channels did not completely generate the outputs when the current channel begins to convert.

To realize the circuits in a causal way, [18], [19] proposed a multi-phase midway feedback TI NS-SAR. As SAR conversion naturally consists of multiple phases [48], the cross-coupled paths could be implemented during the conversion, making midway feedbacks. Fig. 13 (a) reveals the prototype's time sequence. During the whole conversion process, only one channel generates the error, with the

residue sent to other channels with scaled coefficients, therefore making a feasible analog routine. Finally, those feedback delays create a 'free' 4th order FIR loop filter. Fig. 13 (b) leads to an NTF as:

$$NTF = \left(1 - 0.5z^{-1}\right)^4. \tag{10}$$

The asynchronous SAR inside each channel, based on the error-feedback structure [49], has a unique charge redistribution CDAC. Fig. 13 (c) draws the pre-amplifier with a residue summation function. Such a pre-amplifier has multiple inputs for different channels, and its low gain requirement allows a single-stage open-loop structure. Yet, to prevent the overloading for the summation, the SAR has to arrange 6 redundant bits for 10b SAR core, which is the cost for combining cross-coupled feedback loops.

Looking back at the transfer function, Eq. (10) uses a coefficient of 0.5 since the resulted coefficients are easier implemented with the SAR conversion capacitance array. The NTF sets all zeros inside the unit circle in the z-plane. The benefit is, even with PVT variations, all shifted zeros will not exceed the unity circle, resulting in a stable NTF. On the contrary, this NTF is not aggressive enough to achieve higher SQNR without zero optimization. Hence, the final SNDR is only 70.4-dB with 50 MHz BW. The effective sample frequency reaches 400 MHz with an OSR equals to 4. Fabricated in 40nm CMOS technology and operated under 1V supply, this work consumes 13mW.

D. EXTRAPOLATING TI NS-ADC

To further avoid hardware redundancy, another attempted approach to generate TI NS-ADC is extrapolating, which was introduced in [50], [51]. This method is based on the NS-ADCs' inherent recursive operation. Specifically, we can write the integrator states in the time domain as a set of difference equations, establishing the relationship between samples. Thereby, the designer can explicitly use one channel's information to extrapolate the other channels. Like this, we can remove redundant analog blocks and possible delayed cross-paths, thus implementing the TI NS-ADC in a more straightforward and neat methodology.

Based on the extrapolating concept, a 4X TI NS-ADC was presented in [20], [21]. Fabricated in 28nm CMOS technology, each channel's clock is 520 MS/s, which leads to an equivalent sampling rate of 2.08GS/s. In NS-ADCs, the increased sampling frequency results in two possible directions: 1) increase the OSR but with a fixed BW or 2) increase the BW with a fixed OSR. This implementation is the latter case. Such ADC increased the effective output OSR from 52 to 208 with the BW fixed at 5MHz. The achieved peak SNDR is 86.1-dB. The ADC consumes a total of 23.1-mW with 1/1.15/1.5V power supplies.

Fig. 14 (a) illustrates the conventional analog extrapolating approach widely used in [52], [53]. The desired channels' outputs can be extrapolated by the input X, and integrator outputs P_1 and P_2. Though such extrapolation effectively

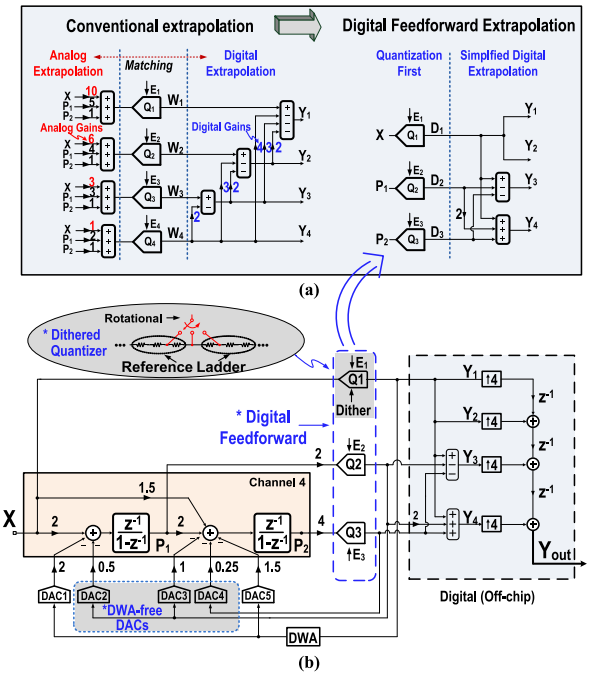

FIGURE 14. (a) Conventional/digital feedforward extrapolation comparison and (b) the system-level architecture of the extrapolating TI NS-ADC proposed in [21].

simplifies the whole scheme with single-channel hardware, the signal overloading phenomenon becomes serious. As the paths' number grows, the signal swings before the quantizers accumulate to an unbearable level. The situation becomes increasingly complicated for additional channels and higher-order cases.

The digital feedforward extrapolation in Fig. 14 (a) solves the problem by firstly digitizing the essential analog nodes' information (i.e., X, P_1, and P_2) from one channel and then fully extrapolating the other channels in the digital domain. This operation removes all burden analog adders and bypasses stringent matching requirements between the analog/digital extrapolating gains. As a trade-off, the quantization noise produced by the feedforward quantizers will also pass the same extrapolating process, thus increasing the final output error.

As a result, this 2nd order extrapolating TI NS-ADC only requires two op-amps to realize four TI paths, which significantly saves analog hardware and power overheads. Fig. 14 (b) presents the system-level architecture of the ADC. Meanwhile, a dithering circuit with rotational references is applied to the input sampling quantizer to reaching high linearity. There is a link between the dithering signal frequency and the channel's sampling frequency. Nevertheless, those high-frequency deterministic dither tones will be out of the interesting band and not affecting the in-band performance.

IV. CONCLUSION

High-resolution ADCs have primarily been achieved by Noise-shaping techniques. Table 1 presents a performance overview of published hybrid NS-ADCs. Among them,

TABLE 1. Performance summary of previously published works.

Architecture	Hybrid NS-ADCs for <MHz BW			Hybrid NS-ADCs for >MHz BW		
Reference	JSSC'21 [30]	JSSC'19 [13]	JSSC'19 [15]	ISSCC'21 [17]	JSSC'19 [19]	JSSC'21 [21]
Tech. (nm)	160	65	180	40	40	28
Supply (V)	1.8	1.2	3	1.2	1	1/1.15/1.5
Fs (MHz)	3.5	10.24	30	450	400	2080
BW (MHz)	0.02	0.02	0.1	3.5	50	5
OSR	87.5	256	150	64	4	208
SNDR (dB)	106.5	100.8	86.6	78.7	70.4	86.1
DR (dB)	109.8	101.8	91.5	79.8	71.7	90
Power(mW)	0.44	0.55	1.098	5.04	13	23.1
Area (mm2)	0.27	0.113	0.363	0.19	0.061	0.07
*FOM_S (dB)	183.1	176.4	171.1	167.1	166.3	169.5

$* FOM_S = SNDR + 10log10(BW/Power)$

I-ADCs rules the frontier of the state-of-the-art works near kHz frequency range. This paper summarized three hybrid I-ADCs: 1) The zoom I-ADC that can boost the SQNR by a quickly range-determined coarse SAR and an accurate fine I-ADC; 2) The linear-exponential I-ADC that combines the excellent thermal noise/linearity property of the first-order I-ADC and the faster accumulation property of the exponential I-ADC; 3) The sliced I-ADC that presents a dynamic power scheme which optimizes the most power-hungry first integrators.

For higher input frequency beyond MHz, this paper investigated three hybrid TI NS-ADCs to enhance the sampling frequency: 1) The N-path type TI NS-ADC that naturally builds a bandpass NTF; 2)The cross-coupling type TI NS-ADC that presents a new attempt to realize arbitrary NTFs; The drawbacks of the above TI NS-ADCs are more complicated hardware and layout, which consequently posed challenges in the circuit implementation; therefore 3) The extrapolating type TI NS-ADC resolves such dilemma by extrapolating the TI channels in the digital domain. Finally, those insights about the hybrid TI NS-ADCs open broader perspectives for the future research direction of high-resolution-oriented designs.

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Prof. Martins received the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016, and also the General Chair of the IEEE Asian Solid-State Circuits Conference in 2019. He was the Founding Chair of IEEE Macau Section from 2003 to 2005 and IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair IEEE Asia–Pacific Conference on CAS in 2008, the Vice-President (VP) Region 10 (Asia, Australia, and Pacific) from 2009 to 2011 and the VP-World Regional Activities and Membership of IEEE CASS from 2012 to 2013, an Associate-Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS from 2010 to 2013, was nominated as the Best Associate Editor from 2012 to 2013. He was also a member of: IEEE CASS Fellow Evaluation Committee (2013, 2014, and 2019–Member, 2018–Chair, 2021 and 2022–Vice-Chair); IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014; and IEEE CASS Nominations Committee in 2016 and 2017. He was the General Chair of ACM/IEEE Asia South Pacific Design Automation Conference in 2016. He was also the Vice-President (2005–2014) and the President (2014–2017) of the Association of Portuguese Speaking Universities, and received 2 Macao Government decorations: the Medal of Professional Merit (Portuguese-1999); and the Honorary Title of Value (Chinese-2001). In July 2010 was elected, unanimously, as the Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician working and living in Asia.