IEEE Open Journal of the
Solid-State Circuits Society

Received 1 July 2021; revised 10 September 2021; accepted 14 September 2021. Date of publication 28 September 2021; date of current version 22 October 2021.

Digital Object Identifier 10.1109/OJSSCS.2021.3116125

Low-Noise Readout Circuit for an Automotive MEMS Accelerometer

ALICE LANNIEL [1,2], TOBIAS BOESER[1], THOMAS ALPERT[1], AND MAURITS ORTMANNS [2] (Senior Member, IEEE)

(Invited Paper)

[1]Department of AE, Robert Bosch GmbH, 72762 Reutlingen, Germany

[2]Institute of Microelectronics, University of Ulm, 89081 Ulm, Germany

CORRESPONDING AUTHOR: A. LANNIEL (e-mail: alice.lanniel@de.bosch.com)

ABSTRACT This paper presents a charge-balanced readout circuit for MEMS capacitive accelerometers. The focus of this work is a design with a low-noise and low area consumption while ensuring the essential linearity and electromagnetic compatibility (EMC) for automotive applications. The readout circuit is composed of a charge-balanced single-ended input C/V stage followed by a second order sigma-delta modulator. The C/V stage uses a Gm stage combined with an integrator to reduce its noise contribution. The measurement results of the readout circuit show a noise floor of $62\,\mu g/\sqrt{\text{Hz}}$ and a temperature dependent offset smaller than ± 0.6 mg after compensation. The measured dynamic range of the complete interface, including readout circuit and sensor, is 95.5 dB. The measured EMC is below 2 mg. The accelerometer readout circuit has been designed in a 130 nm technology. Its power and area consumption is 1.4 mW and 0.26 mm^2.

INDEX TERMS Switched-capacitor circuit, MEMS accelerometer readout circuit, charged-balanced frontend, automotive applications.

I. INTRODUCTION

MICRO-ELECTROMECHANICAL (MEMS) accelerometers are employed in various applications especially in automotive, such as airbag or electronic stability control (ESP), as well as in consumer applications. They have several advantageous characteristics such as their small size or low power consumption. Fig. 1 shows an exemplary MEMS accelerometer with a human hair to highlight the small size of the sensor together with its simplified electrical model. There exists a continuous demand for high-performance and low-noise MEMS readout circuits for consumer as well as automotive applications. Furthermore, in safety critical automotive applications, the circuits may be exposed to harsh working conditions, as for instance high temperature range, electromagnetic interferences (EMI) or high vibrations.

Two main groups of readout architectures can be found in literature, which are closed-loop [1]–[3] and open-loop [4]–[6]. Closed-loop architectures employ a feedback force on the sensor to maintain the proof mass in its original position. This improves several characteristics of the sensor as for example dynamic range, linearity and bandwidth [7], [8]. On the other hand, open-loop architectures are smaller, less complex and consume less power such that they are usually used in consumer applications [9]. A particular case of open-loop architecture is the charge-balanced architecture [7]–[13] combining some advantages of closed- and open-loop designs. It has a higher linearity than open-loop and a reduced complexity compared to closed-loop architectures. Furthermore in the presence of high accelerations, the required feedback voltages in a charge-balanced architecture are smaller than in a closed-loop system [9].

The charge-balanced architectures presented in literature are based on the concept of Leuthold and Rudolf [10]. It ensures that the charges on both sensing capacitances are equal such that the net electrostatic force on the proof mass

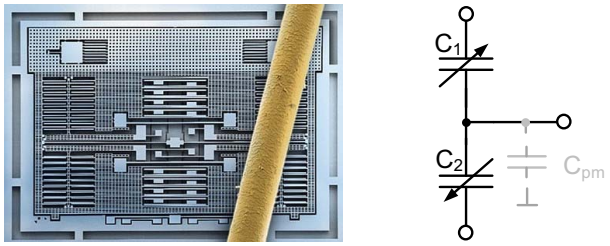

FIGURE 1. Exemplary MEMS accelerometer with human hair and simplified electrical model.

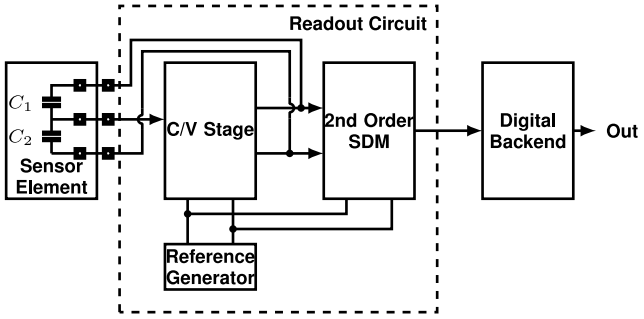

FIGURE 2. Block diagram of the analog frontend and the digital backend.

is zero. This is generally done by using a feedback voltage. A charge-balanced open-loop interface composed of a charge-sensitive amplifier and an integrator followed by a second-order sigma-delta modulator was presented in [7]. The output of the integrator was fed back to both sides of the capacitive bridge. Additionally to the open-loop interface an AC feedback, using a proportional-derivative controller, was implemented to reduce the high quality factor of the sensor. Furthermore, a positive feedback current was applied on the common-mode electrode to reduce the input limitations created by the parasitic capacitance of the sensor. The measurements presented in [7] show good noise performance and an input range of $\pm 1.5\,g$. Furthermore, [7] shows measurements of offset, non-linearity and gain performance over a temperature range from $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. Though, in automotive applications, the temperature requirement increases up to at least $125\,^{\circ}\mathrm{C}$ and the input range is generally significantly higher than $\pm 1.5\,g$. Another charge-balanced concept was presented in [8], where a sigma-delta modulator was used and the feedback was applied on both sides of the capacitive bridge and on the common-mode electrode. It was optimized regarding power consumption but at the cost of a low bandwidth of only 25 Hz. Another concept was introduced in [12], where the input and feedback paths were separated in order to improve the output power. The concept showed good SNDR versus power consumption performance in simulations. Nonetheless, the input range in this architecture was significantly lower than required for automotive applications and no information about the (measured) noise and linearity performance was provided. An additional concept achieving very low power consumption while limiting the noise contribution was shown in [13]. A feedforward noise reduction technique was used additionally to the conventional charge-balanced concept. A power consumption of 252 nW was achieved with a noise floor of $290\frac{\mu g}{\sqrt{\mathrm{Hz}}}$. However, the input range was limited to $\pm 5\,g$, which is lower than the one required for automotive applications and no temperature measurements were provided. Another concept focusing on low power consumption and reduced noise contribution was presented in [14]. This concept used a bandwidth-enhanced oversampling successive approximation readout technique to reduce the impact of the parasitic capacitance and thus to improve the noise performance as well as achieving a low power consumption. The input range was constrained to $\pm 8g$ and no measurements of offset or temperature performance were shown. Finally, [9] applied a feedback voltage in addition to the reference voltage on the sensing capacitances to ensure the charge balancing. This reduced the non-linearity created by the parasitic capacitance between the common-mode electrode and the substrate.

A similar concept is used in this work, but with a modified charge to voltage conversion stage (C/V stage) in order to reduce the area consumption and improve the noise performance. This is done to realize a low cost, robust, high dynamic range design for automotive applications. The targeted application in this work requires a dynamic range higher than 90 dB for a bandwidth near 100 Hz. This translates into a noise floor in the range of $100\frac{\mu g}{\sqrt{\mathrm{Hz}}}$. A high linearity and robustness against EMI as well as a temperature range from $-40\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$ must be maintained. Finally, an output range of $50\,g$ must be achieved to ensure that the mechanical clipping of the sensor appears before the electrical clipping of the readout circuit. The presented design fulfills such automotive requirements, which were only partly addressed in prior works.

This paper is organized as follows. Section II reviews the concept of the charge balanced architecture. Section III describes the proposed implementation of the frontend architecture and Section IV presents the corresponding measurement results. Section V concludes the paper.

II. CHARGE-BALANCED READOUT CIRCUIT WITH GM STAGE

The accelerometer readout circuit is composed of a C/V stage and a sigma-delta modulator (SDM), cf. Fig. 2.

The C/V stage consists of a single-ended input Gm stage, an integrator as well as a hold stage, see Fig. 3. A $\Delta C/C$ charge-balanced concept is used [10]. Thus, the biasing voltage V_{ref} is applied on both sides of the capacitive bridge of the sensor and the signal is provided on the common-mode electrode.

As in [9], the charge-balancing is ensured by the C/V stage. The sensor is embedded in a negative feedback loop, where the feedback voltage provided by the C/V stage is dynamically adjusted such that in a steady state no charge flows on the common-mode electrode. Additionally, the feedback voltage is applied on the common-mode electrode such that no force is applied onto the proof mass.

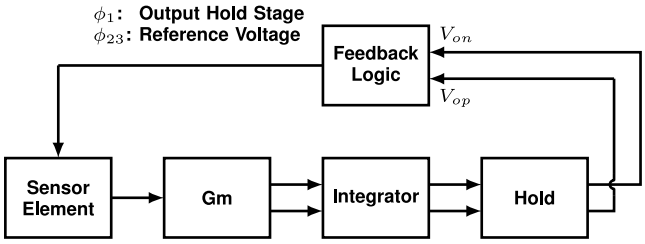

FIGURE 3. Blockdiagram of the C/V stage.

The integrator in the C/V stage provides high gain. The summing amplifiers of [9] are replaced by a hold stage to save area. The latter samples the output of the integrator and holds the relevant signal to provide it back to the sensor and the sigma-delta modulator in the desired phases.

Unlike [9], a Gm stage is used in front of the integrator to reduce the noise contribution of the C/V stage. This firstly provides additional gain such that all the noise contributions of the following stages are relaxed. Then in combination with the integrator, the boxcar sampler principle is used [15], [16]. The latter is equivalent to a sinc filter with the first notch at $\frac{1}{T_{int}}$, where T_{int} is the integration time, hence reducing the aliasing of noise [15]. The Gm stage combined with the integrator reduces the noise of the switches sampled on the sensor capacitances and relaxes the impact of the parasitic capacitance C_{pm} between the common-mode electrode and the substrate. Without the Gm stage the sensor parameters impact the integrator stage, degrading its feedback factor, so that its noise contribution is increased. With the Gm stage they only influence the first stage, where their impact is smaller. Additionally, the selection of the circuit parameters becomes more flexible when using the Gm stage to reach the required noise and stability. A noise improvement of about 32% is achieved thanks to the additional Gm stage placed in front of the integrator. Detailed analysis of the noise improvements obtained with the Gm stage in front of the integrator was previously presented in [16]. Even though the C/V stage concept is not identical to the prior work, the major advantages provided by adding the Gm stage, as described above, are still valid for this work.

Furthermore, the Gm stage combined with the integrator also allows to reduce the impact of EMI, since an additional attenuation is provided.

The power consumption increases with the additional stage. However, the sampling frequency, which is necessary to meet the noise requirements including the Gm stage, is lower than without the Gm stage. Hence, the additional stage effectively reduces the power consumption. In detail, when considering only an increase in the sampling frequency to obtain the same noise contribution as with the Gm stage, the power consumption would increase by a factor of 1.89.

The transconductance of the Gm stage is sensitive to process and temperature variations. However, the parameters of the circuit were selected such that a variation of 10% of the transconductance is allowed. This is obtained by using

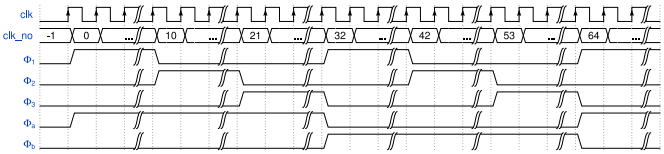

FIGURE 4. Clock diagram of the C/V stage.

a PTAT current source, which is trimmed depending on the process. The transconductance impacts the noise and stability performances, but it does not impact the output voltage of the C/V stage at DC, which can be derived as

$$V_o = V_{ref} \cdot \frac{(C_1 - C_2)}{C_1 + C_2}. \tag{1}$$

Therefore, even though the circuit may be more sensitive to PVT with the Gm stage, its impact, which is reduced by design, is not critical for the concept.

The bandwidth is not limited by the Gm stage. The transconductance of the Gm stage is selected according to noise specification, which results in a higher bandwidth than required. However, as mentioned previously, without the Gm stage the sensor would be directly connected to the integrator, which would decrease its feedback factor. Thus, its noise contribution would be higher and the bandwidth would need to be designed larger to ensure the settling of this stage.

The gain of the forward path of the C/V stage is defined by the ratio between the transconductance of the Gm stage, the integrating capacitance and the integration time, leaving some flexibility in the parameter selection. The gain requirements of the Gm stage are much lower than for the integrator stage and hence its gain is significantly lower.

Finally, the Gm stage enables to have a single-ended input, with a fully-differential integrator, hold stage and sigma-delta modulator. Thus, the noise contribution is reduced compared to a pseudo-differential architecture, while keeping the advantages of a fully-differential architecture.

III. FRONTEND IMPLEMENTATION

A. C/V STAGE

A more detailed circuit-level block diagram of the implemented C/V stage is given in Fig. 5. The readout circuit uses three non-overlapping phases at a clock frequency f_S. The clock diagram is shown in Fig. 4. The clock provided by the oscillator is divided into 32 cycles. ϕ_2 and ϕ_3 are equal and hence equivalent to 11 clock cycles while ϕ_1 is only 10 cycles.

In ϕ_1 the feedback voltage, $V_{op,n}$, is applied at the end of the capacitive bridge of the sensor and the common-mode electrode. The Gm stage and the integrator perform offset cancellation during this phase: auto-zeroing in the case of the Gm stage and correlated double sampling (CDS) in the case of the integrator. In opposite to [9] the unity feedback used for the offset cancellation of the integrator performed in ϕ_1 is replaced by a feedback including C_{xx}. In this configuration the offset is canceled by CDS using the sampling capacitance C_{off}. Thanks to C_{xx} the variations at

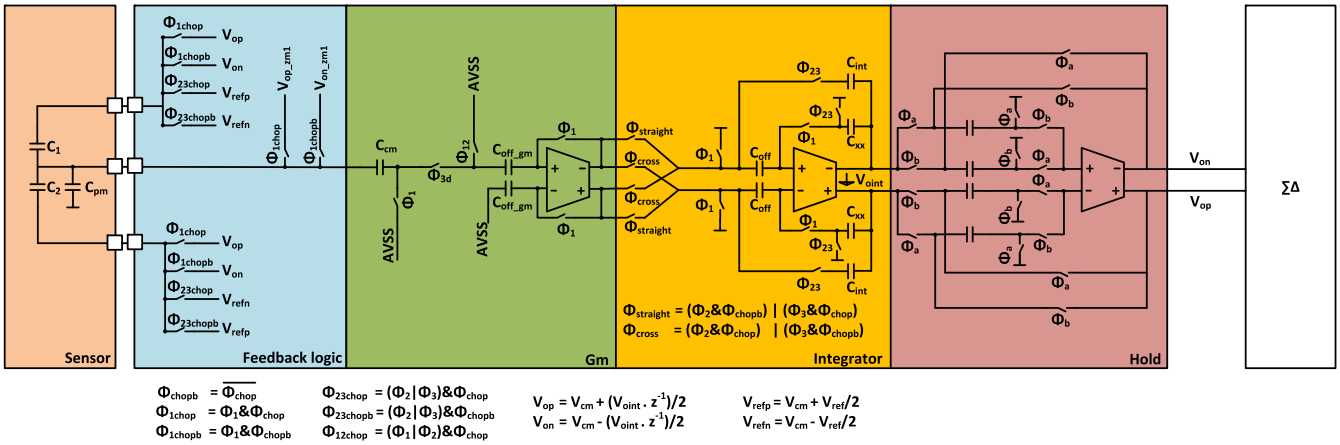

FIGURE 5. Schematic of the frontend including sensor, C/V stage and sigma-delta modulator.

the output of the integrator are minimized, which improves the settling behavior leading to an improved accuracy and linearity performance.

In ϕ_2 and ϕ_3 the reference voltage V_{ref} is applied on the sensor creating a charge transfer equivalent to the acceleration. ϕ_2 is used to cancel the residual offset of the Gm stage as well as $\frac{k \cdot T}{C}$ noise sampled on the capacitance $C_{off_{gm}}$, while ϕ_3 is the phase where the acceleration signal is passed through the C/V stage. Hence, the sensor is connected to the Gm stage only in ϕ_3, while in ϕ_2 the input of the Gm stage is connected to ground.

The switches at the output of the Gm stage, $\phi_{straight}$ and ϕ_{cross}, are connected such that the output signal of the Gm stage is integrated with opposite sign in ϕ_2 and ϕ_3. This way, the residual offset and the $\frac{k \cdot T}{C}$ noise, which are sampled on the input capacitance of the Gm stage $C_{off_{gm}}$, are integrated in one direction in ϕ_2, while in ϕ_3 they are integrated in the opposite direction in addition to the acceleration signal. Hence these non-idealities are effectively canceled out.

The output of the integrator is then provided to a hold stage. In contrast to prior art using a sample and hold stage [17], [18], the hold stage in this work continuously samples the output of the integrator and holds the relevant integrator signal of ϕ_3 to transfer it to the sensor and to the sigma-delta modulator in ϕ_1. Therefore, ϕ_a and ϕ_b are reversed signals holding each for three phases. This clocking scheme reduces the settling requirements of the OTA and hence improves the accuracy and reduces the power consumption. Non-idealities of the OTA, as offset or $\frac{1}{f}$ noise, are reduced by chopping and the gain of the C/V loop.

In the presented frontend, a random chopping scheme is used. While a periodic chopping is efficient to cancel out low frequency disturbers, as flicker noise or offset, it is insufficient for EMI robustness, since interferences appearing near the chopping frequency are sampled back to DC [9]. EMI couples capacitively through the bondwire connecting the sensor and the frontend. When using random chopping, the interference is spectrally spread, which significantly reduces the impact of EMI close to DC [9]. The random chopping consists of a pseudo-noise sequence, which is spectrally attenuated at DC and $\frac{f_S}{2}$ in order to minimize the power in the baseband and the coupling of high frequency tones to the reference voltage [19].

The chopper is realized at the output of the Gm stage and at the output of the hold stage. Therefore, $\phi_{straight}$ and ϕ_{cross} are not only dependent on the two phases $\phi_{2,3}$ but also on the chopper state (ϕ_{chop}). The positive output of the hold stage is fed back to the sensor in one chopping phase $\phi_{1_{chop}}$ and the negative output in the next chopping phase. Delayed phases are used where necessary to reduce the impact of charge injection.

B. NOISE OF THE C/V STAGE

The transconductance of the Gm stage and the capacitance C_{int} are set according to noise, stability and area requirements. The noise contribution of the C/V stage is minimized by increasing the transconductance of the Gm stage, since the overall gain is increased. Disadvantageously, an increase of the transconductance leads to instability of the C/V stage since the gain is increased. This needs to be compensated by an increase of C_{int} resulting in the same gain, but less area efficiency. With the noise requirement being smaller than $100 \frac{\mu g}{\sqrt{\text{Hz}}}$, the Gm stage combined with the integrator have a gain of 4, while the hold stage has a gain of 1.

Thermal noise is the dominant noise source of the C/V stage. While Flicker noise also has an impact, it is reduced by chopping. The noise of the C/V stage is a combination of the noise generated from the OTAs and the switches of each stage. These noises are uncorrelated and therefore they can be determined individually [20]. The noise power of each component in each phase is calculated, referred to the output of the C/V stage and eventually added up to obtain the noise of the complete C/V stage. Hence, the individual noise sources are shaped by the loop gain of the C/V stage. The total noise power of the C/V stage is then:

$$N_{cv} = \left(\frac{N_{sw} \cdot z^{-2} \cdot G_{intgm}}{-z^2 + 2 \cdot z^{-1} - 1 + z^{-2} \cdot G_{cv}^2} \right)$$

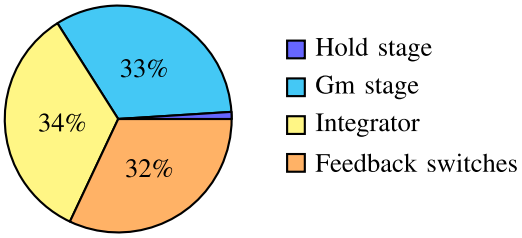

FIGURE 6. Noise contribution of each stage at DC.

$$+\left(\frac{N_{gm}\cdot G_{int}\cdot z^{-2}}{-z^2+2\cdot z^{-1}-1+z^{-2}\cdot G_{cv}^2}\right)+\left(\frac{N_{int}\cdot z^{-2}}{-z^2+2\cdot z^{-1}-1+z^{-2}\cdot G_{cv}^2}\right)+\left(\frac{N_{hs}\cdot\left(z^{-2}-z^{-1}+1\right)}{-z^2+2\cdot z^{-1}-1+z^{-2}\cdot G_{cv}^2}\right) \quad (2)$$

where N_{sw}, N_{gm}, N_{int} and N_{hs} are the output referred noise contributions of the individual stages, e.g.: feedback switches, Gm stage, integrator stage and hold stage. G_{cv} is the overall gain of the C/V stage, G_{int} is the gain of the integrator and G_{intgm} is the gain of the Gm stage combined with the integrator.

The noise contribution of the C/V stage is generated by the integrator, the Gm stage and the noise of the switches sampled on the sensor capacitances. While the latter is box-car sampled in ϕ_2 and ϕ_3, it has a significant impact in ϕ_1. The noise of the hold stage is significantly reduced by the loop gain of the C/V stage such that it is negligible in the signal bandwidth. The noise of the Gm stage is significantly impacted by the noise contribution of the switches at its input. Since the OTA of this stage does not have high gain and bandwidth requirements, its design can be optimized according to noise performance. For the OTA of the integrator stage, the noise performance is also dictated by the feedback factor and the trade-off between gain, bandwidth, area, power consumption, noise and stability of the C/V stage. The noise distribution at DC (i.e., z = 1) between the stages of the C/V stage is illustrated in Fig. 6.

C. SIGMA-DELTA MODULATOR

The sigma-delta modulator connected to the hold stage is a single-bit second-order chain of integrator with feedforward compensation (CIFF). The coefficients were determined with the sigma-delta toolbox in MATLAB and adapted according to the required input range and output swing of the OTAs. The sigma-delta modulator was designed to provide a SNR of at least 100 dB. The sampling frequency is selected to 800 kHz yielding an OSR = 400, which allows a SNR = 118 dB. The noise contribution of the sigma-delta modulator is chosen such that it is more than two times lower than the one of the C/V stage. Note that the Nyquist rate of the sigma-delta modulator is about 10x larger than the specified signal inband of the overall sensor frontend. Even though the inband is specified to 86 Hz in this work, the overall C/V stage including the sigma-delta modulator has to allow a bandwidth of at least 1 kHz to avoid any vibration induced offset fed back to the sensor. This effectively makes the whole frontend being designed for and working with a 1kHz bandwidth instead of the needed signal bandwidth of 86Hz, while digital postfiltering is used to reduce the digital output to the required signal.

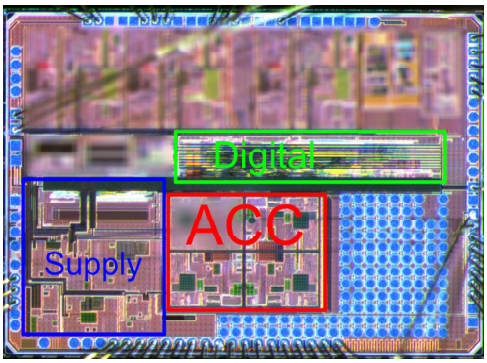

FIGURE 7. Die micrograph.

D. REFERENCE VOLTAGE

The same reference voltage is used for the C/V stage and the sigma-delta modulator to provide ratiometric operation. Hence, the impact of disturbances on the reference voltage is reduced [9]. Regarding signal-to-noise ratio it is beneficial to increase the reference voltage since the signal at the output of the C/V stage is equivalent to equation (1). However, V_{ref} is limited by the pull-in incidence linked with the mechanical behavior of the sensor [21].

IV. MEASUREMENT RESULTS

The capacitive MEMS readout circuit has been implemented in a 130 nm CMOS technology and the fabricated chip is shown in Fig. 7. The supply block generates the supply voltage of 2.8 V for the readout circuit as well as the reference voltage of 1.74 V. The latter is buffered, including offset cancellation, and used in the readout circuit. A digital backend processes the output of the sigma-delta modulator and provides a communication interface through SPI. The backend circuit includes among others a third-order decimation filter followed by a low-pass filter for bandwidth reduction to the required inband frequency of 86 Hz. The digital backend circuit additionally provides the clock signals, which are then refined in the readout circuit to generate the non-overlapping clocks.

The indicated accelerometer (ACC) block corresponds to the readout circuit, which includes the C/V stage, the sigma-delta modulator, the reference buffer and the non-overlapping clock generator. The simulated power consumption of the readout circuit is 1.4 mW and its area is 0.26 mm^2. Since the circuit is also composed of other blocks, it is not possible to

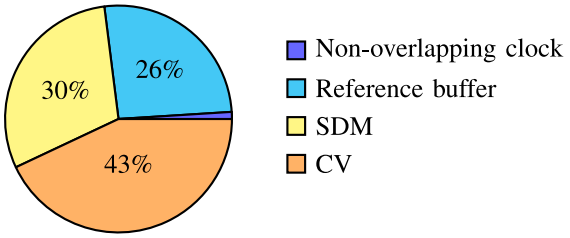

FIGURE 8. Power consumption of each stage.

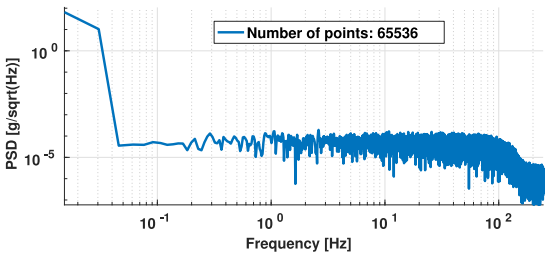

FIGURE 9. Noise power spectral density at output of third-order low pass filter with a corner frequency of 86 Hz.

measure the power consumption of only the readout circuit. The power share of each stage is shown in Fig. 8.

The following measurements are carried-out at the SPI interface and thus at the output of the filters. The measurement results are converted from LSB_{ADC} into acceleration in g by dividing them by the various gains in the digital signal processing path. The converted output will be called filtered output of the sigma-delta modulator in the following.

A. MEASUREMENTS WITHOUT SENSOR

First the noise of the readout circuit is evaluated without sensor at the worst case temperature of 150°C. The temperature was applied with a thermal air stream system. A MATLAB generated power spectral density plot of the filtered output of the sigma-delta ADC is illustrated in Fig. 9. The measurements are sampled with 500 Hz at the output of the third-order low-pass filter with a corner frequency of 86 Hz following the decimation filter (cf. Section III-C). The resulting measured noise density in the baseband is $62\frac{\mu g}{\sqrt{\text{Hz}}}$. With the signal bandwidth being 86 Hz, the minimum detectable signal is $616.6\,\mu g$ accounting for a factor of 1.15 for the effective bandwidth of the third-order digital low-pass filter.

As the undecimated bitstream of the sigma-delta modulator was made available for test, its corresponding power spectral density plot can be shown in Fig. 10. The about 10x larger inband (cf. Section III-C) is clearly seen. The noise density of $61\frac{\mu g}{\sqrt{\text{Hz}}}$ is insignificantly smaller as in Fig. 9 but maintained up to 1 kHz. The inband noise is slightly worsened by the decimation and low pass filters and the corresponding down folding in decimation.

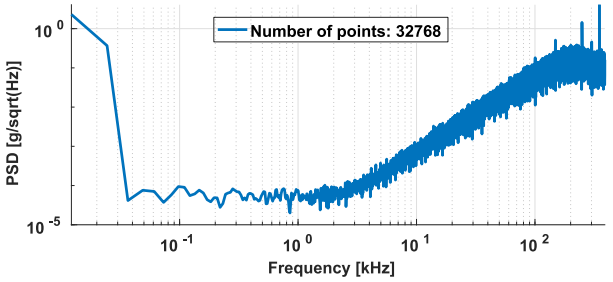

FIGURE 10. Power spectral density of the bitstream at the output of the single-bit sigma-delta modulator.

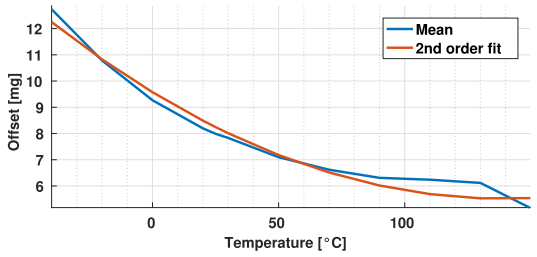

FIGURE 11. Mean offset of the readout circuit and second-order polynomial fit.

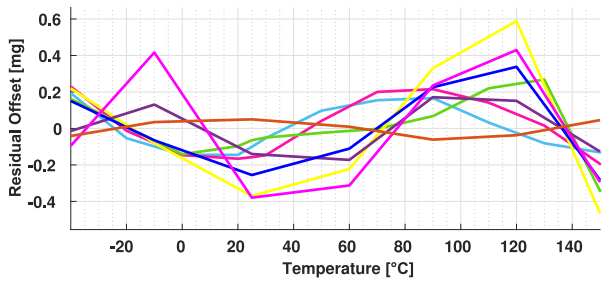

FIGURE 12. Residual offset of the readout circuit after second-order polynomial fit correction.

Next, the offset of the readout circuit is analyzed without sensor. Fig. 11 shows the mean value of the offset over temperature in the interval from −40 °C to 150 °C measured for one exemplary device. The measurements were done every 20 °C. Additionally, a second-order fit of the measurements is added in Fig. 11 to show the correlation between them. Fig. 11 shows that the offset is highly dependent on the temperature, which can be significantly improved with a temperature compensation using the second-order polynomial fit. The residual offset of such temperature compensation is illustrated in Fig. 12 for 8 devices. It shows that the residual offset is smaller than $\pm 0.59\,mg$ for those samples, which is in the same range of the minimum detectable signal. The temperature compensation is implemented in a DSP.

B. MEASUREMENTS WITH SENSOR

Next, the readout circuit with a MEMS capacitive accelerometer is measured on a centrifuge. High-precision centrifuges capable of high centripetal acceleration are used. The centrifuge puts the ASIC with the sensor in rotation around a fixed axis. Hence, it applies a centripetal acceleration perpendicular to the rotational axis to the chip. The

TABLE 1. Summary of the measurement results and comparison with previously published works using MEMS capacitive accelerometers.

Parameters	This work	[9]	[7]	[1]	[22]	[8]	[23]	[3]	[2]	[13]	[14]
Technology (CMOS)	130 nm	180 nm	350 nm	180 nm	350 nm	250 nm	500 nm	350 nm	500 nm	180 nm	180 nm BCD
Supply [V]	2.8	1.9	3.6	3	3.3	2.5	5	3.3	7	1	1.8
Temperature range [°C]	-40 - 150	-40 - 150	-40 - 85	/	/	-30 - 85	/	/	-40 - 85	/	/
Noise Density $[\mu g/\sqrt{Hz}]$	84	380	2	220	54	340	80	6.2	0.2	290	900
Output Range $[g]$	50	45	1.4	9.14	2	4	2	20 (24)	1.2	5	8
Bandwidth [Hz]	86	50	200	1000 (usable:200)	500	25	/	250	300	50	10k
Dynamic Range [dB]	95.5	84.4	93.9	69.4	64.4	67.43	/	108	111	67.7	39
Power [mW]	1.4[1]	1.1[2]	3.6[3]	3.1[4]	2.57[5]	0.24[6]	40[7]	16.7[7]	23[8]	0.25e-3[9]	0.47[10]
Area [mm^2]	0.26[1]	1.1[2]	6.66[3]	1.35[4]	2.8[5]	0.45[11]	17.2[7]	5.5[7]	7.8[8]	1.45[9]	0.56[10]
Nonlinearity [%]	0.05	0.33 [12]	0.27	/	1.28	0.35	0.2	0.2	0.15	<1	0.5
EMC $[mg]$	< 2	< 3	/	/	/	/	/	/	/	/	/

1 includes one readout interface: C/V stage, sigma-delta modulator, non-overlapping clock and reference buffer. Noise floor maintained up to 1kHz analog bandwidth. Signal bandwidth limitation digitally generated.
2 includes two-axis readout interface: C/V stage, sigma-delta ADC, clock, reference generator, LDO, bandgaps, bias currents, self-test circuit
3 includes one readout interface: analog interface, analog buffer, sigma-delta ADC, bit register, DSP, voltage regulator, clock generator
4 includes one readout interface: C/V stage, time-multiplexer, integrator, compensator, quantizer and clock generator, area provided corresponds to active area
5 includes one sensor and one readout interface: 5-bit offset trimming, differential amplifier, oscillator, modulation generator, 3-bit gain control amplifier and a low-pass filter
6 includes one readout interface: sigma-delta modulator, decimator, clock, LDOs, reference voltage buffers, voltage/current/frequency reference generators
7 includes one readout interface: fourth order sigma-delta interface
8 includes one readout interface: fifth order sigma-delta interface
9 includes one readout interface: C/V stage, SAR ADC, voltage/current reference circuit, bias, clock generator, finite state machine, register, SPI interface. For the power consumption IOs are excluded
10 includes one readout interface: C/V stage, clock generator, calibration circuits, buffers, voltage and current references
11 includes a second-order sigma-delta modulator
12 calculated based on reported plot

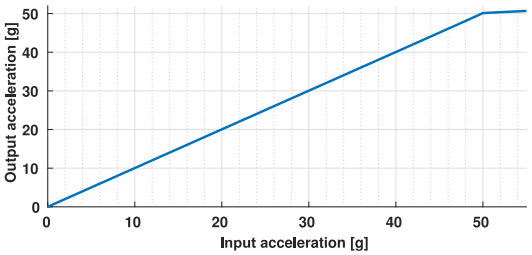

FIGURE 13. Output acceleration versus input acceleration.

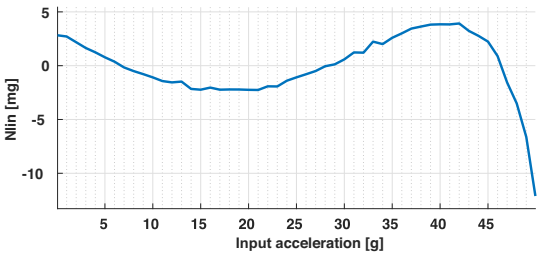

FIGURE 14. Non-linearity of the frontend.

acceleration is defined by the rotation speed and the arm length. The centrifuge provides a constant rotation. Fig. 13 illustrates the filtered output of the sigma-delta modulator for various accelerations. It shows that the mechanical clipping appears near $50\,g$. The noise of the frontend including the exemplary sensor and the readout circuit is $84\,\frac{\mu g}{\sqrt{\text{Hz}}}$ equivalent to a minimum detectable signal of $835.4\,\mu g$. Hence the equivalent dynamic range is 95.5 dB. Fig. 14 visualizes the measured static non-linearity of the frontend over an input range between $0\,g$ and $50\,g$. The non-linearity increases significantly for an input higher than $45g$ due to

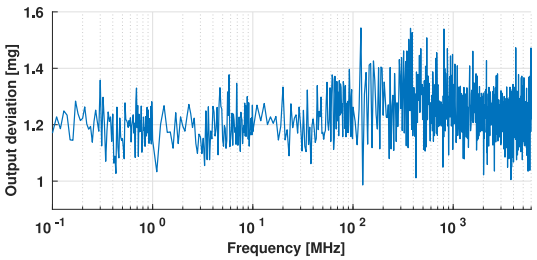

FIGURE 15. EMC performance.

the MEMS. The maximum non-linearity determined from the measurements over the complete input range is 0.05 %.

Finally the EMC performance was analyzed with an IC-stripline. Several electric field amplitudes and frequencies were applied. The measurements were carried-out on the filtered output of the sigma-delta ADC for various frequency ranges. Fig. 15 shows the standard deviation of the measurements for an interference frequency range from 100 kHz up to 6 GHz. From 100 kHz up to 800 MHz a CW electric field of $800\,\text{Vm}^{-1}$ is applied, while from 800 MHz up to 6 GHz a CW electric field of 1200Vm^{-1} is used. Fig. 15 shows that up to 10 MHz the disturbance is small thanks to the shielding provided by the package. Additionally, the use of random chopping enables to remove high peak errors induced by the EMI. Hence, the EMI is rather distributed over the bandwidth such that the output results in an envelope shaped response, which is below $2\,mg$ rms.

C. COMPARISON TO THE STATE OF THE ART

Table 1 shows a comparison between the measured performance of the presented readout circuit and previously

published works using MEMS capacitive accelerometers, whereas oscillating MEMS accelerometers are not considered. The presented work has a very competitive input sensing range, up to 50 g and the best linearity performance. The noise was measured at 150 °C, which corresponds to the worst case scenario, but even operated at that temperature it is competitive to the state of the art. In the presented design, about half of the total noise is contributed by the readout circuit and the other half by the sensor element. A very good noise performance is also reported in [2], [3] and [7], but with a much lower output range, an increased power and area consumption compared to the presented design. In Table 1, the power and area consumption reported for the presented design includes the C/V stage, the sigma-delta modulator, the reference buffer and the non-overlapping clock generation. It does not take into account the supply generation and the backend circuit. A very low power consumption is shown in [8], [13], [14] at the cost of an increased noise contribution and again much lower output range and dynamic range compared to this work. In Table 1 the dynamic range was calculated based on the provided noise density, output range and bandwidth. EMC was not reported in most of the published works shown in Table 1 and if the temperature range was reported it generally goes only up to 85°C. Though, the shown higher temperature range and the EMC performance are typical automotive requirements. Even though the signal bandwidth is digitally limited to 86Hz, the analog bandwidth of the whole frontend including the sigma-delta converter is 1kHz, which together with the noise floor and power consumption is competitive in the state of the art.

The measurement results show that the presented frontend meets the original requirements of an automotive MEMS readout circuit and is still very competitive to other works. It is designed for robustness and shows performance over temperature and against EMI. A specific focus was placed on the automotive requirements, regarding linearity, offset stability and EMC while limiting the noise contribution and the area consumption.

V. CONCLUSION

This work presented a charge-balanced $\Delta C/C$ frontend for accelerometers in automotive applications. The combination of the Gm stage and the integrator in the C/V stage enables an improved noise and EMC performance. The concept details were presented and its performance was verified with measurements on silicon. These results showed good performance regarding linearity, offset, EMC and noise.

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ALICE LANNIEL received the M.S. degree in electrical engineering from the University of Chemistry, Physics and Electronics, Lyon, France, in 2016. She is currently pursuing the Ph.D. degree with Robert Bosch GmbH, Reutlingen, Germany, in cooperation with the University of Ulm, Ulm, Germany. Her focus is on low-noise readout circuits for MEMS accelerometers in automotive applications. Her research interests include MEMS accelerometers, frontends, and IC design.

TOBIAS BOESER received the Dipl.-Ing. degree in electrical engineering from the University Karlsruhe, Karlsruhe, Germany. In 2009, he joined Robert Bosch GmbH, Reutlingen, Germany, where he studied the robustness of capacitive acceleration frontends for MEMS acceleration sensors. Since 2012, he has been investigating, developing, and characterizing new concepts for automotive acceleration sensor readout circuits on system level and analog design.

THOMAS ALPERT received the Dipl.-Ing. and Dr.-Ing. degrees from the University of Stuttgart, Stuttgart, Germany, in 2008 and 2013, respectively. During his doctoral study, his research was focused on high-speed digital-to-analog and analog-to-digital converters in CMOS technology for optical communication applications. Since 2012, he has been a Research and Development Engineer with Robert Bosch GmbH, Reutlingen, Germany. He is working in the field of inertial sensor system architecture and circuit design.

MAURITS ORTMANNS (Senior Member, IEEE) received the Dipl.-Ing. degree in electrical engineering from Saarland University, Saarbruecken, Germany, and the Dr.-Ing. degree from IMTEK, University of Freiburg, Freiburg, Germany, in 1999 and 2004, respectively. Since 2008, he has been a Full Professor and the Director of the Institute of Microelectronics, University of Ulm, Ulm, Germany. He holds several patents, has coauthored the book *Continuous-Time Sigma-Delta A/D Conversion*, and published more than 180 IEEE journal and conference papers. His research interests include mixed-signal integrated circuit design, self-correcting and reconfigurable analog circuits, with special emphasis on data converters and biomedical applications.