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Harmonic Oscillators in CMOS—A Tutorial Overview

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(Invited Paper)

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ABSTRACT The harmonic oscillator is a truly irreplaceable as well as ubiquitous analog integrated circuit. Starting from the basics of its CMOS implementation, we will discuss the phase noise of the harmonic oscillator in some detail, where the intrinsic large-signal operation mandates a time-variant analysis. This will be followed by a survey of the most popular design techniques enabling a low phase noise and a wide range of oscillation frequencies.

INDEX TERMS Oscillator, harmonic, phase noise, tuning range, CMOS.

I. INTRODUCTION

AS ONE of the very few areas of analog electronics still withstanding the irresistible onslaught of its digital nemesis, frequency generation keeps attracting the interest of beginners and specialists alike, oscillators being especially fascinating for their ability to create time-varying periodic signals out of a constant power supply; and while it is not difficult to generate an oscillation, at least at low enough frequencies, ensuring its high quality in the presence of several conflicting constraints (low power supply, limited power consumption, frequency tunable over a wide range, compliance with digital CMOS processes, etc.) is a never-ending challenge, which, despite valiant attempts to enlist digital-friendly ring oscillators in the struggle [1], [2], is made somewhat less daunting only by turning to harmonic oscillators — i.e., oscillators based on inductor(s) and capacitor(s) — whenever a good frequency purity at a reasonable power consumption is desired.

Of paramount importance in this context is the oscillator phase noise, which modulates the phase of the oscillation (the *carrier* in radio communication parlance) through the action of various thermal and possibly $1/f$ noise sources. Phase noise easily becomes the performance bottleneck in any application making use of an oscillator. In a communication system, phase noise is transferred onto the information signal during frequency modulation/demodulation, deteriorating the signal-to-noise ratio (SNR). Similarly, phase noise impairs the received signal in a carrier-based radar system. In communication systems, phase noise is also responsible for the so-called reciprocal mixing in the receiver: if an undesired signal (referred to as an interferer) is located at a frequency offset $\Delta\omega$ from the desired signal, phase noise at $\Delta\omega$ from the carrier translates the interferer to the frequency of the desired signal, again causing an SNR deterioration. If transmitter and receiver are active at the same time, the receiver SNR is also affected by the phase noise in the transmitter oscillator mixing with the transmitted signal. In sampled data systems, such as data converters and discrete-time filters, phase noise on the sampling clock (more commonly referred to as jitter) is critical, as it introduces a sampling error that increases with the bandwidth of the sampled signal.

It is therefore clear that oscillator design quickly becomes a quest for a sufficiently low phase noise.

The literature on harmonic oscillators is vast, which forces us to limit the scope of this survey to implementations in CMOS — their bipolar counterparts would be very similar, with however two major differences: bipolar transistors cannot be allowed to enter saturation, and the lack of a natural switch in purely bipolar processes severely complicates frequency tuning (Section V). Furthermore, we will not take up the specific problems encountered in the design of mm-wave oscillators, where the resonator is made of distributed rather than lumped components. Likewise, we will not treat oscillators delivering more than one signal or two differential signals, and we will deal only with the most popular

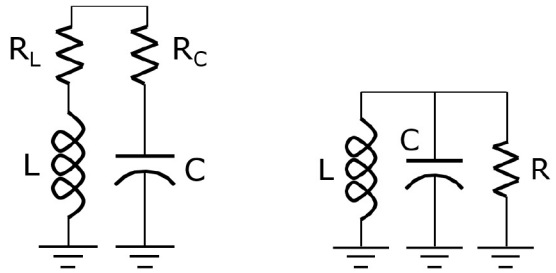

FIGURE 1. Lossy LC resonator and its equivalent shunt model.

oscillator architectures, fascinating as more exotic architectures may be. Finally, we will mainly consider applications to wireless systems, although most of the discussion applies in general.

II. FUNDAMENTALS

The simplest harmonic oscillator is built around a resonator made of one inductor (L) in parallel with one capacitor (C), as in Fig. 1: a combination often referred to as an LC tank, as it acts as a reservoir of energy. The resonance of the LC tank occurs at an angular frequency $\omega_0 = 1/\sqrt{LC}$, where the two impedances cancel each other.

In general, both L and C have losses, exemplified by the series resistances in Fig. 1; if these are not large compared to the impedance of L (or C, equivalently) at resonance, ω_0 is largely unaffected by them. In the vicinity of ω_0, all losses are conveniently compacted into a single equivalent parallel resistance R, as in Fig. 1 (it should be noted though that this is not correct if the parallel coupling of L and C is not maintained across the whole oscillation period $T_0 = 2\pi/\omega_0$, as in, e.g., class-D oscillators [3]). Thus, at resonance the impedance of the lossy LC tank is simply R, which tends to infinity as the tank becomes more ideal. A measure of the quality of the tank is its quality factor Q, defined as $R/(\omega_0 L)$ or $R\omega_0 C$.

To create a harmonic oscillator, we need a transconductor acting as an active negative resistance replenishing the losses caused by R. Since it is placed in parallel to R, this negative resistance must have an absolute value lower than R, or equivalently a conductance higher than $1/R$ to make the circuit unstable. An elegant implementation of a negative resistance was invented by E. Colpitts in 1918 [4]–[6]: Fig. 2 shows a simplified view of a singled-ended common-gate Colpitts oscillator, where only one active device is needed, as the current source may be a simple resistor (as a matter of fact, R. Hartley had already invented the eponymous oscillator in 1915 [7], where C and L swap places compared to its Colpitts counterpart).

The positive feedback from nMOS drain to source, which yields the sought negative resistance, is implemented with the tapped capacitor C_1-C_2. Once the values of the passive components are given, we can determine the minimum values of the nMOS transconductance g_m needed to start the oscillation by breaking the loop at a suitable node, e.g.,

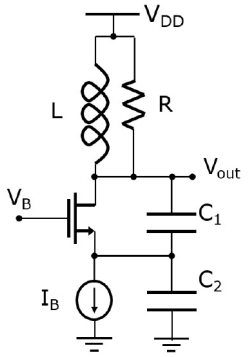

FIGURE 2. Simplified schematic view of a Colpitts oscillator.

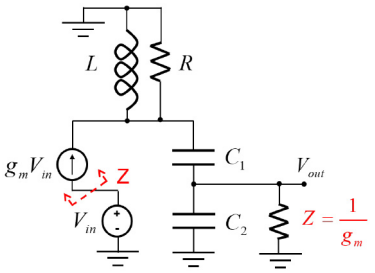

FIGURE 3. Small-signal equivalent circuit for the Colpitts oscillator in Fig. 2.

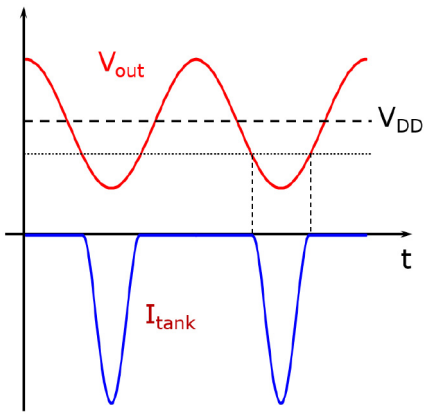

FIGURE 4. Voltage and current waveforms for the Colpitts oscillator in Fig. 2.

the nMOS source, and applying standard circuit analysis to the linearized small-signal circuit, as shown in Fig. 3, where the loop output must be loaded with the impedance seen looking into the loop input, i.e., $1/g_m$ (very suitably, we have assumed an infinitely high output resistance for the nMOS transistor). Barkhausen's criterion for the onset of instability is that the loop gain be equal to $1e^{j0}$, a condition yielding the minimum value $g_{m,min}$ of g_m as

$$g_{m,min} = \frac{1}{R}\frac{1}{n(1-n)} \tag{1}$$

where $n = C_1/(C_1 + C_2)$ is the feedback factor.

The steady-state regime of a Colpitts (or any other) oscillator is, however, very much non-linear, as we can appreciate from Fig. 4, which shows that the current delivered by the transistor is made of tall and narrow pulses. Assuming though

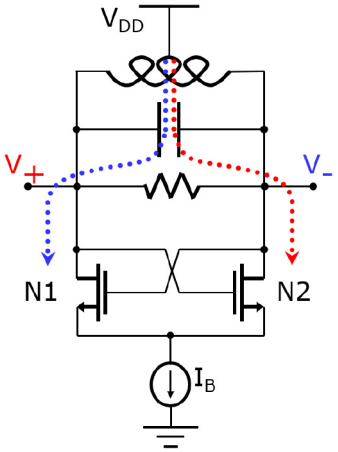

FIGURE 5. Simplified schematic view of the class-B oscillator with single cross-coupled differential pair.

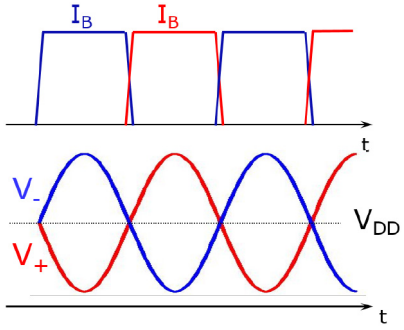

FIGURE 6. Voltage and current waveforms for the class-B oscillator in Fig. 5.

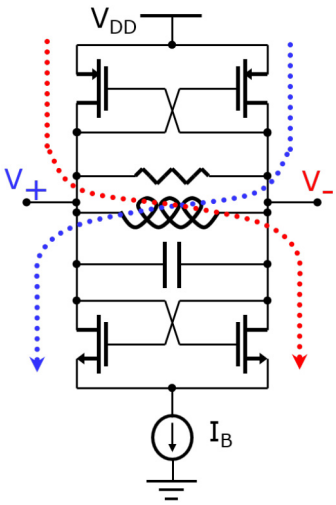

FIGURE 7. Simplified schematic view of the class-B oscillator with double cross-coupled differential pair.

that the tank Q is not too low, all higher current harmonics are filtered out by the tank, and only the fundamental current harmonic contributes significantly to the oscillation amplitude, which is therefore almost sinusoidal.

While deriving the oscillation amplitude in such a nonlinear system may appear overwhelmingly difficult, it is in fact surprisingly straightforward by means of the describing-function technique [5], which posits that the amplitude of the fundamental current harmonic is largely independent of the oscillation amplitude. This may seem too drastic a simplification, but it does indeed lead to very accurate predictions. Thus, if the current pulses of Fig. 4 are narrow enough, they can be represented as Dirac deltas, and then the amplitude of the fundamental current harmonic is easily found to be twice the bias current I_B, a value that changes very little with the actual shape of the current pulses, as long as they are narrow compared to T_0. This allows us to substitute the nMOS transistor in Fig. 2 with an independent current source of value and frequency equal to the fundamental current harmonic, immediately finding the amplitude A_{pk} of the sinusoidal voltage oscillation as [5]

$$A_{pk} \approx 2I_B R(1-n) \tag{2}$$

The deleterious factor $(1-n) < 1$ is caused by the feedback network effectively loading the tank.

Beautiful as the Colpitts oscillator is, the real star in the world of integrated electronics is the cross-coupled differential-pair oscillator (Fig. 5), as differential phases are needed anyway in almost all modern applications. This allows us to implement the negative resistance by simply cross-coupling the differential tank outputs to the differential nMOS pair inputs (gates), obtaining a value of $-2/g_m$, where g_m is the transconductance of a single transistor at DC.

This oscillator works in class B (and we will refer to it as the class-B oscillator in the following), or at least very close to it, since in steady state each nMOS injects the whole I_B into the tank for (almost) half of the oscillation period (swapping the power supply V_{DD} and ground, flipping the direction of I_B, and substituting the nMOS pair with a pMOS pair, we obtain a pMOS class-B oscillator, with an otherwise identical operation). The current waveforms are therefore square waves alternating between 0 and I_B (Fig. 6), with a first harmonic of amplitude $2I_B/\pi$. Notice that the inductor has a center tap connecting to V_{DD}, whereby the oscillation swings symmetrically above and below V_{DD}, reaching close to twice V_{DD} at maximum oscillation amplitude. The fact that V_{DD} is fed through the center tap of the inductor has the consequence that each current wave sees only half of the tank impedance at resonance, i.e., $R/2$. The oscillation amplitude across the differential tank is therefore $2\,(2I_B/\pi)\,R/2 = 2I_B R/\pi$.

A very popular variant of the class-B oscillator is that in Fig. 7, where two cross-coupled pairs are used, one nMOS and one pMOS, which, if their gain factors are identical, double the overall transconductance. The single-ended voltage oscillations are now those in Fig. 8: they resemble half sinusoids, since during half of the oscillation period each output is stuck at V_{DD} when the respective pMOS is on; differentially, though, the tank voltage is again (almost) sinusoidal with amplitude $4\pi I_B R$, i.e., double that in the class-B

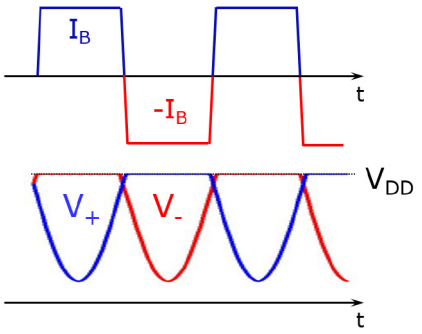

FIGURE 8. Voltage and current waveforms for the class-B oscillator in Fig. 7.

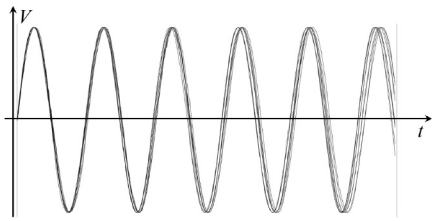

FIGURE 9. Oscillations affected by a (strong) white noise source.

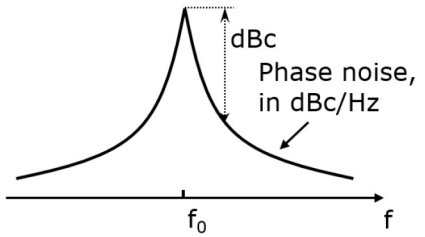

FIGURE 10. Frequency spectrum of a noisy oscillator.

oscillator with a single cross-coupled pair. This is because now the square wave current, commutating between I_B and $-I_B$, flows across the whole tank, not just half of it. Notice though that the oscillation is contained between V_{DD} and ground, and not between $2V_{DD}$ and ground as in Figs. 5–6.

III. PHASE NOISE

The uncertainty on the phase of the oscillation in a real oscillator grows without bound with time because of the action of various noise sources. In the time domain, this uncertainty is referred to as jitter: as shown by the simulations of Fig. 9, where the impact of (white) noise has been highly exaggerated, the uncertainty on the zero crossings grows in time in a random-walk fashion. The same phenomenon is called phase noise in the frequency domain, a terminology derived from the fact that noise affects only the phase of the oscillation for frequencies close to ω_0, the amplitude noise being rejected by the oscillator itself. Phase noise is expressed in dB with respect to the carrier and over a bandwidth of 1 Hz, i.e., in dBc/Hz (Fig. 10).

The simplest way to approach phase noise is via a standard linear time-invariant (LTI) analysis, starting with the assumption that active negative resistance and parallel tank

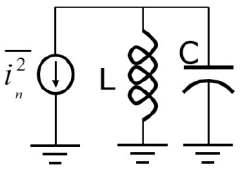

FIGURE 11. Oscillator circuit model for LTI phase noise analysis.

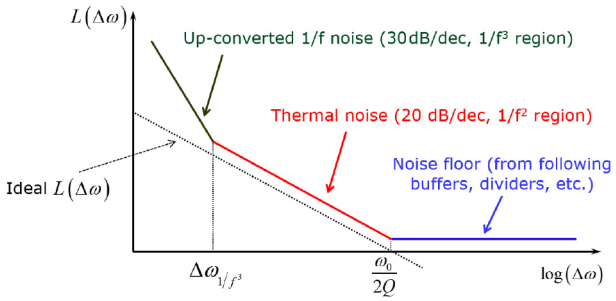

FIGURE 12. Asymptotic plot of the phase noise sideband in log-log scale.

resistance exactly cancel each other out. If we now want to analyze the impact of the thermal noise introduced by R (which, obviously, is not canceled by the uncorrelated noise generated by the negative resistance), the relevant circuit reduces to that in Fig. 11, where $\overline{i_n^2}/\Delta f = 4k_BT/R$, k_B being Boltzmann's constant and T the absolute temperature. It is straightforward to show that the power spectral density (PSD) of the noise voltage generated by $\overline{i_n^2}/\Delta f$ at a frequency $\Delta\omega$ from ω_0, with $\Delta\omega \ll \omega_0$, is

$$\frac{\overline{v_n^2}}{\Delta f} \approx 4k_BTR\left(\frac{1}{2\,Q}\,\frac{\omega_0}{\Delta\omega}\right)^2 \tag{3}$$

This expression, though, does not discriminate between amplitude noise and phase noise, while we have already stated that only phase noise survives close to the carrier. The correct phase noise expression is therefore half of (3), divided by the power of the sinusoidal carrier, yielding

$$\mathcal{L}(\Delta\omega) = 10\,\log_{10}\left(\frac{2k_BTR}{A_{pk}^2/2}\left(\frac{1}{2Q}\,\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{4}$$

This is the absolute minimum phase noise we can expect, since all noise sources but the tank have been neglected. It is worth remarking explicitly that $\Delta\omega$ at the denominator of (4) makes phase noise fall by 20 dB/dec with $\Delta\omega$.

Equation (4) lies at the core of the famous phase noise equation by Leeson [8],

$$\mathcal{L}(\Delta\omega) = 10\,\log_{10}\left(F\cdot\frac{2k_BTR}{A_{pk}^2/2}\left[1+\left(\frac{1}{2Q}\,\frac{\omega_0}{\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right) \tag{5}$$

plotted in Fig. 12. The additional factor F captures the impact of all white noise sources besides the tank, and primarily the negative resistance; moreover, the region closest to ω_0 is

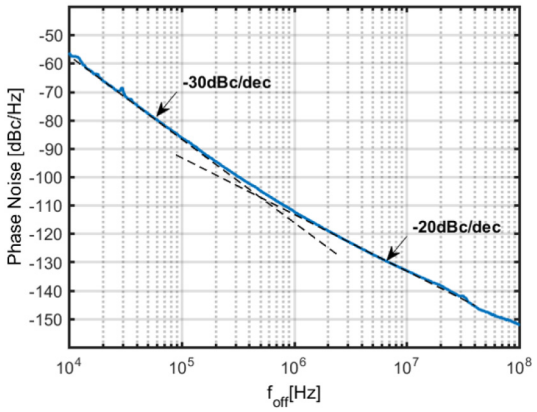

FIGURE 13. Example of phase noise measurement, from [10].

typically dominated by low-frequency $1/f$ noise upconverted to frequencies close to the carrier. In this region, extending up to a corner frequency of $\Delta\omega_{1/f^3}$, phase noise falls by 30 dB/dec with increasing $\Delta\omega$. Finally, phase noise may hit a floor, where it becomes white. This region is not, however, intrinsic to the oscillator itself, but originates from the additive noise introduced by circuits using or distributing the oscillation, such as buffers. Obviously, such a noise floor does not have to start at an offset frequency of $\omega_0/(2Q)$; rather, it is in the neighborhood of this offset frequency where amplitude noise starts adding up to phase noise in a well-designed oscillator [9]. Fig. 13 shows an actual phase noise measurement, with superimposed $1/f^2$ and $1/f^3$ asymptotes.

While fairly successful as a phenomenological description, it is obvious that the Leeson equation leaves much to be desired: a factor of two was removed from (4) by hand, $\Delta\omega_{1/f^3}$ is a fitting parameter, and it is difficult to see how the equation could be extended to, e.g., the treatment of noise generated by the negative-resistance transistors, whose operation varies wildly across T_0.

A turning point for the comprehension of phase noise in the SSCS community has been Ali Hajimiri and Thomas H. Lee's linear time-variant analysis [11]–[14]: the lightness and yet rigor of the approach have earned it a just and enduring fame (although, it goes without saying, many advances have intervened in the 20+ years since its appearance).

The need for a time variant analysis becomes inescapable when we realize that the conversion of noise into phase noise depends on when it occurs across T_0, even when a time invariant noise source (e.g., R) is considered. In fact, if we inject a noise pulse at the top of the oscillation sinusoid (Fig. 14), no disturbance is caused to the phase of the sinusoid, i.e., no phase noise is generated. On the other hand, if we inject it at a zero crossing, the phase disturbance is at a maximum.

Leaving the mathematical details aside, the lesson from [11] is that any current noise source i_n must be weighed by an associated impulse sensitivity function (ISF) Γ_{i_n} before

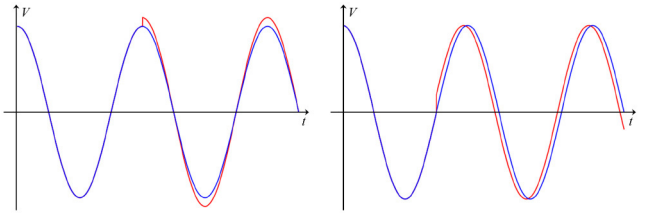

FIGURE 14. Ideal LC oscillation when a noise impulse is injected at the waveform peak (left) or at the zero crossing (right).

its contribution to phase noise can be assessed correctly, yielding an effective current noise

$$i_{n,\mathrm{eff}}(\phi) = i_n(\phi)\Gamma_{i_n}(\phi) \tag{6}$$

where $\phi = \omega_0 t$ is the phase of the oscillation (the same approach applies to voltage noise sources, see, e.g., [3]). Traditionally, the ISF is normalized to be dimensionless, frequency and amplitude independent, and with period 2π. If i_n is a cyclo-stationary noise source, it is convenient (and indeed very often possible) to express it as the product of a wide-sense stationary (WSS) noise source and a modulating function capturing the time variance of the noise process. Hence,

$$i_{n,\mathrm{eff}}(\phi) = i_{n,\mathrm{wss}}(\phi)\Gamma_{i_n,\mathrm{eff}}(\phi) \tag{7}$$

where now all time variance is contained in an effective $\Gamma_{i_n,\mathrm{eff}}(\phi)$. If i_n is a white current noise source, either stationary or cyclo-stationary, it can be shown that its contribution to phase noise is [11], [14]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\overline{i^2_{n,\mathrm{wss}}}/\Delta f\ \Gamma^2_{i_n,\mathrm{eff,rms}}}{2C^2A^2_{pk}\Delta\omega^2}\right) \tag{8}$$

where $\overline{i^2_{n,\mathrm{wss}}}/\Delta f$ is the PSD of $i_{n,\mathrm{wss}}$ and $\Gamma_{i_n,\mathrm{eff,rms}}$ is the root-mean-square value of $\Gamma_{i_n,\mathrm{eff}}$.

An equation similar to (8) applies when i_n is a $1/f$ noise current source (as we will discuss in more detail in Section IV-A, there is no upconversion of $1/f$ noise into $1/f^3$ phase noise in ideal Colpitts or class-B oscillators in CMOS).

Another way to understand the role of the ISF is to turn to the frequency domain: as shown in Fig. 15, the various harmonics of $\Gamma_{i_n,\mathrm{eff}}$ convolve with the relevant noise sidebands of $i_{n,\mathrm{wss}}$, causing phase modulation of the carrier, and ultimately phase noise.

Very conveniently, the ISF in a harmonic oscillator is (to the first order) a sinusoid of unit amplitude in quadrature to the voltage across the (single) tank, i.e., with arbitrary initial phase for the oscillation,

$$\Gamma_{i_n} = \sin(\phi) \tag{9}$$

If, on the other hand, the oscillator employs two independent tanks, the value of the ISF is halved [15]. Be as it may, such simple ISF expressions readily enable a symbolic analysis of phase noise. As an example, we can calculate (again)

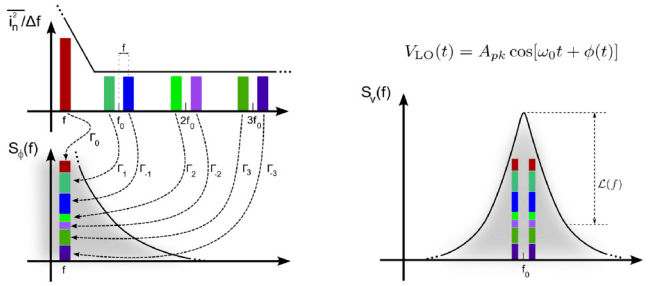

FIGURE 15. Noise folding due to the time-variant conversion of noise current into phase noise.

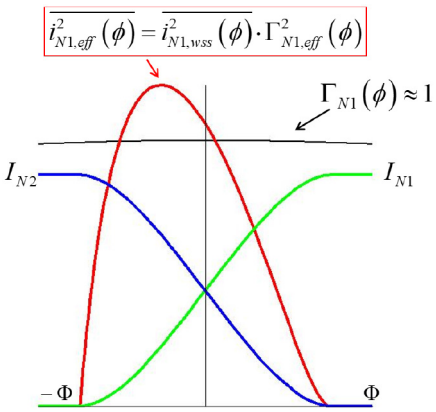

FIGURE 16. Current waveforms, ISF and effective noise current in the class-B oscillator of Fig. 5.

the phase noise induced by tank losses using (6)-(9), where $\overline{i_n^2}/\Delta f \cdot \Gamma_{i_n,\text{eff,rms}}^2 = 2\,k_B T/R$, since $\Gamma_{i_n,\text{eff,rms}}^2 = 1/2$. Thus, (8) allows us to recover (4), without the necessity, however, of invoking the empirical disappearance of the amplitude noise, which is instead accounted for in a natural way by $\Gamma_{i_n,\text{eff,rms}}^2$ being equal to $1/2$ instead of 1.

Even more interesting is that we can now do something new, namely, find the phase noise contribution from the cross-coupled nMOS pair in the class-B oscillator of Fig. 5.

Here, the PSD of the noise current generated by each transistor is given by $4\,k_B T \gamma_n g_m(\phi)$, where γ_n is the channel noise factor for the nMOS transistor. Each transistor contributes noise only during the short time when I_B commutates from one branch to the other, for a total of two commutations for each transistor over T_0 (transistor noise is otherwise rejected by the infinite impedance of the tail current source). Fig. 16 shows the effective noise from one transistor: since the associated ISF is almost constant and equal to 1 across the commutation, the whole of the nMOS noise is turned into phase noise, not just half of it.

Calculations are lengthy, but the final expression for the phase noise induced by both tank losses and MOS pair is very simple [15]:

$$\mathcal{L}_{\text{class-B}}(\Delta\omega) = 10\,\log_{10}\left(\frac{2k_B TR(1+\gamma_n)}{A_{pk}^2/2}\left(\frac{1}{2Q}\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{10}$$

Notably, the two transistors appear only through the factor γ_n, and, assuming $\gamma_n = 1$ for simplicity (its long-channel value being $2/3$), the tank and the nMOS pair contribute equally to phase noise. Equation (10) is in fact remarkable, as it states that, no matter the gain factor of the transistors, their phase noise contribution is always proportional to the tank's. This unexpected and nevertheless correct prediction can be traced back to the following mechanism: the effective current noise generated by the transistors is proportional to the current commutation time (Fig. 16), which is inversely proportional to the amplitude of the oscillation, which is proportional to the tank resistance, whose current noise is inversely proportional to its value. Of course, this does not mean that transistors do not matter, but rather that it is sufficient that their strength be large enough to ensure a quick current commutation, which yields the highest possible oscillation amplitude; transistors, on the other hand, should not be larger than this, in order to limit their parasitic capacitances, whose impact will be discussed in Section IV.

It is important to realize that a naive LTI analysis would have predicted, very wrongly, that the phase noise induced by the transistors increases with their small-signal transconductance. That this is not the case can be qualitatively understood from the following argument: if we increase the transconductance by, e.g., making the transistors larger, current noise is increased but commutation time is reduced, the two effects canceling each other exactly.

Turning to the class-B oscillator of Fig. 7, it can be shown [16] that its phase noise is

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{2k_B TR\left(1+\frac{\gamma_n+\gamma_p}{2}\right)}{A_{pk}^2/2}\left(\frac{1}{2Q}\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{11}$$

where γ_p is the channel noise factor for the pMOS transistor. Assuming $\gamma_p = \gamma_n$, the only difference between (10) and (11) is the oscillation amplitude, which, we recall, is twice as large in the class-B oscillator with complementary switch pairs, meaning that it enjoys a 6 dB phase-noise advantage over the class-B oscillator with a single switch pair. That it should be so is not wholly obvious, as the former contains four noise-generating transistors instead of only two in the latter. The difficulty is resolved when we consider that a doubled oscillation amplitude halves the commutation time for the switch pairs, which means that the four transistors in Fig. 7 generate together as much phase noise as the two transistors in Fig. 5 together.

We have already mentioned that the transistor ISF in the class-B oscillators is very nearly unity when it matters, which means that we would have had the theory (almost) right even bypassing the ISF theory altogether [17]. However, while this is true for a class-B oscillator, it would definitely not be the case in, e.g., a Colpitts oscillator, where ignoring the ISF results in a badly wrong phase noise prediction. The reason for this is obvious from Fig. 17: far from being

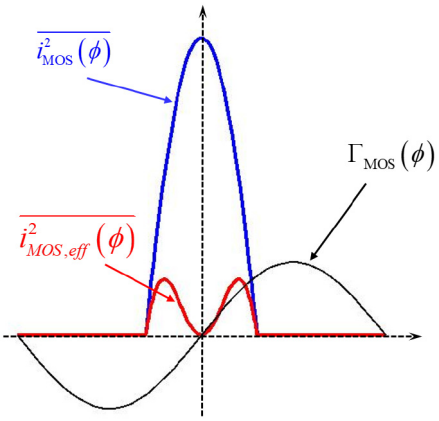

FIGURE 17. Noise current, ISF and effective noise current for the Colpitts oscillator of Fig. 2.

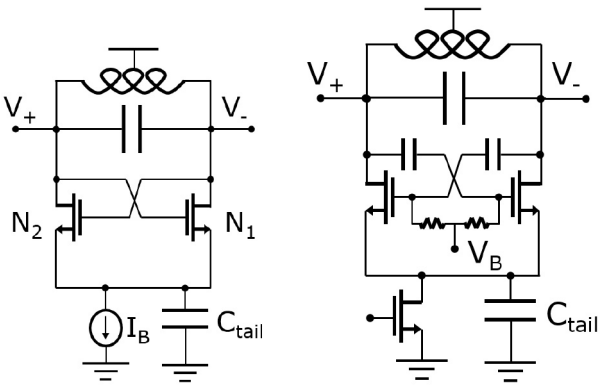

FIGURE 18. Simplified schematic view of a class-C oscillator.

unity, the transistor ISF is in this case small, even vanishing when transistor noise is at a maximum. Thus, the effective transistor noise is here much smaller than the native transistor noise.

The phase noise equation for a Colpitts oscillator is [15]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{k_B T}{4I_B^2 R^3 (1-n)^2 C^2 \Delta\omega^2}\left(1+\gamma_n\frac{1-n}{n}\right)\right] \tag{12}$$

where the oscillation amplitude has been written in terms of I_B, R and n to emphasize the dependence of (12) on n, showing that there is an optimal value of n minimizing phase noise (close to 0.3 for reasonable values of γ_n). In absolute terms, Colpitts phase noise is (marginally) higher than in a class-B oscillator, assuming identical R and I_B. In fact, while it is true that the Colpitts class-C current waveform yields a superior conversion of I_B into the first current harmonic, the feedback n from MOS drain to source, essential to generate the negative resistance, increases phase noise, as it decreases the oscillation amplitude [denominator of (12)] and boosts the transistor contribution [last term in (12), where the fraction is equal to 2 when $n = 1/3$].

These drawbacks can be avoided, while retaining a class-C operation, by moving to a differential architecture, since there the negative resistance is immediately synthesized, as we have already seen, by cross-coupling the feedback signals from the differential tank to the gates of the transistor pair. This means that we can set n to 0, i.e., we can remove C_1 altogether, keeping C_2 to shape the class-C current, as in Fig. 18 [18].

Ideally, the class-C oscillator yields a $20\log 10\ (\pi/2) \approx 4$ dB lower phase noise than the class-B oscillator with the same I_B. The class-C oscillator comes, however, with a number of issues, and primarily that the differential pair must not be allowed to enter the linear region of operation, which would thwart class-C operation by shorting tank and C_2 together, bringing about a large phase noise penalty. This means that we must shift the DC gate voltage of the transistor pair downwards, as done in Fig. 18 by means of an RC filter that should load the tank as little as possible. Another possibility is to replace the tank inductance with a transformer and use the center-tapped secondary coil for feedback and DC bias [18]. The DC bias voltage is generated by a low-frequency feedback loop for optimal oscillation amplitude [19]–[21].

Still, the demand that the transistor pair should stay safely in the active region entails that we can obtain a higher maximum oscillation amplitude in the ideal class-B CMOS oscillator (*ideal* being the keyword here), since the MOS devices there are mostly working as switches deeply in the linear region. When we deal with *real* implementations, though, the class-C oscillator may have an edge, albeit not a large one [21]. Finally, since BJT transistors cannot be allowed to enter saturation, the class-C topology is definitely very attractive for BJT oscillators [22].

It is noteworthy that, in all phase noise expressions derived so far, transistors contribute in proportion to the tank through γ_n (γ_p), where the proportionality factor depends on the specific oscillator topology. In fact, this is not a coincidence, but rather a general result for harmonic oscillators [9], [18], [23]: if 1) the ISF is sinusoidal and in quadrature with the tank voltage (which is typically the case); 2) all negative-resistance devices are either off, or working as transistors in the active region (this is effectively the case in a class-B oscillator as well, even though transistors there work in the linear region for most of the time, since they do work in the active region when they generate their contribution to phase noise [15]); and 3) the current noise PSD of these transistors is proportional to their transconductance, then it is possible to show that the phase noise caused by the transistors depends only on tank losses and oscillator topology, and nothing else. Actually, the first condition above can be removed by adopting a more powerful (and much less intuitive) phase noise analysis, where no assumptions are required on the nature of the resonator, which may be much more complex than a simple LC tank [24]. As a final word on this theme, we remark that compacting all tank losses into an equivalent parallel tank resistance may not be correct in some (uncommon) cases, due to the fact that

high-frequency noise from the resistance in series with C acts almost unimpeded on the transistor pair, since C itself offers a negligible impedance at frequencies much higher than ω_0 (opposite to L, whose impedance blocks all high frequency noise). If the transconductance of the transistor pair is inordinately large, as it may be in particular topologies, the high frequency noise from such a resistance can mix with the relevant transconductance harmonic to be folded in the vicinity of ω_0, increasing phase noise [25]. Even in this case though, tank and transistors contribute in the same fixed proportion to phase noise.

A. A REMARK ON THE ISF

If we consider an oscillator where the negative-resistance transistors act as transconductors with an ideally infinite output impedance, as in all cases above, then it is correct to take the fist-order expression of the ISF as a pure sinusoid proportional to the derivative of the voltage across the resonator – which coincides with the voltage across the transistors – when the resonator is a simple LC tank with a reasonable Q [24]. Things are different when the negative-resistance transistors are pushed into the linear region of operation over a fraction T' of T_0, where they come to work as (small) resistors. When this happens, the voltage across the transistors becomes almost constant, which would seem to imply that the ISF is negligible across T' – in fact, it is often assumed that in this situation the noise from the transistors, or from the tank, or both, is not converted into phase noise thanks to a supposedly close-to-zero ISF.

This is a wrong conclusion, stemming from the belief that the ISF can always be calculated by injecting a current pulse in parallel to the LC tank [11], and that such a pulse is completely drained by the small resistance presented by the transistors without affecting the LC tank. In reality, the notion of equivalent parallel tank resistance breaks down if the transistors work as small resistors [3], when the most convenient way to derive the ISF is by modeling a linear-region transistor as a voltage noise source rather than a current noise source [3] (by virtue of Norton's theorem, voltage-mode and current-mode models are mathematically equivalent, but the former lends itself most naturally when the impedance presented by the transistor is low). This approach applies to the LC tank losses as well, and makes it clear that the ISF is far from negligible even when the large-signal voltage across the transistors hardly moves [3], and may in fact be quantitatively identical to (9) [26].

IV. BIAS

So far, we have assumed an ideal bias current I_B in all oscillators, but this is hardly the case in practice, and in fact the way we implement the real bias current may become a major limitation for the phase noise performance.

As shown in Fig. 19, we can use a resistance, perhaps tunable in steps: this is very simple and has the advantage that the resistance does not generate any $1/f$ noise. This resistance is typically not large however, due to the low V_{DD} in modern CMOS processes, which means that the oscillator behavior may depart significantly from the ideal situation we have assumed so far. In particular, the upconversion of $1/f$ MOS noise may become significant, from being negligible in the ideal case (see Section IV-A). The bias resistance may be dispensed with altogether, making the current consumption of the oscillator wholly dependent on V_{DD} (which is such an important feature that these are referred to as voltage-mode oscillators) and transistor strength, and usually exacerbating $1/f$ noise upconversion. Clever countermeasures to the latter have been devised, e.g., resistors in series with the drains of the transistors [27], [28] or a commom-mode resonance at twice the oscillation frequency [29], [30] (about which more presently). In general, one would wish that the $1/f^3$ performance of voltage-mode oscillators were more robust with respect to unavoidable voltage, process, and temperature (PVT) variations.

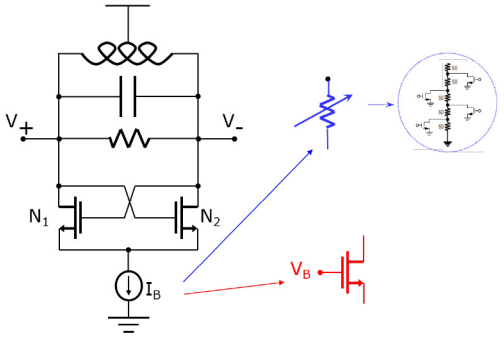

FIGURE 19. Possible implementations of the tail current source.

A popular alternative is an active current source (Fig. 19), which benefits from a high output impedance and a more ideal oscillator operation with it; the drawback is that it itself generates a possibly large amount of $1/f$ noise, which is actually much more prone to upconversion that the one from the MOS pair.

A certain amount of parasitic capacitance at the common source of the MOS pair is unavoidable, and simulations show that this may result in a deterioration of phase noise, even by a large amount, if the transistors are allowed to enter the linear region of operation as is typical in class-B designs. Again, it is the upconversion of $1/f$ noise that is of particular concern.

A popular and effective solution to this problem is the noise filter [31] of Fig. 20. The parasitic capacitance C_{par} is made to resonate with L_{tail} at $2\omega_0$, i.e., at the natural frequency of the common source, boosting its impedance and recovering close-to-ideal current waveforms. C_{tail} filters the high frequency noise from the tail, besides giving an AC ground to L_{tail}. At the same time, the parasitic capacitance in the tail nMOS current source can be absorbed into C_{tail}, which means that the dimension of this nMOS can be large; in particular, a long device generates a lower $1/f$ noise, while a large aspect ratio minimizes the DC drop across the channel. A (minor) drawback is that an extra inductor is needed,

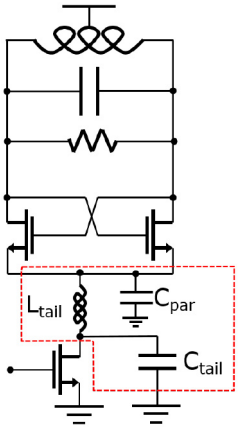

FIGURE 20. The tail noise filter.

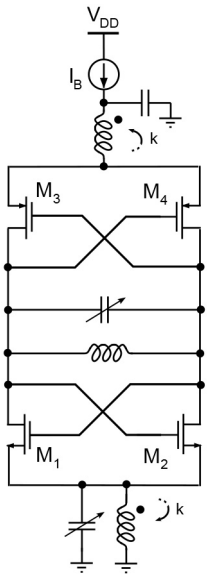

FIGURE 21. Class-B oscillator with noise filters as proposed in [32].

but the technique has proved so effective that it has spawned a large number of variations and has become a staple of class-B oscillator design. As an example, Fig. 21 shows a class-B oscillator with complementary switch pairs, where L_{tail} has been substituted with a transformer to increase the impedance at the common source of both pairs. The overall performance of this oscillator is excellent [32].

Alternatives to the noise filter have been proposed simultaneously by two research groups [29], [33]. The idea (Fig. 22) is to design a transformer-based tank having two distinct resonances: at ω_0 for differential signals, as usual, and at $2\omega_0$ for common-mode signals. It can be shown that this is equivalent to a noise filter, at least in principle [30].

A. 1/f NOISE

The analysis of the upconversion of $1/f$ noise into phase noise in harmonic oscillators is particularly difficult, since such an upconversion vanishes if we stop the analysis at the first order of approximation, i.e., if we assume that

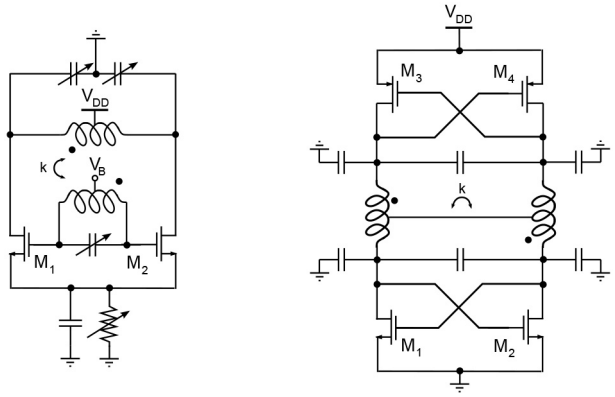

FIGURE 22. Transformer-based oscillators implementing differential-mode resonance at ω_0 and common-mode resonance at $2\omega_0$, as proposed in [29], [33].

both (voltage) oscillation and ISF are pure sine waves in quadrature with each other [11] (which is usually enough for a satisfactory treatment of the conversion of white noise into phase noise, as we have seen). The situation is actually even more complex than that: the upconversion vanishes in both class-B and class-C oscillators if they employ ideal, square-law MOS transistors with no parasitic capacitances, independently of the shape of the oscillation waveforms, provided the PSD of the $1/f$ noise is proportional to the transistor current, i.e., to the square of the transistor transconductance [10], [34].

Thus, unlike, e.g., CMOS ring oscillators, where the $1/f$ noise upconversion is a first-order effect [35]–[37], harmonic oscillators force us to consider a number of second-order effects (transistor non-idealities, parasitic capacitances, the exact dependence of $1/f$ noise on device parameters, etc.) that make the analysis repulsively intricate. To date, only one such analysis has been carried out [10], and this under strongly simplifying hypotheses and addressing a single transistor non-ideality (velocity saturation of the charge carriers in the MOS channel). Even so, it is anything but trivial.

Despite the above, simulations and measurements alike have consistently shown that a strong common-mode resonance at $2\omega_0$ (and *a fortiori* at all even harmonics) in class-B oscillators is effective in limiting the $1/f$ noise upconversion to a low level, the main concern of the technique being its robustness to PVT variations, as well as to intentional variations of ω_0 (discussed in Section V). A simple qualitative explanation of this is that the current waveforms in the class-B oscillator get closer to the ideal ones when even current harmonics are suppressed by the common-mode resonance at $2\omega_0$, and we have already seen that no $1/f$ noise upconversion occurs in an ideal class-B operation.

A different route to the containment of $1/f$ noise upconversion is via the class-C oscillator, which, to repeat, is ideally immune to it [10], [34]. Notice that this is true even though class-C current waveforms do contain even harmonics: the apparent contradiction is resolved by recalling that the core

transistors in a class-B oscillator are allowed to enter the linear region of operation, becoming switches, while those in a class-C oscillator are not (if, on the other hand, the class-B transistors are kept out of the linear region, no noise filter is needed to prevent $1/f$ noise upconversion, the oscillator effectively working somewhere between ideal class-B and ideal class-C depending on the amount of C_{par} [10]). In a class-C oscillator, too, the MOS current generator can be made long and wide, as was the case in the class-B oscillator with noise filter, since its parasitic capacitances can be absorbed into C_{tail} (up to a limit, though, as the exotic *squegging* behavior must be avoided [18]). Despite encouraging results [10], the effectiveness of the class-C oscillator in rejecting $1/f$ noise has yet to be probed in earnest.

B. FIGURE OF MERIT

To assess the performance of an oscillator in terms of phase noise, and possibly compare it to that of other oscillators, phase noise is normalized vs oscillation frequency, offset frequency, and power consumption (P, traditionally normalized to 1 mW). The resulting figure of merit, FoM, is

$$\text{FoM}(\Delta\omega) = -L(\Delta\omega) + 20\log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) - 10\log_{10}\left(10^3 P\right) \tag{13}$$

It is easy to show that the FoM can be written as

$$\text{FoM}(\Delta\omega) = 10\log_{10}\left(\frac{2Q^2}{k_B T}\frac{\eta}{F}\right) - 30\,\text{dB} \tag{14}$$

where the maximum FoM_{max} is obtained for an oscillator power efficiency η of 1 (when all power is consumed in the resonator) and a noise factor F of 1 (when only the tank generates phase noise). The strong FoM dependence on the resonator Q is obvious.

The FoM is an important instrument for the oscillator designer, who can gauge the oscillator quality across various design stages, provided this information is combined with a knowledge of the discrepancy that can be reasonably expected between FoM and FoM_{max}.

The FoM is also useful in comparing different oscillator topologies, for instance the class-B oscillator with a single switch pair vs two complementary switch pairs. Perhaps surprisingly, these two topologies are ideally capable of the same FoM_{max}, which however is attained at different levels of phase noise and power consumption. This opens up for a reconfigurable architecture where one or the other configuration is selected, based on specific phase noise requirements [38].

The importance of a high FoM in boosting the perceived importance of a work cannot be overstated. This is not entirely positive, as the FoM is not well suited to capture vital oscillator features in real-life applications, such as robustness to PVT variations and EM disturbances. As an example, we can mention that using an 8-shaped inductor can dramatically improve the oscillation insensitivity to external magnetic fields, but also (slightly) decreases tank Q and FoM with it [39], [40].

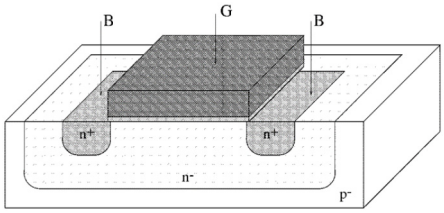

FIGURE 23. Cross section of an AMOS varactor.

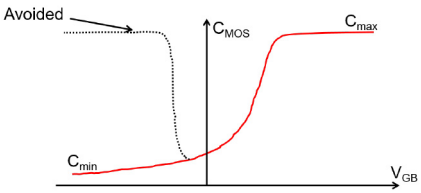

FIGURE 24. C-V curve of an AMOS varactor (in red) as compared to a pMOS device.

V. FREQUENCY TUNING

An oscillator where the oscillation frequency cannot be varied at least to some extent is useless in practice, as this is needed to counteract uncertainties in component values as well as PVT variations. Since the oscillation frequency is typically adjusted through a control voltage, real oscillators are voltage-controlled oscillators (VCOs, or, if the control voltage is a purely digital signal, DCOs).

The easiest way of tuning the oscillation frequency is by replacing part of the tank capacitance with a component whose capacitance is dependent on the DC voltage across the component itself, realizing a variable reactor (varactor). Two such components are readily available in any CMOS process: the (parasitic) *pn* diode and the MOS device itself. Particularly attractive is the two-terminal accumulation-mode nMOS device in an N-well (AMOS), shown in Fig. 23 [41]–[43], replacing the standard four-terminal nMOS device in a P-well. This maximizes the capacitance variation vs DC voltage between gate and substrate, as the AMOS works between accumulation (maximum capacitance) and depletion (minimum capacitance) while avoiding inversion (where the capacitance would climb back to its maximum value), as depicted in Fig. 24. Moreover, compared to a pMOS device in a P-well, losses are minimized by the higher electron mobility.

An efficient frequency tuning is thus obtained by connecting two back-to-back AMOS devices to the oscillator tank, each gate to the respective differential tank node, while the common AMOS substrate is acted upon by the control voltage. Compared to the reverse-biased diode, which may carry a large DC current if it becomes forward biased by too large an oscillation amplitude, which would destroy the tank Q, the AMOS varactor allows for a more robust design, as it is a natural DC blocker.

In principle we can increase the frequency tuning range (TR) of the oscillator by means of a larger varactor. This is not a popular choice though, as the noise present on

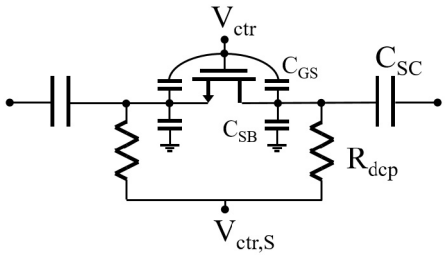

FIGURE 25. Typical circuit for a switchable differential capacitance C_{SC}.

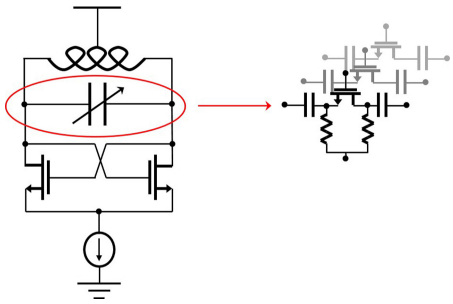

FIGURE 26. Switchable capacitor bank for discrete frequency tuning.

the control voltage is also going to affect the oscillation frequency, contributing a surplus of phase noise: if the varactor is very large, the control voltage would have to be extremely clean to avoid a significant phase noise deterioration. Furthermore, the various $1/f$ current noise sources in the oscillator may determine a change in the oscillation amplitude across the varactor, inducing a change in the effective capacitance presented by the varactor itself: this is invariably a major mechanism of $1/f$ noise upconversion if the varactor is large [44], [45].

The varactor is therefore not larger than what is needed to ensure phase lock when the oscillator is used in a phase-locked loop (PLL), possibly accommodating phase modulation as well, while the rest of the TR is covered in discrete steps by switching a number of linear capacitors in and out of the oscillator tank [46].

A. DISCRETE TUNING

A typical arrangement for switching one such differential capacitor is shown in Fig. 25. When V_{ctr} is high (e.g., equal to V_{DD}), the (minimum-length) MOS device becomes a small resistance R_{on} in series with the two capacitors C_{SC}, each connecting to one side of the differential tank. In this way, the overall tank capacitance is increased, decreasing f_0. Obviously, R_{on} must be low to avoid a degradation of the overall tank Q [47], which means that $V_{ctr,S}$ should be low (e.g., 0 V) to maximize the MOS overdrive voltage. When V_{ctr} is low, on the other hand, ideally no extra capacitance loads the tank, leaving f_0 unaffected; in reality, the parasitic MOS capacitances between gate and drain/source and between drain/source and bulk (since no DC current flows in the device, drain and source swap place together with the direction of the AC MOS current), i.e., C_{GS} and C_{SB}, make the off-state capacitance approximately equal to $C_{GS} + C_{SB}$, forcing a deleterious drop in f_0. It is therefore advantageous to set $V_{ctr,S}$ as high as possible in the off-state, which minimizes the value of the reversed-biased diode capacitance C_{SB}. Care must be taken though that the peak value of the oscillating voltage, added to $V_{ctr,S}$, does not exceed the maximum rating for the MOS device; the availability of two (or more) supply voltages eases the task considerably [39].

It is immediate to see that there is a hard trade-off between R_{on} and C_{SB}, as a larger MOS device decreases R_{on} and increases C_{SB} by the same amount. The same trade-off acts between tank Q and TR, since a large C_{SB} impairs the latter. By the same argument, the product of R_{on} and C_{SB} is a (first-order) technology constant, and should be as low as possible in a harmonic-oscillator-friendly CMOS process [e.g., a fully-depleted silicon-on-insulator (FD-SOI) CMOS process].

Finally, the value of the decoupling resistance R_{dcp} should be so high as to leave the tank Q unaffected in the off-state; yet, the desired value of R_{dcp} may be limited by the following interesting mechanism: the low-frequency noise voltage from R_{dcp} modulates the MOS source voltage, which modulates the value of the non-linear C_{SB}, which modulates the frequency of oscillation, which is tantamount to generating phase noise. An FD-SOI CMOS technology may be of great help also in this respect.

We conclude this section by mentioning that phase noise and tuning range are often baked together in an augmented figure of merit, FoM_T. Unlike the FoM of (13), FoM_T does not rest on a firm theoretical ground, making its widespread use questionable.

B. VERY WIDE FREQUENCY TUNING RANGE

The ongoing band proliferation in wireless communication favors VCOs with a very wide TR, where a TR larger than one octave is especially attractive, as all lower frequencies can be generated by repeated frequency division by two, which is easy enough to implement.

The simplest way of obtaining a very wide TR is to design the LC tank with a relatively small inductance and a sufficiently large array of switchable capacitances (Fig. 26), which must vary by at least a factor of four from minimum to maximum to cover one octave of TR. The corresponding large number of MOS switches introduces a large parasitic non-linear capacitance as well. In this solution, power is likely to be wasted at the lowest oscillation frequencies, compared to reasonable phase noise specifications: as soon as we are able to establish an oscillation, phase noise is already unnecessarily low, as can be appreciated from, e.g., (10) when R is very low (which is a consequence of the relation $Q = R\omega_0 C$, assuming a very large C and a reasonable Q). One might think of reducing power by scaling down A_{pk} in (10) by a sizeable amount, but this is not without complications, as it needs a dedicated and precise controller of the oscillation amplitude and, moreover, the circuitry driven by

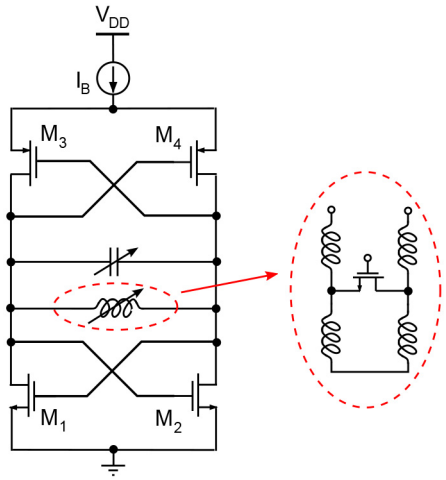

FIGURE 27. Switched inductor, as proposed in [48].

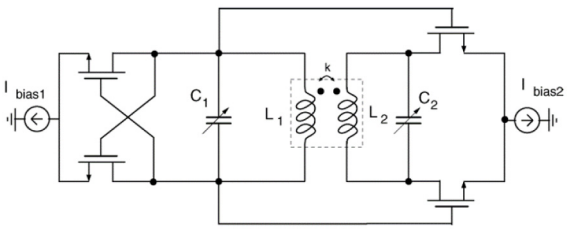

FIGURE 28. Transformer-based dual-mode oscillator.

the oscillator (distribution buffers, frequency dividers, etc.) typically expects an input close to rail-to-rail.

It is also possible to switch inductors [48] instead of capacitors, as shown in Fig. 27. Two problems may affect this approach: the MOS switch turning the inductor on and off may have to carry a (large) DC current, and the parasitic capacitances introduced by the switch may shunt at least part of the inductor. To date, switched inductors are not behind the best VCOs, although very wide TRs have been demonstrated.

A more attractive choice is a magnetic transformer [49] (hereafter simply referred to as a transformer), with which two distinct resonances can be realized [50], [51]; a very large overall TR can then be obtained by joining two overlapping TRs, each tuning one of the resonances. While two active oscillator cores are needed (Fig. 28), the great advantage here is that it is the cores that are turned on/off (one at a time, depending on which of the resonances should be active) by turning on/off their bias current, so that no switch is placed in series with any inductor, with great benefit for the resonator Q.

The mutual inductance between the coupled coils of the transformer increases the energy stored in the resonator at the lower resonance while decreasing it at the higher resonance [52], [53]. If only one resonance is used, then this must be the lower one, as the resonator Q is thus maximized. Nevertheless, the resonator Q increases with frequency, as long as it is limited by the transformer itself. Hence, when

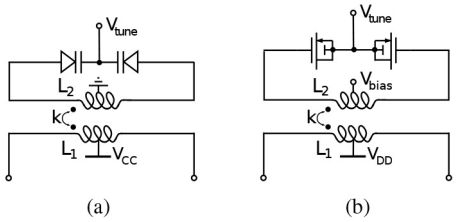

FIGURE 29. Examples of varactor coupling using a magnetic transformer: (a) *pn*-varactor; (b) MOS varactor.

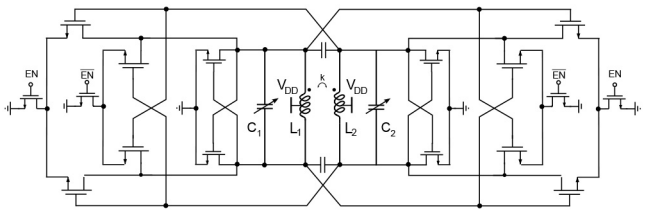

FIGURE 30. Dual-mode oscillator proposed in [57].

both resonances are used to expand the TR, it is still possible to achieve a comparable Q at both. As an aside, it must be noted that the increase in Q due to the mutual inductance between the transformer primary and secondary windings is enjoyed by a standard inductor as well, as its turns are also mutually coupled. As a consequence, there is no intrinsic Q improvement from the sheer use of a transformer [54], [55].

A transformer is useful for frequency tuning from a different perspective, too: it provides a means to AC-couple the varactor to the tank and, simultaneously, a convenient bias point for the varactor via the center tap of the secondary winding, as shown in Fig. 29. This is especially effective at mm-wave frequencies (and higher), where capacitor Q is lower than inductor Q. AC-coupling the varactor is typically required to explore the entire TR without the need of a separate DC voltage, or, when a *pn* diode is used, as in Fig. 29(a), to avoid the junction turn-on during part of the oscillation cycle, which would heavily deteriorate the tank Q [52], [56], as already mentioned.

An elegant development of the dual-mode oscillator is shown in Fig. 30 [57], yielding excellent phase noise and FoM with a TR wider than one octave; a mm-wave example is presented in [58], with oscillation frequency spanning from 25 to 38 GHz.

A different take in the same spirit is the mode-switching VCO in [59], with four inductors and, again, two oscillation modes. Here, MOS switches are used to hop between the two oscillation modes, but in such a way that they do not carry any signal, thereby avoiding again any Q deterioration. The mode-switching VCO achieves a very wide TR, a very low phase noise and an excellent FoM at the same time, the (partial) downside being the large area needed by the four coils. A further desirable feature of this architecture is its rejection of external magnetic fields (the same property of the aforementioned 8-shaped inductor).

The success of these works has attracted a great deal of interest in transformer-based/mode-switching techniques, which are currently a very active research area [60]–[64].

Finally, since low power consumption and design simplicity and robustness are priorities in portable wireless applications, we note that commercial designs often obtain a very large effective TR in the most straightforward way, i.e., by optimizing two (or more) VCOs with much narrower TRs and letting the TRs overlap one another, trading silicon area for power efficiency.

VI. IMPROVING PHASE NOISE

In the evolution of systems for communication, radar, and data conversion, the requirement of ever higher spectral purity is relentless. At the same time, the constantly dropping power supply voltage in modern ultra-scaled CMOS technologies thwarts this very goal, as a lower supply voltage translates to a lower maximum attainable oscillation amplitude, yielding a higher minimum phase noise, as is clear from (5). Since the resonator Q is set by technology and frequency of operation, (5) points out that the only possibility to reach a lower phase noise is to reduce the resonator parallel resistance R (which entails a reduction of L), thereby trading a higher power consumption for a lower phase noise. This approach cannot be pursued indefinitely, however, as there is a lower bound to the minimum practical value of R.

The use of a transformer-based resonator can help obtaining a lower value of R: it can be shown that the equivalent resistance of such a resonator is similar to what would be achieved by shunting the coupled coils in the transformer (while adjusting the capacitance to keep a constant resonance frequency).

A transformer brings about an additional advantage: it may provide a passive voltage gain. This is leveraged to introduce a gain A_v between the output (drain) and the input (gate) of the negative-resistance transistors, resulting in a reduction of the transistor contribution to phase noise [18], [52], with a lower factor F in (5), which becomes

$$F = 1 + \frac{\gamma}{A_v} \tag{15}$$

It must be noted that this approach is viable as long as the voltage swing at the input of the transistors does not compromise their reliability.

Yet another option offered by a transformer-based resonator is to introduce an additional differential-mode resonance located at $3\omega_0$, often together with the already discussed common-mode resonance at $2\omega_0$, as in the class-F oscillator in [65]. The rationale behind this is that a steeper slope is obtained in the waveform of the oscillation, which shortens the time interval when the negative-resistance transistor generates noise, lowering phase noise; now, however, noise at $3\omega_0 \pm \Delta\omega$ also contributes to phase noise, which may even increase overall if the resonator Q at $3\omega_0$ is not sufficiently high [24], [66]. Nevertheless, an additional resonance at $3\omega_0$ may still be used with advantage to extract a sufficiently strong third harmonic from an oscillator working at ω_0, realizing an implicit frequency multiplication by three [67], [68], which is especially useful at mm-waves.

Multiple coupled inductors potentially allow all node voltages in the oscillator to swing below ground and/or well above the power supply [61], [69], increasing the maximum amplitude of oscillation, with obvious benefits for phase noise. This is particularly welcome when very low supply voltages are used. It also results in an improved DC-to-RF power efficiency, and hence a higher FoM. The downside is that the higher voltage excursions may exceed the voltage ratings of the transistors, raising reliability concerns.

A. MULTI-CORE OSCILLATORS

To further improve phase noise, N identical oscillators can be coupled and operated in a synchronous fashion [70]–[75], thereby lowering the phase noise power by a factor N. In this way, a higher power consumption is traded for a lower phase noise, ideally keeping a constant FoM and accepting the drawback of a larger silicon area.

The implementation of large arrays of coupled oscillators and the achievement of the related phase noise benefit is not trivial. Ideally, the coupling network should not affect the operation of the synchronized oscillators, nor degrade the phase noise performance. However, if the oscillator coupling is weak (i.e., the coupling impedance is high) the mentioned phase noise improvement may be experienced only at small frequency offsets from the carrier. Additionally, mismatches between the resonance frequencies of the individual resonators induce a phase noise degradation that increases with the impedance of the coupling network [73]. Thus as N increases, the coupling network becomes correspondingly more difficult to design; a star connection, where each oscillator is globally coupled to all the others, becomes impractical, and one has to resort to nearest-neighbor bilateral coupling. This sets some challenges, as it is more susceptible to mismatch-induced phase noise degradation [73], [76]. Moreover, the coupling network of a large array of oscillators tends to introduce more parasitics, due to its larger footprint, potentially creating unwanted systematic mismatches between the oscillators and shifts in the oscillation frequency. Another issue related to oscillator coupling is that undesired modes of oscillation might emerge, which must be suppressed by a judicious design of the coupling network [71], [72]. As the lowest achievable phase noise may not always be needed by the system where the oscillator operates, reconfigurability of the coupled-oscillator array is a welcome feature [73], where the goal is to be able to switch off some oscillators to save power when the attending phase noise deterioration is acceptable. Such reconfigurability requires the possibility to individually turn on/off and disconnect the oscillators from the array (Fig. 31); the latter operation is non-trivial, as it requires additional switches in the coupling networks, which may increase the coupling impedance and phase noise with it.

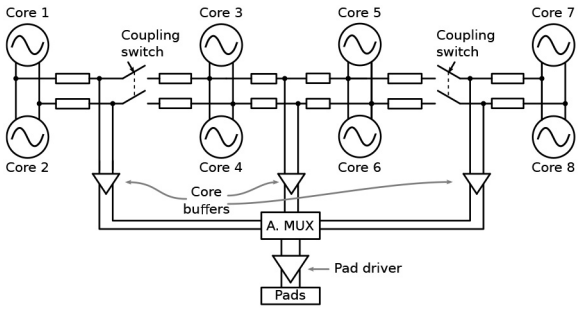

FIGURE 31. Reconfigurable coupled-oscillator array.

VII. CONCLUSION

Harmonic oscillators are the designer's prime choice whenever a high frequency purity is required in communication, radar, and data-conversion systems alike. Achieving a low phase noise in harmonic oscillators calls for two main ingredients: a large oscillation amplitude and a small tank impedance (resistance) at resonance, while a high resonator Q is primarily beneficial for power consumption. The design of a good oscillator is not limited to resonator and negative resistance, as the bias circuitry may easily become a bottleneck for the overall performance. Similarly, implementing a wide frequency tuning is far from trivial, with an inherent trade-off between phase noise, power consumption, and tuning range. The introduction of transformer-based resonators has spawned a variety of multi-mode oscillators that aim to break this trade-off, improving phase noise and tuning performance. Finally, multiple oscillators can be coupled together to lower the minimum achievable phase noise in practical implementations, at the cost of a larger area.

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REFERENCES

[1] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M.-C. F. Chang, "A blocker-tolerant inductor-less wideband receiver with phase and thermal noise cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2948–2964, Dec. 2015.

[2] M. Mikhemar, D. Murphy, A. Mirzaei, and H. Darabi, "A cancellation technique for reciprocal-mixing caused by phase noise and spurs," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec. 2013.

[3] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[4] E. Colpitts, "Oscillation generator," U.S. Patent 1 624 537, 1918.

[5] T. H. Lee, *The Design of CMOS Radio-Freqency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[6] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2011.

[7] R. V. L. Hartley, "Oscillation generator," U.S. Patent 1 356 763, 1915.

[8] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.

[9] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.

[10] A. Franceschin, P. Andreani, F. Padovan, M. Bassi, and A. Bevilacqua, "A 19.5-GHz 28-nm class-C CMOS VCO, with a reasonably rigorous result on 1/f noise upconversion caused by short-channel effects," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1842–1853, Jul. 2020.

[11] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[12] A. Hajimiri and T. H. Lee, "Corrections to 'a general theory of phase noise in electrical oscillators,"' *IEEE J. Solid-State Circuits*, vol. 33, no. 6, p. 928, Jun. 1998.

[13] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, Mar. 2000.

[14] L. Lu, Z. Tang, P. Andreani, A. Mazzanti, and A. Hajimiri, "Comments on 'comments on 'a general theory of phase noise in electrical oscillators,"' *IEEE J. Solid-State Circuits*, vol. 43, no. 9, p. 2170, Sep. 2008.

[15] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[16] P. Andreani and A. Fard, "More on the $1/f^2$ phase noise performance of CMOS differential-pair LC-tank oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.

[17] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2000, pp. 569–572.

[18] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[19] W. Deng, K. Okada, and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," in *Proc. ESSCIRC*, Sep. 2011, pp. 499–502.

[20] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in *Proc. ESSCIRC*, Sep. 2011, pp. 495–498.

[21] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.

[22] S. Veni, P. Andreani, M. Caruso, M. Tiebout, and A. Bevilacqua, "Analysis and design of a 17-GHz all-pnp push-pull class-C VCO," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2345–2355, Sep. 2020.

[23] J. Bank, "A harmonic-oscillator design methodology based on describing functions," Ph.D. dissertation, Dept. Signals Syst., Chalmers Univ. Technol., Göteborg, Sweden, 2006.

[24] F. Pepe and P. Andreani, "A general theory of phase noise in transconductor-based harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 432–445, Feb. 2017.

[25] F. Pepe and P. Andreani, "Still more on the $1/f^2$ phase noise performance of harmonic oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 6, pp. 538–542, Jun. 2016.

[26] F. Pepe, A. Bevilacqua, and P. Andreani, "On the remarkable performance of the series-resonance CMOS oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 531–542, Feb. 2018.

[27] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Analysis and minimization of flicker noise up-conversion in voltage-biased oscillators," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2382–2394, Jun. 2013.

[28] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Suppression of flicker noise up-conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz band," *IEEE J. Solid-State Circuit*, vol. 48, no. 10, pp. 2375–2389, Oct. 2013.

[29] D. Murphy, H. Darabi, and H. Wu, "A VCO with implicit common-mode resonance," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 1–3.

[30] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.

[31] E. Hegazi, H. Sjöland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2002.

[32] M. Garampazzi, P. M. Mendes, N. Codega, D. Manstretta, and R. Castello, "Analysis and design of a 195.6 dBc/Hz peak FoM P-N class-B oscillator with transformer-based tail filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1657–1668, Jul. 2015.

[33] M. Shahmohammadi, M. Babaie, and R. Staszewski, "25.4 A 1/f noise upconversion reduction technique applied to Class-D and Class-F oscillators," in *Proc. IEEE Int. Solid- State Circuits Conf.*, Feb. 2015, pp. 1–3.

[34] A. Bevilacqua and P. Andreani, "An analysis of 1/f noise to phase noise conversion in CMOS harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 938–945, May 2012.

[35] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[36] A. Homayoun and B. Razavi, "Relation between delay line phase noise and ring oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 384–391, Feb. 2014.

[37] F. Pepe and P. Andreani, "An accurate analysis of phase noise in CMOS ring oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 8, pp. 1292–1296, Aug. 2019.

[38] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A power-scalable DCO for multi-standard GSM/WCDMA frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 646–656, Mar. 2014.

[39] P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattsson, "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1618–1626, Jul. 2011.

[40] L. Fanori, T. Mattsson, and P. Andreani, "A 2.4-to-5.3GHz dual-core CMOS VCO with concentric 8-shaped coils," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 370–371.

[41] C.-M. Hung, Y.-C. Ho, I.-C. Wu, and K. O. Kenneth, "High-Q capacitors implemented in a CMOS process for low-power wireless applications," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 5, pp. 505–511, May 1998.

[42] T. Soorapanth, C. P. Yue, D. K. Shaeffer, T. I. Lee, and S. S. Wong, "Analysis and optimization of accumulation-mode varactor for RF ICs," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1998, pp. 32–33.

[43] R. Castello, P. Erratico, S. Manzini, and F. Svelto, "A $\pm$30% tuning range varactor compatible with future scaled technologies," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1998, pp. 34–35.

[44] S. Levantino, C. Samori, A. Zanchi, and A. L. Lacaita, "AM-to-PM conversion in varactor-tuned oscillators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*,, vol. 49, no. 7, pp. 509–513, Jul. 2002.

[45] A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*,, vol. 53, no. 3, pp. 481–488, Mar. 2006.

[46] H. Sjöland, "Improved switched tuning of differential CMOS VCOs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 5, pp. 352–355, May 2002.

[47] S. Dal Toso, A. Bevilacqua, A. Gerosa, and A. Neviani, "A thorough analysis of the tank quality factor in LC oscillators with switched capacitor banks," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 1903–1906.

[48] B. Sadhu, J. Kim, and R. Harjani, "A CMOS 3.3-8.4 GHz wide tuning range, low phase noise LC VCO," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2009, pp. 559–562.

[49] P. Andreani, "A 1.8-GHz monolithic CMOS VCO tuned by an inductive varactor," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 4, May 2001, pp. 714–717.

[50] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "A 3.3-7 GHz transformer-based dual-mode wideband VCO," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Montreux, Switzerland, Sep. 2006, pp. 440–443.

[51] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.

[52] A. Mazzanti and A. Bevilacqua, "On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2334–2341, Sep. 2015.

[53] A. Bevilacqua and A. Mazzanti, "Doubly-tuned transformer networks: A tutorial," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 2, pp. 550–555, Feb. 2021.

[54] P. Andreani and J. Long, "Misconception regarding use of transformer resonators in monolithic oscillators," *Electron. Lett.*, vol. 42, no. 7, pp. 387–388, 2006.

[55] A. Bevilacqua, "Fundamentals of integrated transformers: From principles to applications," *IEEE Solid-State Circuits Mag.*, vol. 12, no. 4, pp. 86–100, 2020.

[56] F. Padovan, M. Tiebout, K. L. R. Mertens, A. Bevilacqua, and A. Neviani, "Design of low-noise K-band SiGe bipolar VCOs: Theory and implementation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 607–615, Feb. 2015.

[57] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, Jun. 2012.

[58] A. Bhat and N. Krishnapura, "A 25-to-38GHz, 195dB FoMT LC QVCO in 65nm LP CMOS using a 4-port dual-mode resonator for 5G radios," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, 2019, pp. 412–414.

[59] M. Taghivand, K. Aggarwal, and A. S. Y. Poon, "A 3.24-to-8.45GHz low-phase-noise mode-switching oscillator," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 368–369.

[60] Y. Shu, H. J. Qian, and X. Luo, "A 18.6-to-40.1GHz 201.7dBc/Hz FoMT multi-core oscillator using E-M mixed-coupling resonance boosting," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, 2020, pp. 272–274.

[61] Y. Shu, H. J. Qian, X. Gao, and X. Luo, "A 3.09-to-4.04GHz distributed-boosting and harmonic-impedance-expanding multi-core oscillator with -138.9dBc/Hz at 1MHz offset and 195.1dBc/Hz FoM," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 296–298.

[62] H. Jia, W. Deng, P. Guan, Z. Wang, and B. Chi, "A 60GHz 186.5dBc/Hz FoM quad-core fundamental VCO using circular triple-coupled transformer with no mode ambiguity in 65nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 1–3.

[63] H. Guo, Y. Chen, P. I. Mak, and R. P. Martins, "A 5.0-to-6.36GHz wideband-harmonic-shaping VCO achieving 196.9dBc/Hz peak FoM and 90-to-180kHz $1/f^3$ PN corner without harmonic tuning," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 294–296.

[64] O. El-Aassar and G. M. Rebeiz, "Octave-tuning dual-core folded VCO leveraging a triple-mode switch-less tertiary magnetic loop," *IEEE J. Solid-State Circuit*, vol. 56, no. 5, pp. 1475–1486, May 2021.

[65] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[66] M. Garampazzi *et al.*, "An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 635–645, Mar. 2014.

[67] Z. Zong, M. Babaie, and R. B. Staszewski, "A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, 2016.

[68] Y. Hu, T. Siriburanon, and R. B. Staszewski, "A low-flicker-noise 30-GHz class-F_{23} oscillator in 28-nm CMOS using implicit resonance and explicit common-mode return path," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1977–1987, Jul. 2018.

[69] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 652–660, Mar. 2005.

[70] S. A. R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, "Analysis and design of a multi-core oscillator for ultra-low phase noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 4, pp. 529–539, Apr. 2016.

[71] D. Murphy and H. Darabi, "A 27-GHz quad-core CMOS oscillator with no mode ambiguity," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3208–3216, Nov. 2018.

[72] F. Padovan, F. Quadrelli, M. Bassi, M. Tiebout, and A. Bevilacqua, "A quad-core 15 GHz BiCMOS VCO with -124 dBc/Hz phase noise at 1 MHz offset, -189 dBc/Hz FOM, and robust to multimode concurrent oscillations," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, 2018, pp. 376–378.

[73] L. Iotti, A. Mazzanti, and F. Svelto, "Insights into phase-noise scaling in switch-coupled multi-core LC VCOs for E-band adaptive modulation links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1718, Jul. 2017.

[74] A. Moroni, R. Genesi, and D. Manstretta, "Analysis and design of a 54 GHz distributed 'hybrid' wave oscillator array with quadrature outputs," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1158–1172, May 2014.
[75] Y. Peng, J. Yin, P.-I. Mak, and R. P. Martins, "Low-phase-noise wideband mode-switching quad-core-coupled mm-Wave VCO using a single-center-tapped switched inductor," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3232–3242, Nov. 2018.
[76] H.-C. Chang, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 5, pp. 604–615, May 1997.

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