IEEE Open Journal of the
Solid-State Circuits Society

Received 11 August 2023; revised 11 October 2023 and 9 November 2023; accepted 13 November 2023. Date of publication 20 November 2023; date of current version 6 February 2024.

Digital Object Identifier 10.1109/OJSSCS.2023.3334228

An Overview of Hybrid DC–DC Converters: From Seeds to Leaves

YAN LU (Senior Member, IEEE), JUNWEI HUANG (Student Member, IEEE), ZHIGUO TONG (Student Member, IEEE), TINGXU HU (Student Member, IEEE), WEN-LIANG ZENG (Member, IEEE), MO HUANG (Senior Member, IEEE), XIANGYU MAO (Member, IEEE), AND GUIGANG CAI (Member, IEEE) (Fellow, IEEE)

(Invited Paper)

State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China

CORRESPONDING AUTHOR: Y. LU (e-mail: yanlu@um.edu.mo)

This work was supported in part by the National Natural Science Foundation of China under Grant 62122001, and in part by the Macao Science and Technology Development Fund (FDCT) under Grant 0023/2022/A1 and Grant 0103/2022/AFJ.

ABSTRACT With the surging demands for higher current at sub-1-V supply level in high-performance digital systems, high-efficiency and high-current-density power converters are essential for system integration. Higher voltage supply buses are emerging for high-current applications to reduce the IR losses on the power delivery networks. Thus, there is a wide voltage gap between the power bus and the digital supply rails at the point of load (PoL). Meanwhile, battery-powered portable or wearable devices favor extremely high-power-density solutions, calling for novel power conversion topologies, which have been the hottest topic in the power management IC area in the past decade. This article reviews the switched-capacitor-inductor (SCI) hybrid dc–dc buck converters from the topology "seeds" to their "leaves." Here, we define six seeds, they are: 1) three-level buck; 2) double-step down buck; 3) inductor-first buck; 4) always-dual-path buck; 5) buck–buck; and 6) multiple-output hybrid buck. We try to analyze and summarize their pros and cons, and to derive the evolution of the hybrid dc–dc converters, with milestone examples. Then, we share our observations, design intuitions, and suggestions to help the researchers and engineers to pick up and design a new SCI hybrid dc–dc converter.

INDEX TERMS 3-D power delivery for chiplet, buck–boost, buck converter, DC–DC conversion, hybrid converter topology, integrated voltage regulator (IVR), multilevel, multiphase, multiple-output, switched-capacitor (SC) converter.

I. INTRODUCTION

SWITCHING-MODE power converter plays a more and more important role in both high-performance computing (HPC) and extremely compact portable device applications. To reduce the IR losses on the power delivery networks, the conventional 12-V power bus on board has been elevated to 48 V, while the digital loads dive into sub-1-V region [1], [2], as shown in Fig. 1. Thus, there is a wide voltage gap between the power bus and the digital supply rails at the point of load (PoL), calling for new system structures and novel dc–dc topologies.

Fig. 2 shows the requirements of hybrid dc–dc converter for different applications. Both high efficiency and high-power density are two key specifications for dc–dc converters. For high-current applications that do not care too much about the solution size, for example, the data centers and HPC, power conversion efficiency is the first priority [3]. For applications that need to be extremely compact and miniaturized, like the wearable and portable devices, power density would be more important. In particular, for drones and micro-flying robots, the weight of a solution is a prioritized requirement, demanding for what we define

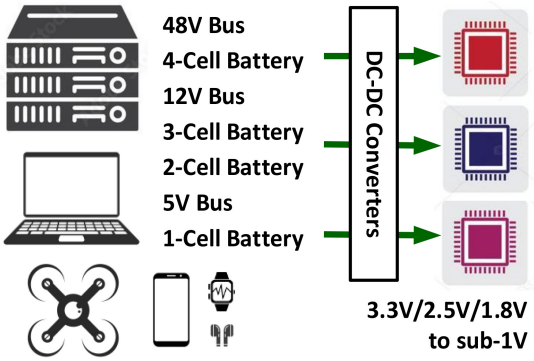

FIGURE 1. Application scenarios of hybrid dc–dc converter for XPUs.

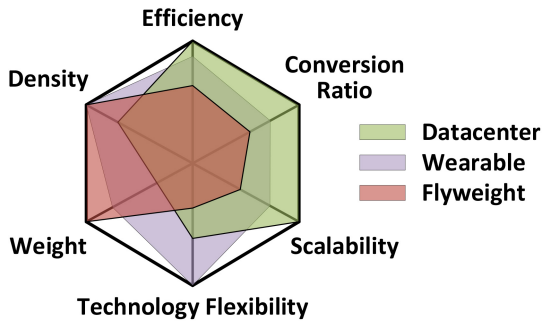

FIGURE 2. Requirements of hybrid dc–dc converter for different applications.

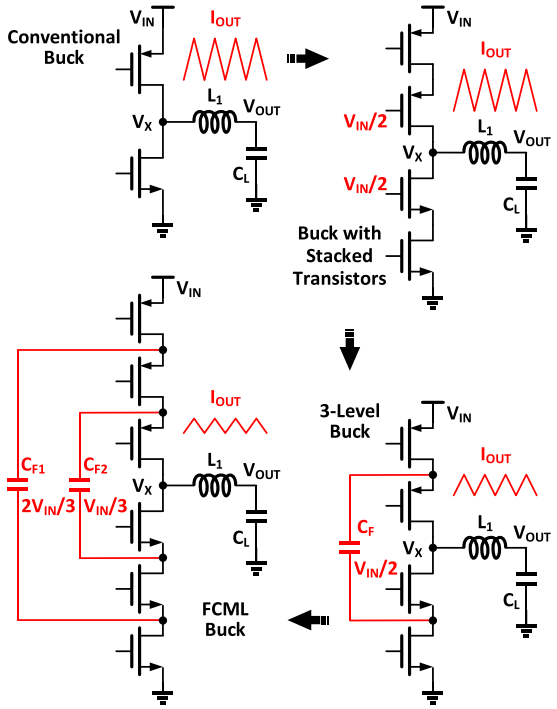

FIGURE 3. Conventional buck with single or stacked-MOSFET, 3-level buck, and FCML buck converters.

here as "flyweight" power conversion solutions. Therefore, according to the target applications, we may define the power density with a unit of Watt per unit volume or Watt per unit weight. For HPC and chip-scale solutions, the maximum current instead of maximum power is more straight forward to represent the power delivery bottleneck. Thus, current density is also a popular metric.

The performances of highly integrated power converters heavily depend on both the figure of merit (FoM) of active devices and the quality factors of passive components (especially the inductor). As the size and quality factor of an inductor are limited by physical constraints, and a large inductance can only be obtained with multiple turns of winding, thus, a high-current power inductor would be bulky and costly. On the other hand, the energy density of a capacitor increases naturally with advanced processes [4]. Thus, switched-capacitor-inductor (SCI) hybrid dc–dc converter becomes a popular choice. Nonetheless, we should find an optimum way to divide the voltages, guide the currents, and deliver the power to the load.

To bridge this gap with a large voltage conversion ratio (VCR) dc–dc converter, several research groups proposed many innovative topologies and a lot of efficient operation schemes [5] and summarized design guidelines [6]. The basic idea of an SCI hybrid dc–dc converter is to use switched-capacitor (SC) cells to reduce the voltage swing on the power inductor such that a smaller inductor can be used. On the other hand, it also brings the drawback of slow transient response as the inductor current slew rate also becomes smaller. When an SC path is in-parallel with the power inductor, it can share the current stress on the inductor and may also provide fast transient output current, as the hard-charging current only depends on the drain–source voltage (V_{DS}) of the switches.

In this article, we review and analyze the hybrid dc–dc buck converters from the topology "seeds" to their "leaves." In Section II, we introduce the existing hybrid converters in six categories, based on their fundamental ideas. Also, we try to analyze and summarize their pros and cons, and to derive the evolution process of the hybrid dc–dc converters, with milestone examples. Then, in Section III, we share our topology summary, observations, design intuitions, and suggestions for new/suitable topologies. In Section IV, we give our design steps and considerations to help the researchers and engineers to pick up the SCI hybrid dc–dc converters for future works. Finally, we draw conclusions in Section V.

II. TOPOLOGY SEEDS TO LEAVES

To better understand various hybrid dc–dc converters, we define and discuss six seeds and their leaves in this section: 1) three-level buck; 2) double-step down (DSD) buck; 3) inductor-first buck; 4) always-dual-path (ADP) buck; 5) buck–buck; and 6) multiple-output hybrid buck converter. The six seeds are somewhat related in a development path.

A. THREE-LEVEL BUCK

Fig. 3 shows the evolution from a simple conventional buck to a stacked-transistor buck, and from 3-level buck [7] to

flying capacitor multilevel (FCML) buck converters [8]. It is proven that stacked low-voltage (LV) transistors would have considerably better FoM of $R_{ON}Q_G$ than a single high-voltage (HV) transistor when they are dealing with the same voltage stress [9], where R_{ON} and Q_G are the on-resistance and gate charge of the switch, respectively. Besides the good switching characteristics, it allows the power switch to be implemented with standard and advanced logic devices, which avoids the cost of extra processing steps for HV devices; and excellent switching characteristics also leads to a reduced chip size [9].

When the input–output voltage gap is large, a conventional buck would have a large voltage swing on the power inductor, resulting in a large current ripple. Then, it is natural to add a flying capacitor C_F between the stacked transistors to obtain a 3-level converter with a reduced inductor voltage swing. With more stacked transistors and more flying capacitors, we will get an FCML buck converter, allowing us to use a much smaller inductance.

However, there are two critical issues associated with the FCML buck. First, all the output current, which is the largest current in a step-down converter, would flow through the power inductor, generating large I^2R conductions loss on the inductor. Second, as the FCML is "series–series" operation for the SC network, the largest current would also flow through all the switches and the flying capacitors. More importantly, usually, all the power switches are integrated on a single chip while the flying capacitors are off-chip, which means the largest current would flow in and out of the chip multiple times, generating large additional conduction losses on the I/O pads, bonding wires, routes, and contacts.

Three-level and FCML bucks need additional control loops for the flying capacitor voltage V_{CF} balancing. Because the capacitor currents are defined by the power inductor, when the switching phase durations and component values have mismatches and variations, the capacitor voltage will shift from its ideal value and may generate unwanted voltage stress on the switches. A dual-branch 3-level converter with cross-connected flying capacitors can solve this balancing issue without an additional control loop [10].

Another advantage of an FCML buck is its wide output range. But, for most of the applications mentioned in this article, we only need a large VCR, not a wide output range. Therefore, we may simplify the operation states or modify the SC topology for a higher efficiency.

As shown in Fig. 4, with the 3-level converter as the "seed," we can integrate any SC block with a post-stage inductor for voltage regulation. For example, [11] and [12] incorporate traditional Dickson converters into hybrid solutions. Reference [13] cascaded two SC stages to further reduce the input voltage.

Similarly, besides the step-down conversion, there are also structures implemented to boost or step-up/step-down the input voltage to implement boost [14] or buck–boost hybrid converters [15], [16], also shown in Fig. 4. In this way, the right-half-plane (RHP) zero in traditional boost and buck–boost converters is eliminated. Nonetheless, the efficiency would be degraded if the additional switches let the existing switches see a higher voltage, because then they need to use higher voltage rating devices.

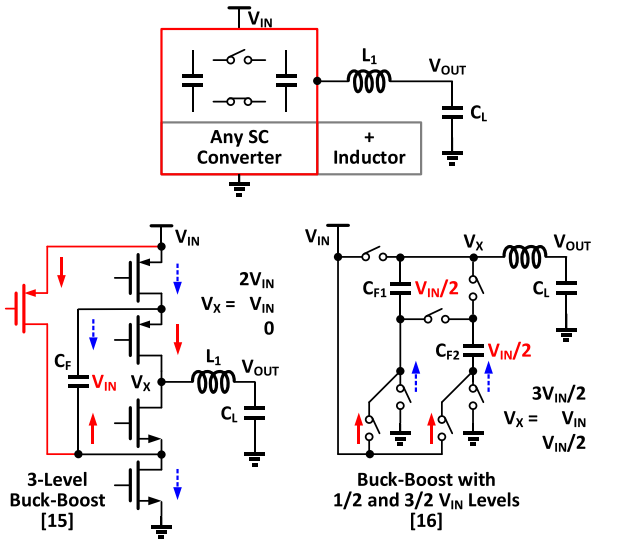

FIGURE 4. Three-level buck–boost converters, and the concept of any SC converter with post-stage inductor topology.

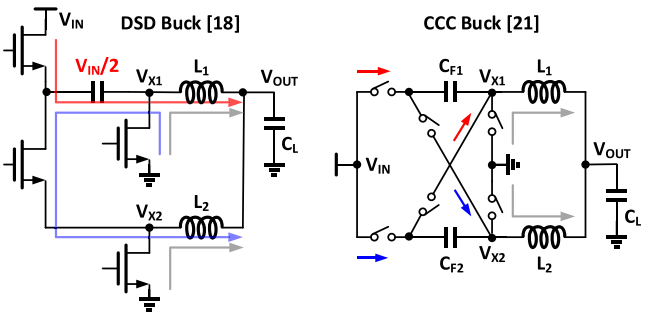

FIGURE 5. DSD topology and CCC topology.

B. DOUBLE-STEP DOWN BUCK

When the application desires a higher current, two or more inductors would be used to share the high output current [17]. Combining the 2:1 SC converter and two-phase buck topologies, the DSD buck topology is a minimalist design [18]. Then, it becomes a popular product for server and laptop applications.

Fig. 5 shows the DSD topology and its variant capacitor cross-connected (CCC) or, namely, symmetrical DSD topology [19], [20], [21]. A DSD converter has an intrinsic rough current balance between the two inductor branches, because the flying capacitor follows charge balance in a steady state. But the capacitor charge balance does not necessarily mean inductor current balance, when duty cycle or component mismatch happens, the two branches would still have certain current mismatch [22].

There is a tradeoff between inductor current ripple and transient response. For smaller current ripple, we use hybrid

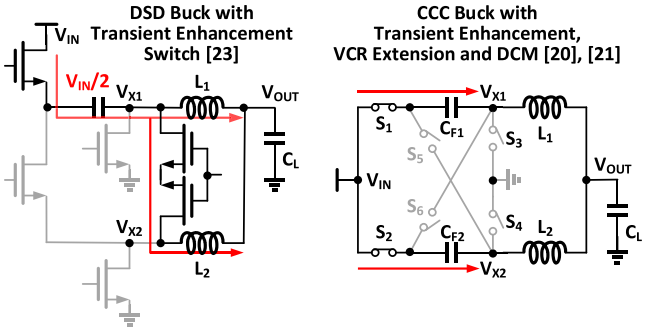

FIGURE 6. DSD buck with transient enhancement switch, and CCC buck with transient enhancement and VCR extension.

topology to reduce the inductor voltage swing, but it also reduces the inductor current slew rate during load transient. Meanwhile, a conventional DSD converter cannot energize its two inductors at the same time; otherwise, one low-side switch will see the high voltage $V_{\rm IN}$, doubling its voltage rating. Therefore, a conventional DSD converter has a severe drawback of slower transient response speed.

To address this issue, as shown in Fig. 6, additional transient enhancement switches can be added for energizing the two power inductors at the same time [23], while the CCC converter can have additional operation state for fast energizing the inductors [21]. Also, we proposed in [21] to compare the transient performance of the DSD and CCC works using the normalized output undershoot with respect to the theoretical minimum undershoot of the conventional DSD converter. With $D > 0.5$ operation state in [21], we obtained a normalized undershoot value of only 0.73.

Notice that the additional state for CCC buck can also help to extend its VCR range from sub-1/4 to sub-1/3, as discussed in [20]. And also, we find that it enables the CCC to operate in discontinuous conduction mode (DCM) without reverse inductor current. Because S_3 and S_4 can be both off during this state, then, both inductors can be energized from zero current.

Fig. 7 shows some representative examples. To further extend the VCR, more switches and capacitors can be employed in front of the DSD topology [24], [25], [26], [27]. The high-voltage prestage may have a different switching frequency $F_{\rm SW}$ with the post-stage DSD [25]. An SC ladder topology is merged with DSD in [26]. To deliver higher output current, the topology can be equipped with more inductors [18], [28], [29], [30]. We will come back to this topic in the topology summary section.

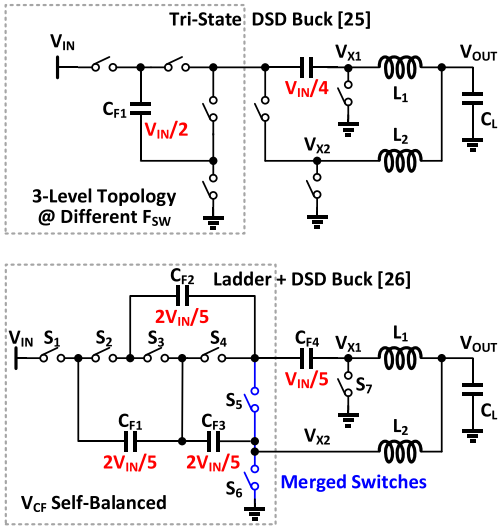

FIGURE 7. Examples with more switches and capacitors merged with the DSD.

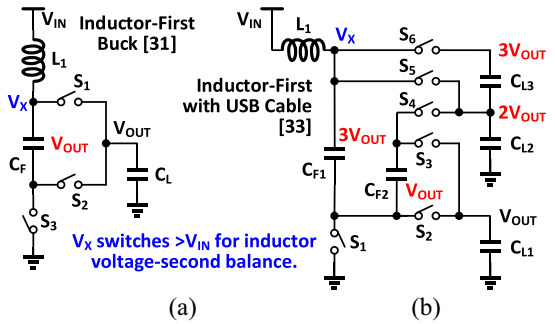

FIGURE 8. Inductor-first topologies: (a) with one flying capacitor and (b) with a more complex SC network for more outputs and wider VCR.

C. INDUCTOR-FIRST BUCK

As depicted in Fig. 8, different from the traditional buck, an inductor-first structure swaps the positions of the inductor and the SC network [31], [32], [33]. In another way around, when reverse operating the inductor-first buck in [31], it becomes the KY boost converter in [14].

For the passive components, the dc resistance (DCR) of the inductor is one of the main sources of power loss. On the other hand, capacitors have dc-value derating versus its stored voltage, which means that the capacitors used in HV stage require large volume and cost. Thus, placing the inductor at the input side of a buck converter allows it to operate with input (lower) current and to block high input voltage. In addition, the inductor-first topology would have a continuous input current which significantly reduces or eliminates the need for input capacitors. Moreover, the continuous input current feature is favorable for electromagnetic interference (EMI) considerations.

Considering the power inductor is followed by an SC network, the inductor voltage swing on the SC side will be an integer multiple of $V_{\rm OUT}$. When there is only one flying capacitor, the maximum voltage on the SC terminal for the inductor can only reach up to 2 $V_{\rm OUT}$. As the switched inductor follows voltage-second balance in a steady state, the simple inductor-first structure in [32] is limited to a VCR of $V_{\rm OUT}/V_{\rm IN} = 1/(2-D)$, where D is the duty cycle. In other words, $V_{\rm IN} < 2V_{\rm OUT}$, which restricts its application in many scenarios.

There are two main directions for the topology improvement. The first one aims to increase the VCR and overall

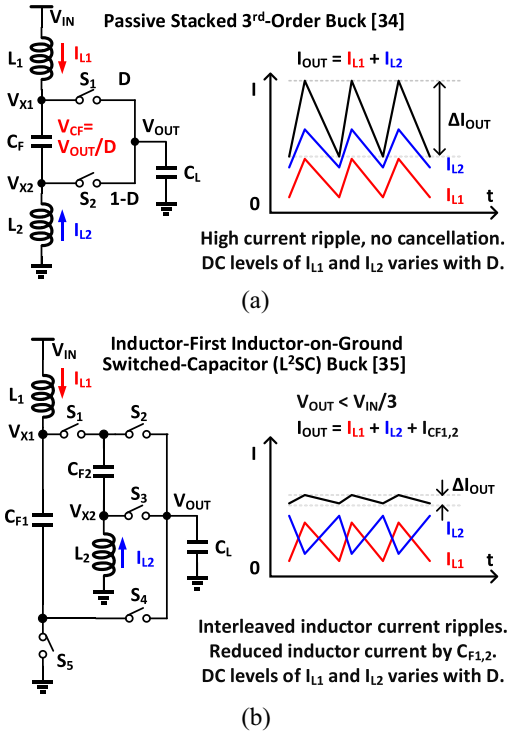

FIGURE 9. Topologies of (a) passive stacked 3rd-order buck and (b) L²SC buck.

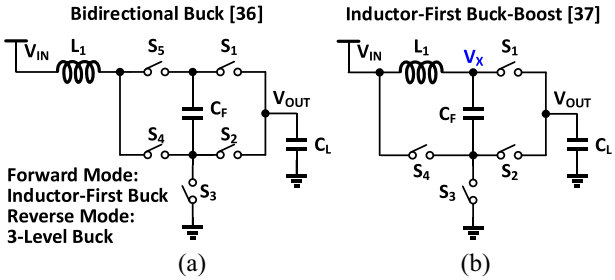

FIGURE 10. Convert the inductor-first buck into a (a) reconfigurable bidirectional buck converter or (b) buck–boost converter.

performances of the inductor-first structure. To increase the VCR, we need to add more flying capacitors to step down the output voltage. As shown in Fig. 8(b), the work in [33] obtains a maximum VCR of 1/3 with multiple capacitors and a complex SC network.

The key to increase the VCR is to boost the voltage on the flying capacitors instead of using too many capacitors. As shown in Fig. 9, the inductor-on-ground cell breaks the voltage tie between $V_{\rm OUT}$ and $V_{\rm CF}$, allowing the flying capacitor to have a higher voltage. Now, $V_{\rm CF} = V_{\rm OUT}/D$, which can be adjusted by duty-cycle control.

The passive-stacked 3rd-order buck (PS3B) in [34] utilizes the inductor-on-ground cell to obtain a VCR of D and to have two inductors sharing the output current. Also, it ensures continuous input, ground, and output currents. However, this structure suffers from large current ripples because both inductor currents rise or fall simultaneously. And, when D deviates from 0.5, the current distribution between the two inductors becomes uneven, leading to increased conduction losses.

We proposed in [35] an inductor-first inductor-on-ground SC (L^2SC) multipath hybrid dc–dc converter. The two inductors and two flying capacitors operate with interleaved charging and discharging states, significantly reduced the current ripple at light load. Furthermore, it introduces a parallel capacitor path to reduce the current flowing through the inductors, advancing the efficiency and power density tradeoff.

The second direction involves reconstruction of the inductor-first topology for specific applications that require flexible VCRs [36], [37]. As depicted in Fig. 10, our work in [36] proposed a reconfigurable bidirectional buck converter, reusing the USB cable as a power inductor. This reconfigurable structure combines the inductor-first operation for the forward mode and a three-level buck operation for the reverse mode. Based on the inductor-first buck, [37] proposed a buck–boost converter with always reduced conduction loss, by adding a switch in parallel with the inductor. Moreover, this hybrid buck–boost converter has always only one switch conducting on the main current paths, achieving outstanding efficiency even with a tiny power inductor. This topology also belongs to the category of ADP converter that to be discussed next.

D. ALWAYS-DUAL-PATH BUCK

Another way to reduce the inductor current is to have a parallel SC path to share the current [38]. In general, a capacitor has higher energy density compared to an inductor, and the capacitor energy density improves proportionally with the technology, while that of an inductor is limited by physical space constraints. Meanwhile, for space-constrained application scenarios, designers would like to have a small-volume power inductor, which would have higher DCR and thus larger conduction loss.

Fig. 11 shows the dual-path [38] and the state-of-the-art ADP converters. An SC parallel path operates in either hard-charging mode [39], [40], [41], [42] or soft-charging mode [43] would help to improve the efficiency, power density, and transient response at the same time. Basically, all the ADP examples in Fig. 11 are based on series–parallel SC or modified series–parallel SC converter [44]. For [39], due to the absence of a path directly to ground for the inductor, the VCR is limited to >1/3, making it unsuitable for wide voltage gap applications. In [40], the VCR is <1/2, with the inductor connects to the ground in certain one or two phases. In [41] and [42], the VCR can be <1/3 with reduced voltage swing across the inductor.

However, for ADP converters with only one inductor, there will be a capacitive current path in both phases. Then, there is a general issue. When the duty cycle largely deviates from 0.5, one phase will have obviously a shorter duration, squeezing the hard-charging time. Then, there will be large current spikes and thus large root-mean-square current $I_{\rm RMS}$

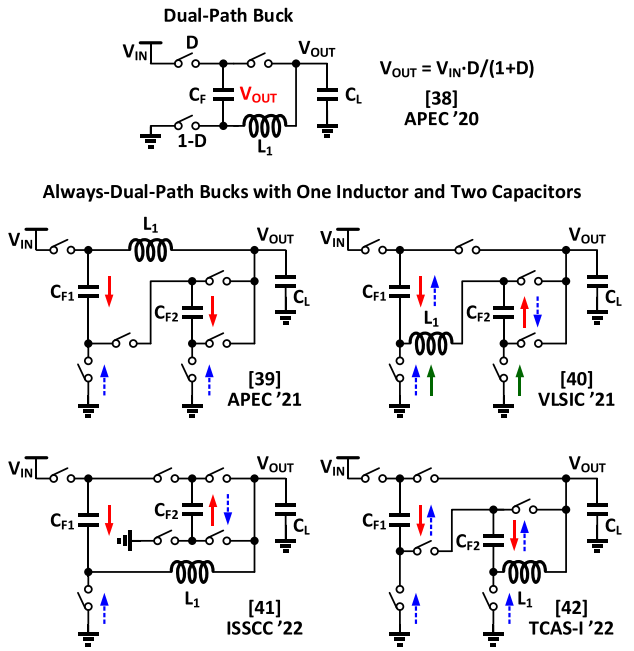

FIGURE 11. Dual-path and ADP hybrid converters.

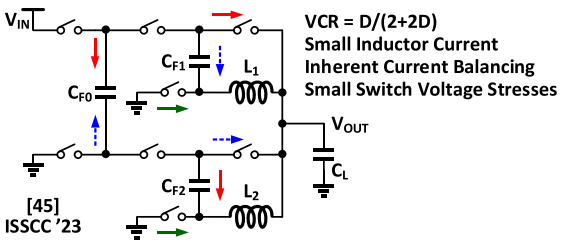

FIGURE 12. Dual-inductor quad-path hybrid dc–dc converter.

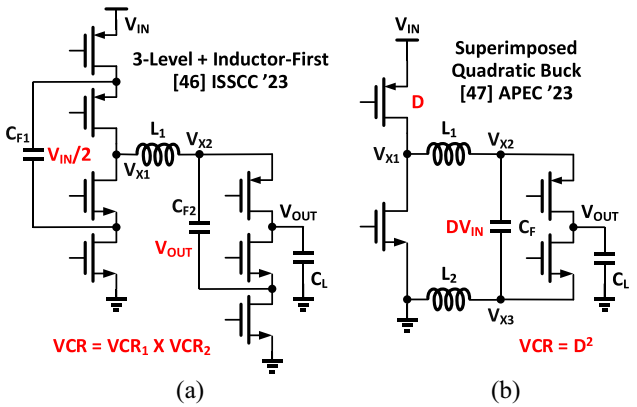

FIGURE 13. Merged buck–buck converters: (a) 3-level converter merged with inductor-first converter and (b) buck merged with PS3B converter.

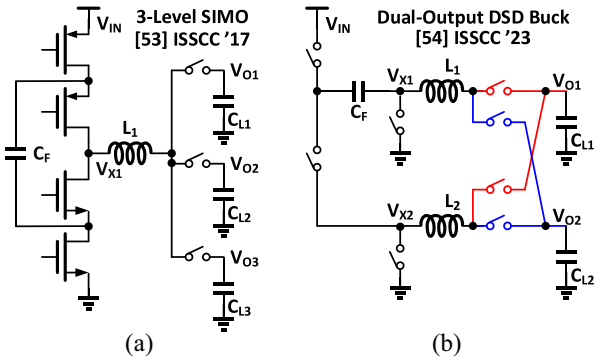

FIGURE 14. Multiple-output hybrid dc–dc converters: (a) 3-level converter with multiple outputs and (b) DSD converter with dual outputs.

for the shorter phase, generate larger output ripple and EMI, and degrade the efficiency.

Combining the concepts of dual-path and DSD structures, we arrive at the solution of dual-inductor quad-path buck topology [45], as shown in Fig. 12. It has a large VCR of $D/(2+2D)$, small inductor currents, and small voltage stress of $V_{\rm IN}/2-V_{\rm OUT}$ on half of the switches. Like the DSD buck, the inductors have inherently current balancing as C_{F0} would charge and discharge equally during a steady state. Moreover, the above-mentioned hard charging current spike issue can be significantly alleviated, as the C_{F1} and C_{F2} discharging duration has been considerably extended in this topology, allowing the use of smaller switches for the capacitor charge transfer. DCM operation has also been demonstrated in [45] with good efficiency as well.

E. BUCK–BUCK CONVERTER

The power inductor can also be placed in the middle of the hybrid converter. As shown in Fig. 13(a), an interesting idea is to merge a conventional buck with an inductor-first buck, sharing one inductor, namely, single-inductor multistage buck converter [46]. Or, the work [47] in Fig. 13(b) uses two inductors, one in the middle, one on the ground, to extend the VCR as the superimposed quadratic buck converter. Since the "seed" idea is to merge two buck converters, its VCR equals to the product of those of the two cascaded stages, we may call this kind of converters as buck–buck converter.

Similar to the inductor-first buck, putting the inductor in the middle can also reduce certain inductor current compared to a conventional buck. The inductor in the middle can also separate the switching frequencies on its two sides. The high side using HV devices can use a lower $F_{\rm SW}$.

F. MULTIPLE-OUTPUT HYBRID BUCK

When it comes down to multicore application, per-core individual power supply has been proven to be an energy-saving system approach [48], [49]. Prior multiple-output designs mainly focused on how to effectively reuse a single power inductor for multiple outputs [50], [51], [52]. However, they are only suitable for low-power applications. When it comes to high output current XPU applications, a single power inductor can hardly handle such high current at tens of amperes level for multiple outputs.

With the hybrid conversion concept and sharing the flying capacitor or intermediate filtering capacitors, a couple of multiple-output hybrid dc–dc converters were proposed recently [53], [54], [55], [56]. We draw examples in Figs. 14 and 15.

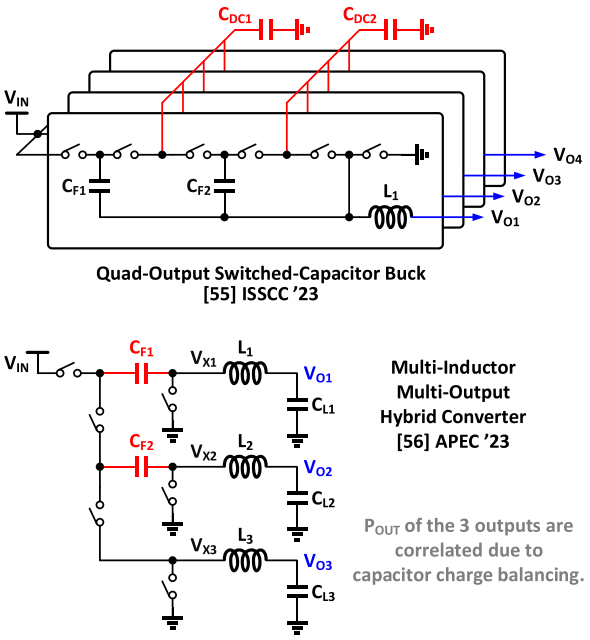

FIGURE 15. (a) Quad-output hybrid converter with shared dc capacitors and (b) multiple-output hybrid converter with shared flying capacitors.

With a three-level conversion in the front stage [53], as shown in Fig. 14(a), the power inductor would have smaller current ripple, the power switches enjoyed the benefits of advanced CMOS process, and the flying capacitor is shared among those three outputs. Also, the three-level operation does not slow down the transient response, as it can still provide high voltage swing to the power inductor during transients, obtaining small cross regulation.

On the other hand, similar to the three-level conversion, the DSD conversion also reduces the inductor current ripple. Meanwhile, it has two relatively small power inductors, capable of delivering higher output current. In [54], as shown in Fig. 14(b), four extra LV switches were added to direct the two inductor currents to two independent outputs, obtaining a two-inductor two-output solution with one shared C_F. To balance the C_F voltage and to further alleviate the cross regulation, [54] used a timing balance mechanism and a hybrid sum and deviation technique.

Nonetheless, both the above works added extra power switches on the high-current paths, like all the conventional single-inductor multiple-output converters did, adding extra conduction losses as well.

In the other way around, the two pioneering works, shown in Fig. 15, employ multiple converters, and try to share some of their capacitors for multiple outputs, thus, to arrive at a higher overall power density and efficiency [55], [56]. Notice that the dc capacitors in [55] do not participate in energy transfer like the flying capacitor does. On the other hand, the shared flying capacitors in [56] need to have charge balance in a steady state, and thus the output power of the three outputs are highly correlated. Also, similar to single-output hybrid converters, it will suffer from load transient response issues.

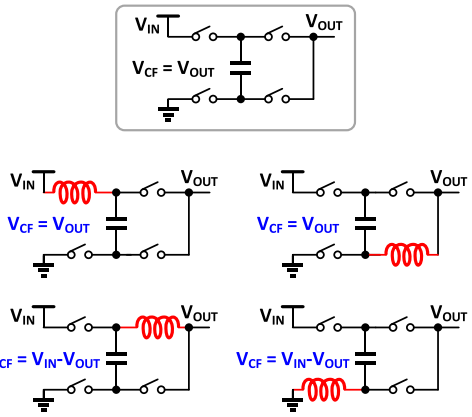

FIGURE 16. Turn the 2:1 SC converter into hybrid converters by replacing any one of the switches with an inductor.

III. TOPOLOGY SUMMARY

From the discussions above, we can find a simple way to invent or reinvent a new hybrid dc–dc topology [6]. With the examples shown in Fig. 16, we find that we can obtain a new (but not necessarily new) hybrid converter by replacing any one of the switches in an SC converter with a power inductor [57]. The embedded power inductor can be on the input side, the output side, or in the middle of the topology [39], [40], [41], [42]. Then, the SC converter becomes a hybrid converter! Furthermore, we can also replace two switches with two power inductors [24], [34], [35]. Again, a new hybrid converter!!

But, with two or more inductors, we should not establish a state with two inductors in series which will generate unwanted energy loss, similar to the charge redistribution loss when two capacitors connect in parallel. And of course, circuit designers still need to analyze the VCR, small-signal transfer function, switch voltage stresses, and inductor current stresses of the new hybrid converter. Although some SC converters could be very complicated with many switches and capacitors, eventually, only a handful of topologies would make sense and be suitable for a targeted application.

Fig. 17 shows the classic SC converters of ladder, Dickson [58], series–parallel, and Fibonacci converters, and how prior arts turned them into hybrid converters [24], [26], [27], [28], [29], [30]. As these hybrid converters are originated from the classic SC topologies, they will most likely inherit the pros and cons of these SC topologies, which means we should revisit the analyses and comparison of these SC topologies. The total V·A metric of the switches, which is the sum of the products of the switch voltage and current stresses, can be used to evaluate the switch utilization of the power converters [59].

Now, with the routes shown in Fig. 18, let us discuss what would be the favorable basic circuit cells and building blocks for an SCI hybrid dc–dc converter [6].

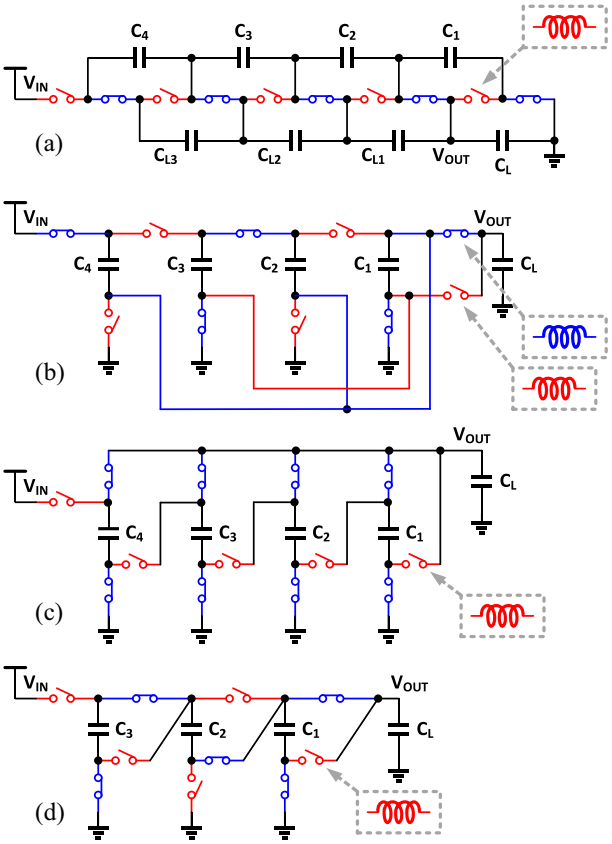

FIGURE 17. Transforming the classic SC converters into hybrid converters: (a) ladder, (b) Dickson, (c) series–parallel, and (d) Fibonacci.

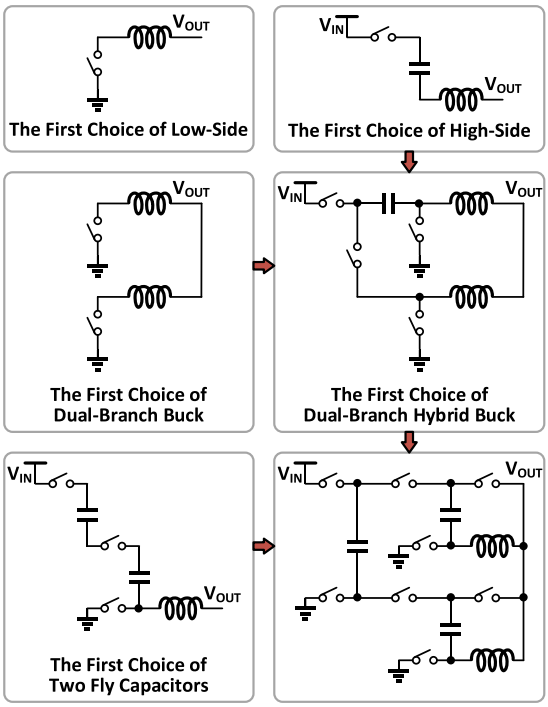

FIGURE 18. Basic circuit cells and building blocks for a hybrid converter.

A. GOOD LOW-SIDE SWITCH

For large VCR step-down dc–dc conversion, when one side of the power inductor connects to the output node, the other side would usually be switched to the ground for most of the time. Therefore, the circuit cell with a single switch that connects the power inductor to the ground is a must-have for high efficiency. Meanwhile, the transistor stacking technique can be easily applied here to withhold high-voltage stress with two or more LV transistors, and improves the FoM of the switches [8].

B. SERIES CAPACITOR(S) ON THE HIGH SIDE

Series capacitor(s) on the high side is for reducing the power inductor voltage stress [43]. For a very large VCR, multiple capacitors may be involved. Therefore, from the topology selection perspective, the high-side part has the most variations [60], [61].

There are several considerations in selecting the high-side series capacitor topology. One major concern is the voltage ratings of the capacitor(s) and the switches. HV capacitor has much less energy density while connecting two or more capacitors in series also results in smaller equivalent capacitance. As the voltage ratings of the capacitors and switches are technology process dependent, and only have limited selections, the high-side series capacitor topology design is highly related to the available component voltage ratings. Bootstrap circuit and intermediate voltage rail designs are also very important for reducing the silicon area and optimizing the switching losses [21].

C. SWITCHED-CAPACITOR HARD CHARGING

When two capacitors with different voltages exchange charges in an SC converter, a high peak initial current would happen, diminishing the benefit of smaller R_{ON} of the switches. Conventionally, hard charging is considered as a disadvantage, as it is the root cause for the inherent charge redistribution loss of an SC converter. However, hard charging has three advantages. First, hard charging provides a large output current to the load, as there is no current limiting component (inductor) on the current path. As capacitors generally have larger energy storage density compared to inductors, we can have large capacitance to reduce the dV on the capacitors and to mitigate the hard charging loss [40]. Second, hard charging provides instant response to output voltage change [62]. When output voltage drops, the SC instant output current increases proportional to the V_{DS} of the power switches, alleviating the shortcoming (slower transient response with reduced inductor voltage swing) of hybrid dc–dc converters. Third, hard charging provides automatic C_F voltage balancing, thus, simplifies the control loop design [10].

D. RESONANT SC OPERATION HELPS THE EFFICIENCY

In a resonant SC operation, the resonant inductor shapes its current waveform into quasi-sinusoidal, reducing the RMS current of the switches when conducting the same

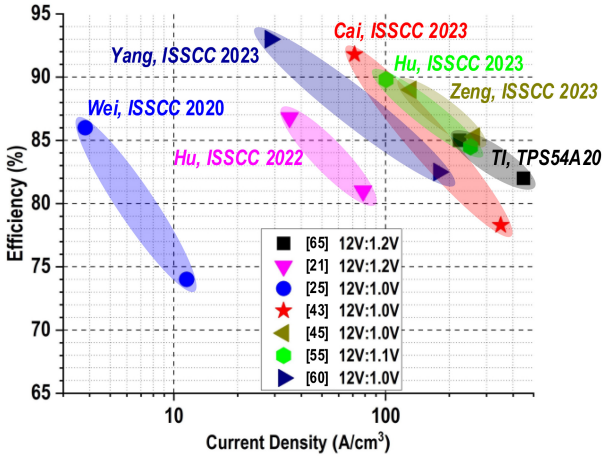

FIGURE 19. Key performance comparison of recent 12-V step-down hybrid dc–dc converters.

average current in the slow-switching limit (SSL) region [63]. To deliver the same amount of power, resonant SC can operate at a lower frequency when compared to an SC converter [43], [64]. On the other hand, the resonant inductor also limits the instant output current, and its DCR adds conduction loss. Usually, the value of a resonant inductor is much smaller than that of the power inductor in a typical buck converter, so its DCR can be negligible. Overall, resonant SC operation would help to improve the peak power conversion efficiency, but would not improve the efficiency and power density tradeoff.

E. HIGH CURRENT, MULTIPLE PATHS, MULTIPLE INDUCTORS

In the past two decades, single-inductor multiple-output dc–dc converter has also been a very popular research topic. However, when it comes to high-current applications, the high-current stress on the power inductor forces people to use multiple inductors. In the past year, a few multioutput converters with multiple inductors have been proposed for high-current applications [54], [55], [56].

F. PERFORMANCE COMPARISON AND FoM

Fig. 19 compares the power conversion efficiency and the current density of recent highly integrated hybrid dc–dc converters with 12-V input and 1.0–1.2-V output. Here, the hybrid converter volume includes the inductors and flying capacitors. The recent works obtained good peak efficiencies for the 12–1 V application, while the DSD product [65] still holds the highest current density but only for 12–1.2 V (not to 1 V) conversion. Since the SCI hybrid dc–dc converters involve much more parameters than the conventional converters, it is hard to have a fair and comprehensive comparison between different topologies. To better evaluate the highly integrated hybrid converters, we proposed in [62] an FoM of hybrid dc–dc converters as

$$\text{FoM} = \frac{J \cdot V_{\text{IN}}}{(1-\eta) \cdot V_{\text{OUT}}} \tag{1}$$

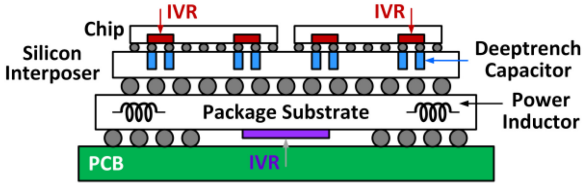

FIGURE 20. Hybrid dc–dc conversion for 3-D power delivery.

where η is the peak efficiency, and J is the current density at peak efficiency. Here, a large VCR, high-current density, and high efficiency result in a better FoM.

IV. DESIGN CONSIDERATIONS

As we mentioned in the introduction part, although we ultimately would like to have a "perfect" (high efficiency, high power density, high current, large VCR, flexible, and scalable) solution, different applications would have slightly different focuses on the above-mentioned specifications. When we are designing converters for server rack and HPC, efficiency is the priority. For portable devices, robots, and drones: volume and weight are more of concern.

For a larger VCR, multistage SC would be favorable. Meanwhile, for multistage step-down conversion, the prestage would process higher voltage but lower current, while the post-stage would deal with lower voltage but higher current. In order to reduce the passive component sizes and to obtain fast transient responses, a higher switching frequency would be essential, on the other hand, that would decrease the efficiency. Thus, a multistage converter should take the advantages of multiple device voltage ratings and advanced packaging technology. The prestage board-level converters use HV devices and high-Q inductors and operate at lower F_{SW} of hundreds of kHz, while the post-stage highly integrated converters use LV (1.8 or 1 V) devices and integrated passives and operate at higher F_{SW} in 1 to tens of MHz range.

Topologies with multipath would naturally be more feasible for the post-stage. Also, we may easily employ more power inductors to share the large current in a multipath topology. The number of inductors for a dc–dc buck converter is mainly decided by three factors: 1) the output current level; 2) the available space; and 3) the equivalent switching frequency. Prior examples show reference numbers ranging from 1 to 10 A/inductor. Here, we capture the value of current per inductor around the peak efficiency point from the references. In space-limited scenarios, a smaller inductor with low-Q may result in 1 A/inductor [35]. For high-current board-level designs with discrete components, bulky high-Q inductors may support 10 A/inductor [28].

Fig. 20 illustrates the conceptual cross section of a vertical package solution with integrated voltage regulators (IVRs). For extremely compact 3-D chiplet solution with advanced packaging technologies, we may have miniaturized package or parasitic inductors that only support sub-1A

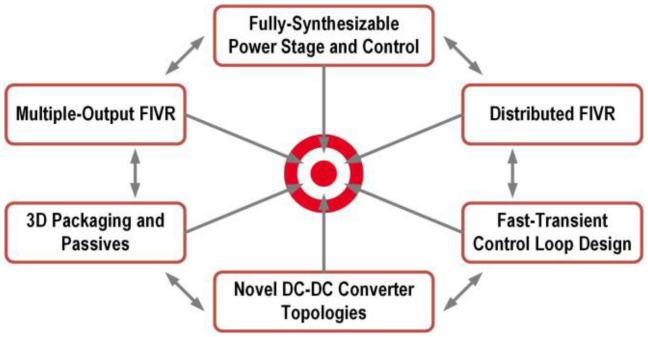

FIGURE 21. Multiple aspects of hybrid power management solution for hitting the advanced power delivery target.

per inductor [66], [67], [68]. The IVR in [49] with an in-package substrate inductor technology called coaxial magnetic integrated inductor (CoaxMIL) [69] demonstrated ∼86% peak efficiency for a 1.8–0.7-V conversion with over 1 A per inductor.

Also, we may have high-density deep-trench or metal–insulator–metal (MIM) capacitor technologies. Then, it would be more feasible to add post-stage SC converters on chip [70], [71], [72], which may also remove the necessity of post-stage on-chip low-dropout (LDO) regulators for dynamic voltage scaling (DVS), as the SC converters can also provide fast transient as well as the LDO does [71]. Eventually, an SC power converter grid may be formed with 3-D packaging and miniaturized passives [73].

In terms of topology and inductor selections, first, we would love to have high-Q inductor in all cases. But for the highly integrated compact solutions, only miniaturized inductor with high DCR can be used. Then, we can choose the capacitor parallel inductor dual-path topologies to reduce the average inductor current [41], [43], [45]. For board-level design, the DSD family, including CCC [21] and quad-step down topologies [30] with less complexity and good inductors, is a good choice. For chiplet 3-D integration, where the high-density capacitors are closer to the load and power delivery suffers from relatively larger I^2R losses, inductor-first buck, and inductor-in-the-middle buck–buck are the possibilities.

Another very important future direction is digitalization of the analog and power-conversion circuits. Both digitally controlled dc–dc power converters [74] and digital LDO regulators [75] have been widely studied. The digital controllers can be more flexible, easy reconfigurable, and process scalable compared to the analog counterparts, especially for high-current applications. One possible step further, new power converter topologies could also be synthesized, there is a recent intriguing development in the domain of automated topology generation [76], by refining the SCI hybrid dc–dc converter design into mathematical questions, equations, and solutions.

Fig. 21 summarizes multiple aspects of fully IVRs (FIVRs) or IVR for hybrid dc–dc power delivery to hit the target. The fully synthesizable, flexibly distributed, multiple-output, fast transient features are highly favorable, to be enabled by novel converter topologies with advanced packaging and passive technologies, and to be design-cycle accelerated by design automation.

V. CONCLUSION

This article reviews the recent very popular topic of SCI hybrid dc–dc converters. We defined six routes or categories for the hybrid topologies, summarized the existing converters into these six routes, and discussed their advantages, drawbacks, and remaining issues. Then, we extracted the favorable basic cells and building blocks for hybrid converters and proposed a way to invent or reinvent new hybrid topologies. Finally, we introduced the design considerations for future IVRs and FIVRs.

Power converter designs are very application driven. The SCI hybrid dc–dc converter topic provides plenty of room for innovations and performance improvements. With the suggested design considerations given in this article, we may easily build hybrid dc–dc converters with favorable basic circuit cells and building blocks. Looking forward, we see that hybrid dc–dc converters would also find their applications in multiple-output and chiplet 3-D integration scenarios, with the highest integration level.

REFERENCES

[1] X. Li and S. Jiang, "Google 48 V power architecture," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017.
[2] Q. Ouyang, R. Samsi, and J. Zhou, "Increasing the power density and efficacy of datacenters using a two-stage solution for 48V power distribution." 2022. [Online]. Available: https://www.monolithicpower.com/
[3] L. Su and S. Naffziger, "Innovation for the next decade of compute efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 8–12.
[4] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018.
[5] C.-H. Chan et al., "Trending IC design directions in 2022," *J. Semicond.*, vol. 43, no. 7, Jul. 2022, Art. no. 71401.
[6] Y. Lu, G. Cai, and J. Huang, "Favorable basic cells for hybrid DC–DC converters," *J. Semicond.*, vol. 44, no. 4, 2023, Art. no. 40301.
[7] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.
[8] C. Schaef et al., "8.1 A 93.8% peak efficiency, 5V-input, 10A max ILOAD flying capacitor multilevel converter in 22nm CMOS featuring wide output voltage range and flying capacitor precharging," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 146–148.
[9] E. A. Burton et al., "FIVR—Fully integrated voltage regulators on 4th generation Intel Core SoCs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 432–439.
[10] C. Wang, Y. Lu, M. Huang, and R. P. Martins, "A two-phase three-level buck converter with cross-connected flying capacitors for inductor current balancing," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13855–13866, Dec. 2021.
[11] P. Assem, W.-C. Liu, Y. Lei, P. K. Hanumolu, and R. C. N. Pilawa-Podgurski, "Hybrid Dickson switched-capacitor converter with wide conversion ratio in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, Sep. 2020.
[12] M. Ashourloo et al., "A masterless fault-tolerant hybrid Dickson converter with 95.3% peak efficiency 20V-to-60V input and 3.3V output for 48V multi-phase automotive applications," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 258–260.

[13] Z. Xia and J. Stauth, "A two-stage cascaded hybrid switched-capacitor DC-DC converter with 96.9% peak efficiency tolerating 0.6V/μs input slew rate during startup," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 256–258.

[14] K. I. Hwu and Y. T. Yau, "A KY boost converter," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2699–2703, Nov. 2010.

[15] J. Baek et al., "11.7 A voltage-tolerant three-level buck-boost DC-DC converter with continuous transfer current and flying capacitor soft charger achieving 96.8% power efficiency and 0.87μs/V DVS rate," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2020, pp. 202–204.

[16] M.-W. Ko et al., "A 97% high-efficiency 6μs fast-recovery-time buck-based step-up/down converter with embedded 1/2 and 3/2 charge-pumps for li-lon battery management," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2018, pp. 428–430.

[17] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000.

[18] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of double step-down two-phase buck converter for VRM," in *Proc. Int. Telecommun. Conf. (INTELEC)*, Sep. 2005, pp. 497–502.

[19] M. Huang, Y. Lu, T. Hu, and R. P. Martins, "A hybrid boost converter with cross-connected flying capacitors," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2102–2112, Jul. 2021.

[20] J. Huang, C.-S. Lam, Y. Lu, and R. P. Martins, "A symmetrical double step-down converter with extended voltage conversion ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 12, pp. 4761–4773, Dec. 2022.

[21] T. Hu, M. Huang, R. P. Martins, and Y. Lu, "A 12-to-1 flying capacitor cross-connected buck converter with inserted D > 0.5 control for fast transient response," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3207–3218, Nov. 2023.

[22] P. S. Shenoy et al., "Automatic current sharing mechanism in the series capacitor buck converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 2003–2009.

[23] J. Yuan, Z. Liu, F. Wu, and L. Cheng, "A 12V/24V-to-1V DSD power converter with 56mV droop and 0.9μs 1% settling time for a 3A/20ns load transient," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 1–3.

[24] G.-S. Seo, R. Das, and H.-P. Le, "A 95%-efficient 48V-to-1V/10A VRM hybrid converter using interleaved dual inductors," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 3825–3830.

[25] K. Wei, Y. Ramadass, and D. B. Ma, "11.1 A direct 12V/24V-to-1V 3W 91.2%-efficiency tri-state DSD power converter with online VCF rebalancing and in-situ precharge rate regulation," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2020, pp. 190–192.

[26] C. Chen, J. Liu, and H. Lee, "A 2.5-5MHz 87% peak efficiency 48V-to-1V integrated hybrid DC-DC converter adopting ladder SC network with capacitor-assisted dual-inductor filtering," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 234–236.

[27] X. Yang et al., "33.4 An 8A 998A/inch^3 90.2% peak efficiency 48V-to-1V DC-DC converter adopting on-chip switch and GaN hybrid power conversion," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 466–468.

[28] R. Das and H.-P. Le, "A regulated 48V-to-1V/100A 90.9%-efficient hybrid converter for POL applications in data centers and telecommunication systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 1997–2001.

[29] R. Das, G.-S. Seo, D. Maksimovic, and H.-P. Le, "An 80-W 94.6%-efficient multi-phase multi-inductor hybrid converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 25–29.

[30] H. Han et al., "A monolithic 48V-to-1V 10A quadruple step-down DC-DC converter with hysteretic copied on-time 4-phase control and 2× slew rate all-hysteretic mode," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technology Circuits)*, Jun. 2022, pp. 182–183.

[31] G.-S. Seo and H.-P. Le, "An inductor-less hybrid step-down DC-DC converter architecture for future smart power cable," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2017, pp. 247–253.

[32] N. Tang, B. Nguyen, Y. Tang, W. Hong, Z. Zhou, and D. Heo, "8.4 fully integrated buck converter with 78% efficiency at 365mW output power enabled by switched-inductor capacitor topology and inductor current reduction technique," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 152–154.

[33] C. Hardy and H.-P. Le, "8.3 A 10.9W 93.4%-efficient (27W 97%-efficient) flying-inductor hybrid DC-DC converter suitable for 1-cell (2-cell) battery charging applications," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 150–152.

[34] A. Abdulslam and P. P. Mercier, "8.2 A continuous-input-current passive-stacked third-order buck converter achieving 0.7W/mm^2 power density and 94% peak efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 148–150.

[35] J. Huang, Z. Tong, Y. Lu, C.-S. Lam, and R. P. Martins, "A 5V-to-0.5V inductor-first inductor-on-ground switched capacitor multi-path hybrid DC-DC converter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[36] Z. Tong, J. Huang, Y. Lu, and R. P. Martins, "A 42W reconfigurable bidirectional power delivery voltage-regulating cable," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 192–194.

[37] J. Jin, Y. Zhou, C. Chen, X. Han, W. Xu, and L. Cheng, "A 98.6%-peak-efficiency 1.47A/mm^2-current-density buck-boost converter with always reduced conduction loss," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 448–450.

[38] K. Hata, Y. Yamauchi, T. Sai, T. Sakurai, and M. Takamiya, "48V-to-12V dual-path hybrid DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 2279–2284.

[39] K. Hata, Y. Jiang, M.-K. Law, and M. Takamiya, "Always-dual-path hybrid DC-DC converter achieving high efficiency at around 2:1 step-down ratio," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Jun. 2021, pp. 1302–1307.

[40] J.-Y. Ko, Y. Huh, M.-W. Ko, G.-G. Kang, G.-H. Cho, and H.-S. Kim, "A 4.5V-input 0.3-to-1.7V-output step-down always-dual-path DC-DC converter achieving 91.5%-efficiency with 250mΩ-DCR inductor for low-voltage SoCs," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[41] G. Cai, Y. Lu, and R. Martins, "A battery-input sub-1V output 92.9% peak efficiency 0.3A/mm^2 current density hybrid sc-parallel-inductor buck converter with reduced inductor current in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 312–314.

[42] C. Wang, Y. Lu, and R. P. Martins, "A highly integrated tri-path hybrid buck converter with reduced inductor current and self-balanced flying capacitor voltage," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 9, pp. 3841–3850, Sep. 2022.

[43] G. Cai, Y. Lu, and R. P. Martins, "A compact 12V-to-1V 91.8% peak efficiency hybrid resonant switched-capacitor parallel inductor (ReSC-PL) buck converter," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 198–200.

[44] J. Jiang, Y. Lu, C. Huang, W.-H. Ki, and P. K. T. Mok, "20.5 A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[45] W.-L. Zeng et al., "A 12V-input 1V-1.8V-output 93.7% peak efficiency dual-inductor quad-path hybrid DC-DC converter," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 10–12.

[46] C. Hardy and H.-P. Le, "A 21W 94.8%-efficient reconfigurable single-inductor multi-stage hybrid DC-DC converter," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 190–192.

[47] J. W. Kwak and D. B. Ma, "Superimposed quadratic buck converter for high-efficiency direct 48V/1V applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2023, pp. 2253–2259.

[48] T. Burd et al., "Zen3: The AMD 2nd-generation 7nm x86-64 microprocessor core," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 1–3.

[49] W. Gomes et al., "Ponte Vecchio: A multi-tile 3D stacked processor for exascale computing," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 42–44.

[50] C.-H. Huang, X. Sun, Y. Chen, R. Pamula, A. Mandal, and V. Sathe, "A single-inductor 4-output SoC with dynamic droop allocation and adaptive clocking for enhanced performance and energy efficiency in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 416–418.

[51] A. Salimath et al., "An 86% efficiency SIMO DC-DC converter with one boost, one buck, and a floating output voltage for car-radio," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2018, pp. 426–428.

[52] S. Kim et al., "11.3 A 1.8W high-frequency SIMO converter featuring digital sensor-less computational zero-current operation and non-linear duty-boost," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 10–12.

[53] L.-C. Chu et al., "10.5 A three-level single-inductor triple-output converter with an adjustable flying-capacitor technique for low output ripple and fast transient response," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2017, pp. 186–187.

[54] W.-C. Hung et al., "11.4 A double step-down dual-output converter with cross regulation of 0.025mV/mA and improved current balance," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 188–190.

[55] T. Hu, M. Huang, Y. Lu, and R. P. Martins, "11.2 A 12V-to-1V quad-output switched-capacitor buck converter with shared DC capacitors achieving 90.4% peak efficiency and 48mA/mm3 power density at 85% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 184–186.

[56] R. Das and H.-P. Le, "Multi-inductor multi-output hybrid (MiMoH) converter for large conversion ratio and multiple outputs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2023, pp. 943–947.

[57] S. Zhen, R. Yang, D. Wu, Y. Cheng, P. Luo, and B. Zhang, "Design of hybrid dual-path DC-DC converter with wide input voltage efficiency improvement," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[58] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

[59] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[60] X. Yang et al., "11.8 A 5A 94.5% peak efficiency 9∼16V-to-1V dual-path series-capacitor converter with full duty range and low V.A metric," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 196–198.

[61] H.-P. Lam, W.-H. Ki, and P. K. T. Mok, "4C 3-level hybrid buck converter for 12∼48V-to-1V point-of-load applications," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[62] G. Cai, Y. Lu, and R. P. Martins, "An SC-parallel-inductor hybrid buck converter with reduced inductor voltage and current," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1758–1768, Jun. 2023.

[63] K. Kesarwani, R. Sangwan, and J. T. Stauth, "4.5 A 2-phase resonant switched-capacitor converter delivering 4.3W at 0.6W/mm^2 with 85% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 86–87.

[64] P. Renz, M. Kaufmann, M. Lueders, and B. Wicht, "8.6 A fully integrated 85%-peak-efficiency hybrid multi ratio resonant DC-DC converter with 3.0-to-4.5V input and 500μA-to-120mA load range," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 156–158.

[65] "TPS54A20 8-V to 14-V input, 10-A, Up to 10-MHz swift step-down converter," Data Sheet TPS54A20, Texas Instrum., Dallas, TX, USA. Accessed: Dec. 1, 2021. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps54a20.pdf

[66] A. Roth et al., "Heterogeneous power delivery for 7nm high-performance chiplet-based processors using integrated passive device and in-package voltage regulator," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[67] N. Desai et al., "Peak-current-controlled ganged integrated high-frequency buck voltage regulators in 22nm CMOS for robust cross-tile current sharing," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 262–264.

[68] H. Lin et al., "Efficient backside power delivery for high-performance computing systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 11, pp. 1748–1756, Nov. 2022.

[69] K. Bharath et al., "Integrated voltage regulator efficiency improvement using coaxial magnetic composite core inductors," in *Proc. IEEE 71st Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2021, pp. 1286–1292.

[70] C. Wang, Y. Lu, and R. P. Martins, "A highly integrated 3-phase 4:1 resonant switched-capacitor converter with parasitic loss reduction and fast pre-charge startup," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2608–2612, Jul. 2021.

[71] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017.

[72] C. Hardy et al., "11.1 A scalable heterogeneous integrated two-stage vertical power-delivery architecture for high-performance computing," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 182–184.

[73] Y. Lu, J. Jiang, and W.-H. Ki, "Design considerations of distributed and centralized switched-capacitor converters for power supply on-chip," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 515–525, Jun. 2018.

[74] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[75] S. Bang et al., "25.1 A fully synthesizable distributed and scalable all-digital LDO in 10nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2020, pp. 380–382.

[76] H. Nguyen and W. Jung, "ConverGenT: Automated topology generation and analysis of hybrid DC–DC converters," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11193–11220, Sep. 2023.

YAN LU (Senior Member, IEEE) received the B.Eng. and M.Sc. degrees in microelectronics from the South China University of Technology, Guangzhou, China, in 2006 and 2009, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, China, in 2013.

In 2014, he joined the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, where he is currently an Associate Professor. He has authored/coauthored more than 150 peer-reviewed technical articles and two books. His research interests include wireless power transfer circuits and systems, and high-density integrated power converters and voltage regulators.

Dr. Lu was a recipient/corecipient of the NSFC Excellent Young Scientist Fund (Hong Kong–Macau) in 2021, the Macau S&T Award Second Prizes in 2018 and 2020, the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award in 2013–2014, the IEEE CAS Society Outstanding Young Author Award in 2017, and the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper. He has served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2022 and 2023, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS in 2019, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS in 2018 and 2019. He has been serving as a Young Editor for the *Journal of Semiconductors* since 2021. He is serving as a TPC Member for ISSCC and CICC, and an IEEE SSCS Distinguished Lecturer in 2022–2023.

JUNWEI HUANG (Student Member, IEEE) received the B.Eng. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2018. He is currently pursuing the Ph.D. degree with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China.

His research interests include hybrid dc–dc converter and analog circuit design.

ZHIGUO TONG (Student Member, IEEE) received the B.E. degree in electronic science and technology from Tianjin University, Tianjin, China, in 2018, and the M.Sc. degree in microelectronics and solid-state electronics from Fudan University, Shanghai, China, in 2021. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China.

His current research interests include analog/mixed-signal circuits and power management IC design.

Mr. Tong was a recipient of the Best Poster Award of the PwrSoC2023.

TINGXU HU (Student Member, IEEE) received the B.E. degree from the South China University of Technology, Guangzhou, China, in 2019. He is currently pursuing the Ph.D. degree with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China.

His research interests include RF energy harvesting, hybrid dc–dc converter, and isolated power converter.

WEN-LIANG ZENG (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and computer engineering from the University of Macau, Macau, China, in 2014, 2016, and 2020, respectively.

In 2013, he joined the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, where he is currently a Postdoctoral Fellow (Macau Fellow) with the Institute of Microelectronics. His research focuses on high-speed fully integrated, ultralow quiescent current integrated, hybrid integrated, and large conversion ratio high power density integrated dc–dc converters.

MO HUANG (Senior Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in microelectronics and solid-state electronics from Sun Yat-sen University, Guangzhou, China, in 2005, 2008, and 2014, respectively.

From 2008 to 2014, he was an IC Design Engineer and a Project Manager with Rising Microelectronic Ltd., Guangzhou. From 2015 to 2016, he was a Postdoctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV), University of Macau, Macau, China. From 2017 to 2019, he was with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou, as an Associate Professor. He is currently an Assistant Professor with AMSV and the Institute of Microelectronics, University of Macau. His current research interests are power management integrated circuits and systems.

Dr. Huang was a recipient of the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper. He has been serving as an Associate Editor for *Microelectronics Journal* since 2021. He has served as a technical program committee member of multiple conferences.

XIANGYU MAO (Member, IEEE) received the B.Eng. and M.Sc. degrees in electronic engineering from Xidian University, Xi'an, China, in 2009 and 2012, respectively, and the Ph.D. degree in electronic and computer engineering from the University of Macau, Macau, China, in 2022.

From 2012 to 2019, he was an IC Design Engineer and then a Project Manager with Hisilicon Corporation, Shenzhen, China, mainly responsible for various analog IPs from 40 to 7-nm CMOS technology. He is currently a Postdoctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. His research interests are power management systems for multicore processors, including dc–dc converters, fully integrated voltage regulators, and power integrity.

GUIGANG CAI (Member, IEEE) received the B.Eng. degree in electrical engineering and automation from Xi'an Jiaotong University, Xi'an, China, in 2013, and the Ph.D. degree in electrical and computer engineering from the University of Macau, Macau, China, in 2022.

Since 2023, he has been an Assistant Professor with the Microelectronic Thrust, Function Hub, The Hong Kong University of Science and Technology (Guangzhou), Guangzhou, China. His current research interests include hybrid dc–dc converter, analog and digital low-dropout regulator, switched-capacitor, and isolated power transfer circuits and systems.