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Low-Power Heterodyne Receiver Architectures: Review, Theory, and Examples

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ABSTRACT The growth of the Internet of Things (IoT) has led to a massive upsurge in low-power radio research. Specifically, low-power receivers (RX) have been developed that efficiently receive data and extend the battery life for energy-constrained IoT systems. This has led to innovations in energy-detector (ED) first RXs which can achieve much lower power than traditional mixer-based heterodyne architectures. However, at such low-power levels, the RX performance is extremely limited. Oftentimes, low-power RXs have severe performance limitations, including lower data rate, limited blocker rejection, lower sensitivity, lower tolerance to PVT, limited modulation compatibility, and increased size and cost of off-chip components to achieve passive gain. This greatly limits the application of such RXs in real-world applications and prevents many of the low-power circuit techniques from translating to commercial standards. In this work, we look to motivate research into low-power heterodyne RX architectures which can support higher order modulation and have improved RX specifications while retaining low power.

INDEX TERMS Energy-detector (ED)-first, frequency-shift keying (FSK), low-power heterodyne, low-power radio, low-power receiver architecture, mixer-first receiver, Narrowband Internet of Things (NB-IoT), OFDM, wake-up radio (WRX), wireless sensor nodes.

I. INTRODUCTION

FROM looking at trends in low-power radio research, there is a clear gap in published works for higher-order modulation radios. As seen in Fig. 1, of all low-power radios published in top conferences from 2005–2023, over 100 of the published works support ON–OFF keying (OOK) or frequency-shift keying (FSK) modulation only [1]. Fewer than 30 published works support PSK modulation, and less than ten published works support QAM/OFDM. In addition, no PSK or QAM radio operating above 1 GHz achieves <1-mW power consumption. Contrast that with the modulation used by today's wireless standards. Only Bluetooth uses GFSK, while ZigBee (OQPSK), LoRa (Chirp), WiFi (QAM/OFDM), and narrowband Internet of Things (NB-IoT) (QPSK/OFDMA) all use more complex modulation and wireless techniques requiring higher power. More interesting from a circuit design standpoint is the underlying hardware limitations that have caused a divide in supported modulations and power consumption. In this work, an overview of low-power radio trends is explored to motivate low-power radio architectures that can support higher-order modulation. First, a brief background on low-power heterodyne architectures is given and contrasted with ED-first RXs. Second, supporting theory for mixer-first receivers is presented, including low-power considerations. Finally, two fabricated chips are highlighted which show an ultralow-power (ULP) heterodyne receiver at 2.4 GHz in FinFET technology and an NB-IoT wake-up radio (WRX) which supports OFDM to show recent advances in heterodyne low-power radios.

II. HETERODYNE VERSUS ED RECEIVERS

In contrast to most low-power radio research, the complexity of commercial wireless standards has increased, demanding more performance out of RXs. The most recent Wi-Fi generation (802.11ax) has a maximum bandwidth of 160 MHz, supports 1024-QAM with OFDM, and has a data rate of >9 Gbit/s [38]. Similarly, 5G also utilizes more complex signaling than current low-power radios can support, including QAM, OFDM, MIMO, and mm-wave (>24 GHz) center frequencies [39]. Cellular Internet of Things (IoT) standards, such as NB-IoT, also present considerable challenges to low-power RX designers, including QPSK modulation

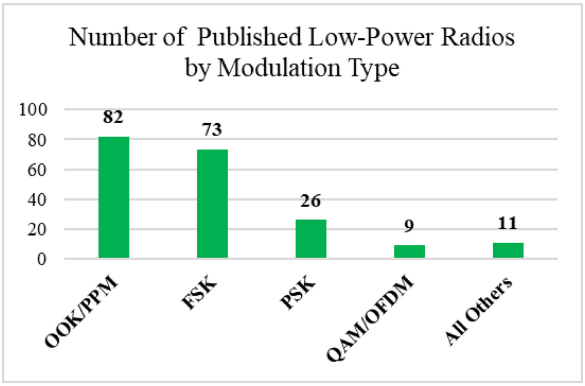

FIGURE 1. Number of published works as modulation type.

and extremely high sensitivities to cover long ranges up to 10 km [40]. It is clear that in order to meet the demands of modern wireless standards while maintaining long battery life, new approaches to low-power RX design are needed. In particular, it is useful to analyze RXs that use an energy-detector (ED)-first, LNA-first, and mixer-first architecture to understand the tradeoffs from a low-power perspective.

Recent publications of ULP receivers and wake-up receivers have achieved extremely low power consumption, where wake-up receivers have been reported on the order of nano-watts and below [2], [3], [4], [5]. To achieve such low power consumption, ED first architectures are often utilized which do not require many of the typical heterodyne receiver blocks, namely the mixer and local oscillator (LO) and LO buffers, allowing them to consume far less power. However, ED-first RXs tradeoff many performance metrics in favor of low power consumption which can limit their application in real-world scenarios. In this section, the performance limitations of ED-first architectures are examined, motivating the benefits of low-power heterodyne architectures as an alternative.

A. ED FIRST ARCHITECTURE

While their extremely low-power floor is attractive, ED-first RX architectures exhibit various performance limitations [6]. First, ED-first RXs are inherently wideband. As a result, they have little-to-no interference rejection in the RF front-end, both in and out-of-band (OOB). Several techniques have been used to regain some blocker tolerance for ED receivers, although all have their drawbacks. The most common is the use of an off-chip matching network. Other techniques which modify the OOK signal, such as CDMA encoding, two-tone OOK, and Manchester encoding can also be used to increase blocker tolerance, but at a bandwidth and complexity cost. Still, large off-chip matching networks are needed to increase sensitivity [7], [46], [47]. This highlights another limitation of ED-first RXs which is their poor sensitivity, which is usually overcome by utilizing large or expensive off-chip components to boost sensitivity through passive gain [8], [9], [10], [11], [12]. Matching network passive gain on the order of 15–30 dB have been reported which is only achievable with large or expensive off-chip components. Still, ED-first RXs have poor NF which results in most ED sensitivities being >-70 dBm. Tradeoffs such as reduced data rate can be used to improve sensitivity. However, the required time-on-air of such low-data rate transmissions can be prohibitively long and can take several seconds to transmit a small data packet. Long time-on-air can actually *increase* the power consumption of the full RX as it is required to be on for much longer to receive data packets, in addition to making scheduling for wireless systems difficult. In addition, ED-first RXs can usually only support amplitude-modulated signals, most commonly OOK, which is spectrally inefficient and highly susceptible to channel noise. All modern communication standards utilize some form of FSK, PSK, or QAM signaling, all of which are incompatible with most ED-first RXs.

B. BENEFITS FOR HETERODYNE RXS

In this work, the term "heterodyne RX" is used to describe any receiver architecture whose LO frequency is different from the input RF frequency and uses a mixer to downconvert to an IF frequency to be processed, regardless if the final baseband conversion and data demodulation is done in the analog or digital domain. Heterodyne RXs, as the preferred RX architecture for most commercial radios, yield several advantages over ED-first RXs. Heterodyne RXs usually have much better blocker tolerance due to additional filtering that can be done at the IF frequency for relatively low-power. In addition, the noise performance of the first block, traditionally an LNA, is usually better than that of an ED, yielding higher sensitivities. Another significant, if obvious, improvement of heterodyne RXs over ED-first RXs is their ability to support higher-order modulation. Since heterodyne architectures preserve frequency, phase, and amplitude information, modulation schemes, such as FSK, PSK, and QAM can be utilized. Supporting higher order modulation is important for wireless systems as it improves spectral efficiency, increases data rate, reduces time-on-air, and has increased resilience to channel noise.

C. CHALLENGES FOR LOW-POWER HETERODYNE RXS

However, heterodyne receivers for low-power applications do pose challenges. One of the primary power savings achieved by ED-first RXs is the absence of an LO. For a heterodyne RX, the LO and buffers often are the dominant sources of power consumption. The phase noise performance of the LO also becomes important as it can lead to a reduction in SNR, reduced selectivity from reciprocal mixing, and increased LO frequency drift [13]. Reducing phase noise usually requires the use of a PLL and a low-phase noise VCO, greatly increasing power consumption. LO buffers are also required to drive the mixer switches. As the mixer switch size increases to reduce conversion loss, capacitive loading on the LO buffers causes high power consumption.

III. LOW-POWER TECHNIQUES FOR HETERODYNE RECEIVERS

Low-power heterodyne architectures proposed in the literature vary greatly based on application. However, four main techniques are highlighted which have been proposed to reduce the power of heterodyne RXs. These techniques can be applied to both RX and wake-up RXs, which can be used to reduce the overall system power of heterodyne RXs. Some of these techniques can be used in conjunction with each other to further reduce power consumption.

A. UNCERTAIN-IF

Uncertain-IF RXs reduce power by eliminating the need for a PLL for the LO [14], [15], [16]. They instead use a simple open-loop oscillator, usually a ring oscillator (RO), for frequency downconversion which is prone to frequency drift, leading to an uncertain-IF frequency. Power consumption on the order of <100 μW has been reported for uncertain-IF wake-up RXs [15]. However, there are drawbacks to this architecture that limit its ability to scale to lower power and higher data rates. First, the required IF-BW is large, limiting its ability to achieve blocker rejection without high Q off-chip filtering at RF as well as increasing power consumption. Second, as commonly implemented, an ED is needed to perform the baseband downconversion as the signal location is uncertain, limiting its use to OOK modulation. Alternatively, a high sample-rate ADC could be used at the uncertain-IF frequency, but with a high power penalty. Finally, this design is highly susceptible to PVT variation due to its open-loop LO and requires frequent recalibration, which adds to the power overhead.

B. SUBHARMONIC MIXING

Another option is to use a subharmonic downconverting mixer [17], [18], [19], [20]. This architecture uses a higher harmonic of the LO to perform downconversion, allowing the LO to run slower while still downconverting at a high RF frequency, saving power in the LO and LO buffers. Power consumption of 220 μW at 5.8-GHz center frequency have been reported for subharmonic RXs [58]. However, the conversion gain of the mixer degrades at higher harmonics, lowering sensitivity or requiring the use of a high-gain LNA. This conversion loss can be overcome somewhat by using additional mixer switches at the cost of increased LO buffer power consumption. In addition, achieving rejection at undesired harmonics often requires precise phase adjustments of the LO, adding additional power overhead to the mixer and LO.

C. SUBSAMPLING

A subsampling mixer can be also used to efficiently downconvert data at RF frequencies [21], [22], [23]. Subsampling mixing differs from subharmonic mixing as the sampler output acts as a zero-order hold rather than returning to zero for a traditional mixer, hence acting as a sample-and-hold circuit. This architecture lowers power by utilizing aliasing to downconvert, allowing a much lower clock speed to be used related to the Nyquist rate of the signal rather than the RF center frequency. However, the major limitation of subsampling mixers is their poor noise performance as wideband noise is folded in-band at multiples of the subsample rate. Therefore, significant filtering is required at RF which is typically achieved with a narrow-band LNA or sharp MEMS filter, adding bandwidth, area, and frequency planning constraints on the design. In addition, the sample-and-hold circuit is highly susceptible to clock jitter, which introduces additional sources of noise at high frequencies.

D. PASSIVE-MIXER FIRST

Passive-mixer first architectures forgo gain at RF and instead connect the antenna directly to a passive mixer for down conversion [24]. Mixer-first RXs remove the LNA which reduces the power consumption of the RF path. Due to the transparency effect of passive mixers, high-Q RF filtering can be achieved due to the upconverted filter response of the baseband stage. As a result, no off-chip matching components are typically required, enabling greater integration [24], [61]. However, off-chip matching networks can still be used to overcome additional losses of the mixer-first RX as well as suppress undesired harmonic downconversion. Additionally, the RF band-pass filtering response can be tuned digitally by varying the baseband filter corner and shifting the LO frequency. This enables a single mixer-first RX to be reconfigured to different frequency bands and retain matching performance. Despite having no LNA, it has been shown that mixer-first RXs can still achieve <3-dB noise figures in practice [50], [51], [52]. However, to achieve low-NF, the mixer switches must be sized up considerably to reduce the on-resistance of the passive mixer, increasing the power consumption of the LO buffers.

E. MOTIVATION FOR LOW-POWER MIXER-FIRST RECEIVERS

Seeking low-power heterodyne solutions, recently published receivers [1] can be further separated based on their use of LNA-first, mixer-first, or ED-first architectures. Fig. 2 shows normalized sensitivity versus power of published RXs separated by architecture, where normalized sensitivity takes into account data rate and is given by $S_{\text{normalized}} = \text{Sensitivity[dBm]} - 10\log(\text{DataRate[kb/s]})$. A clear trend can be seen that LNA-first tends to have the highest power and lowest normalized sensitivity, while ED-first has the lowest power and highest normalized sensitivity, with mixer-first lying in between. Importantly, ED-first architectures can only support OOK modulation, which means mixer-first designs show promise as a lower power receiver architecture for higher order modulation radios. This motivates a closer look at the power and performance tradeoffs of mixer-first RXs to inform design decisions when focusing on lowering power consumption.

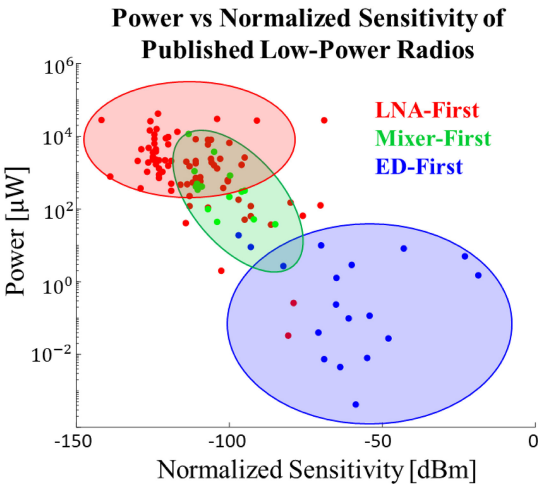

FIGURE 2. Normalized sensitivity versus power of recently published radios.

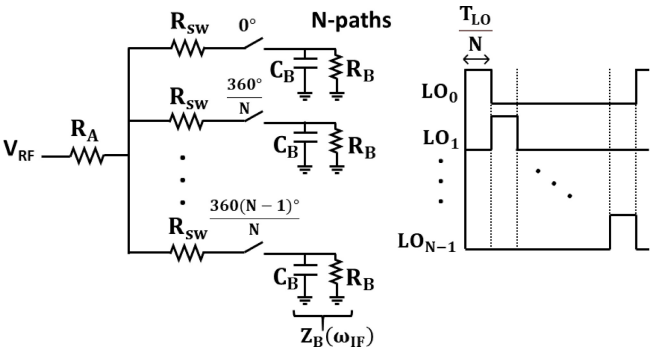

FIGURE 3. LTV Model of an *N*-stage passive sampling mixer.

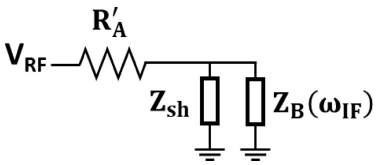

FIGURE 4. LTI model of passive mixer.

IV. GENERALIZED MIXER FIRST THEORY

Passive mixers have been analyzed extensively in [24], [25], [26], [27], [28], [29], [30], [31], [50], [51], and [52]. As a result, many interesting properties have been discovered and exploited to produce mixer-first receiver architectures. Prior work includes a range of mixer topologies, and downconversion using the fundamental or a harmonic of the LO. For instance, Andrews and Molnar [24] used a passive mixer composed of four or eight switches and downconversion at the fundamental of the LO, while Andrés et al. [31] focused on a two-switch 50% duty cycle mixer. A more generalized design approach for mixer-first receivers is needed to explore low-power receiver architectures which often utilize subharmonic mixing to lower power. The main considerations for passive mixers are input impedance, conversion gain, noise figure, linearity, and power consumption. In this section, a generalized model for these specifications using a nonoverlapping passive sampling mixer with an arbitrary number of switches and arbitrary LO harmonic downconversion is derived. This analysis is consistent with previously derived analysis but generalized to include an arbitrary number of mixer switches and switching at the fundamental or at an arbitrary subharmonic.

A. INPUT MATCHING

An LTV model of a general passive sampling mixer is shown in Fig. 3. It is assumed that the phases of the switches are nonoverlapping and each switch path is identical. R_A represents the antenna resistance, R_{SW} is the switch resistance, R_B is the baseband resistance, and C_B is the baseband capacitor. R'_A is an intermediate variable defined as $R'_A = R_A + R_{SW}$, denoting the impedance before the ideal switches. Nonoverlapping clocks provide various benefits as discussed in [29] and [30] including minimizing loss by maintaining isolation between each switch path. This analysis will assume nonoverlapping clocks are utilized for minimal loss. However, overlapping phase mixers are sometimes used and have some beneficial properties as seen in [31] and [32].

For a passive sampling mixer to operate as a "mixer," $\omega_{LO} >> (1/C_B R_B)$ and $\omega_{LO} >> (1/C_B R'_A)$ must be satisfied. Otherwise, the mixer will begin to behave as a sample and hold circuit [28]. Typically for a mixer first receiver, $\omega_{LO} >> (1/C_B R'_A)$ tends to be the tighter constraint. These conditions can be used in design to help size the baseband capacitor.

The LTI model can be represented as an LTI network in Fig. 4 for a low-IF downconversion. Equating the input impedances of the two models gives the shunt impedance Z_{sh}

$$Z_{sh} = \frac{N\gamma R'_A Z_B}{NR'_A(1-\gamma) + Z_B(1-N\gamma)} \tag{1}$$

$$\gamma = \frac{\text{sinc}^2\left(\frac{\pi n}{N}\right)}{N} \tag{2}$$

$$\omega_{RF} = n\omega_{LO} + \omega_{IF} \tag{3}$$

where N represents the number of switches and n represents the harmonic multiple of the LO frequency at which downconversion is desired. γ is a constant that denotes the scaling factor of the baseband impedance as seen at the input of the mixer and is commonly used in passive mixer analysis. From the LTI model, the input impedance can be written as

$$Z_{in}(n\omega_{LO} + \omega_{IF}) = R_{sw} + Z_{sh}(\omega_{IF}) || Z_B(\omega_{IF}). \tag{4}$$

Fig. 5 shows the input impedance versus the baseband resistor and displays good alignment between the analytical theory and LTV simulation. Fig. 6 shows plots of the real and imaginary components of the input impedance versus RF frequency, where the bandpass-response of the input impedance can be seen. This is an important property of passive mixer-first receivers and first identified as

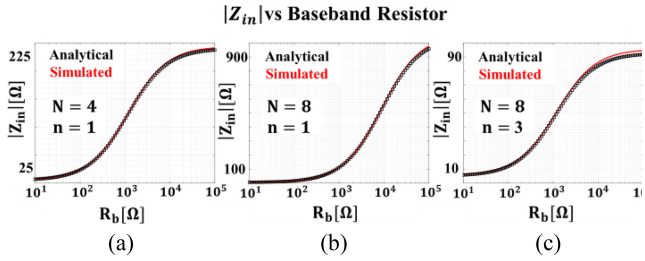

FIGURE 5. Magnitude of Zin versus baseband resistance for (a) $n = 1$ and $N = 4$, (b) $n = 1$ and $N = 8$, and (c) $n = 3$ and $N = 8$ when R_A is 50 Ω, R_{sw} is 5 Ω, C_B is 50 pF, F_{LO} is 2400 MHz, and F_{IF} is 1 kHz.

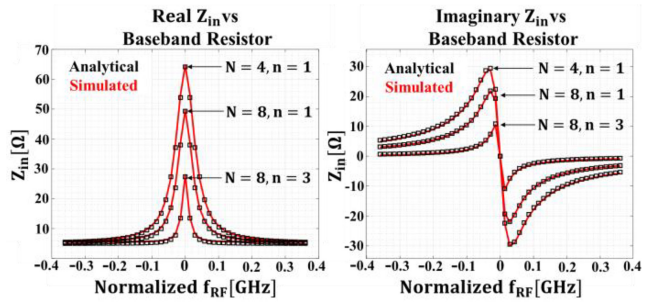

FIGURE 6. Real and imaginary Zin versus RF Frequency for (a) $n = 1$ and $N = 4$, (b) $n = 1$ and $N = 8$, and (c) $n = 3$ and $N = 8$ when R_A is 50 Ω, R_{sw} is 5 Ω, C_B is 50 pF, R_B is 390 Ω, and F_{LO} is 2400 MHz.

the "transparency property" in [25]. Intuitively, the low-pass filter response of the baseband R_B and C_B effectively becomes up-converted to RF and provides high-Q bandpass RF filtering at the desired LO subharmonic frequency of the mixer. An S_{11} plot in Fig. 7 shows that with properly tuned matching via the baseband resistor, S_{11} can be optimized at the desired LO subharmonic. Moreover, S_{11} at every LO harmonic diminishes as the frequency offset from the desired LO subharmonic increases, ultimately limited by the finite resistance of the mixer switch. Two interesting approximations of Z_{sh} can be seen as follows:

$$\lim_{Z_B \to \infty} Z_{sh} = \frac{\mathrm{N}\gamma R'_A}{1 - N\gamma} \tag{5}$$

$$\lim_{R'_A \to \infty} Z_{sh} = \frac{\gamma Z_B}{1 - \gamma} \tag{6}$$

where Z_{sh} becomes independent of Z_B or R'_A as Z_B or R'_A becomes large. Practically, the approximation that Z_B is large is accurate as long as $R'_A << R_B[(1 - N\gamma)/N(1 - \gamma)]$. In receiver design, this tends to be true and further analysis using this approximate Z_{sh} is shown to provide greater insights to help guide design. A plot of the analytical shunt impedance and gamma is shown in Fig. 8 displaying consistency with specific cases analyzed in prior art.

By tuning the baseband resistor, the input impedance of the mixer can be tuned. The range in which the input impedance can be tuned is

$$R_{sw} \leq Z_{\text{in}} \leq R_{sw} + Z_{sh}. \tag{7}$$

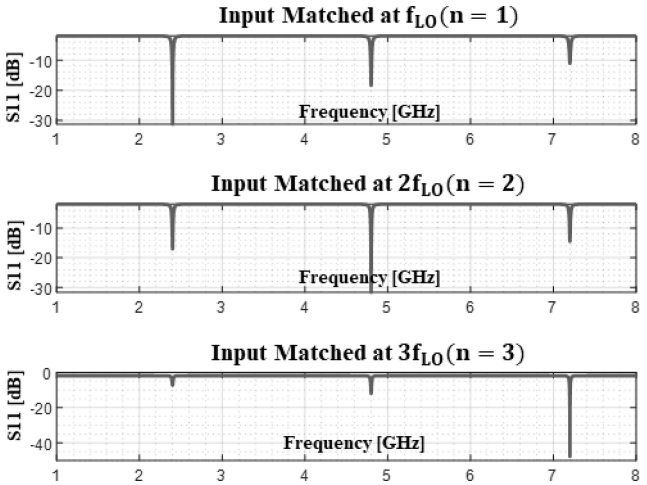

FIGURE 7. S_{11} versus RF Frequency matched at $n = 1$ ($R_B = 390$ Ω), $n = 2$ ($R_B = 542$ Ω), and $n = 3$ ($R_B = 1.144$ kΩ) when $N = 8$, R_A is 50 Ω, R_{sw} is 5 Ω, C_B is 50 pF, $F_{IF} = 1$ kHz, and F_{LO} is 2400 MHz.

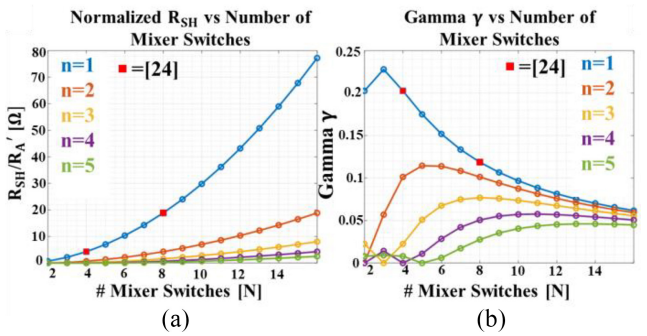

FIGURE 8. (a) Normalized shunt resistance and (b) gamma parameter as a function of number of mixer switches for various harmonic subsampling indexes.

Clearly, Z_{in} can only be input matched if the switch resistance R_{sw} is less than or equal to the antenna resistance. Therefore, this sets a lower limit on switch transistor sizing if input matching is desired, in turn defining the power needed to drive the gate capacitances of the switches. Assuming the switch resistance is zero, a simple condition can be derived to achieve input matching. When this condition is true, the input impedance must be less than or equal to Z_{sh}

$$0 \leq Z_{\text{in}} \leq Z_{sh}. \tag{8}$$

Using (5) and the fact that Z_{in} is defined as R_A under the matched condition

$$0 \leq R_A \leq R'_A \frac{N\gamma}{1 - N\gamma}. \tag{9}$$

In plugging in (2) and reorganizing, it can be seen that in order to achieve input matching the following must be true:

$$\frac{n}{N} \leq 0.443. \tag{10}$$

This result shows that to achieve input matching at a higher subharmonic ($n > 1$), the number of mixer switches must increase. This can be used as a simple and highly conservative starting point in guaranteeing a match is achievable.

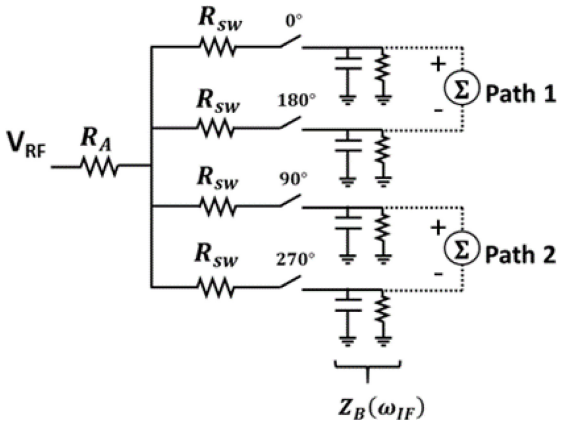

FIGURE 9. Four-phase mixer outputted as a two-path system.

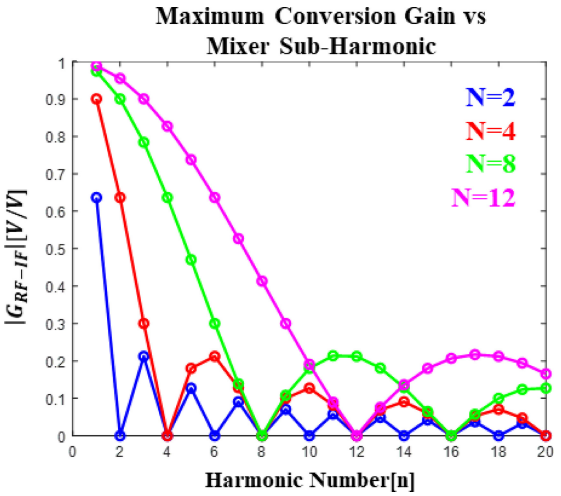

FIGURE 10. Maximum conversion gain per switch at a given subharmonic for various number of switches.

However, matching can be achieved beyond this inequality by utilizing a higher switch resistance at the cost of narrower tuning range. A more exact relation of guaranteed input matching to this ratio for an arbitrary switch resistance can be shown to be

$$R_{sw} \leq R_A \bigcup \text{sinc}^2\left(\frac{\pi n}{N}\right) \geq \frac{1}{2}\left(1 - \frac{R_{sw}}{R_A}\right). \quad (11)$$

B. CONVERSION GAIN

Conversion gain for a passive mixer with a sine wave input can be defined as the IF voltage amplitude divided by input RF voltage amplitude. More specifically, in the LTV model voltage-mode conversion gain can be defined for each individual switch as

$$G_{\text{RF}-\text{IF}}|_{\text{switch}} = \text{sinc}\left(\frac{n\pi}{N}\right)\frac{Z_B}{Z_B + NR'_A}. \quad (12)$$

The first term of the switch conversion gain arises due to the sampling effect being a pulse-train, while the second half arises due to the switch seeing the input every Nth clock phase. A plot of the maximum conversion gain per switch can be seen in Fig. 9. For a traditional switching mixer, the above conversion gain is divided by the number of switches (N). Therefore, it can be seen that a passive sampling mixer exhibits better conversion gain than a passive switching mixer. The improvement in conversion gain comes from the sizing constraint set for the baseband capacitor discussed in Section IV-A, which provides some memory to the network. Interestingly, when viewed as a differential output, the overall conversion gain can be greater than 0 dB. For example, consider the four-switch mixer seen in Fig. 10. If the 0° and 180° phase path is defined as an output and the 90° and 270° phase path is defined as a second output, then the overall maximum conversion gain of a single path is $(4\sqrt{2})/\pi$ (5.1 dB). In practice, greater than 0-dB conversion gain can be achieved, but is typically not maximized for mixer first receivers as the input matching requirement can create non-negligible voltage division.

C. NOISE FIGURE

In [25], it is shown that the passive mixer noise figure can be derived from the input matching LTI model. In doing so for our LTI model, the noise factor is

$$F = 1 + \frac{R_{sw}}{R_A} + \frac{\text{Re}\{Z_{sh}\}}{R_A}\left|\frac{R_A + R_{sw}}{Z_{sh}}\right|^2 + \frac{R'_B}{\text{Re}\{R_A\}}\left|\frac{R_A + R_{sw}}{R'_B}\right|^2 \quad (13)$$

where R'_B represents the physical resistance seen at the output of the mixer switch. R'_B may be different from R_B. For example, if a resistive feedback amplifier follows the passive mixer, the feedback resistor may be modeled as a resistor at the input to ground valued as $[R'_B/(1 + A_{OL})]$ according to the Miller effect (where A_{OL} is the amplifiers open loop gain). Therefore, $R_B = [R'_B/(1 + A_{OL})]$, however the noise is contributed by R'_B. Assuming R'_B is much larger than R'_A and $\text{Re}\{Z_{sh}\} >> \text{Im}\{Z_{sh}\}$, both of which are typically true in receiver design, the noise factor can be simplified to

$$F \approx \frac{\left(1 + \frac{R_{SW}}{R_A}\right)}{\text{sinc}^2\left(\frac{\pi n}{N}\right)}. \quad (14)$$

The passive nature of the mixer causes it to be lossy and therefore causes the contribution of the successive gain stage to be the dominant source of noise. However, designing a baseband amplifier with low noise can be easily done and at low power cost compared to an RF LNA.

D. LINEARITY

Passive mixer first architectures have better linearity compared to active LNA first architectures. This can be understood intuitively as a passive mixer in its ideal operating condition is simply a linear resistor. Therefore, it qualitatively is expected that a passive mixer first architecture will tend to have higher IIP3 values as compared to LNA first

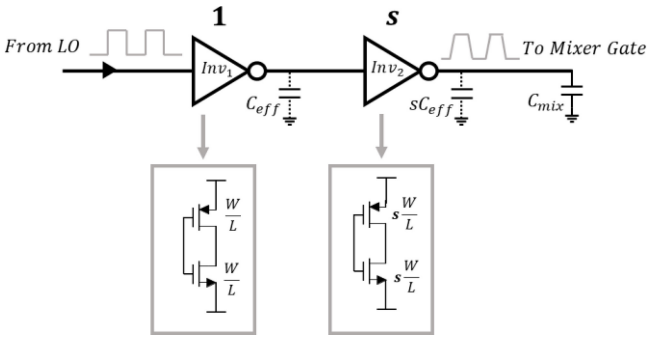

FIGURE 11. Schematic of two-stage LO buffer.

architectures. In-band IIP3 values of 14 dBm and OOB IIP3 values of 25 dBm have been reported for passive mixer-first RXs [24], [59]. The IIP3 for mixer-first receivers is often limited by the baseband circuitry. A more analytical discussion of passive mixer linearity can be seen in [33] and [34].

V. POWER CONSUMPTION OF MIXER FIRST RECEIVER

While the power consumption of a passive mixer in isolation is zero, the power consumed by the LO buffer circuitry is proportional to the gate capacitance of the mixer switches. In many low-power radio designs, the LO buffer is one of the dominant power consuming blocks and should be minimized as much as possible, given that the cost of increased phase noise from the buffers is acceptable. However, the capacitance seen at the gate of the mixer is directly proportional to the mixer on resistance R_{sw}, a key parameter for NF and input matching. This means there is a relationship between mixer NF and power consumption of the LO buffers that has been not explored in previous works.

A. BUFFER DESIGN

Fig. 11. shows a typical two-stage LO buffer. The first stage is a minimum sized inverter used to prevent the larger stage buffer from loading the preceding stage, usually a frequency divider or directly connected to the LO.

The second inverter is sized up by scale of s depending on the size of the load capacitance presented by the mixer, C_{mix}. C_{mix} is defined as the gate capacitance of the switch in the triode region

$$C_{\text{mix}} = (2C_{ov} + C_{ox})\text{WL} \tag{15}$$

where C_{ov} is the gate overlap capacitance, C_{ox} is the oxide capacitance, and W and L are the width and length of mixer switch. This can be alternatively defined in terms of mixer on resistance

$$C_{\text{mix}} = \frac{2C_{ov} + C_{ox}}{\mu_n C_{ox}(V_{\text{DD}} - V_{\text{th}})}\frac{L^2}{R_{sw}}. \tag{16}$$

This equation defines gate capacitance for a single nMOS mixer switch, and would be scaled by N switches to calculate total mixer capacitance. From (14) and (16) the inverse relationship between C_{mix} and noise factor F can be seen through R_{sw}.

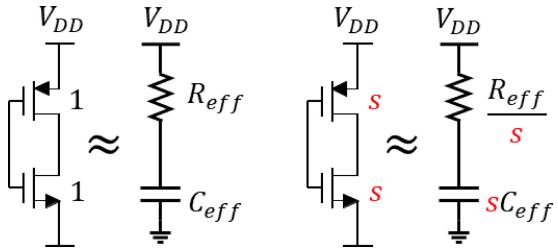

FIGURE 12. First order RC approximation for an inverter based on a W/L scale factor of s.

B. INVERTER SIZING FOR GIVEN PROCESS

Using a lumped approximation for the nonlinear MOS capacitors and resistors, we can analyze the reference inverter in its on-state as a simple first-order RC network as shown in Fig. 12. The intrinsic rise (fall) time $t_{r0}(t_{f0})$ from 10% to 90% can be calculated as

$$t_{r0} = t_{f0} = \ln(9)R_{\text{eff}}C_{\text{eff}} \tag{17}$$

where C_{eff} and R_{eff} are the effective lumped element approximations for the internal capacitances and resistance of the inverter, respectively.

C. MINIMUM BUFFER SIZING

To achieve a sharper rise/fall time, the width of the final inverter must be sized up. However, sizing up the width increases the internal capacitance of the inverter, increasing its self-loading. A minimum rise time can be chosen to set an upper bound on buffer sizing. However, this upper bound on sizing may be increased further to reduce the phase noise contribution of the buffers if critical for the design. For a size increase of s, C_{eff} increases approximately by a factor of s while R_{eff} decreases approximately by a factor of s. Therefore, $t_{r,\text{min}}$ can be defined as

$$t_{r,\text{min}} = \ln(9)R_{\text{eff}}\left(C_{\text{eff}} + \frac{C_{\text{mix}}}{s}\right) = \frac{p}{f_{\text{LO}}} \tag{18}$$

where p is the fraction of LO period for the rise (fall) time. A $p = 0.1$ gives a reasonable rise (fall) time with minimal impact on mixer performance. Following this, the minimum s can be solved as

$$s > \frac{R_{\text{eff}}C_{\text{mix}}}{0.455\frac{p}{f_{\text{LO}}} - R_{\text{eff}}C_{\text{eff}}}. \tag{19}$$

With the required sizing of the output buffer calculated, the power consumption of the two inverters can be calculated. While the dynamic power of the output buffer consumes the most power due to its large capacitive load, for low-power designs the dynamic power of the first buffer contributes a non-negligible percentage of the overall power and should not be ignored. The gate capacitance C_g of the inverters can be defined as

$$C_{\text{eff}} = \gamma_p C_g \approx C_g \tag{20}$$

where γ_p is a proportionality factor and is close to 1 for most submicron processes [35], yielding that output internal

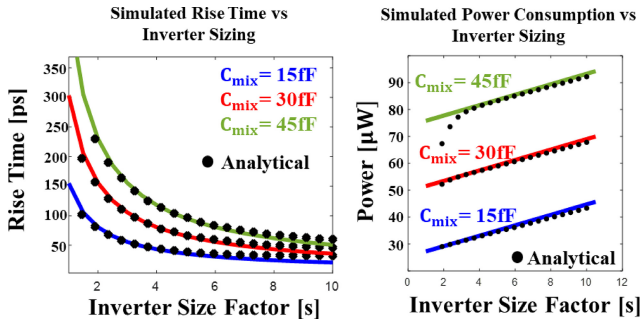

FIGURE 13. Analytical versus simulated results for rise time (left) and power consumption (right) versus inverter buffer sizes 2 GHz for a 65-nm process. The analytical equations used are (22), (21), and (19) with a $p = 0.1$.

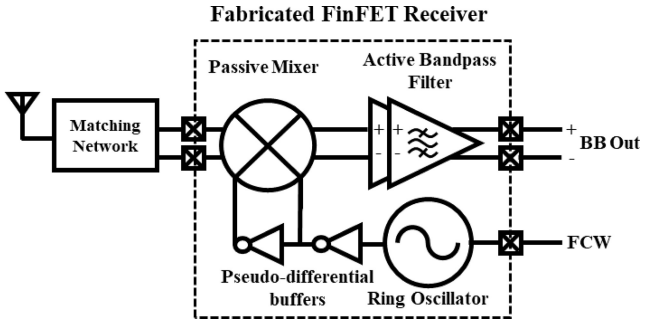

FIGURE 14. Block level of fabricated low-power mixer-first front end.

capacitance is approximately equal to input capacitance for an inverter. Finally, the power of each inverter can be calculated as

$$P_{\text{inv},1} \approx V_{\text{DD}}^2 C_{\text{eff}}(s+1) f_{\text{LO}} \tag{21}$$

$$P_{\text{inv},2} \approx V_{\text{DD}}^2 (sC_{\text{eff}} + C_{\text{mix}}) f_{\text{LO}}. \tag{22}$$

which ignores short circuit current, which is negligible. As can be seen, by utilizing (22), (21), and (19), the power of the LO buffers can be estimated given the mixer gate capacitance and minimum rise/fall time spec. To verify this, R_{eff} and C_{eff} were measured for a 65-nm process and rise time and power consumption were simulated to compare to theory. Fig. 13 shows good agreement of the theory versus simulation for various C_{mix} values.

D. FREQUENCY DIVIDER

Between the LO and mixer-buffers, a frequency divider is commonly used to achieve the correct duty-cycle for the mixer. In low-power receivers, the power of the frequency divider between the LO and mixer-buffers can be non-negligible. At minimum, a 2× frequency divider is needed to achieve a 50% or 25% duty cycle needed for most mixer designs, which also increases the power consumption of the LO which must operate at 2× the frequency. The choice of frequency divider and sizing used depends on RX specifications such duty-cycle percent, phase noise, and I/Q mismatch. However [57] provides a table of comparison for 25% duty-cycle dividers simulated at 2.5 GHz. When using the proposed windmill divider, a total power consumption of <70 μW was achieved in 22-nm FDSOI. However, the frequency divider must be designed within a given process, sizing, and frequency for accurate power estimations.

E. RING OSCILLATOR

For low-power receivers, using a RO for LO generation is preferred for its low-power compared to LC-oscillators. However, ROs suffer from much higher phase noise typically. The power of a typical RO can be estimated from a given phase noise specification [48]

$$L\{\Delta f\} \approx \frac{8}{3\eta} \frac{kT}{P_{\text{RO}}} \frac{V_{\text{DD}}}{V_{\text{char}}} \frac{f_{\text{LO}}^2}{\Delta f^2} \tag{23}$$

where P_{RO} is the power consumption of the RO, η is a rise time-stage delay proportionality constant that is close to 1, V_{char} is the characteristic voltage of the given process, and Δf is the frequency offset where phase noise is measured. Power consumption of the RO directly can be calculated as

$$P_{\text{RO}} = 2\eta N V_{\text{DD}}^2 (2s' C_{\text{eff}}) f_{\text{LO}} \tag{24}$$

$$s' = s_w s_L \tag{25}$$

where N is the number of RO stages, and s' represents the scale factor from the minimum inverter for both W and L given by s_w and s_L, respectively. The factor of 2 arises due to the fact that each inverter in the RO sees its own self-capacitance and the gate capacitance of the next stage.

VI. ULTRALOW-POWER FINFET MIXER-FIRST FRONT END

In the above analysis, it can be observed that the power consumption of a mixer-first RX front end with a RO is entirely from digital power consumption. It can also be seen that the architecture is highly digital in nature and consists only of logic gates and switches. Therefore, it is assumed this technology will benefit greatly from technology scaling. An ULP RX front end in FinFET technology was fabricated to showcase the performance limits of a mixer-first receiver with a primary focus on minimizing power. GlobalFoundries 12-nm (GF12) FinFET technology was used to demonstrate the benefits of technology scaling on low-power mixer-first architectures.

A. MIXER-FIRST RECEIVER ARCHITECTURE

The fabricated FinFET ULP RX front end is shown in Fig. 14. The receiver uses a differential passive mixer first architecture. The mixer switches are minimum size to take full advantage of the FinFET technology scaling to reduce the capacitive loading and therefore power consumption of the LO buffers. While using minimum mixer switches greatly increases the on-resistance of the mixer, an external matching network is used to help overcome the increased loss. Following the mixer is a two-stage active-bandpass filter implemented using self-biased current reuse amplifiers. To exploit the high output resistance of FinFETs which is significantly higher than planar FETs, the bias network is

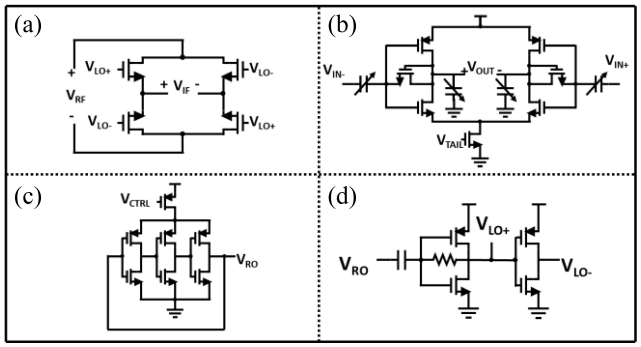

FIGURE 15. Block Level Architecture of (a) passive mixer, (b) baseband amplifier, (c) RO, and (d) LO buffer.

designed to not resistively load the output of the amplifier and therefore achieve maximum gain despite very low current consumption. The transistor level design of the circuits is shown in Fig. 15.

B. LOCAL OSCILLATOR DESIGN

The LO is designed as a three-stage current-starved RO. The RO again uses small FET sizing to maximize the power savings from technology scaling. The RO has a simulated phase noise of −63 dBc/Hz at 1-MHz offset with a center frequency of 2.46 GHz. Due to the emphasis on lowering power as much as possible, the phase noise performance is worse than that typically used for RF receivers. However, for FSK modulation, poor phase noise can be withstood at the cost of lower data rate, an acceptable tradeoff for energy-constrained IoT applications which do not require high-data rates [37]. A pseudo-differential LO buffer is used to produce positive and negative phases to the mixer with minimal power. The first stage of buffering is designed as a level shifter to boost the reduced oscillator swing due to the current-starved RO and to correct duty-cycle. The second stage of the buffer is enabled to be a simple minimum-sized inverter due to the small mixer capacitance. This both minimizes power consumption and allows for minimal overlap between the differential LO phases, allowing the pseudo-differential buffer structure to be used without power-hungry LO-divider structures being needed.

C. MEASUREMENT RESULTS

The receiver consumes a total of 52.4 μW with the RO consuming 36 μW, LO buffers consuming 16 μW, and baseband amplifiers consuming 0.4 μW. The total on-chip gain and bandwidth can be seen in Fig. 16. The gain of each baseband amplifier is 16.5 dB and mixer conversion gain is −3 dB. The matching network provides 12.6 dB of passive gain with an S_{11} seen in Fig. 17. The total baseband 3-dB bandwidth is measured to be 110 kHz. Noise figure was measured to be 48.2 dB. To help compare this receiver front end to existing works, link budget sensitivity was calculated to be −64.5 dBm using $S = -174 + \mathrm{NF} + 10\,(\mathrm{BW}) + \mathrm{SNR}_{\mathrm{min}}$. For a BER of 0.1%, $\mathrm{SNR}_{\mathrm{min}}$ is 10 dB for FSK [60]. A plot

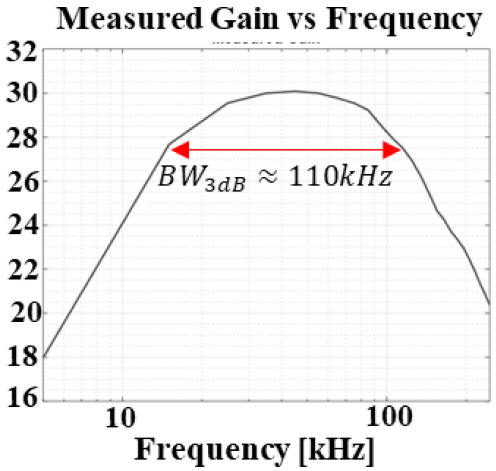

FIGURE 16. Measured RX voltage gain.

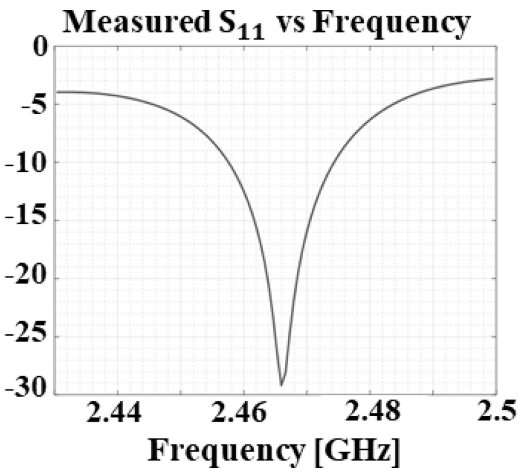

FIGURE 17. Measured S_{11} with external matching network.

of active power consumption versus sensitivity [1] can be seen in Fig. 18 for receivers operating in the 2.4-GHz ISM band. Simulated in-band IIP3 is −51 dBm. The active area is 0.0274 mm^2. A die photograph can be seen in Fig. 19.

VII. WAKE-UP RECEIVER FOR NB-IOT

Given the performance tradeoffs of low-power radio techniques, it is often challenging to translate these techniques to standard-compliant radios. Most modern communication standards require higher data rates, stricter blocker tolerance, higher sensitivity, support more spectral efficient modulations, and/or need to be highly reconfigurable to support advanced techniques at the higher networking layers. Due to these challenges, a system-level approach that addresses lowering power at the networking, signaling, system, and transistor-level is often needed. In addition, heterodyne architectures are virtually always required over alternative radio topologies. In this section, a brief background on the challenges of standard-compliant radios is given as well as a fabricated example of an NB-IoT standard WRX is highlighted.

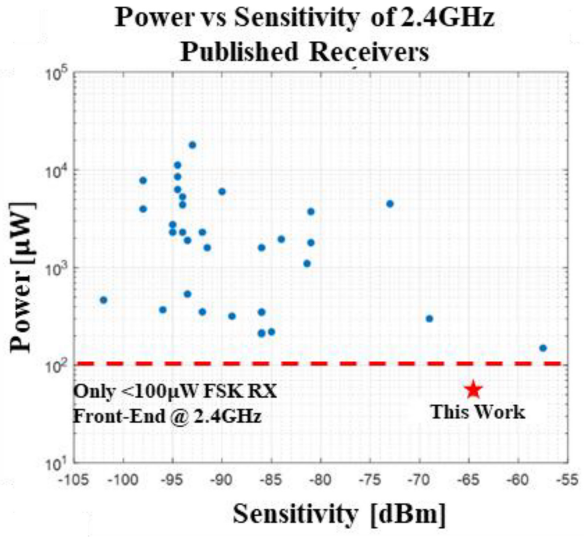

FIGURE 18. RX active power versus sensitivity for published FSK receivers operating at 2.4 GHz.

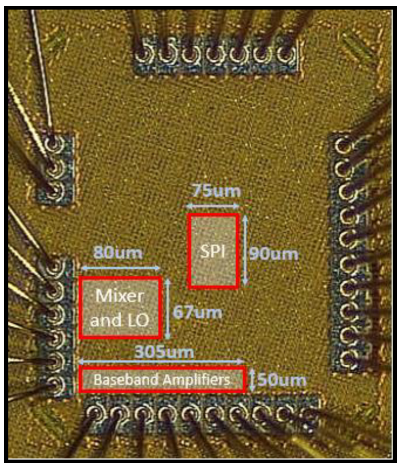

FIGURE 19. Die photograph of mixer-first receiver.

A. BENEFITS OF A WAKE-UP RECEIVER

One way to address the high-power consumption of standard-compliant RXs is through the use of duty cycling [41]. With this system-level approach, the RX is only reachable during set intervals in time and can be turned off in-between, directly saving power at the cost of latency. In extreme cases, the RX may only be reachable several times a day. However, for event-triggered IoT applications, this long latency may be unacceptable. A different solution that can break the latency versus power tradeoff is the use of a WRX [6]. In the wake-up paradigm, an always-on or frequently-on WRX listens for a wake-up message when the main RX is off. Once this wake-up message is detected by the WRX, the main RX is turned on for payload information on demand. As the wake-up message only contains 1 bit of information (turn on or not), simplified signaling and demodulation techniques can be used such as correlation against a stored template which can make the power of the WRX much less than the RX.

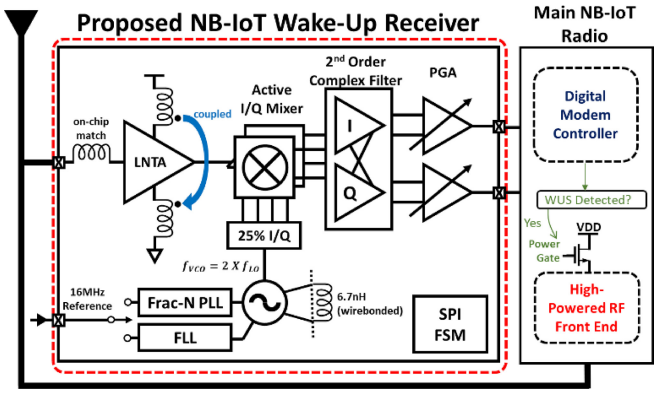

FIGURE 20. Block diagram of the fabricated wake-up receiver, showing configuration with the main NB-IoT radio.

Increasingly, commercial standards such as Wi-Fi, NB-IoT, and 5G NR are including wake-up signaling as standard compliant. A design example for the cellular NB-IoT standard is highlighted to show the power savings for commercial radios when operating with a WRX.

B. NB-IOT BACKGROUND

NB-IoT is a low-power, wide-area network (LPWAN), cellular IoT protocol defined by 3GPP to target long-range, low data rate, and long battery life. While based on the same sub-6-GHz technology as LTE, NB-IoT is officially included by 3GPP as a 5G standard and will experience continuous support and growth throughout the lifetime of 5G [40]. Cellular IoT standards such as NB-IoT serve a different use case than other wireless protocols used for IoT such as BLE, WiFi, or LoRa, as they operate on licensed spectrum from commercial cell towers and do not rely on locally installed routers. This means NB-IoT scales to a larger number of devices and has the ability to maintain coverage "coast-to-coast" compared to other IoT protocols. However, due to the need for integration with existing 4G/5G standards, NB-IoT is much more complex than other IoT protocols and requires not only high-performing analog components but also more advanced digital baseband processing.

Recently reported commercial NB-IoT radios have not addressed NB- IoT RX power consumption or explored integration of wake-up receivers. In [42], an NB-IoT TRX with integrated PA and multitone TX support is reported; however, the RF receiver consumes 53 mW of power in lower band operation. In [43], emphasis was put on GNSS and NB-IoT integration but not low power, with an RF RX power consumption of 50 mW reported. The SAW-less NB-IoT TRX of [44] duty cycles the RX LO to achieve a lower power consumption, but still spends considerable power on the RF front-end and reports an RX power of 11.8 mW. The work of [62] achieves a very low power but is only an RF-front end and does not include PLL power. Reference [63] similarly reports a high power of 43 mW for the RX. The limiting factor for these receivers is the use of high-powered RF front-end components and frequency synthesizers which are

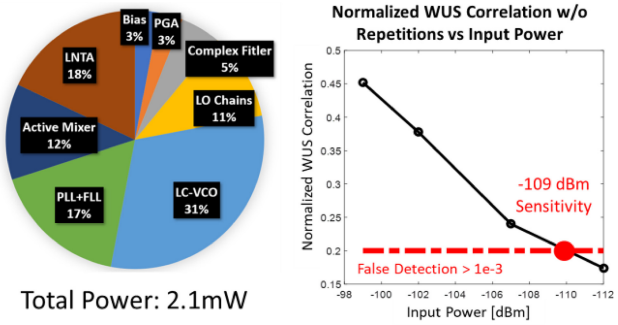

FIGURE 21. Power and sensitivity.

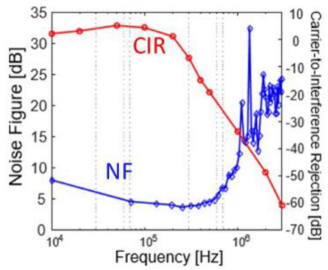

FIGURE 22. Carrier-to-interference-ratio of CW interferer and noise figure.

needed to demodulate OFDM QPSK messages while still meeting high sensitivity. The novelty of this work is the introduction of a stand-alone WRX for NB-IoT to reduce power. Thus, ease of integration with the NB-IoT standard is important in addition to the WRX power and sensitivity performance. The WUS is not modified from that sent from commercial cell towers utilizing Rel 15 NB-IoT, meaning no logistical cost is associated with our implementation of a WRX. This is a key difference between WRX architectures for other protocols that require firmware changes or nonstandard compliant OOK signaling to be transmitted [45].

C. WRX ARCHITECTURE

The RF front-end consists of a current-reuse Low-Noise transconductance amplifier (LNTA), active I/Q mixers, complex filter, 4th order bandpass filters, and programmable gain amplifiers (PGAs) [49]. A block diagram of the RF components is shown in Fig. 20. The LO consists of a fractional-N PLL with LC-VCO which utilizes an off-chip inductor to reduce power consumption through its high Q. The fine frequency resolution of the fractional-N PLL is needed to align to the NB-IoT symbols with minimal center frequency offset (CFO). The phase noise of the LO can be relaxed to save power due to the lower SNR requirement of the correlation-based WUS signal. The RF front-end operates in the RF frequency range of 750–960 MHz and converts the signal to a low-IF.

D. MEASURED RESULTS

The NB-IoT WRX was fabricated in 28-nm CMOS, operates at 0.9 V, and occupies an area of 1.08 mm^2 [49]. Power

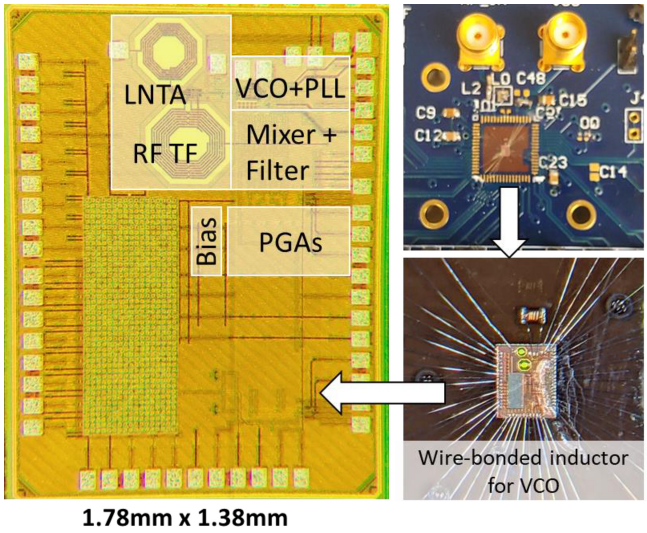

FIGURE 23. Fabricated NB-IoT WRX.

breakdown and sensitivity are shown in Fig. 21. Sensitivity performance was measured by sending the standard-specified Zadoff–Chu OFDM WUS signal to the WRX, then using an FFT and correlating the baseband signal off-chip. Both the correct WUS signal and incorrect WUS signals were swept to find false detection probabilities. A normalized correlation of >0.2 was found to be needed to ensure false detection probability fell below $>10^{-3}$, and sensitivity was taken at this value. An NF of 4–8 dB is measured in the low-IF bandwidth and a carrier to interference ratio of −35 dB at a 1-MHz offset from a CW interferer as reported in Fig. 22. Fig. 23 shows the fabricated WRX and wire-bonded inductor.

VIII. CONCLUSION

While there have been great advances in reducing the power for OOK receivers, there still exists a considerable gap in innovations for low-power RX designs that can support spectrally efficient modulation, higher data rates, increased blocker performance, and increased reconfigurability. This will become increasingly important as RX spectrum becomes more and more congested and modern wireless standards continue to advance in complexity. Low-power heterodyne architectures need to be re-examined for new innovations to lower power while mainlining acceptable performance. One such promising architecture is the mixer-first RX. Presented here is a background on low-power heterodyne architectures and a detailed generalized theory for low-power mixer first RXs. Formalizing the power performance of heterodyne architectures can inform low-power designs in the future. In addition, an ULP mixer-first RX and a standard compliant NB-IoT WRX highlight recent directions for low-power heterodyne RXs. This background, theory, and design examples will motivate more investigation into low-power heterodyne RXs to complement existing research on other types of low-power RXs such as ED-first.

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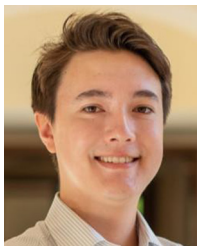

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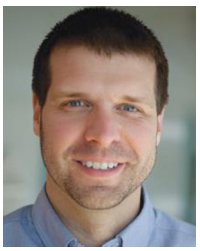

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