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Continuous-Time Pipelined ADC: A Breed of Continuous-Time ADCs for Wideband Data Conversion

HAJIME SHIBATA (Senior Member, IEEE)

(Invited Paper)

Toronto Design Center, Analog Devices Canada, Toronto, ON M5G 2C8, Canada

CORRESPONDING AUTHOR: H. SHIBATA (e-mail: hajime.shibata@analog.com)

ABSTRACT The continuous-time (CT) pipelined analog-to-digital converter (ADC) is an emerging ADC architecture suitable for wide-bandwidth (BW) digitization in fully integrated receiver applications. It inherits the integration-friendly features of CT $\Delta\Sigma$ ADCs, such as inherent anti-aliasing, while achieving the wide-BW operation originating from discrete-time (DT) pipelined ADCs. In this review article, we introduce a gain-centric ADC model and apply the key criteria derived from the model to transform a DT pipelined ADC into a CT pipelined ADC. We then discuss the design considerations and essential building blocks of the CT pipelined ADC. Finally, we examine several implementations of this architecture with their highlights and challenges.

INDEX TERMS Analog-to-digital converter (ADC), continuous-time (CT) ADC, oversampling ADC, pipelined ADC, wideband ADC.

I. INTRODUCTION

WHEN classifying analog-to-digital converter (ADC) architectures, one aspect is based on how the arithmetic operations are performed to digitize the amplitude levels in the analog domain, which distinguishes architectures, such as $\Delta\Sigma$ (including traditional single-loop and MASH structures), pipelined, and successive approximation register (SAR) ADCs. Another aspect can be based on how the analog signal processing is performed, either in the continuous-time (CT) or discrete-time (DT) circuitry. Fig. 1 provides a visual representation of this classification framework. Historically, most ADC architectures have been implemented in DT circuits, and CT implementation has been applied almost exclusively to $\Delta\Sigma$ ADCs.

Within these classifications, CT $\Delta\Sigma$ ADCs have been the favored choice for fully integrated wireless receiver applications due to their inherent anti-aliasing and resistive input interface [1], [2], [3], [4], [5], [6], [7], [8]. Fig. 2 shows the bandwidth (BW) as a function of sampling frequency (f_S) for CT $\Delta\Sigma$ ADCs over the years based on [9]. The plot also includes typical BW requirements for 3G, 4G, and 5G cellular radio systems. It is clear that CT $\Delta\Sigma$ ADCs have successfully met the BW requirements for 3G and 4G applications. However, they have yet to satisfy the BW requirement for 5G (approximately 500 MHz) because the f_S becomes excessively high to achieve the BW even with the latest CMOS technologies.

In contrast, the pipelined ADC is known as an architecture for wide-BW digitization. However, it has historically been implemented in DT circuits [10], [11] and requires additional circuits, such as an anti-aliasing filter (AAF) and ADC driver when it is used in fully integrated wireless receiver applications, thus incurring higher system-level power consumption.

Considering these situations, a compelling solution for applications requiring both wide-BW operation and the benefits of CT signal processing could be an architecture that combines the CT benefits from CT $\Delta\Sigma$ ADCs and the wide-BW operations from DT pipelined ADCs as in Fig. 1. The CT pipelined ADC [12], [13], [13], [14], [15], [16], [17], [18], [19], [20], [21] is one such architecture developed with this motivation in mind.

In this review article, we first introduce a gain-centric ADC model and discuss the differences between CT and DT ADCs based on the model in Section II. In Section III, we derive a CT pipelined ADC from a DT pipelined

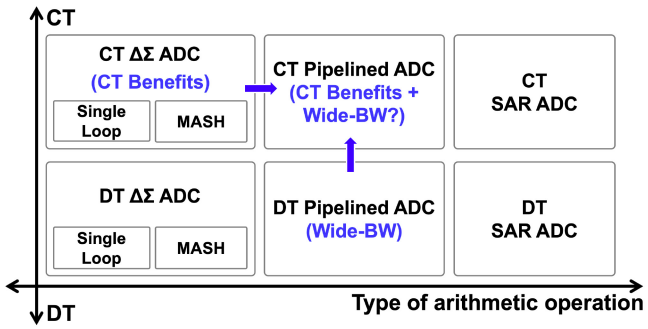


FIGURE 1. Classification of ADC architectures.

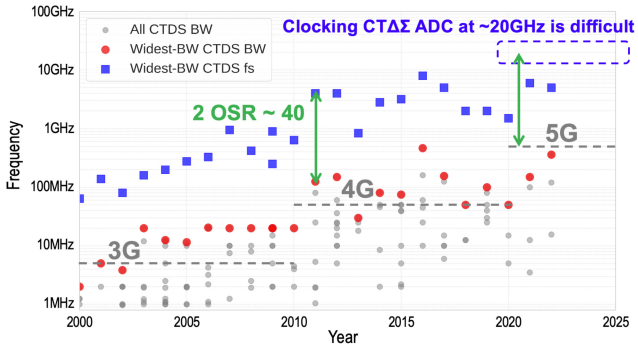


FIGURE 2. BW and f_S of CT ΔΣ ADCs over the published years. Typical ΔΣ ADC requires OSR > 20, and f_S limited < 10 GHz due to process technology limitations.

ADC by applying the criteria derived from the gain-centric ADC model. In Section IV, the building blocks of the CT pipelined ADC are discussed. Design examples are reviewed in Section V, and conclusions are presented in Section VI.

II. CONTINUOUS-TIME ADC VERSUS DISCRETE-TIME ADC

A. GAIN-CENTRIC ADC MODEL

High-resolution ADCs typically consist of four key sub-blocks: 1) a linear analog gain block; 2) a linear digital signal processing block; 3) quantizers; and 4) digital-to-analog converters (DACs). As depicted in Fig. 3, the linear analog gain and the linear digital signal processing blocks are interconnected via the quantizers and the DACs. In this model, we treat both the DAC and the quantizer as linear blocks, with the quantizer introducing a quantization noise Q_N determined by its LSB at its output.

The primary purpose of the linear analog gain block is to provide a gain G from the ADC input to the last quantizer, thus reducing the quantization noise Q_N of the last quantizer to Q_N/G when it is input-referred. In contrast, the purpose of the DAC is to cancel the input signal as much as possible to ensure that the amplified signal is bounded within the full scale of the last quantizer. This is critical because the saturation of the quantizer can cause Q_N to exceed the value determined by the LSB step of the quantizer, thereby invalidating the Q_N/G assumption.

In the proposed ADC model, all input and output nodes of the linear analog gain block, except for the analog input

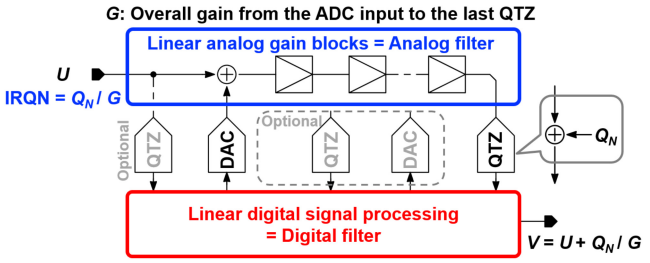


FIGURE 3. Gain-centric ADC model.

signal node, are fully provided to and from, or observed by, the linear digital signal processing block. Therefore, as discussed in Appendix A, the analog input signal U can be reconstructed as the digital signal V as

$$V = U + \frac{Q_N}{G} \tag{1}$$

with an error of Q_N/G when an appropriately designed linear digital signal processing block, or a digital filter, is employed. Consequently, the system operates as a high-resolution ADC with an input-referred quantization noise suppressed by the gain G as Q_N/G.

Two critical observations drawn from this gain-centric ADC model are as follows.

1) The gain G from the ADC input to the last quantizer determines the quantization noise level at the digital output. Therefore, the gain G must be maximized to design a high-resolution ADC.
2) For successful reconstruction of the input signal using linear signal processing in the digital domain, the signal processing in the analog domain must be linear (or nonsaturated) and the quantizer inputs must remain within their full scale.

Given these principles, the primary task of an ADC designer is to design a system that maximizes the gain and BW of G within the constraints of not saturating the analog gain block and the quantizers. Note that additional quantizers and DACs can be incorporated as shown in Fig. 3, and such detailed examples are discussed in Appendix B. As in Appendix B, G can also be a frequency-dependent gain.

B. CT AND DT ADCS

Applying the gain-centric ADC model, we define CT and DT ADCs in this article as follows. A CT ADC employs a CT analog filter as the linear gain block, as illustrated in Fig. 4(a). This analog filter block commonly uses active-RC filters or g_m-C filters. Conversely, a DT ADC uses a DT analog filter as the linear gain block, as shown in Fig. 4(b). Typically, a switched-capacitor filter is utilized in this case. It is important to note that DT ADCs incorporate a sample-and-hold circuit at their input, either explicitly or implicitly, as part of the switched capacitor filter.

C. ADVANTAGES OF CT ADC

CT ADCs have two key advantages over their DT counterparts: 1) a resistive input interface and 2) inherent

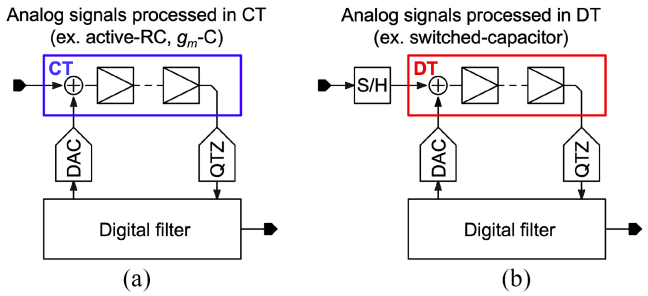
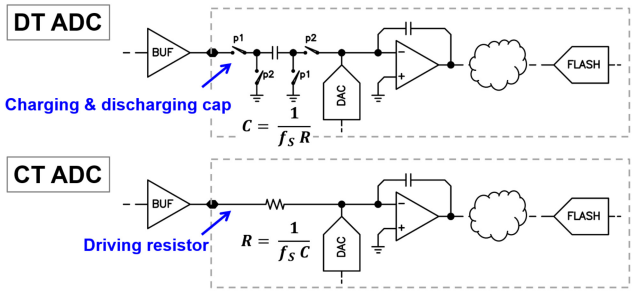


FIGURE 4. (a) CT and (b) DT ADCs. DACs are typically driven by quantizers without any filtering. See Appendix A.



DT ADC peak driving current > CT ADC peak driving current

FIGURE 5. Typical input structure of DT and CT ADCs.

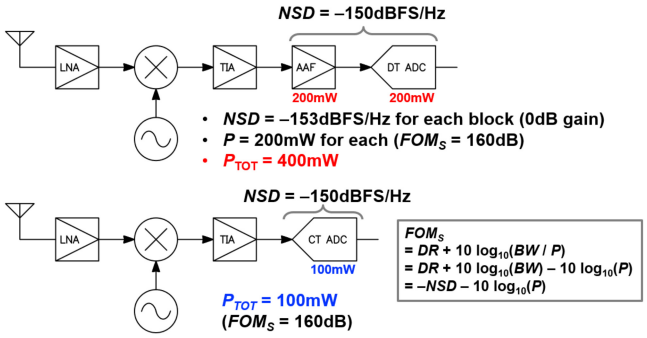


FIGURE 6. Benefit of inherent anti-aliasing in a wireless receiver application.

anti-aliasing, especially when used in a fully integrated signal chain where the circuits driving the ADC are also integrated on the same IC chip. A typical input structure of a DT ADC and a CT ADC is shown in Fig. 5, where a switched capacitor circuit connects the ADC input to the summation node in the DT ADC, while a resistor connects these two nodes in the CT ADC. If these circuits are designed to add the same kT/C and thermal noise, the sampling capacitor C is designed to be $C = 1/(f_S R)$. Such a capacitor requires a much higher peak driving current than the resistor (typically more than 5× [14]), resulting in higher power consumption in the ADC driver. The same applies to the internal operational amplifiers in the switched capacitor filter in the DT ADCs. As a result, the signal chain, including a CT ADC, generally outperforms one including a DT ADC in terms of power efficiency.

Another advantage of the CT ADC is the inherent anti-aliasing, or the ADC also acts as an anti-AAF. The DT ADC has a sampler at the ADC input as shown in Fig. 5. Thus, a signal at f_S is aliased at dc without any attenuation. In the CT ADC, however, sampling is performed implicitly by the last quantizer connected at the end of the analog gain or filter section. In CT $\Delta\Sigma$ ADCs, the analog gain block is typically a cascade of integrators, allowing signals at multiples of f_S to be attenuated compared to the signal near dc before reaching the quantizer where the sampling occurs. Thus, the ADC provides attenuation of the aliased signals, in other words, *inherent anti-aliasing* is achieved [12].

The inherent anti-aliasing improves power efficiency at the system level. To illustrate the benefit, consider a fully integrated wireless receiver application that uses either a DT or a CT ADC as the baseband digitizer, as shown in Fig. 6. When a DT ADC is used, it generally requires an anti-AAF and an ADC driving buffer if not included in the ADC, thereby inducing additional thermal noise. In contrast, a CT ADC often does not require these additional blocks for the same anti-aliasing performance thanks to its inherent anti-aliasing.

We then compare the power consumption of the DT and CT signal chains under the conditions where: 1) the DT and CT baseband sections maintain the same noise spectral density (NSD) and 2) Schreier figure of merit (FOM$_S$) for the CT, DT ADCs, and AAF are the same. Under these assumptions, the DT configuration consumes more power than its CT counterpart. This is because the AAF and ADC in the DT signal chain must achieve a lower NSD to maintain the same NSD for the entire baseband section, resulting in higher power consumption for each block.

In the scenario shown in Fig. 6, a –150 dBFS/Hz NSD and a 160-dB FOM$_S$ are assumed for conditions 1) and 2), respectively. Note that ADCs typically exhibit a 160-dB FOM$_S$ for ∼100-MHz BW, as in Section V, and the FOM$_S$ of the AAF is typically in the range of 150–160 dB [21]. In the DT signal chain, both the AAF and ADC must achieve an NSD of –153 dBFS/Hz to maintain the overall NSD of –150 dBFS/Hz with the 0-dB AAF in-band gain. This leads to a power consumption of 200 mW for each block and 400 mW in total. In contrast, the CT signal chain achieved the target NSD with 100 mW, resulting in a 4× power efficiency in the CT signal chain in this example.

Note that this comparison is simplified and has limitations. The FOM$_S$ of AAF, CT, and DT ADCs may not be the same for a given design target. A comprehensive analysis must also consider various other factors, such as f_S, OSR, and digital signal processing complexity.

As demonstrated in this example, the inherent anti-aliasing of CT ADCs improves the power efficiency of the entire signal chain. This is the main reason why CT $\Delta\Sigma$ ADCs are frequently used in systems that require anti-aliasing to be integrated on the same chip.

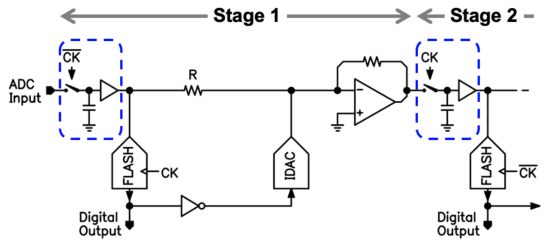


FIGURE 7. One stage of a DT pipelined ADC. A flash ADC is used as a quantizer which is activated based on the clock [14].

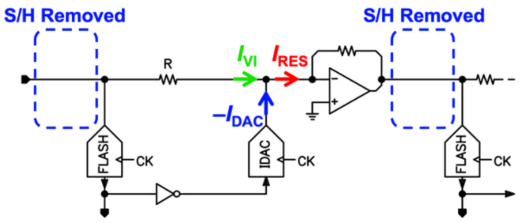


FIGURE 8. CT residue generation stage derived from a DT residue generation stage by removing S/H [14].

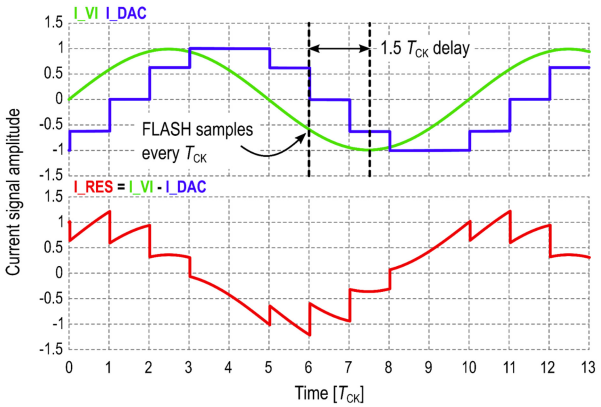


FIGURE 9. Summing-node current waveforms of CT stage in Fig. 8 [14].

D. DISADVANTAGES OF CT ΔΣ ADC

While CT ΔΣ ADCs offer the CT benefits, they have a limited achievable BW. ΔΣ ADCs are oversampling ADCs and typically require a high oversampling ratio ($OSR = f_S/(2\text{BW})$) as in Appendix B especially when a single-loop structure is used. This limitation is a consequence of the digital feedback inherent in the architecture. To maintain stability, the loop gain, which includes both the gain G and the digital feedback, must be kept below 0 dB within a Nyquist frequency as discussed in Appendix B. Consequently, the digitization BW, where the gain G is maintained at a high level, becomes a small fraction of $f_S/2$.

This BW limitation can be circumvented when the DAC is controlled in a feedforward manner. With feedforward control, the BW of the gain G can be decoupled from the stability requirement, thereby allowing the BW to increase. The ADC architecture that relies solely on feedforward cancellation is the pipelined ADC. Therefore, implementing a pipelined ADC with a CT circuit can effectively address the BW problem associated with CT ΔΣ ADCs.

III. CONTINUOUS-TIME PIPELINED ADC

The structural difference between CT ADCs and DT ADCs is how the analog gain block is implemented as discussed in Section II-B. Therefore, one could theoretically transform a DT pipelined ADC into a CT pipelined ADC by simply replacing the DT gain block with a CT gain block. However, such a direct replacement fails since internal signals tend to saturate and thereby violate the two criteria of the gain-centric ADC model discussed in Section II-A. To combat this problem, two additional techniques have been developed: 1) delay alignment [5], [6], [7], [8], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23] and 2) low-pass interstage amplifiers [6], [14], [16], [17], [18], [19], [20], [21]. The following example demonstrates the transformation of a DT pipelined ADC into a CT pipelined ADC, illustrating how simple replacements can violate the criteria and how the two additional techniques rectify these violations [14].

Fig. 7 depicts an example of a DT pipelined ADC stage. In this example, a sampler is connected to the stage input, but all internal operations are performed in CT circuits. Therefore, simply removing the sampler could convert the DT pipelined ADC into an intermediate CT pipelined ADC, as shown in Fig. 8.

Fig. 9 illustrates the waveforms of the summing-node current when a full-scale input signal of 1 GHz is applied to the system clocked at 10 GHz. The system utilizes a 4-bit flash ADC and DAC, with the DAC being activated one clock cycle after the flash ADC samples the signal. The full scale is assumed to be ±1 at all nodes.

As mentioned in Section II-A, the DAC's purpose is to cancel the input signal. However, due to the timing difference between the input signal and the DAC output current, the cancellation is not effectively realized, leading to the residue signal exceeding stage 1's input full scale. This results in saturation, thereby violating the criteria outlined earlier. This 1.5 T_{CK} timing difference in Fig. 9 consists of two components: 1) 1 T_{CK} for flash conversion, data propagation, and DAC settling time and 2) 0.5 T_{CK} for an effective delay of a nonreturn-to-zero DAC output waveform, where T_{CK} represents one clock period. Aligning this delay difference between the upper and lower paths is straightforward and can be achieved by adding a delay, as shown in Fig. 10. The waveform with the added delay is illustrated in Fig. 11. This confirms that the cancellation is effective and that the input residue current remains within the full-scale range, thus avoiding saturation.

Although timing alignment has reduced residue amplitude, the resulting amplitude is still not satisfactory. With deploying a 4-bit flash ADC–DAC pair, we expect a peak residue of 1/16, or 6.25% as in DT pipelined ADCs. However, the peak residue signal reaches 40% of the full scale. With such a high residue amplitude, the stage gain is limited to only 2.5×. This limitation hampers the achievement of a high gain G.

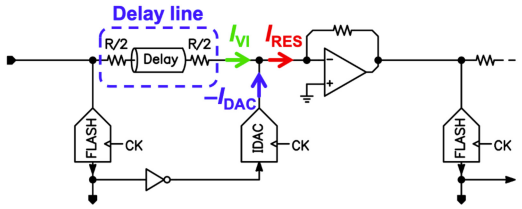


FIGURE 10. CT residue generation stage with the delay alignment [14].

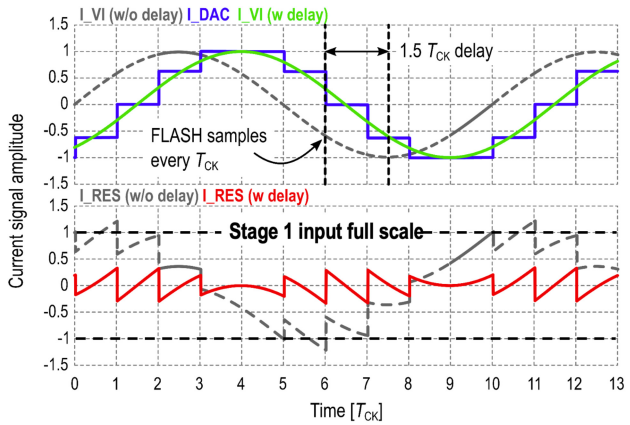


FIGURE 11. Summing-node current waveforms of CT stage in Fig. 10 [14].

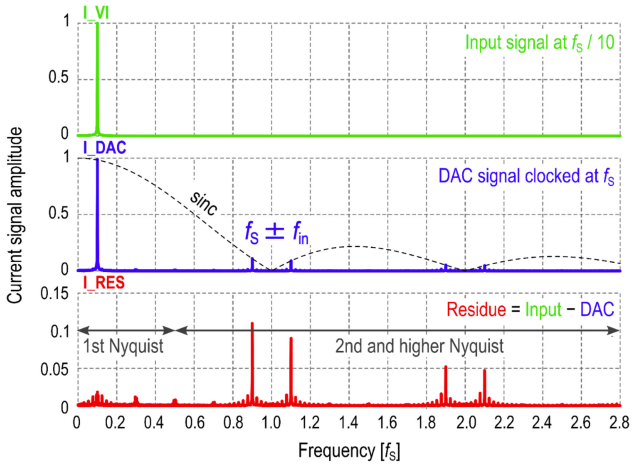


FIGURE 12. Summing-node signals in the frequency domain [14].

This unexpectedly high residue is due to DAC image signals, as evidenced by the frequency-domain waveforms depicted in Fig. 12. By transitioning the interstage amplifier from a flat gain amplifier to a low-pass amplifier, as illustrated in Fig. 13, we can attenuate the DAC image signals. Fig. 14 presents the stage voltage output waveform with and without the low-pass filtering and an 8× dc gain. This comparison confirms that the stage output waveform stays within the input full scale of the subsequent stage, thereby effectively avoiding saturation.

As discussed throughout this example, the two criteria can be satisfied by a CT implementation of a pipelined ADC with the timing alignment and the low-pass interstage gain techniques. By incorporating such a stage, we can derive a

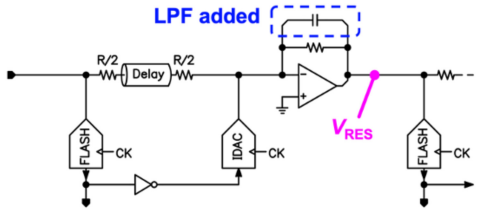


FIGURE 13. CT residue generation stage with a low-pass interstage amplifier [14].

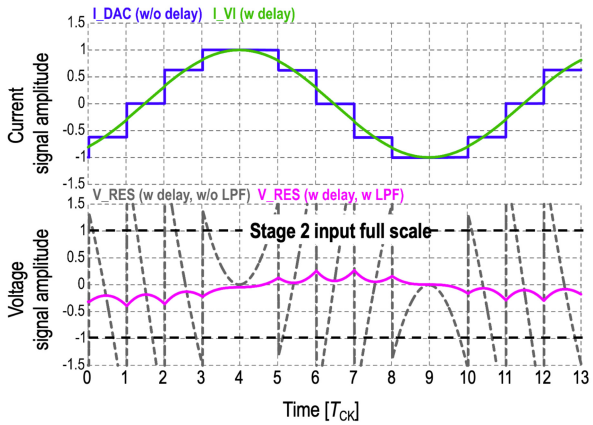


FIGURE 14. Stage output voltage waveforms with/without the low-pass interstage amplifier with associated input current waveforms [14].

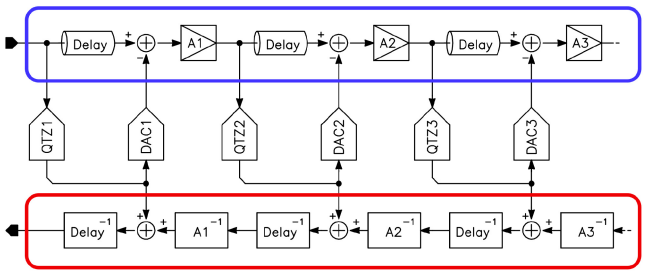


FIGURE 15. Generalized CT pipelined ADC.

generic pipelined CT ADC as illustrated in Fig. 15, where the details of each block are discussed in Section IV.

This system has no sample-and-hold circuits in the analog filter section, thus enjoying all the CT benefits. In addition, due to the transfer function matching and the low-pass interstage amplifiers, the system maintains a high and wide BW gain G from the ADC input to the last quantizer. Therefore, it should perform as a wideband CT ADC.

IV. BUILDING BLOCKS OF CT PIPELINED ADC

This section discusses the building blocks of the CT pipelined ADC in Fig. 15 including the digital reconstruction filter.

A. INTERSTAGE AMPLIFIER

An interstage amplifier together with a delay element provides a voltage gain and low-pass filtering transfer function. Thus, the block can be designed based on three parameters: 1) dc gain; 2) cut-off frequency; and 3) order of the filter.

The dc gain is dictated solely by the resolution of the quantizer–DAC pair connected to the summing node of the interstage amplifier. In an ideal DT pipelined ADC with no component errors, the residue amplitude produced by cancellation is bounded to $1/M$ of the input full scale of the subsequent stage, where M represents the number of comparators in a flash-ADC-based quantizer. However, practical implementation introduces certain errors, such as comparator offsets, which increase the residue amplitude. To prevent saturation of the quantizer in the subsequent stage, the dc gain is typically set to $M/2$ in DT pipelined ADCs. The same approach can be applied to the CT pipelined ADC.

The cutoff frequency is determined by three factors: 1) ADC BW since the cascade transfer function of the interstage amplifier represents the gain G that determines Q_N suppression; 2) the image suppression requirement of the DAC, which requires less than 0 dB gain in the second or higher Nyquist zones; and 3) cancellation quality, which is discussed further in Section IV-C.

The filter order presents another design parameter. While a higher-order filter is generally advantageous for extending the BW and reducing the leakage term, an excessively high order could complicate the digital filter as we discuss in Section IV-D. Consequently, a second-order filter appears to be a reasonable choice.

B. PASSIVE DELAY ELEMENT

The primary role of the delay element is to achieve a similar transfer function to the flash–DAC path to minimize the signal leakage as discussed in Section III. If the DAC is activated one clock cycle (T_{CK}) after the flash sampling, and DAC generates a nonreturn-to-zero waveform, the flash–DAC transfer function G_{FD} is modeled as

$$G_{FD}(s) = \frac{I_{FS}}{V_{FS}} \frac{1 - \exp(-s\ T_{CK})}{s} \exp(-s\ T_{CK}) \qquad (2)$$

in the first Nyquist zone, where I_{FS} and V_{FS} represent the output full-scale current of the DAC and the input full-scale of the flash ADC, respectively [12], [14]. The resulting group delay at dc is 1.5 T_{CK}, which aligns with the observations in Fig. 9.

G_{FD} exhibits a sinc magnitude response. However, it is approximately unity below $f_S/8$. Its phase response is depicted in Fig. 16. Consequently, G_{FD} can be approximated as an all-pass delay transfer function, and the delay element is thus designed to synthesize this all-pass transfer function.

Such a transfer function can be implemented by RC and LC lattice structures as shown in Fig. 17. In the case of the RC lattice, the maximum phase rotation is limited to 180°, as shown in Fig. 16. This level of phase rotation is typically sufficient for ADCs with an OSR greater than 4 [5], [6], [7], [8], [14], [16], [17]. When an improved matching across a wider BW is needed, an LC lattice or an LC ladder can be used [14], [19]. Cascading multiple sections further rotates the phase, enabling a more precise transfer function match across a wider BW. Another drawback of using

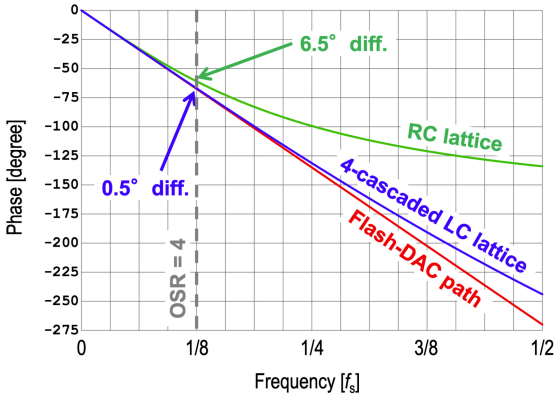


FIGURE 16. Phase response comparisons, including the ideal flash–DAC response, an RC lattice, and an LC lattice.

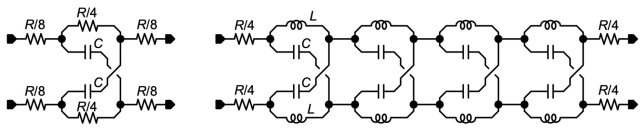


FIGURE 17. Examples of passive delay elements. (a) RC lattice delay. (b) LC lattice delay.

RC-based structures is that the input impedance decreases at high frequencies, resulting in a higher ADC driving current. However, the input impedance still contains a relatively high series resistance component. Therefore, the additional drive current is still less than that of the DT counterpart.

To simplify the discussion, only phase or delay matching is discussed here. However, in recent publications, more precisely approximated delay elements are used, including magnitude response matching, as shown in Section V. Note also that, as in (2), $G_{FD}(s)$ varies depending on the delay from the flash sampling to DAC activation. If a shorter delay is assumed (e.g., if the DAC is triggered after $T_{CK}/2$ instead of T_{CK} after flash sampling), $G_{FD}(s)$ has less phase rotation, thus the same delay line provides better phase matching up to higher frequencies. Also, the resolution of the flash–DAC path has an indirect effect on the BW where the matching is maintained. If a lower resolution is used, the interstage gain is reduced, and a higher phase error can be accommodated.

C. SIGNAL LEAKAGE TRANSFER FUNCTION

In CT pipelined ADCs, achieving perfect cancellation between the voltage-to-current (V-to-I) path and the flash–DAC path across a wide BW is inherently challenging. With increasing input signal frequency, a greater amount of signal leaks to the interstage amplifier, potentially leading to saturation of the subsequent stage. To alleviate this issue, a low-pass interstage transfer function can be employed especially when the cancellation provided by the delay element is insufficient.

The magnitude of the leakage term is evaluated using the signal leakage transfer function $L(s)$ defined as

$$L(s) = \frac{V_{OUT}}{V_{IN}} = \{G_{DLY}(s) - G_{FD}(s)\}\ H_{TIA}(s) \qquad (3)$$

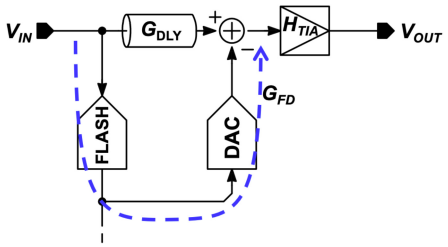


FIGURE 18. Signal leakage transfer function.

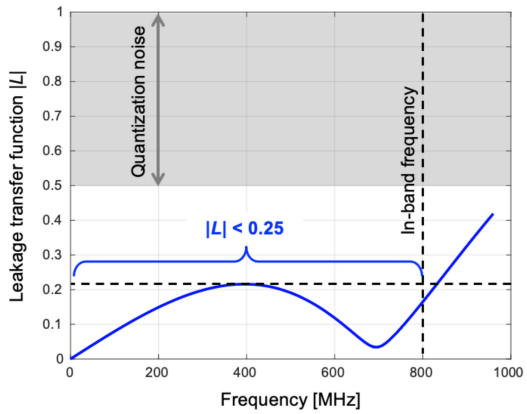


FIGURE 19. Frequency response of a signal leakage transfer function with a practical RC delay element.

where G_{DLY}, G_{FD}, and H_{TIA} are the transconductance of the delay element, the transconductance of the flash-to-DAC path, and the transimpedance of the interstage amplifier, respectively, as shown in Fig. 18 [12], [14], [16], [22], [23]. As a rule of thumb, $|L(s)| < 0.25$ in the in-band frequency range should be maintained to prevent saturation of the subsequent stage, accounting for the presence of quantization noise and other errors.

Fig. 19 illustrates an example of a leakage transfer function. In this example, an RC delay element is used together with a second-order low-pass interstage amplifier to achieve an 800-MHz BW. The leakage transfer function shows that the leaked term is kept below 20% of the subsequent stage's full scale for in-band frequencies.

A practical consideration in the design of the leakage-associated circuits is the matching and tracking of the transfer functions over the operating temperature. There are several sources of error, including the flash ADC reference voltage error and the DAC reference current error in the flash–DAC path, as well as resistance and capacitance variations in the delay path. To mitigate the effects of these errors, initial power-up calibrations can be performed.

D. DIGITAL RECONSTRUCTION FILTER

The digital reconstruction filter is a multi-input–single-output digital filter whose job is to reconstruct the analog input signal of the ADC. To determine the required filter coefficients for this digital filter, we examine the behavior of such a block within the context of a traditional DT pipelined ADC and then apply the same scheme to a CT pipelined ADC [12].

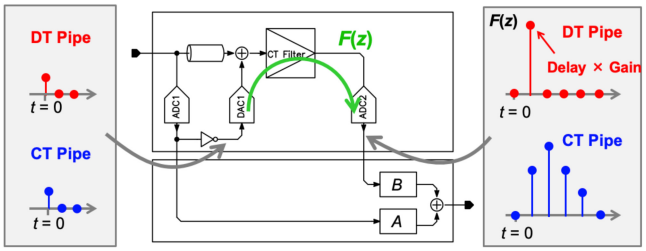


FIGURE 20. DT impulse response $F(z)$, which represents the FIR coefficients in the digital reconstruction filter.

In a DT pipelined ADC, the interstage amplifier typically consists of a DT residue amplifier with a certain gain, such as 8. When an impulse is applied through a DAC at one stage, the same impulse is observed at the input of the last quantizer, but with an amplification based on the amplifier's gain. Additionally, the output signal is delayed due to the DT operation as shown in $F(z)$ in Fig. 20.

To reconstruct the signal in the DT pipelined ADC, the inverse of the gain (1/8) and the delay are applied to Filter B. This is equivalent to implementing $1/F(z)$ as Filter B assuming Filter A to be unity in Fig. 20.

The reconstruction in a CT pipelined ADC follows the same process. The impulse response from the first-stage DAC to the final quantizer is measured as $F(z)$, which may be spread over multiple cycles due to filtering. Filter B is then designed as $1/F(z)$ to reconstruct the input signal. In practice, $1/F(z)$ could be noncausal, but causality can be restored by introducing an appropriate delay in Filter A.

While we have discussed the reconstruction signal processing using a two-stage example, the same technique can be extended to accommodate multistage cases within the CT pipelined ADC architecture.

Considering real-world applications, background estimation of digital filter coefficients is necessary as the CT filter response fluctuates with operating conditions, such as temperature and supply voltage. Cross-correlation-based [24] or LMS-based [25] coefficient estimation methods have been proposed for MASH ADCs and can be applied to CT pipelined ADCs. The mapping of the coefficients into the filter structure is another interesting issue to be addressed. Even in the simple structure shown in Fig. 20, several choices can be considered, such as 1) Filter $A = 1$, $B = 1/F(s)$; 2) Filter $A = F(s)$, $B = 1$; or 3) mapping decomposed coefficients of $F(s)$ to filter A and B. Each choice presents different trade-offs among digital filter complexity, number of taps, power consumption, and signal transfer function (STF). When considering multistage pipelined structures, the filter design space can be further expanded. Also as suggested in Fig. 20, the CT filter response could affect $F(z)$, thus the CT filter and digital filter could be co-designed with the aim of minimizing the digital filter complexity, or the total number of filter taps.

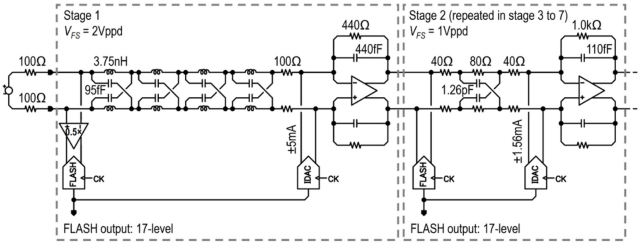


FIGURE 21. 1125-MHz BW CT pipelined ADC in 28-nm CMOS [14].

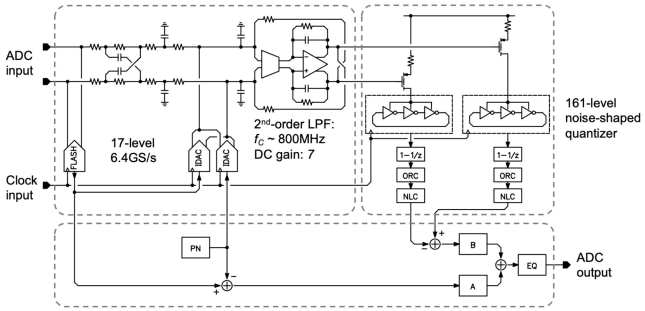


FIGURE 22. 800-MHz BW CT pipelined ADC in 16-nm FinFET [17].

V. CT PIPELINED ADC EXAMPLES

In this section, we review some of the reported implementation examples of CT pipelined ADCs with their technical highlights and challenges.

A. EXAMPLE 1: 1125-MHZ BW CT PIPELINED ADC IN 28-NM CMOS

The first example is a 5-stage CT pipelined ADC implemented in a 28-nm CMOS process with 2.3-W power consumption [14]. This ADC achieves –164-dBFS/Hz NSD over an 1125-MHz BW when clocked at 9 GHz, with a competitive 160-dB FOM_S for this BW thanks to the power-efficient CT implementation. A simplified schematic of the first and second stages of the pipelined ADC is shown in Fig. 21. The analog gain section employs cascaded first-order low-pass filters, along with an LC lattice in the first stage or RC lattice delay elements in the second or subsequent stages.

This ADC is the first silicon demonstration of a multistage CT pipelined ADC that implements the two key techniques: 1) timing alignment with delay elements and 2) a high effective interstage gain (8.8× at dc in Stage 1 and 6.25× in Stage 2 or later) realized by the low-pass interstage amplifiers. These techniques enabled multistage pipelining, which was not feasible due to the limited interstage gain of 4/3 even with a 9-level quantization in the former implementation [12]. Note that the effective stage gain is the stage gain when the stage input and output full scales are normalized to unity, which is the gain that reduces the quantization noise of the last quantizer when the noise is referred to the input full scale. The voltage gain and the effective gain of a pipelined stage may differ as a result of thermal noise optimization when a large voltage swing is allowed at some nodes, such as at the ADC input.

Compared to recent implementations, several aspects remain rudimentary: 1) the order of the interstage filter is limited to one; 2) the delay element is designed only to align the phase; and 3) the digital signal reconstruction is performed entirely off-chip.

B. EXAMPLE 2: 800-MHZ BW CT PIPELINED ADC IN 16-NM FINFET

The second example is a 2-stage CT pipelined ADC archiving –149-dBFS/Hz NSD for 800-MHz BW at 6.4-GHz clock frequency with 230 mW in 16-nm FinFET, resulting in 155-dB FOM_S [17]. The front-end stage is a CT residue generation stage similar to Example 1. The back-end stage is a 161-level output VCO ADC. The simplified schematic is shown in Fig. 22.

Several improvements have been incorporated into this ADC, including: 1) the delay element now matches both the phase and magnitude, reducing signal leakage; 2) the order of the interstage filter has been increased to two, extending the BW and suppressing out-of-band leakage with the sharper roll-off; and 3) the digital reconstruction filter and all associated hardware required to extract the filter coefficients have been fully implemented on-chip, with a background calibration capability that updates the digital filter coefficients based on die temperature changes. Note that 1-dB NSD degradation is observed over a 5 °C die temperature change. Therefore, to keep NSD degradation in the sub-dB range, background calibration should be performed at least once every few seconds, assuming a worst-case thermal increment rate of 1 °C/s.

While [14] effectively demonstrated the power efficiency of the analog section of the CT pipelined ADC, it did not address the feasibility of the digital processing. In contrast, Shibata et al. [17] proved that CT pipelined ADC technology is commercially viable and offers competitive performance as a wideband digitizer, even when the digital signal processing power consumption is included.

C. EXAMPLE 3: CT PIPELINED ADC WITH BUTTERWORTH STF

Manivannan et al. explored several interesting aspects of a CT pipelined ADC using a 4-stage CT pipelined ADC in 65-nm technology shown in Fig. 23 [18], [21], [26], [27], [28]. It achieves a 100-MHz BW and 70-dB SNR with 800-MHz f_S in 29 mW, resulting in a competitive 165-dB FOM_S. The ADC employs a single-opamp biquad configuration in the interstage amplifiers, along with an asynchronous SAR as the back-end quantizer.

Among the several findings, one of the highlights of [21] and [27] is discussing the STF design flexibility in CT pipelined ADCs. As discussed in Section II-C, CT ΔΣ ADCs offer the advantage of combining filtering and digitization functions, resulting in improved power efficiency for receiver systems. However, the design of the STF in CT ΔΣ ADCs

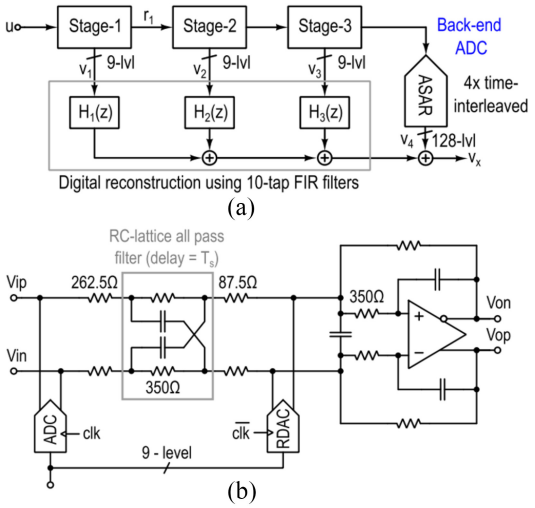


FIGURE 23. 100-MHz BW CT pipelined ADC in 65-nm CMOS. (a) Block diagram of the ADC. (b) Simplified schematic of the first stage [27].

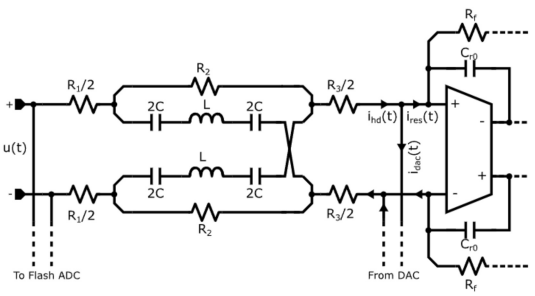


FIGURE 24. LCR delay element used in 3-GHz BW CT pipelined ADC in [19].

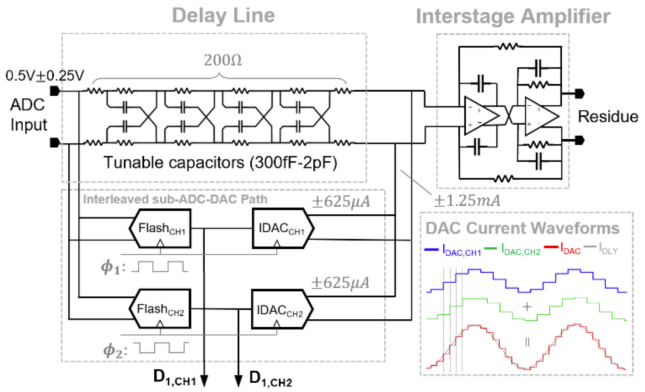


FIGURE 25. Stage 1 schematic for the 1000-MHz BW interleaved CT pipelined ADC [20].

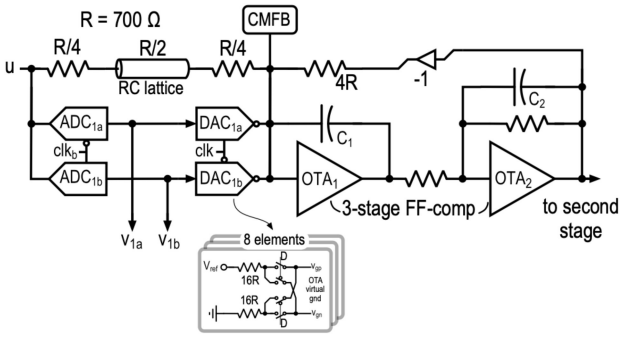


FIGURE 26. Simplified stage 1 schematic of the interleaved CT pipelined ADC [21].

is constrained by the need to satisfy loop stability requirements. In [21] and [27], it is shown that the filter design in CT pipelined ADCs is much less constrained since there are no stability requirements to satisfy.

D. EXAMPLE 4: CT PIPELINED ADC WITH NEAR NYQUIST BW

The primary motivation for incorporating a pipelined architecture is to extend the digitization BW. In the previously discussed implementations, the OSR was limited to 4 to suppress the signal leakage when using RC or LC lattice element delay elements.

To reduce the OSR in order to increase the digitization BW, Ismail introduced a synthesized LCR lattice-based delay element, as shown in Fig. 24 [19]. This delay element incorporates two zeros in the leakage transfer function, resulting in an enhanced BW of 60% of the Nyquist frequency (corresponding to an OSR of 1.67), and a 3-GHz BW with a 10-GHz clock frequency is demonstrated in circuit simulations. Considering that some level of oversampling is typically required in practical applications, an OSR of 1.67 is considered sufficient for most use cases.

E. EXAMPLE 5: INTERLEAVED CT PIPELINED ADC

To further extend the BW, another possible approach is to increase f_S. In the case of DT ADCs, the effective f_S can be increased by using time-interleaving techniques. However, applying the time interleaving to CT $\Delta\Sigma$ ADCs has had limited success because the flash-to-DAC latency limits the loop BW, thereby limiting the digitization BW in CT $\Delta\Sigma$ ADCs.

In the case of CT pipelined ADCs, the latency of the flash-to-DAC path is only related to the delay element requirement and decoupled from the interstage amplifier BW. Consequently, the digitization BW can be increased by introducing time-interleaved flash-to-DAC paths.

Mittal et al. proposed an interleaved CT pipelined architecture as shown in Fig. 25. It demonstrated the extension of the BW to 1 GHz with an interleaving operation by utilizing both edges of a 6.4-GHz clock frequency [20]. Pavan et al. [21] independently developed a similar interleaved structure as shown in Fig. 26 with several additional features, including a filtering STF, embedded decimation, resulting in an effective OSR of 2.

F. COMPARISONS OF CT PIPELINED AND OTHER ADCS

This section discusses a comprehensive comparison of the performance of CT pipelined ADCs, as outlined in Table 1. The comparison includes CT pipelined ADCs and notable ADCs using other architectures, such as single-loop CT $\Delta\Sigma$ [29], MASH CT $\Delta\Sigma$ [8], and DT interleaved and pipelined SAR ADCs [30]. It can be seen from Table 1 that most of the CT pipelined ADCs have an OSR of 4 or

TABLE 1. Performance comparisons of CT pipelined and other state-of-the-art ADCs in the relevant application space.

	Example 1 JSSC 2017 [14]	Example 2 ISSCC 2020 [17]	Example 3 TCAS-I 2022 [27]	Example 4 TCAS-I 2023 [19]	Example 5 VLSI 2023 [20]	Example 5 JSSC 2023 [21]	VLSI 2019 [16]	ISSCC 2019 [29]	JSSC 2022 [8]	ISSCC 2019 [30]
Architecture	CT pipelined	CT pipelined	CT pipelined w/ decimation	CT pipelined	Interleaved CT pipelined	Interleaved CT pipelined	CT pipelined	Single-loop CT ΔΣ	MASH CT ΔΣ	DT Interleaved pipelined SAR
BW [MHz] (App BW* [MHz)	1125	800	100	3000 (1667)	1000	100	40	160	360	2500 (833)
f_S [MHz]	9000	6400	800	10000	6400	400	2400	2880	5000	5000
OSR	4	4	4	1.67	3.2	2	30	9	7	1 (3)
Power [mW]	2330	280	29	-	240	52	3.2	40	158	159
NSD [dBFS/Hz]	–164	–149	–150	-	–154	–154	–154	–154	–153	–152
Anti-aliasing	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Easy to drive	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Technology [nm]	28	16	65	28 (simulation)	16	65	28	16	40	28
FOM_S [dB]	160	153	165	-	160	166	179	168	158	160
Delay	LC + RC	RC	RC	LC	RC	RC	RC	-	RC	-
Inter-stage amp	1st-order ~8×	2nd-order 7×	2nd-order 4×	2nd-order 6×	2nd-order 8×	2nd-order 4×	1st-order 7.5×	-	-	-
DRF	Off chip	On chip background cal.	Off chip	Off chip	Off chip	Off chip	Off chip	Not needed	Off chip	On-chip
Other remarks	1st CTP w/ delay + low-pass inter-stage amp	CTP with on-chip DRF	Butterworth STF, decimation	Near Nyquist OSR	1st interleaved CTP	1st interleaved CTP	High FOM_S			No input buffer

* App BW assumes OSR ≧ 3 for anti-aliasing purpose

less. This enables wide BW operation, along with the CT benefits, such as anti-aliasing and the easy-to-drive input structure due to its resistive input.

Another example of a CT pipelined ADC [16] demonstrates its high efficiency with an excellent 179-dB FOM_S. As discussed in Section II-A, the ADC consists of analog and digital filters connected by quantizers and DACs. In design scenarios where the digital signal processing power consumption can be significantly lower than its analog counterpart (e.g., at low f_S and/or low NSD with advanced CMOS technology), the efficiency of the ADC is largely dictated by the analog filter section. The efficiency of the analog filter section can be optimized by maximizing the front-end gain, which minimizes the input-related thermal noise of the filter back-end circuits. CT pipelined ADCs incorporate a residue cancellation stage at the front end, providing high and wideband gain that effectively suppresses back-end noise. This is an essential advantage of CT pipelined ADC and 0-x MASH in terms of ADC power efficiency, which is not found in traditional single-loop CT $\Delta\Sigma$ ADCs.

The conventional single-loop CT $\Delta\Sigma$ ADC [29] provides a decent 168-dB FOM_S at 160-MHz BW, but with the OSR limited to 9. Considering that the CT pipelined ADC requires additional complexity, such as DRF and its background coefficient estimation, it may be prudent to choose a simpler CT $\Delta\Sigma$ ADC if the BW can be achieved by the f_S, which is limited by the process technology.

Compared to a CT MASH $\Delta\Sigma$ ADC such as [8], CT pipelined ADCs provide about 2× BW for the same f_S, as suggested by the 2× OSR difference as shown in Table 1. On the other hand, MASH ADCs can be designed with a small number of stages due to their cascaded integrator structure from the ADC input to the last quantizer compared to the cascaded lossy integrators in CT pipelined ADCs. Thus, CT MASH can be a hardware efficient solution compared to a CT pipelined ADC if the required BW can be satisfied by its OSR.

Furthermore, consider a comparison with the state-of-the-art DT interleaved and pipelined ADC [30], which achieves similar application BW and NSD compared to the CT pipelined ADCs [17] and [20]. The DT ADC [30] achieves a wider BW with a 7 dB or 2 dB better FOM_S than [17] and [21], respectively. However, in fully integrated zero-IF or low-IF wireless receiver applications, where an on-chip active-RC filter is integrated on the same chip to serve as an anti-AAF, the usable BW is reduced to a fraction of $f_S/2$. This limitation, denoted as App BW in Table 1, is imposed to maintain a certain level of anti-aliasing performance with the on-chip filter. Consequently, [17], [20], and [30] yield approximately the same application BW. When an on-chip active-RC filter and an ADC driving buffer are added to the DT signal chain, the FOM_S advantage of [30] is either neutralized or surpassed, as discussed in Section II-C. Therefore, a signal chain using CT pipelined ADCs could potentially match [17] or even outperform [20] the DT solutions. This argument can be supported by assuming that a CT pipelined ADC is essentially an active RC filter followed by an ADC, but with a high active-RC filter gain due to its front-end signal cancellation [21].

As with most comparisons, a different conclusion could be reached if a different application space is assumed. For example, when a direct RF sampling receiver application is considered, the BW provided by a CT pipeline ADC, even with the latest process technology, may not be sufficient, making it unsuitable as a solution. In these applications, an off-chip passive filter, such as a SAW filter, is often used

as an anti-AAF. In such cases, the above argument loses its validity, and a DT ADC becomes the solution.

VI. CONCLUSION

This review article presented the CT pipelined ADC, which has been developed as an ADC architecture for wideband digitization while retaining the CT benefits. The CT pipelined ADC architecture addresses the BW limitations of CT $\Delta\Sigma$ ADCs while maintaining the wideband operation inherited from DT pipelined ADCs. The article covered the principles of the CT pipelined ADC, ADC building blocks, and example implementations to provide an overview of this ADC architecture.

Although several implementations of this architecture have been presented, the CT pipelined ADC is still in its infancy and offers numerous research opportunities for further improvements and enhancements at the circuit, system, and signal processing levels. The author hopes that this article, along with the references provided, will serve as a comprehensive guide to this exciting area of research.

APPENDIX A
DERIVATION OF (1)

The configuration of the analog gain block within an ADC, along with its corresponding inputs and outputs, including DACs and quantizers, is shown in Fig. 27. Since the analog gain block is a linear block, the relationship between the inputs and the output can be formulated as a linear summation, which can be expressed as

$$Y_0 = G\ U - G_1 X_1 - G_2 X_2 - \cdots \tag{4}$$

where X_1, X_2, ... are digital signals driving the DACs, Y_0 is the analog output signal of the analog gain block, and G, G_1, G_2, ... are the transfer functions from U, X_1, X_2, ... terminals to Y_0, respectively. The quantizer is modeled as a linear block with an additional quantization noise Q_N as

$$V_0 = Y_0 + Q_N \tag{5}$$

where V_0 is the output signal from the quantizer. Based on (4) and (5), the analog input signal U can be represented as

$$U = -\frac{Q_N}{G} + \frac{1}{G}\begin{pmatrix}1 & G_1 & G_2 & \cdots\end{pmatrix}\begin{pmatrix}V_0\\ X_1\\ X_2\\ \vdots\end{pmatrix}.$$

The second term in this equation is the dot product of two vectors; one vector contains the filter responses and the other vector contains digital signals provided to or from a digital filter. If a digital representation of the filter vector is available (see Section IV-D), the second term can be computed using a digital filter. When the digital filter output is represented as V, then (6) becomes to

$$U = -\frac{Q_N}{G} + V \tag{6}$$

and thus (1) is derived.

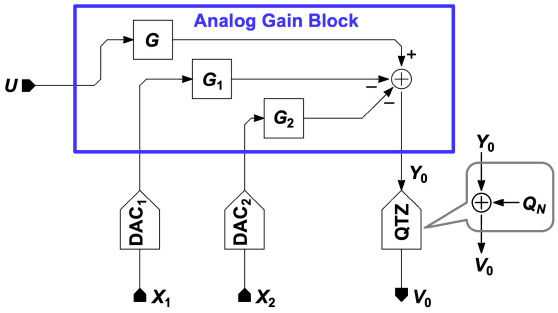


FIGURE 27. Inputs and the output of the analog gain block with the driving DACs and the quantizer.

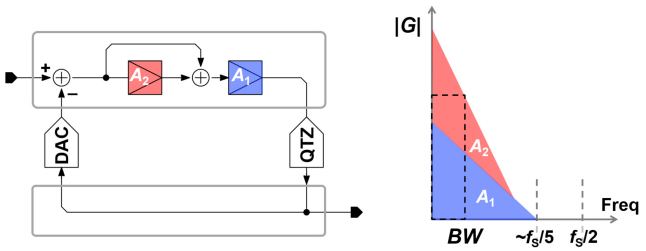


FIGURE 28. $\Delta\Sigma$ ADC based on the gain-centric ADC model and its frequency response of the analog gain block.

APPENDIX B
APPLICATIONS OF GAIN-CENTRIC ADC MODEL

A feedforward CT $\Delta\Sigma$ ADC can be adequately discussed based on the gain-centric ADC model as shown in Fig. 28. As discussed in Section II-A, the quantization noise of the last quantizer Q_N is reduced by the gain G, which is provided by the cascaded integrators A_1 and A_2. To prevent the analog gain block and the quantizer from saturating, the DAC, which is driven by the last quantizer, cancels the input signal (at low frequencies). The DAC and the quantizer form digital feedback, and this feedback loop must be stable. To keep the feedback stable, the gain G is designed to be reduced below 0 dB well below $f_S/2$. Thus, the bandwidth BW where G is sufficiently high is limited to a small fraction of $f_S/2$, or BW $= f_S/(2\ \text{OSR})$.

A DT pipelined ADC can also be discussed based on the gain-centric model with some additional quantizers and DACs, as shown in Fig. 29. As in the CT $\Delta\Sigma$ ADC example, the quantization noise of the last quantizer Q_{N3} is suppressed by the gain from the ADC input to the last quantizer QTZ_3: $G = A_1\ A_2$. The analog gain section is kept from saturating by a feedforward cancellation followed by a fixed (limited) gain. For example, if the canceled signal remains up to 1/4 of the full scale, the gain is limited to 4×. Note that the analog filter is now in DT. Therefore, linearity only needs to be maintained at the end of each DT operation. Also, the digital filter is now a multi-input–single-output filter due to the additional quantizers (QTZ_1 and QTZ_2). The intermediate quantizers QTZ_1 and QTZ_2 also introduce quantization noise. In pipelined ADCs, however, these quantization noises are fully canceled by a digital filter if the digital filter is appropriately designed.

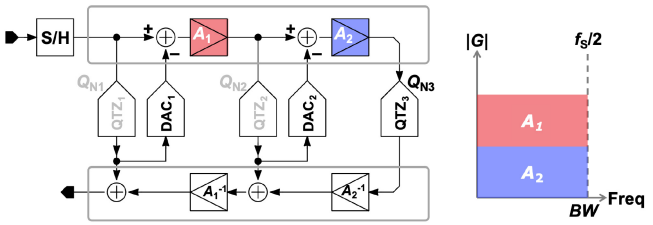


FIGURE 29. DT pipelined ADC based on the gain-centric ADC model and its frequency response of the analog gain block.

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HAJIME SHIBATA (Senior Member, IEEE) received the B.E. and M.E. degrees in electrical engineering from the University of Electro-Communications, Tokyo, Japan, in 1997 and 1999, respectively, and the Dr.Eng. degree from the Tokyo Institute of Technology, Tokyo, in 2002.

He joined Analog Devices, Toronto, ON, Canada, in 2002, where he has been an Analog Devices Fellow since 2021. His interests include continuous-time ΔΣ and continuous-time pipelined analog-to-digital converter design.

Dr. Shibata was a co-recipient of the Beatrice Winner Award at ISSCC 2006. He is currently a member of the Technical Program Committee of the International Solid-State Circuits Conference and has served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS from 2017 to 2019.