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Design Techniques for Energy-Efficient Analog-to-Digital Converters

MOONHYUNG JANG [1] (Member, IEEE), XIYUAN TANG [2,3] (Member, IEEE), YONG LIM [4] (Member, IEEE), JOHN G. KAUFFMAN [5] (Member, IEEE), NAN SUN [6] (Senior Member, IEEE), MAURITS ORTMANNS [5] (Senior Member, IEEE), AND YOUNGCHEOL CHAE [7] (Senior Member, IEEE)

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[1]Department of Electrical Engineering, Stanford University, Stanford, CA 94306, USA
[2]Institute for Artificial Intelligence, Peking University, Beijing 100871, China
[3]School of Integrated Circuits, Peking University, Beijing 100871, China
[4]System LSI Division, Samsung Electronics, Hwaseong 18448, South Korea
[5]Institute of Microelectronics, University of Ulm, 89081 Ulm, Germany
[6]Department of Electronic Engineering, Tsinghua University, Beijing 100084, China
[7]Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea

CORRESPONDING AUTHOR: Y. CHAE (e-mail: ychae@yonsei.ac.kr)

ABSTRACT The energy efficiency of analog-to-digital converters (ADCs) has improved steadily over the past 40 years, with the best reported ADC efficiency improving by nearly six orders of magnitude over the same period. The best figure-of-merit (FoM) is achieved with a limited class of ADC in terms of resolution and speed, but the coverage of the best FoM ADC has been expended. Many ADCs with the record FoM open up new applications and often incorporate multiple combinations of architectural and circuit innovations. It would be very interesting to follow a path of relentless optimization that could be useful to further expand the operating bandwidth of energy-efficient ADCs. To help along this path, this review article discusses the design techniques that focus on optimizing energy efficiency, involving successive approximation, pipelining, noise-shaping, and continuous-time operation.

INDEX TERMS Analog-to-digital converter (ADC), continuous-time (CT), delta-sigma modulation, energy efficient, low power, noise-shaping (NS), pipelining, successive approximation.

I. INTRODUCTION

THERE have been remarkable innovations in analog-to-digital converter (ADC) design, and all performance metrics in ADCs have also been improved [1], [4], [5], [6]. Over time, the performance comparison between ADCs has been made with the energy efficiency, with ADCs with high energy efficiency becoming the most important [5], [6]. The race for higher energy efficiency has led to constant innovations in technologies, architectures, and circuits [6], taking ADCs to levels of energy efficiency that people in the past could not have imagined. As a result, the best reported ADC efficiency has improved nearly by six orders of magnitude over the past 40 years.

In addition, achieving best-in-class energy efficiency is extremely important, as it defines the frontier of what is possible and also opens up new applications. After a closer look at the reported data, one can notice that the best figure-of-merit (FoM) is only achieved with a limited class of ADCs in terms of resolution and speed. However, the coverage of the best FoM ADCs has been expended steadily to higher bandwidth. Given this trend, it would be interesting to take a look at recent examples of energy-efficient ADCs: how their architectures and circuits are smartly arranged and achieve such high energy efficiency, because they can be very useful for further improvements.

In this review article, the focus is on architectures and circuit techniques to achieve high power efficiency. In this context, the generic ADCs' basic functionality is omitted, and many recent examples are described instead. In Section II, the ADC FoM and the trend toward energy efficiency are discussed to properly assess the design techniques. Considering the ADC trends over the last decade, the techniques for SAR ADCs are first discussed in Section III, since SAR ADCs have become ubiquitous in scaled CMOS due

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to their superior efficiency. Next, the design techniques to improve the resolution, pipelining, and noise-shaping (NS) are covered in Section IV. Furthermore, Section V discusses continuous-time (CT) ADCs, which are gaining popularity as a successful alternative with many hybridizations. A brief conclusion is drawn in Section VI.

II. ADC FIGURE OF MERIT

Over the last four decades, thousands of ADCs have been published, sometimes with different motivations—researchers, readers, designers, and reviewers, needed a way to compare their performances. ADCs are probably among the most specified building blocks for integrated circuits, and no research paper today misses to state at least one FoM. The two most commonly used FoMs are the Walden FoM_W, proposed in 1994 [1], and the Schreier FoM_S, described by Schreier in his textbook published in 2005 [2] but proposed as early as 1997 in [3]. The nowadays used expression for those FOMs are

$$\text{FOM}_W = \frac{P}{2^{\text{ENOB}} \cdot f_N} \tag{1}$$

$$\text{FOM}_S = \text{DR}_{\text{dB}} + 10 \cdot \log\left(\frac{\text{BW}}{P}\right) \tag{2}$$

where P is the power consumption, ENOB is the effective number of bits, f_N is the effective Nyquist frequency, BW is the useful signal bandwidth, and DR is the dynamic range of the ADC. FoM_S in (2) is essentially the same definition as that in [3] that $a \times 2$ in power, bandwidth, and DR are equally weighted. In contrast, FoM_W in (1), which is the inverse of the original definition in [1], weights resolution less, i.e. $a \times 4$ in power and bandwidth are treated equally to $a \times 2$ in resolution. Thus, FoM_W generally favors low-resolution designs, whereas thermal noise-limited designs exclusively use FoM_S. Also, DR in (2) has been replaced by the signal-noise-(distortion) ratio and, thus, effectively again by ENOB, in order to take into account the increase in noise-floor and distortion for full-scale input signals.

Many other FoMs have been proposed over the past two decades, including supply voltages, technology, area consumption, and more [4], [5]. Although the underlying idea is valid that more parameters justify a good design, only Walden- and Schreier-FoM are used today. As trend lines indicate the majority of ADCs are now limited by thermal noise, FoM_S, which equally values bandwidth, resolution, and power consumption, is the surviving FoM metric in the most recent publications.

Today, Murmann's ADC performance survey [6] covers all ISSCC and VLSI publications on ADCs since 1997 and is referred to in almost all publications on ADCs. Even larger databases have been gathered in [5], where an overview of ADC surveys can also be found. It has turned out over the years that while individual, excellent, and even performance-leading designs are missing when referring only to [6], the general trend lines are well captured. It is though important to keep emphasizing that a single number like the FoM does not tell the whole story of an ADC; FoM comparisons should be made between ADCs in the same performance range and ideally between ADCs intended for similar applications. Furthermore, power consumed for calibration engines, decimation filters, and input/reference buffers, which are often neglected in reporting FoMs, have to be considered. Fortunately, the recent state-of-the-art (SOTA) shows an increasing focus on ADCs with easier drivability, implicit filtering, better and calibration-free linearity, etc., rather than just on the next record FoM.

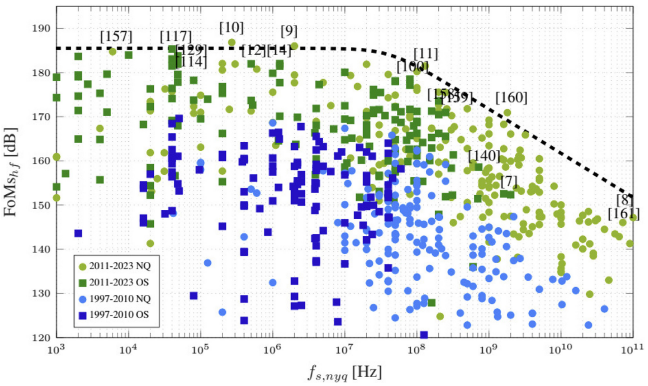

FIGURE 1. FoM_S versus f_{snyq} of published ADCs based on [6].

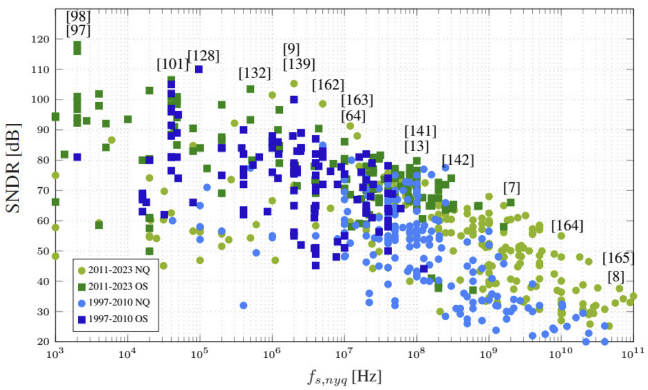

FIGURE 2. SNDR versus f_{snyq} of published ADCs based on [6].

Two charts are shown in Figs. 1 and 2. First, the reported FoM_S and second, the reported SNDR, both over the achieved Nyquist frequency. In both plots, older designs are separated from newer publications, and we separate Nyquist (NQ) ADC from oversampling and NS (OS) ADC [6]. This is done to show the current front of the SOTA. Moreover, in the next sections, it allows for highlighting a few architectures and designs defining this front. The charts also show that it is very rare for a single ADC to outperform in more than one performance plot and only [7], [8], and [9] achieve this.

Both charts show data points split into an early and a late time period and separate Nyquist-rate and oversampling (or NS) ADCs. This allows us to see the tremendous performance evolution over the last decade, which is partially due to technology, but evenly important due to innovations

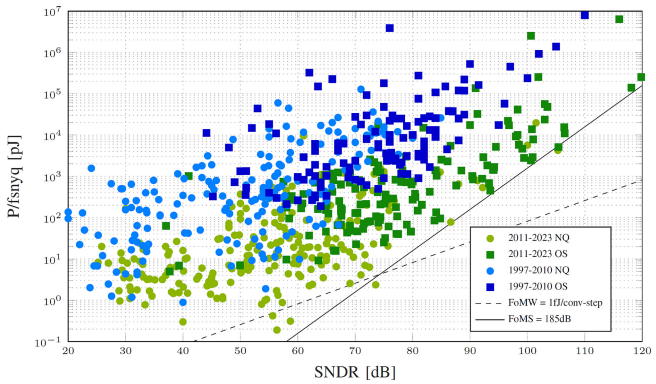

FIGURE 3. P/f_{snyq} vs. SNDR of published ADCs based on [6].

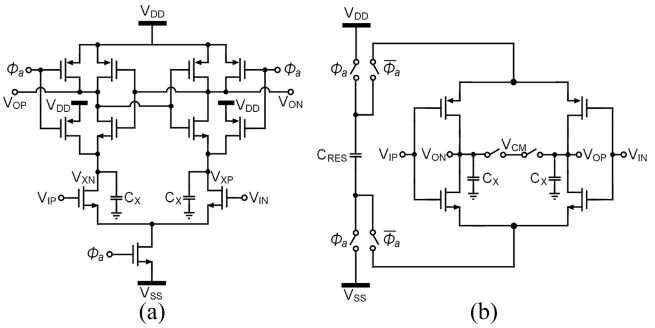

FIGURE 4. Schematic of (a) SA latch and (b) FIA [27].

on circuit and architectural levels. Moreover, when we look at the evolution of ADC efficiency over reported SNDR, we can see that even though Nyquist ADC has usually been outperformed by NS ADCs, recent contributions impressively show the opposite [9], [10], [11] (see Fig. 3).

The SAR ADC has become an essential part of energy-efficient ADCs and is one of the most energy-efficient ADCs to the fastest ADCs. The use of NS in SAR ADCs blurs the distinction between delta–sigma ($\Delta\Sigma$) ADCs [12], and $\Delta\Sigma$ ADCs also include the SAR ADC as a quantizer in SOTA works [13]. Therefore, hybrid ADCs are gaining popularity [14] and becoming a successful alternative to classical architecture.

III. DESIGN TECHNIQUES FOR SAR ADC

In the last decade, the SAR ADC has dominated the development of energy-efficient ADCs for low-to-medium resolution applications, leveraging both technology scaling and circuit techniques [15]. A SAR ADC consists of three main blocks: 1) the comparator; 2) the SAR logic; and 3) the DAC. While the power consumption of the SAR logic benefits directly from technology scaling, reducing the comparator and DAC power consumption relies on various innovative techniques. In this section, emerging techniques for energy-efficient SAR ADCs are reviewed, with a focus on comparator and DAC design.

A. LOW-POWER COMPARATORS

As the critical circuit block that converts the difference between the input signal and the analog DAC voltage into a digital output, the comparator directly determines the SAR ADC performance. A comparator usually consists of a preamplifier that amplifies the input signal, followed by a latch to resolve the final decision. The strong-arm (SA) latch is one of the most popular designs [16], [17], [18], as shown in Fig. 4(a). When ϕ_a is low, the comparator is turned off with the integration nodes V_{XP}/V_{XN} and output nodes V_{OP}/V_{ON} reset to V_{DD}. When amplification starts, the integration nodes are discharged at different rates depending on the input voltages. Eventually, the latch operates and makes its decision. Over the past few decades, various techniques have been investigated to outperform the SA latch. Schinkel et al. [19] introduced a two-stage dynamic comparator that separates the latch stage from the preamplifier, thus accelerating comparison speed. However, the latch's input starts from in the triode region, equivalently reducing the pregain and degrading the overall accuracy. To address this, Miyahara and Matsuzawa [20] and van Elzakker et al. [21] modified this by ensuring the latch's input transistor starts in the saturation region, reducing the comparator offset and noise. Hsieh and Hsieh [22] proposed cascaded input pairs for higher preamplifier gain through vertical stacking of input transistors, resulting in an improvement of energy efficiency.

Another observation is that the load capacitor C_X of the preamplifier (preamp) discharges completely during the comparison, thus consuming a fixed amount of energy: $2C_X V_{DD}{}^2$. A large C_X is usually required to suppress the noise, and so this energy consumption often dominates in a low-noise comparator design. Hence, there is a strong need to improve the preamp's energy efficiency. Liu et al. [23] presented a bidirectional dynamic comparator to save the preamp's reset power. The preamp consists of nMOS and pMOS input pairs. During the first half of the amplification, the pMOS input turns on, and the preamp outputs are charged up from the ground. Once the preamp outputs exceed $V_{DD}/2$, the pMOS side turns off and the nMOS pair continues the second half of amplification, restoring the preamp outputs to their initial state at the end of the amplification. This avoids reset power, while still achieving the same gain and noise performance as the conventional design.

Although only the initial portion contributes to the noise performance, the preamp's load capacitors are fully discharged [24], [25]. Bindra et al. [26] proposed a dynamically biased preamp to address this issue by incorporating a degeneration capacitor at the source of the input pair. This dynamically turns off the gate-source voltage V_{GS} of the input pair and prevents the load from being fully discharged. In addition, the reduced V_{GS} boosts the g_m/I_D, which increases its gain, resulting in an improvement of energy efficiency. Tang et al. [27] further improved energy efficiency by introducing the floating inverter amplifier (FIA). As shown in Fig. 4(b), a CMOS inverter is adopted as a

preamp, but its power supply is connected to a floating reservoir capacitor that ensures a constant common-mode output voltage. It elongates the amplification time and increases the gain. It avoids the common-mode discharge of the loading capacitor, resulting in significant energy savings. In addition, the reservoir capacitor makes the gain insensitive to input common-mode voltage and PVT variations and boosts the preamp's g_m/I_D similar to [26]. Therefore, a dynamic comparator with an FIA preamp showed a 7× improvement in energy efficiency compared to the SA latch.

B. SYSTEM-LEVEL COMPARATOR POWER REDUCTION TECHNIQUES

In addition to optimizing the standalone comparator, many architecture-level solutions have been explored to reduce the comparator power consumption. Note that only one of the comparisons during SAR conversion has a differential input that is less than half LSB. In theory, it must be ensured that the comparator's noise is minimal during this critical comparison. Given this, Harpe et al. [28] proposed a judgment circuit to identify the critical comparison cycle by detecting the comparison time. Once identified, it repeats the comparison multiple times and adopts the majority result, effectively reducing the comparator noise. Accordingly, a comparator can be reconfigured into a low-noise mode for critical decisions.

Another approach is to provide redundancy in SAR conversion that can tolerate errors in earlier bits. Based on that, Giannini et al. [29] proposed a two-comparator scheme, where the low-power comparator in the early bits and the low-noise comparator for the last few bits after the redundancy. Harpe et al. [30] further simplified the comparator design by proposing a load-switching comparator that dynamically changes the comparator's loading capacitor, thus changing its noise performance, without incurring an offset mismatch as in the two-comparator approach. In addition, statistical estimations were explored to improve the energy efficiency of the comparator. By utilizing the maximum-likelihood estimator (MLE) [31] or Bayes estimator (BE) [32], the residue voltage of the comparator input can be estimated, which is used to reduce the noise of SAR ADCs effectively.

C. CDAC DESIGNS AND CDAC SWITCHING TECHNIQUES

DAC switching is one of the power contributors in SAR ADCs that often limits energy efficiency. To reduce switching energy, the capacitive DAC (CDAC) is commonly used and should be sized to match the thermal noise limit to achieve the best power and area efficiency. However, this is usually impeded by the minimum capacitor size offered by the foundries. The use of custom metal–oxide–metal (MOM) capacitors is becoming increasingly popular. For instance, Harpe et al. [33] reported a CDAC array with a 0.5-fF unit capacitor, and Huang et al. [34] enclosed the top plate of the CDAC with the bottom plate, reducing the parasitic effects associated with the top plate. A unit-length capacitor consists of two strips, the capacitor value of which is defined by the difference in the strip length, giving a unit capacitor of 125 aF [35].

TABLE 1. Average Switching Energy of a 10-Bit SAR ADC [15].

Architecture	Conversion energy (CV^2)*	Reset energy (CV^2)*	Normalized total energy	No. of unit cap**
Conventional	682.65	0	1	2^{N+1}
Monotonic	255.5	0	0.37	2^{N}
Bi-directional	42.7	191.5	0.34	2^{N-1}
V_{cm}-based	170.2	0	0.25	2^{N}
Split-cap	170.2	255.5	0.63	2^{N+1}

* Normalized to the same V_{FS} and C_{dac}
** Calculated for a N-bit differential SAR DAC

Besides the capacitor size reduction, various switching techniques for the CDAC array have been investigated. The conventional switching technique is a trial-and-error approach [36]. About 50% of switching energy goes into the reset operation, which is quite power consuming. To overcome these limitations, CDAC switching techniques have been explored. Liu et al. [37] proposed the monotonic switching technique. By employing top plate sampling and resetting the DAC's bottom plates to V_{refp}, the reset power and the MSB switching power are eliminated. However, changing the top-plate common-mode voltage can degrade the ADC linearity due to the varying comparator offset [38]. Sanyal and Sun [39] presented the bidirectional switching technique. The MSB capacitors are reset to the opposite reference, reducing the common-mode variation. Zhu et al. [40] reported the V_{cm}-based switching technique. The DAC's bottom plates are connected to V_{cm}, eliminating the reset power and keeping the common-mode voltage constant. To eliminate the use of additional V_{cm}, Ginsburg and Chandrakasan [41] split each capacitor into two equal subcapacitors that are reset to V_{refp} and V_{refn}, respectively. This is equivalent to the V_{cm}-based switching, but it brings reset power. Tai et al. [42] introduced a more systematic approach called a detect-and-skip (DAS) technique, where a small coarse DAC resolves the first few MSB bits, while the large fine DAC resolves the remaining LSBs. The MSB results are applied directly to the fine DAC, avoiding unnecessary switching. The DAS technique is widely used, especially for designs requiring large DAC arrays. Table 1 compares the average conversion energy, reset energy, and the total number of required unit capacitor elements. The designers should also notice that with the unit capacitor size reduction, capacitor mismatches may become the limitation of the ADC linearity. Powerful techniques have been proposed to address this concern, including calibration [43] and mismatch error shaping [44].

D. KT/C CANCELATION TECHNIQUE

The sampling kT/C noise represents a fundamental SNR limit for discrete-time (DT) ADCs and the SAR ADC is no exception. The limitation of the DAC switching energy still comes from the DAC size, which is determined by

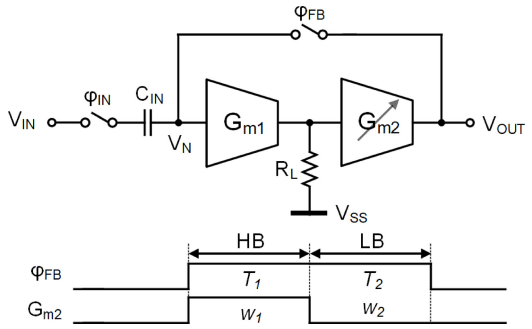

FIGURE 5. Active sampling circuit with a 2-stage amplifier [46].

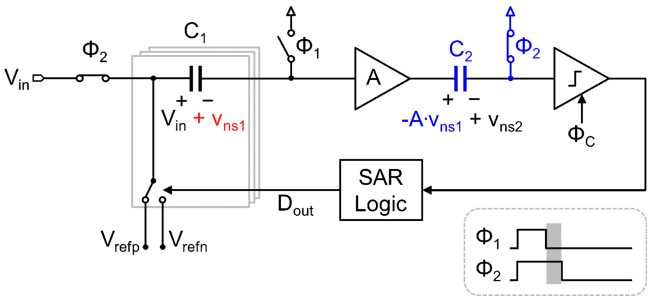

FIGURE 6. SAR ADC with kT/C noise cancelation [47].

the kT/C noise limit. Hence, it is highly desirable to figure out ways to reduce the capacitor size without incurring a kT/C noise penalty. Kapusta et al. [45] proposed a sampling circuit with a kT/C noise cancelation. Inspired by [45], Li et al. [46] explored an active sampler, which decouples the noise PSD and BW. This is achieved by using an active sampling circuit with a specially designed two-stage amplifier, as shown in Fig. 5. The input-referred noise PSD is inversely proportional to the first stage g_{m1}. By placing the dominant pole at the second-stage output, the noise BW is proportional to $g_{m1}r_{o1}g_{m2}$, where r_{o1} is the first-stage output impedance. It successfully decouples the noise PSD and BW and, thus, the total integrated noise is presented in the form of $r_{o1}g_{m2}\times$kT/C. By introducing a switchable g_{m2} stage, this work provides high bandwidth initially for signal sampling and low bandwidth toward the end for noise reduction.

A more popular design is proposed in [47], as shown in Fig. 6, which is also inspired by [45]. In a classic SAR ADC, a capacitor C_2 and a switch ϕ_2 are added to form an additional sampling stage at the preamp output. When the ϕ_1 phase is complete, the sampling kT/C_1 noise across C_1 is represented as an offset at the preamp input. During the ϕ_2 phase, it is amplified and stored via the C_2. Since the C_2 operates as an offset cancelation capacitor, the kT/C_1 noise at the comparator input is canceled. The sampling noise on C_2 can be attenuated by the preamp gain. Hence, both C_1 and C_2 can be small without introducing excessive noise penalty. Although an additional preamp is required, it is worth considering the substantial power and area savings for the ADC input driver and reference buffer. Although the kT/C cancelation technique is relatively new, it has been

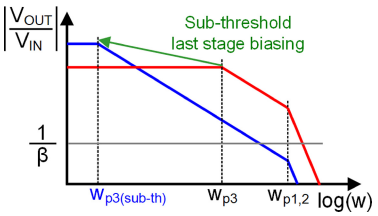

FIGURE 7. Frequency response of a ring amplifier.

quickly adopted by the community and is widely used in emerging energy-efficient ADC designs [48], [49], [50], [51].

IV. DESIGN TECHNIQUES FOR PIPELINING AND NOISE-SHAPING

Pipelining and NS are effective ways to improve the resolution of ADCs. Especially in combination with SAR ADCs, the high energy efficiency can be maintained even for medium-to-high resolution applications. Such an ADC requires two additional blocks: 1) the residue amplifier for pipelining operation and/or 2) the loop filters for NS operation. This section surveys emerging techniques for implementing residue amplifiers and loop filters.

A. LOW-POWER RESIDUE AMPLIFIERS

A pipelined SAR ADC typically consists of two low-resolution SAR ADCs coupled with a residue amplifier. However, the use of a conventional OTA-based amplifier consumes a significant amount of power and, thus, the design of an energy-efficient residue amplifier is essential to improving energy efficiency.

1) RING AMPLIFIER

Hershberg et al. [52] proposed a ring amplifier, which is essentially a three-stage inverter-based amplifier, but the differentiated stabilization strategy makes the ring amplifier more efficient than conventional multistage OTAs. The multistage OTAs typically use frequency compensation to form the dominant pole at the first-stage output and push the other poles of subsequent stages to sufficiently higher frequencies, requiring a significant power consumption, thus leading to their efficiency reduction. A ring amplifier employs an opposite stabilization strategy for higher energy efficiency. In the steady state, a ring amplifier forms the dominant pole at the last stage output ($w_{p3(subth)}$ in Fig. 7) by operating the last stage in the subthreshold region, while maximizing the bandwidth of internal amplifier nodes ($w_{p1,2}$ in Fig. 7). This subthreshold operation minimizes the static current and also provides the benefit of relatively higher stage gain and near rail-to-rail output swing. It also provides a reasonably constant open-loop gain. On the other hand, during its slewing, the ring amplifier fully drives to achieve maximum drive strength from the last stage. This dynamic operation provides the core benefit of the ring amplifier: slew-based charging. Even with small last-stage transistors, the ring amplifier can still produce a high slew rate, which

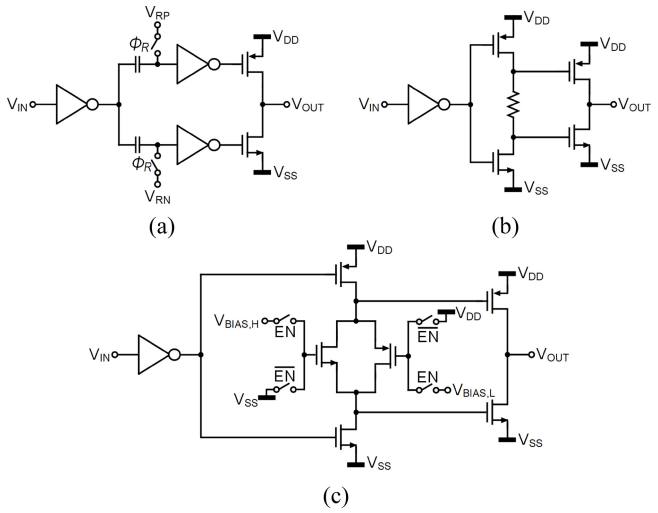

FIGURE 8. Ring amplifiers in the literature. (a) First [52], (b) Self-biased [55], and (c) CMOS switch biased [55], [58].

means that the second stage can be loaded minimally and, thus, a nondominant pole is easily formed. Furthermore, the multistage configuration enables high gain. To achieve the dynamic biasing of the last stage, the first ring amplifier [52] splits the second stage into two paths and applies an offset voltage to the second-stage inputs using floating capacitors, as shown in Fig. 8(a). However, the offset voltage is sensitive to PVT variations and, thus, requires additional trimming or digital calibration [53]. This offset voltage is later moved to the third-stage inputs without splitting the second stage [54] to control the last-stage bias more precisely.

Lim and Flynn [55] eliminated the need for an external bias by using a resistor placed between the drains of the second inverter, as shown in Fig. 8(b). The resistor dynamically generates the last-stage biases by using the short circuit current of the second stage. The self-biasing technique is further employed in the fully differential version [56], which consists of a current-reused differential pair for the first stage. This demonstrates robustness to variations in supply voltage and temperature. The self-biasing technique is also applied to the first stage with a reverse offset to improve the bandwidth and slew rate of the second stage [57], [59]. However, it relies on absolute resistance, which can lead to instability due to small offset, or slow settling and reduced gain due to excessive offset. To address this issue, a tunable resistor based on a CMOS switch [55], [58] was used, as shown in Fig. 8(c). However, extra care is required to achieve PVT robustness, such as monitoring the ring amplifier behavior using an on-chip stochastic ADC [60], [61], or background digital calibration [62]. To achieve robust PVT biasing, instead of a self-biasing resistor, a floating current source is used like a class-AB biasing circuit [49], [63]. The second-stage inputs are individually biased with the current mirrors during the sampling phase, and the bias voltages are stored on capacitors.

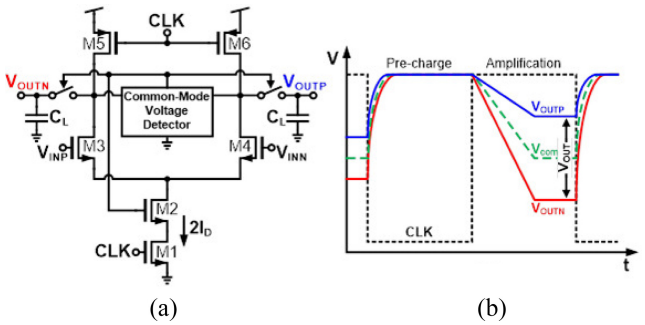

FIGURE 9. (a) Dynamic amplifier with common-mode voltage detector [65] and (b) operation waveform.

For high-resolution ADCs, a composite ring amplifier [54] has been introduced, consisting of a coarse ring amplifier with fast slew but low gain, and a fine ring amplifier with high gain but slow slew. The coarse ring amplifier automatically turns off after slewing, and then the fine ring amplifier takes over high gain amplification. It achieved 75.9-dB SNDR at 20 MS/s and consumed 2.96 mW, resulting in 171.2-dB FoM$_S$. A similar strategy is applied in [64], utilizing two parallel output stages. The ADC achieved 91-dB SNDR at 15 MS/s and consumed 9.8 mW, resulting in 179.8-dB FoM$_S$. For high-speed operation [58], [59], [60], [61], [62], [63], the gain of the ring amplifier is compromised to achieve a high slew rate and wide bandwidth, but this is also aided by the gain calibration. A single-channel ADC using ring amplifiers [58] achieved 58.1-dB SNDR with first-order gain calibration at 600 MS/s and consumed 14.5 mW, resulting in 161.9-dB FoM$_S$. The linearity of the fast ring amplifier is further improved in [59], and the ADC achieves 57.1-dB SNDR at 1 GS/s while consuming 24.8 mW.

2) DYNAMIC AMPLIFIER

Most dynamic amplifiers [65], [66], [67], [68], [69], [70], [71], [72], [73] are basically G_m-C integrators that stop integration when the integrated output reaches a desired gain. This can be used as an energy-efficient open-loop residue amplifier. One of the early approaches to control the integration time is the technique of detecting the common-mode voltage at the output [65], as shown in Fig. 9(a). The dynamic amplifier operation is described in Fig. 9(b). When a clock is low, the output load capacitors C_L are precharged to the supply voltage. As the clock goes high, the tail current source (M_1) turns on, and as a result, the outputs start discharging and integrating the differential output current of $G_m \times V_{\mathrm{IN}}$ on the load capacitors, where G_m is the transconductance of the input transistors (M_3 and M_4). The integration continues until the output common-mode voltage reaches the desired common-mode voltage (V_{COM}). The common-mode voltage detector then stops the tail current, thereby finishing the integration. The gain of the dynamic amplifier is expressed as $G_m \times T_{\mathrm{int}}/C_L$, where T_{int} is the integration time. The dynamic amplifier also filters out the input noise with the integrator noise bandwidth

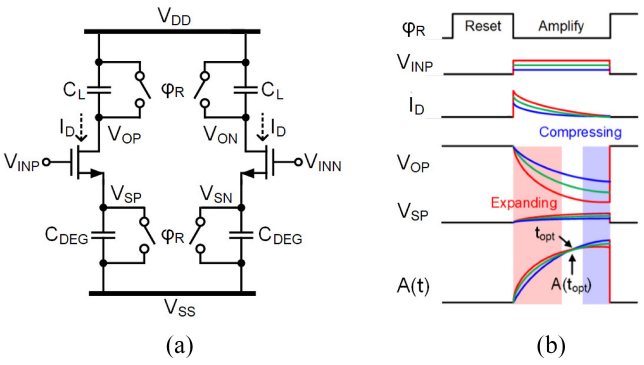

FIGURE 10. (a) Schematic of the capacitively degenerated dynamic amplifier [74] and (b) its timing diagram.

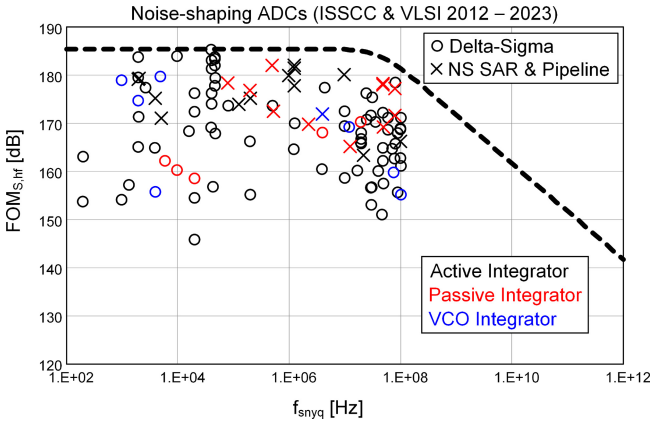

FIGURE 11. Schreier's FoMs versus speed of NS ADCs from 2012 to present according to loop filter implementation based on [6].

of $1/2T_{\text{int}}$. However, the gain of this dynamic amplifier is relatively small ($\leq$10) due to the limited output common-mode voltage swing range. Furthermore, the open-loop gain is sensitive to PVT variations and, thus, requires continuous background analog or digital calibration for the residue amplification [66], [67], [68], [69], [70].

There are several approaches to improve the gain of dynamic amplifiers, suitable for residue amplifiers. The cascode integrator [68] increases gain by extending the effective output common-mode voltage swing through two-step integration. The cascode device automatically switches the integration current between two integration capacitors as soon as the first integration turns on the cascode device. The resulting dynamic amplifier gain is about 16×, which is applied in an 80-MS/s pipelined SAR ADC, achieving 68-dB SNDR and 172.3-dB FoM$_S$ with background digital gain calibration. Another approach is to add fixed bypass currents [71], which reduce the common-mode charging current of the C_L, thus increasing the integration time and gain. The resulting gain is 13.3×, which is applied in a 132-MS/s 5-MHz bandwidth NS SAR ADC, yielding 79.74-dB SNDR and 180.1-dB FoM$_S$.

A PVT-stabilized dynamic amplifier has been actively investigated. Huang et al. [72] eliminated the need for background gain calibration and achieved impressive PVT robustness; low gain variation of 1.5% and 1.2% at a supply voltage ranging from 1.25 to 1.35 V and a temperature ranging from –5 °C to 85 °C, respectively. The T_{int} of the dynamic amplifier is determined to be proportional to C_L/G_m using the slew rate of a replica amplifier. The technique is applied in a 330-MS/s pipelined SAR ADC, which achieves a 67.7-dB SNDR and 171.9-dB FoM$_S$ with only foreground analog gain calibration.

Akter et al. [74] introduced a capacitively degenerated dynamic amplifier (Fig. 10) which is a completely different approach. The weak inversion input pair provides an exponential V–I relation, and a charge transfer-based amplification occurs with a degeneration and load capacitors (C_{DEG} and C_L). After capacitors are reset, C_{DEG} is charged with I_D and V_S is started to increase (gain ($A(t)$) expanding). As C_{DEG} is charged, it becomes strongly degenerating the input pair, and $A(t)$ exhibits compression. The crossing point between expanding and compressing (t_{opt}) ensures linear signal-independent gain $A(t_{\text{opt}})$ of $C_{\text{DEG}}/(2nC_L)$ (n = weak inversion slope-factor). Kim et al. [75] investigated a weak inversion slope-factor (n) compensation to further improve the linearity. By adding a degeneration MOS pair cross-coupled to the outputs, it achieves 11.4-dB SFDR improvement compared to [74]. A PVT-robust capacitively degenerated dynamic amplifier was introduced in [76] which is used as a residue amplifier of pipeline SAR ADC. The ADC achieves 65-dB SNDR and 79.8-dB SFDR at 50 MS/s, and 0.7/1.86-dB SNDR variations over 0.8–1.0-V supply and 0 °C–100 °C temperature variation using an on-chip timing generator.

B. LOW-POWER LOOP FILTERS

The loop filters are one of the key building blocks in NS ADCs that determine energy efficiency and are implemented in different ways depending on the target applications. The loop filters of NS SAR ADCs can be simplified than ΔΣ ADCs, because they normally process a small residue, and many recent NS SAR ADCs are implemented without OTAs. In ΔΣ ADCs, however, active integrators are dominantly used, which normally aim for a higher SQNR, and the loop filters handle a large residue with a small number of quantizer bits, compared to NS SAR ADCs. Fig. 11 shows NS ADCs (BW $\leq$ 50 MHz) that have been presented at ISSCC and VLSI symposium [6]. They can be classified by their implementations: 1) passive integrator; 2) active integrator; and 3) VCO-based integrator.

1) PASSIVE INTEGRATORS

The passive integrators have advantages over the others in the perspective of simplicity, PVT robustness, and power consumption. However, they suffer from insufficient gain and a lack of driving capability. Therefore, the recent advances in energy efficiency are being made in NS SAR ADCs rather than ΔΣ ADCs. There are three strategies for passive integrators: using 1) a multi-input comparator;

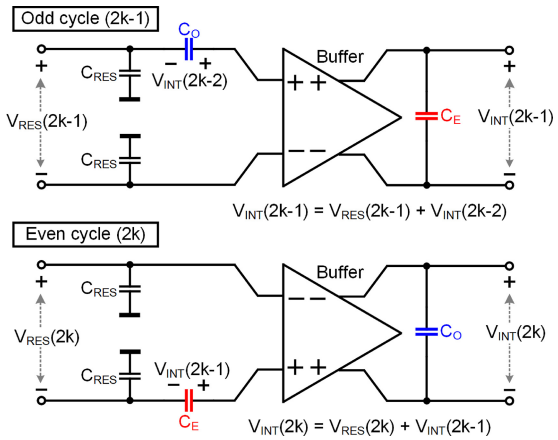

FIGURE 12. NS technique using capacitor stacking and buffering [12].

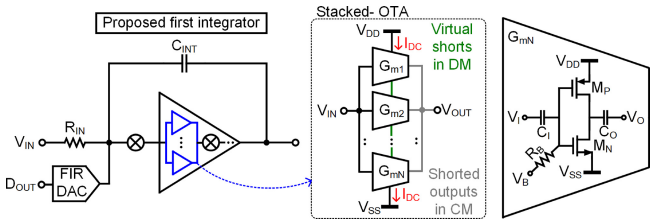

FIGURE 13. CT ΔΣ ADC with OTA stacking [111].

2) a capacitor-stacking technique; or 3) an interstage gain (or buffer) between passive integrators. Fredenburg and Flynn [77] introduced the use of a multi-input comparator. The multiple signal and residue inputs are matched to the filter's coefficients and added to the current domain, allowing for improved NS with the passive integrators. Although the additional input path results in increased noise, it is simple and power efficient, and is therefore becoming popular [78], [79], [80], [81], [82], [83], [84], [85]. The noise penalty of the multi-input comparator can be avoided by using a capacitor-stacking technique [86]. Each residue is sampled into multiple capacitors and stacked in a series configuration to obtain the desired gain. The parasitic capacitance of the stacked capacitors can limit the number of stacking (and, thus, the gain) and contribute to gain error. Therefore, careful design is required to minimize top/bottom parasitic capacitance. A few outstanding NS ADCs show up, achieving an FoM$_S$ of 178 dB [87]. An interstage gain (or buffer) has been used in [12], [88], [89], and [90], allowing cascading of passive integrators without gain loss and implementation of a high-order NS. In particular, Liu et al. [12] implemented a fourth-order NS using a unity-gain buffer and a capacitor stacking technique for the residue integration and achieved 93.3-dB SNDR and FoM$_S$ of 182 dB. Fig. 12 shows a simple first-order example, where the integration is realized by stacking a residue capacitor (C_{RES}) and an integration capacitor (C_O or C_E) and the stacking result is stored on the output capacitor (C_E or C_O) of the buffer. Even and odd phases are achieved by shuffling C_E and C_O. In this way, four groups of capacitors and buffers achieve the fourth-order NS, which is very energy efficient and robust to PVT variations.

2) ACTIVE INTEGRATORS

Loop filters using active integrators provide high gain and driving capability, which offers lots of freedom in architecture development. Since the first integrator has a substantial influence on the overall ADC performance, the research efforts aimed at improving the 1st integrator's noise, linearity, and energy efficiency. An inverter-based integrator is widely used because of its simplicity and noise efficiency [31], [91], [92], [93], [94], [95], [96], [97], [98], [99], [100], [101], [102]. It was first investigated in ΔΣ ADCs [91], [92] and remains popular today, regardless of DT or CT loop filters. Recently, an inverter-based dynamic integrator has been investigated to improve energy efficiency [14], [50], [103], [104], [105]. For example, Tang et al. [14] used a two-stage FIA as a loop filter, allowing an aggressive NTF with PVT tolerance. Wang et al. [50] introduced an error-feedback (EF)-CIFF loop filter with an open-loop FIA to obtain third-order NS, thus achieving outstanding FoM$_S$ of 182 dB. This is further developed into a fourth-order loop filter [103]. Liu et al. [104] used an FIA in an incremental zoom ADC to realize self-timed operation. A single-stage FIA using the correlated level shifting (CLS) technique was introduced by Hu et al. [105] to increase the loop filter's gain.

Steiner and Greer [97] introduced integrator-stacking to improve energy efficiency. However, it requires a high supply voltage and extra effort to deal with the integrator's mismatch. In [106], a dynamic power reduction in an incremental ΔΣ ADC is introduced by utilizing nonuniform weights in a cascade-of-integrator (CoI) filter. Using the same principle of nonuniform CoI filter weights as [106], [107] has implemented a single-bit to multibit reconfigurable incremental DSM taking advantage of a first phase intrinsically linear single-bit DAC and a second phase multibit operation with low quantization noise, in order to achieve 104-dB DR and 106-dB SFDR. Chandrakumar and Markovic [108] added a capacitively coupled gain stage before the 1st integrator in the ΔΣ-loop, which effectively reduces the noise and power of the loop filter. An OTA-stacking introduced in [109] improves the noise-current tradeoff [110]. Mondal et al. [111] used stacked OTA in the first integrator, as shown in Fig. 13. The AC-coupled inverters are stacked and reuse the current, and they are differentially decoupled with their source nodes, effectively shorted. Therefore, with a 3-stack OTA, the CT ΔΣ ADC obtains 3× Gm-boosting, thus achieving a SOTA FoM$_S$ of 183.3 dB.

Jang et al. [112] introduced a negative-R (NR) assisted integrator. By including NR at the integrator's virtual ground, OTA noise (both thermal and 1/f noise) is attenuated and the integrator's distortion is also canceled, thus significantly improving the energy efficiency. To reduce 1/f noise for narrowband applications, the chopped OTAs are widely used, but chopping in CT ΔΣ ADCs causes quantization-noise

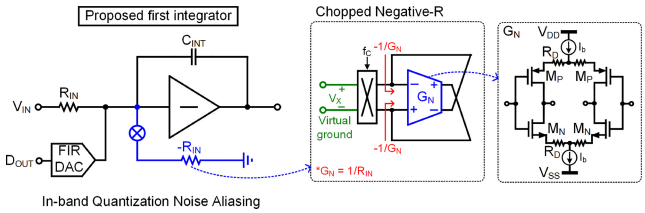

FIGURE 14. CT ΔΣ ADC with chopped NR [114].

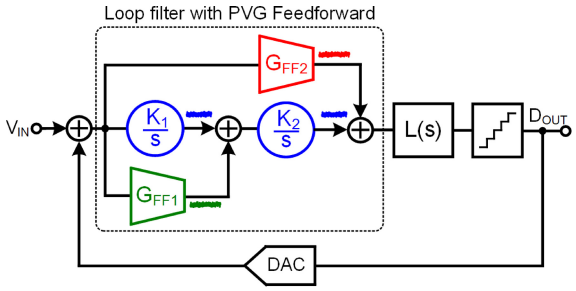

FIGURE 15. VCO-based ΔΣ ADC with PVG feedforward technique [125].

folding [113]. In [114], the chopped NR is applied to the first integrator (Fig. 14). The OTA noise is attenuated by the NR [115], and then NR is chopped to remove its $1/f$ noise. With the chopped NR, the Q-noise aliasing can be reduced by 30 dB compared to the chopped OTA [116]. Therefore, the CT ΔΣ ADC with the chopped NR achieves an FoM$_S$ of 181.9 dB.

Lee and Moon [117] proposed the single-ended ring amplifier with the pseudo-pseudo-differential (PPD) architecture in the first integrator. The pole of the first stage is placed out-of-band so that the stability of the second and third stages is not compromised. The steady-state bandwidth is also kept low to filter the noise in the first stage, which provides additional area and power savings. The DT ΔΣ ADC with PPD-based ring amplifier [118] achieves an FoM$_S$ of 185.3 dB with an area of 0.0375 mm^2.

3) LOOP FILTERS WITH VCO INTEGRATORS

Loop filters using VCO integrators are relatively new and offer several advantages over the active or passive integrators in the perspective of infinite dc gain, power efficiency, and scaling friendliness. However, the VCO integrator usually suffers from VCO nonlinearity that limits the linearity performance. Therefore, architectural development and circuit techniques to improve VCO linearity or circumvent this issue have been investigated.

A VCO-based integrator in [119] consists of two pseudo-differential G_m-CCOs and their calibration unit. The use of an open-loop G_m-CCO limits the NS to the first order and requires its calibration to cancel out the large nonlinearity. In [120], the VCO is placed in a feedback loop, which significantly improves the linearity. In [121], a third-order loop filter was implemented with VCO-based integrators, which however suffers from VCO nonlinearity and limits the ADC linearity. In [122], passive and VCO integrators were combined by using a parasitic capacitor at the VCO input. While a second-order loop filter was achieved, its SNDR was still limited to less than 70 dB.

More recently, Huang et al. [123] introduced differential pulse-code modulation (DPCM) to make the VCO processes a small error, thereby minimizing VCO nonlinearity. With an OSR of 32, –40-dB signal attenuation was achieved at the VCO input, significantly improving its linearity and achieving –105-dB THD. However, this requires a high-resolution 11-bit DAC and is truncated to 9 bits, resulting in a truncation error and, hence, SQNR leakage. To address this issue, a noise shaping of truncation error was introduced in [124], and excellent efficiency was achieved.

Pochet et al. [125] implemented a third-order ΔΣ ADC with VCO-based integrators, whose nonlinearity is leveraged with a pseudo-virtual ground (PVG) feedforward technique (Fig. 15). The VCO-based integrator uses a G_m-CCO followed by a phase-frequency detector (PFD) that extracts the integrator's phase difference and whose outputs control the current in the next-stage CCO. The first integrator input, i.e., the PVG node of the ADC, is tapped and forwarded to the other integrators' outputs using G_m-cells, which reduces the signal swings significantly. As a result, it achieved 92.1-dB SNDR with a 1.8-V input and a FoMs of 179.6 dB.

V. TECHNIQUES FOR CONTINUOUS-TIME ADCS

A. LOW POWER ΔΣ ADCS

ΔΣ ADCs have classically been used for highest resolution ADCs and achieved the best energy efficiencies in their class. Over the past two decades, their operating frequencies have expanded from classical narrowband audio and sensor readout applications to wideband applications [126], mainly due to the benefits of their CT implementation. While a few years ago, there was a distinct Nyquist gap for high-efficiency and high-resolution ADCs, i.e., there were mainly ΔΣ ADCs in the leading front. It is very interesting to note that concerning energy efficiency Nyquist rate ADCs are in the lead across all frequency ranges in Fig. 1 nowadays. ΔΣ ADCs still dominate the high-resolution domain from narrowband up to about 1-GS/s Nyquist frequency, but a few outstanding Nyquist converters appear in the 1–10-MS/s conversion range [9]. Next, we take a look at the leading front, discussing which architectures promise the best power efficiency in the narrowband and wideband, and which techniques yield the best resolution (see Figs. 1–3).

1) TECHNIQUES FOR NARROWBAND ΔΣ ADCS

Over the last few years, several zoom ADCs have been reported that achieve both high energy efficiency and high resolution. Chae et al. [94] originally proposed for a quasi-static input, where a coarse SAR ADC performed a single conversion per Nyquist clock cycle that set the reference levels of an incremental ΔΣ ADC. This operation originally defined the name zoom ADC. On the contrary, more recent zoom ADCs justified as the coarse ADC runs on

the same clock frequency as the ΔΣ ADC, which allows continuous updating of the reference and, thus, uses wider bandwidth. This implementation achieved outstanding resolution and efficiency in [98], where a dynamic zoom ADC was proposed over a 1-kHz band, in [101] over an audio bandwidth, and over a 50-kHz band in [127]. From an architectural point of view, the zoom ADC is the same as the 0-X MASH ADC. The fact that they achieved such a leading position is actually very interesting, as this is also observed in very wideband designs, as will be discussed in Section V-B.

The audio ADC in [128] actually dates from 1997 and still has a distinct spot in SNDR versus f_{nyq} comparison. In Fig. 2, the work competes with the much more recent work from [126] but achieves an FoM$_S$ of only 158 dB, about 25 dB worse than the leading SOTA today. Three more energy-efficient audio ADCs are mentioned here, first, the work of Lee and Moon [117], where a DT single-loop ΔΣ ADC is implemented using ring-amplifier-based integrators in a mature 180-nm CMOS process. Lo et al. [129] proposed a CT ΔΣ ADC, which offers easier drivability and an implicit anti-aliasing filter, in contrast to [117]. It uses a tri-level DAC like [128] but is based on a current-steering DAC. Similarly, Jang et al. [114] also used a CT ΔΣ ADC with a trilevel DAC but additionally employed an FIR DAC [130], [131] and a chopped negative resistor to increase the energy efficiency.

In the sensor and industrial frequency range, we can then highlight a few further designs. First, Theertham et al. [132] implemented again a CT ΔΣ ADC employing an FIR DAC and chopping, where the chopping artifacts advantageously fall into the FIR notches, as also originally proposed in [130]. Also, this design is implemented in a mature 180-nm technology.

The incremental ADC of Hsieh and Hsieh [10] has a distinct spot in the efficiency comparisons. As an incremental ΔΣ ADC is actually a Nyquist ADC, but it should not be mentioned in comparison to the ΔΣ ADC. The design is very low voltage with only a 400mV supply and uses an opamp-less time-domain loop filter. This is an example of the recent trend to employ time-domain signal processing that scales nicely with technology. Finally, the until now fastest published incremental ΔΣ ADC shall be mentioned [133], which employs an incremental SMASH architecture and variable bit-width to achieve 2 MS/s and an intrinsic linearity of 97 dB.

2) TECHNIQUES FOR WIDEBAND ΔΣ ADCS

Wideband ΔΣ ADC obviously has different demands than narrowband implementations. The excessive sampling frequency is usually avoided, as it poses severe challenges to clock generation, decimation filter operation, and signal integrity in the overall system. From the beginning, therefore, techniques were used that allowed a reduction of the oversampling ratio. Most wideband ΔΣ ADC are nowadays multibit designs [126], as they come with intrinsically better

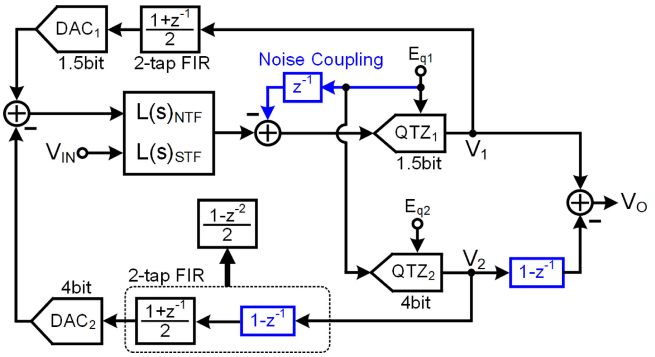

FIGURE 16. Block diagram of the CT dual-loop SMASH in [13].

resolution, more aggressive NS, and about 3–4-dB higher maximum stable amplitude (MSA). Only a few exceptional designs have shown that single-bit implementations can compete with the efficiency and performance of their multibit counterparts [134]. Moreover, almost exclusively wideband ΔΣ ADC are implemented with CT loop filters. The CT loop filter not only offers better drivability due to its resistive or G_m-based input [135] but also features implicit signal filtering; often reduced to an implicit anti-aliasing filter. It also allows the attenuation of out-of-band interference signals [136], which can be even enhanced by embedding analog [137] or mixed-signal filtering [138]. It is worth noting that such features can lead to significant advantages for a system's complexity and power consumption, but are not covered in any FoM$_S$ in Figs. 1 and 2.

Looking at the front of the SOTAs, it is worth mentioning that most of the leading designs are MASH ΔΣ ADCs. The early design in [139] is a multibit cascaded 2-2-0 ΔΣ ADC and keeps a distinct spot in the SNDR versus bandwidth (see in Fig. 2). Cenci et al. [100] achieved excellent efficiency for a wideband ΔΣ ADC, where a coarse SAR ADC and a fine ΔΣ ADC were used to achieve 0-X MASH, effectively the same architecture as a zoom ADC. Also, Liu et al. [140] employed a 1-1-1 MASH for the incredibly wideband design, achieving a sweet spot in energy efficiency. Qi et al. [13] aimed for extended linearity, where a 3-0 sturdy MASH ADC was employed (Fig. 16), achieving 90-dB linearity without calibration. It was based on a noise-coupled SAR ADC in the first stage and a requantization in the second stage to build the CT Sturdy MASH loop filter. This achieves a leading spot in the resolution comparison, leaving alone that the uncalibrated linearity is not even reflected there. These designs, some of which are at the front of SOTAs in the SNDR or efficiency comparison, suggest that the MASH concept offers distinct advantages.

Nonetheless, other architectures also achieve outstanding performance. He et al. [141] implemented a CT ΔΣ ADC with excellent linearity. Its third-order multibit loop filter not only uses DAC mismatch correction, but also allows on-chip calibration for unequal DAC rise and fall times and, thus, ISI reduction. Finally, the outstanding wideband designs of Shibata et al. [7] and Shibata et al. [142] should be

mentioned. Shibata et al. [142] was the most wideband ΔΣ ADC at the time of its publication and allowed to expand the possible performance goals for ΔΣ ADC into the GHz range. It employs a sixth-order loop filter that can be reconfigured from lowpass to band-pass operation. However, two external inductors were employed for efficient bandpass filtering.

B. CT- AND DT HYBRID ADCS

Classically, the multibit quantizer in wideband CTΔΣMs consists mainly of flash ADCs. In this case, the design complexity increases rapidly to increase the quantization bits. It can be leveraged by the energy-efficient ADCs and, thus, early hybridization starts with replacing the flash ADC with the SAR ADC [143], [144], [145], [146]. By embedding the SAR ADC, the quantizer bits are rapidly increased, thus reducing the loop filter order and OSR. However, the introduction of the SAR ADC inevitably brings additional delays. A dedicated delay compensation path is often developed for stability reasons [147]. Also, multibit feedback DAC suffers from mismatch errors that require calibration or dynamic element matching [148].

More hybridization at the architectural level can be considered to further improve performance. Wu et al. [149] introduced noise coupling (NC) in the SAR quantizer. In a SAR operation, the quantization error is naturally produced at the comparator input, which can be easily extracted and fed back into the loop filter for extra NC. It further improves the NS effect and loop-filter stability can be co-designed between the NC SAR and the remaining conventional loop-filter. As a result, it realized a sixth-order NS with a fourth-order loop filter and a second-order NC and achieved a 75.3-dB SNDR at 45-MHz-BW with a low OSR of 10. Jang et al. [150] explored the NC implementation in a digital domain, further simplifying the loop filter design.

The researchers also tried to leverage the recent NS SAR ADCs. Liu et al. [151] proposed to embed a second-order NS SAR in the loop filter and, hence, only one OTA is required to realize the third-order noise shaping. Shi et al. [152] further extended the design by combining a single-amplifier-biquad (SAB) loop filter with a second-order NS SAR. It realizes a fourth-order noise shaping with only one OTA, resulting in exceptional efficiency. Note that the stability of the hybrid fourth-order CT-DT ΔΣ ADC is similar to a second-order CT ΔΣM, which greatly simplifies the loop filter design.

To take full advantage of CT ADCs, some traditional DT architectures are being converted to their CT counterparts. Gubbins et al. [153] proposed incorporating a CT-ADC as the first stage of a pipelined ADC. Together with anti-aliasing filtering, the use of resistive input can greatly simplify the system design. The CT pipeline stage has two delay paths; one comes from the input as the fast path, and the other goes through the first-stage quantizer as the slow path, as shown in Fig. 17. Path delays must be matched to avoid signal overflow in the following stages. Usually, either a positive delay in the fast path [154] or a negative delay

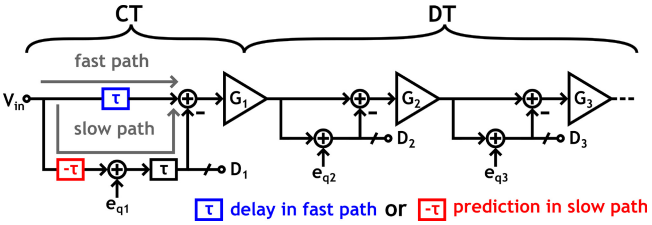

FIGURE 17. Continuous-time pipeline architecture.

(prediction) in the slow path [153] can be added. However, the analog delay suffers from PVT variations and requires careful design. Removing the sampling process improves the ADC conversion speed, e.g., the design in [154] runs at 9 GS/s.

Similarly, Shen et al. [155] introduced the CT 1st stage to the SAR design. With the sampling operation removed, it does not suffer from kT/C noise and, thus, the 13-bit SAR only requires a small DAC of 120 fF. The first stage operates at high speed, minimizing slow path delay. Together with the built-in redundancy, no additional delay is required for path matching. This concept has been extended to other advanced architectures. Li et al. [156] implemented a CT NS SAR for inherent anti-aliasing filtering from the CT front-end and achieved great energy efficiency from the NS SAR. A duty-cycled integrator is adopted to deal with the timing conflict between the NS SAR and the CT integrator.

In the past few years, researchers have explored various CT-DT hybrid architectures. The first stage is usually implemented with CT front-ends that feature easy driving, sampling-free, and anti-aliasing filtering. The DT quantizer is used to increase energy efficiency.

VI. CONCLUSION

Over the last ten years, the energy efficiency of ADCs has improved substantially thanks to constant innovations in both architectures and circuits. The available bandwidth of the best FoM ADCs has been expanded by almost the same factor. In this context, the energy efficiency of ADCs is still improving, and these trends are exacerbated by hybrid ADCs. The clear distinction between ADC architectures becomes blurred when looking at the best FoM ADCs that leverage the architecture combinations. Due to many advantages, CT ADCs are gaining more and more attention, and additional hybridization with CT and DT promises successful alternatives to classic architectures.

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MOONHYUNG JANG (Member, IEEE) received the B.Sc. (summa cum laude) and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2014 and 2021, respectively.

His Ph.D. research was in the field of High-Resolution Power-Efficient Continuous-Time Delta-Sigma A/D Conversion. He is currently a Postdoctoral Research Fellow with the Murmann Mixed-Signal Group, Stanford University, Stanford, CA, USA. His current research interests include low-power data converters, high-bandwidth single-cell resolution brain–machine interfaces, in-memory computing-based deep neural network accelerators, and various high-performance mixed-signal-integrated circuits and systems.

Dr. Jang was the recipient of the 2020–2021 IEEE Solid-State Circuits Society Predoctoral Achievement Award, the 2020 Yonsei-Samsung Semi-conductor Research Center Best Paper Award, the 2020 Samsung Human-Tech Paper Award Silver Prize in Circuit Design, and the 2018 Samsung Human-Tech Paper Award Bronze Prize in Circuit Design. He has served as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS.

XIYUAN TANG (Member, IEEE) received the B.Sc. degree (Hons.) from the School of Microelectronics, Shanghai Jiao Tong University, Shanghai, China, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from The University of Texas at Austin, Austin, TX, USA, in 2014 and 2019, respectively.

He was a Design Engineer with Silicon Laboratories, Austin, from 2014 to 2017, where he was involved in the RF receiver design. He was a Postdoctoral Researcher with the University of Texas at Austin from 2019 to 2021. He is currently an Assistant Professor with the Institute for Artificial Intelligence and the School of Integrated Circuits, Peking University, Beijing, China. His research interests include digitally assisted data converters, low-power mixed-signal circuits, and analog data processing.

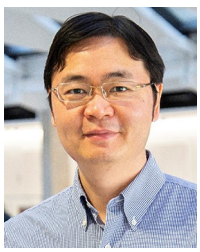
YONG LIM (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Yonsei University, Seoul, South Korea, in 2004 and 2006, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2017, with support from the Samsung Fellowship.

He joined Samsung Electronics, Hwaseong, South Korea, in 2006, where he focused on developing CMOS image sensor readout circuits until 2012. Since 2017, he has been developing data converters for SoCs and mixed-signal ICs.

Dr. Lim was a recipient of the ISSCC 2022 Anantha P. Chandrakasan Award for Outstanding Distinguished Technical Paper, and the 2023 IEEE Brokaw Award for Circuit Elegance. He currently serves for the Technical Program Committee of the IEEE Asian Solid-State Circuits Conference and the IEEE Custom Integrated Circuits Conference.

JOHN G. KAUFFMAN (Member, IEEE) received the B.Sc. and M.Sc. degrees from Worcester Polytechnic Institute, Worcester, MA, USA, in 2004 and 2005, respectively, and the Ph.D. degree from the University of Ulm, Ulm, Germany, in 2013.

From 2005 to 2008, he worked with the MEMS Division, Analog Devices, Wilmington, MA, USA. From 2008 to 2009, he worked with the DC/DC Design Group, Linear Technology, Munich, Germany. From 2013 to 2017, he was with Intel GmbH, Munich, as an Intel Member of Technical Staff designing receiver ADC's for Intel's LTE products. While at Intel, he designed three different multimode CT delta–sigma ADCs and received five U.S.-granted patents. From 2017 to 2019, he was with Nokia Networks, Silicon Valley, CA, USA, as a Technical Leader for TX DAC design and later became a Research and Development Manager for 5G RFIC design delivering a 4T4R Sub 6-GHz transceiver for in-house platforms. Since 2019, he has been with the University of Ulm as a Group Leader furthering research in ADCs, DACs, and other mixed-signal architectures for high-speed and precision designs.



NAN SUN (Senior Member, IEEE) received the B.S. degree (Hons.) from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 2006, and the Ph.D. degree from the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA, in 2010.

He is currently a Professor with the Department of Electronic Engineering, Tsinghua University. He was an Assistant Professor and then a Tenured Associate Professor with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX, USA. As an Advisor/Co-Advisor, he has graduated 26 Ph.D. students, ten of whom are professors at leading universities in the U.S. and China. He has published over 200 journal and conference papers, including over 50 IEEE JOURNAL OF SOLID-STATE CIRCUITS and ISSCC papers. He has also written seven book chapters and held seven U.S. patents. His research interests include analog, mixed-signal, and RF-integrated circuit design, analog circuit design automation, sensor interfaces, miniature spin resonance systems, and solid-state platforms to analyze biological systems for biotechnology and medicine.

Dr. Sun received the Inaugural IEEE Solid-State Circuits Society New Frontier Award in 2020 and the NSF Career Award in 2013. He was the Co-Chair of the IEEE Solid-State-Circuits Society and Circuits-and-Systems Society Joint Chapter in the Central Texas Section from 2011 to 2018, and won the Chapter of the Year Award in 2014. He holds the Zhou Bingkun Endowed Professorship at Tsinghua University. He was the holder of the AMD Endowed Development Chair, Texas Instruments Jack Kilby Endowed Fellowship, Temple Foundation Endowed Fellowship, and Silicon Labs Endowed Fellowship at UT Austin. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS and *Journal of Semiconductor*, and a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has served for the Technical Program Committee (TPC) of ISSCC, CICC, and ASSCC. He is currently the TPC Chair of CICC 2024. He has also served as the Conference Chair and the TPC Chair for the ICAC Workshop. He has served as an IEEE Circuits-and-Systems Society Distinguished Lecturer from 2019 to 2021 and an IEEE Solid-State-Circuits Society Distinguished Lecturer from 2021 to 2022.

MAURITS ORTMANNS (Senior Member, IEEE) received the Dr.Ing. degree from the University of Freiburg, Freiburg im Breisgau, Germany, in 2004.

From 2004 to 2005, he was with Sci-Worx GmbH, Hannover, Germany, working in the field of Mixed-Signal Circuits for Biomedical Implants. In 2006, he joined the University of Freiburg as an Assistant Professor. Since 2008, he has been a Full Professor with the University of Ulm, Ulm, Germany, where he is currently the Head of the Institute of Microelectronics. He has authored the textbook *Continuous-Time Sigma-Delta A/D Conversion* and authored/coauthored several other book chapters and over 250 IEEE journal articles and conference papers. He holds several patents. His current research interests include mixed-signal-integrated circuit design with special emphasis on data converters and biomedical applications.

YOUNGCHEOL CHAE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from Yonsei University, Seoul, South Korea, in 2003, 2005, and 2009, respectively.

From 2009 to 2011, he was a Postdoctoral Researcher with the Delft University of Technology, Delft, The Netherlands, he developed high-precision sensors and interface circuits for many applications. After joining Yonsei University in 2012, he has been a Full Professor of Electrical and Electronic Engineering, leading a Yonsei Mixed-Signal IC Group focused on innovative analog and mixed-signal circuits and systems for communication, sensing, and biomedical applications. This has resulted in over 130 technical articles and over 50 patents.

Dr. Chae received the ISSCC 2021 Takuo Sugano Award for Outstanding Far-East Paper, the Best Young Professor Award in Engineering from Yonsei University in 2018, the Haedong Young Engineer Award from the Institute of Electronics and Information Engineers Korea in 2017, the ISSCC Silkroad Award in 2017, the Outstanding Research Award of Yonsei University in 2017, 2019, and 2020, and the Outstanding Teaching Awards of Yonsei University in 2013 and 2014. He has been serving as a TPC Member for the International Solid-State Circuits Conference, Asian Solid-State Circuits Conference, and Custom Integrated Circuits Conference. He has been serving as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and a Distinguished Lecturer for IEEE Solid-State Circuits Society.