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A Digital Power Amplifier With Built-In AM–PM Compensation and a Single-Transformer Output Network

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ABSTRACT This article presents a digital power amplifier (DPA) with a built-in AM–PM compensation technique and a compact single-transformer footprint. The AM–PM distortion behavior of the current-mode/voltage-mode power amplifiers (PAs) is detailed and an AM–PM compensation technique for both modes is introduced. The proposed design utilizes one current-mode DPA as the main path PA and a class-G PA voltage-mode digital PA as the auxiliary path PA, combined through a single-transformer footprint. It provides enhanced linearity through built-in adaptive biasing and hybrid current-/voltage-mode Doherty-based power combining. As a proof of concept, a 1.2–2.4-GHz wideband DPA is implemented in the Globalfoundries 45-nm CMOS SOI process. The measurements show a 37.6% peak drain efficiency (DE) at 1.4 GHz, and 21.8-dBm saturated output power (Psat) and 1.2×/1.4× power back-off (PBO) efficiency enhancement, compared to the ideal class-B at 3 dB/6 dB PBO at 1.2 GHz. This proposed digital PA supports 20-MSym/s 64-QAM modulation at 14.8-dBm average output power and 22.8% average PA DE while maintaining error vector magnitude (EVM) lower than −23 dB without any phase predistortion. To the best of our knowledge, this is the first demonstration of hybrid current–voltage-mode Doherty power combining on a single-footprint transformer over a broad bandwidth (BW).

INDEX TERMS AM–PM compensation, CMOS, digital power amplifier (DPA), Doherty, hybrid, linearity, load modulation, phase distortion, polar modulation, power back-off (PBO).

I. INTRODUCTION

MODERN communication systems adopt spectrally efficient modulation schemes to enhance the link throughput within a given frequency bandwidth (BW) at the cost of a large peak-to-average ratio (PAPR). This poses stringent requirements on the energy efficiency of RF power amplifiers (PAs) for both peak output power and also at power back-off (PBO) to ensure efficiency under modulation. Therefore, there is an increasing interest in exploring PBO efficiency enhancement techniques to achieve high PA average efficiency under these high-PAPR modulation schemes [1], [2], [3], [4], [5]. Doherty load modulation is one of the widely used techniques to boost PA PBO efficiency. However, when the Doherty PA's main path and auxiliary (Aux) path do not cooperate well together, they have limited linearity and require a large area to support the load modulation output matching network [6], [7], [8], [9]. Outphasing PAs support PBO efficiency enhancement but require significant baseband computation to generate the outphasing signals often with limited dynamic range [10], [11], [12], [13]. Envelope tracking (ET) PAs exhibit a tradeoff for the envelope tracker's own efficiency, dynamic range, speed, and accuracy, which are unsuitable for high-speed (>100 MHz) and high-PAPR signals [14], [15], [16], [17].

Analog PAs are widely used in modern wireless communication systems. However, their designs cannot be readily transferrable across process nodes, benefit from device scaling, or support direct synthesis. Thus, there is an increasing interest in digital PA (DPA) research [18], [19], [20], [21], [22], [23], [24], [25]. DPAs support the ability to implement multiple functionalities within one compact formfactor block, extensive digital reconfigurability, and performance and design tracking aggressive CMOS process scaling [26]. Such digital Pas would be a good solution for applications

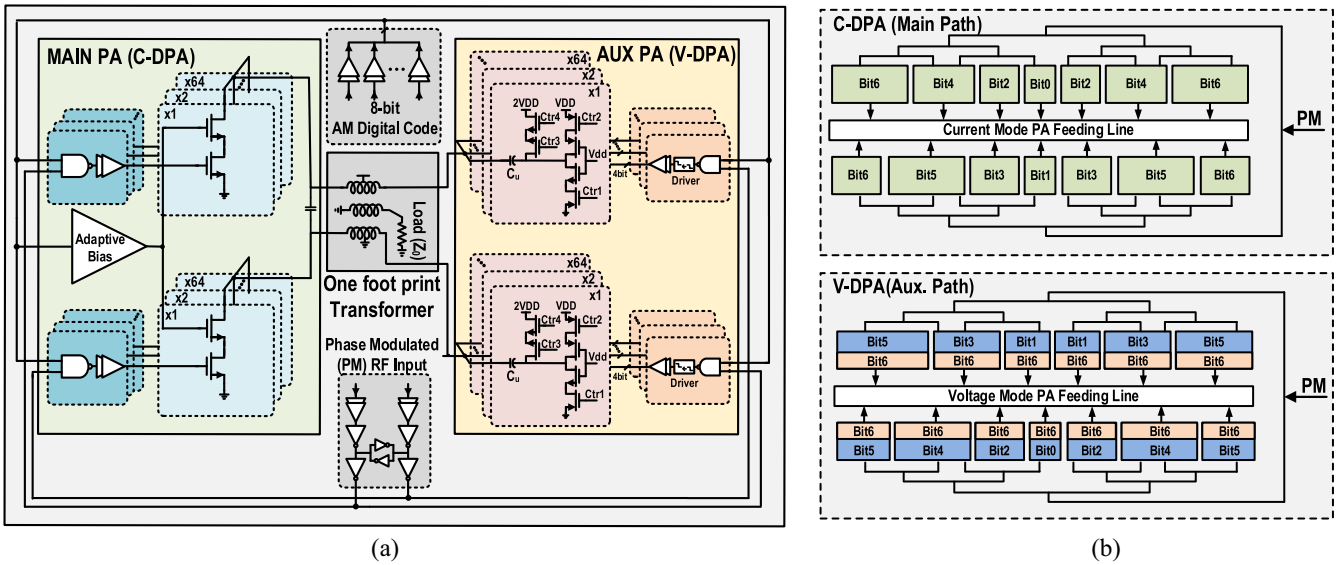


FIGURE 1. (a) Schematic of the proposed hybrid polar Doherty digital PA. (b) Routing line floorplan for the Main and Aux. (auxiliary) PA paths.

such as low-cost IoT, which uses appropriate power, small size, and not too complicated modulation. In particular, in the case of low-cost PA targeting such NB-IoT, it would be reasonable to consider digital PA, which has good linearity, not require DPD that increases complexity and cost.

A DPA can be generally divided into two categories based on their power cells, the current-mode DPA such as the class-D^{-1}, and the voltage-mode DPA such as the switched capacitor PA (SCPA). Current-mode DPAs typically support higher output power levels for a fixed supply voltage as the output voltage swing can exceed the supply voltage, but they suffer from large signal nonlinearities due to distortion [27], [28], [29], except for some recent designs which utilize built-in analog compensation techniques, such as AM–PM linearization [30]. Voltage-mode DPAs achieve good linearity and efficiency but provide limited output power levels as their output voltage swing is lower than the supply voltage [31], [32], [33]. Recently, a hybrid technique that improves the linearity by implementing the current-mode and voltage-mode DPAs together has been demonstrated [34]. However, it sacrificed the peak drain efficiency (DE) of the current-mode DPA by tuning on only half of its total power cells and suffers from area overhead and major passive loss penalty by connecting three transformers in series as its output matching network.

While a large amount of research to increase the PBO efficiency for complex modulation communication has been conducted, the techniques applied typically deteriorate the overall linearity [35], [36], [37]. Therefore, many digital PAs inevitably use 2-D digital predistortion (2D DPD) tables or models to compensate for their linearity. However, using 2D DPD comes with various limitations. First, it is necessary to accurately characterize the PA and create an inverse function in the 2-D space. Second, it increases the system power consumption and complexity. Furthermore, it is often incapable of sufficiently canceling all the PA nonlinearity. In particular, output impedance variations may aggravate DPD performance [38]. Therefore, it is essential to ensure intrinsic PA linearity with built-in linearization.

To address the aforementioned issues, we propose a fully integrated single-footprint hybrid current–voltage-mode digital Doherty PA [39]. In our proposed DPA topology, adaptive biasing is implemented for the current-mode DPA to minimize its AM–PM nonlinearity and the voltage-mode DPA used a class-G DPA [40], which has its own AM–PM compensation characteristic. In addition, the proposed DPA used a single-footprint transformer to apply a hybrid self-compensation technique consisting of a current-mode DPA and voltage-mode DPA. Note this reported design differs from the design in [34], in that it implements two paths as a single transformer, utilizes all cells in the current-mode DPA using the adaptive biasing scheme, and improves linearity and efficiency using characteristics of class-G DPA. This article is organized as follows. Section II introduces the proposed hybrid polar Doherty DPA architecture. Section III presents the analysis of AM–PM distortion within the current-/voltage-mode DPAs and proposes methodologies to improve the linearity of both, and measurement results are shown in Section IV. Section V concludes this article.

II. PROPOSED ARCHITECTURE

Fig. 1 shows the system architecture of the proposed hybrid (current/voltage) polar Doherty digital PA and routing line floorplan for the Main/Aux. PA paths. The proposed architecture consists of a current-mode DPA, a voltage-mode DPA, phase modulation (PM) driver, AM driver, adaptive biasing R2R DAC, and an AM buffer array and a single-transformer

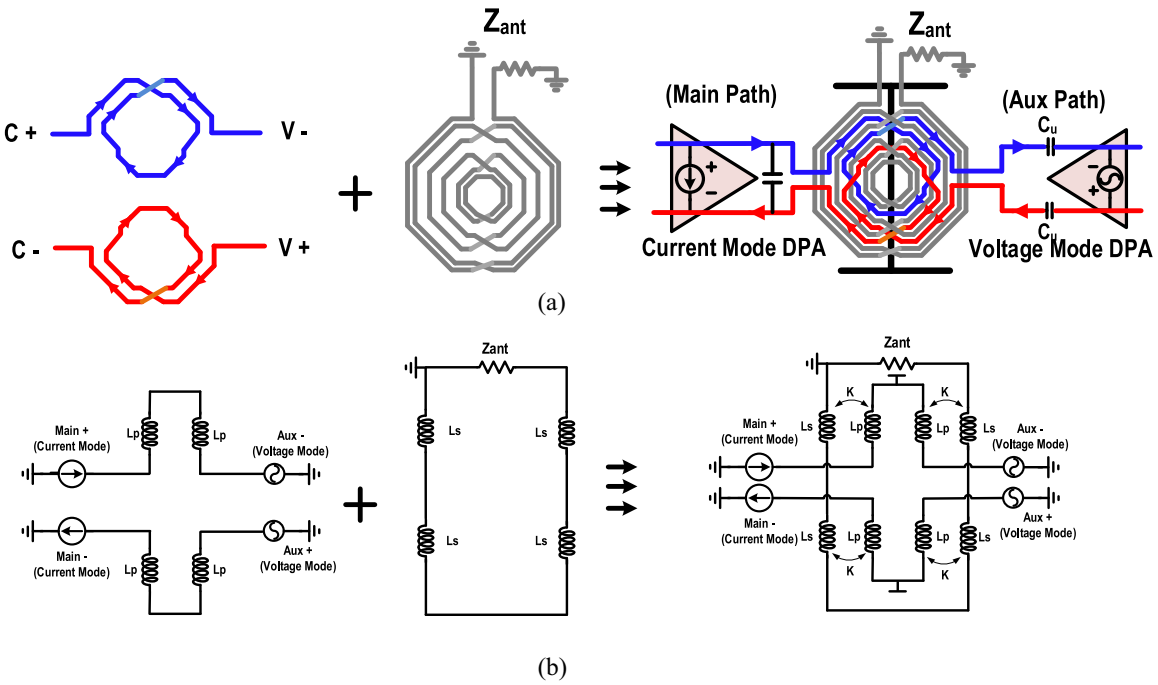


FIGURE 2. Proposed single-footprint transformer as the DPA output matching network. (a) Layout of the OMN. (b) Schematic of folded form of the OMN (L_p = 1.08 nH, L_s = 9.95 nH, k=0.713, Q_p = 6.2, Q_s =7.2, and n=2.975. Note the Main-path PA is current-mode, while the Aux-path PA is voltage-mode.

output network. 8-bit AM codes control both the output power and adaptive biasing. The constant envelope PM carrier signal is buffered by a comparator and a digital driver that then feed the two sub-PAs. The AM signal is digitized to an 8-bit parallel AM control code and is then fed to the PA to control the numbers of PA cells enabled. The main path (C-DPA) and Aux. path (V-DPA), which are distributed symmetrically along the output feedline, apply a fork shape configuration to minimize the phase offset and deliver PM signals evenly to the Main and Aux paths.

A. SINGLE FOOTPRINT BROADBAND LOAD MODULATION NETWORK FOR HYBRID VOLTAGE/CURRENT DPA

This design utilizes a single-footprint parallel-combining transformer to achieve the broadband Doherty power combining network [41]. The transformer occupies 430 μm $\times$ 430 μm die area. Fig. 2 shows the proposed single-footprint transformer load modulation output matching network. To achieve the desired impedance transformation ratio and enhance the quality factor, the three-coil parallel-combining transformer is implemented with nine turns, of which three turns are the two primary inductances (connected to the Main and Aux. path PAs) and the other six turns are the secondary inductance (connected to the 50-Ω antenna load). The passive efficiency of this single-footprint transformer at the peak PA output power is shown in Fig. 3. The definition of passive efficiency can be described as the proportional power delivered to the load to the power delivered to the

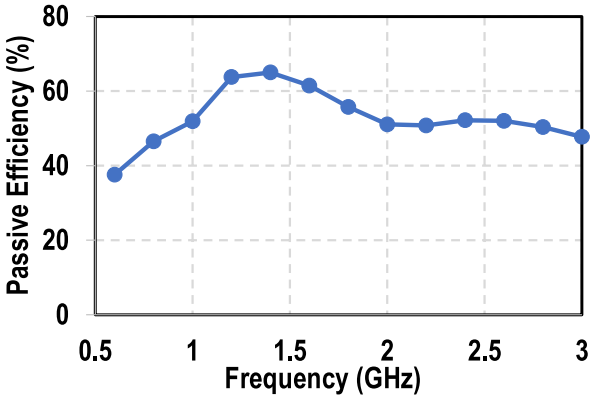


FIGURE 3. EM-simulated passive efficiency of the PA output network.

network, as shown in

$$\text{Passive efficiency} = \frac{P_{\text{delivered to the load}}}{P_{\text{delivered to Network}}} = \left[1 + \frac{R_s}{R_{\text{in}}}\right]^{-1} = \left[1 + \frac{Q_{\text{loaded}}}{Q_{\text{unloaded}}}\right]^{-1}$$

where R_s and R_{in} are the impedance of source and input, respectively, and the loaded quality factor of the network is defined as

$$Q_{\text{loaded}} = \frac{2\pi fL}{R_{\text{opt}}} = \frac{1}{2\pi fCR_{\text{opt}}}$$

where Q_{loaded} is the loaded quality factor of the series resonant network. Note that this proposed load modulation

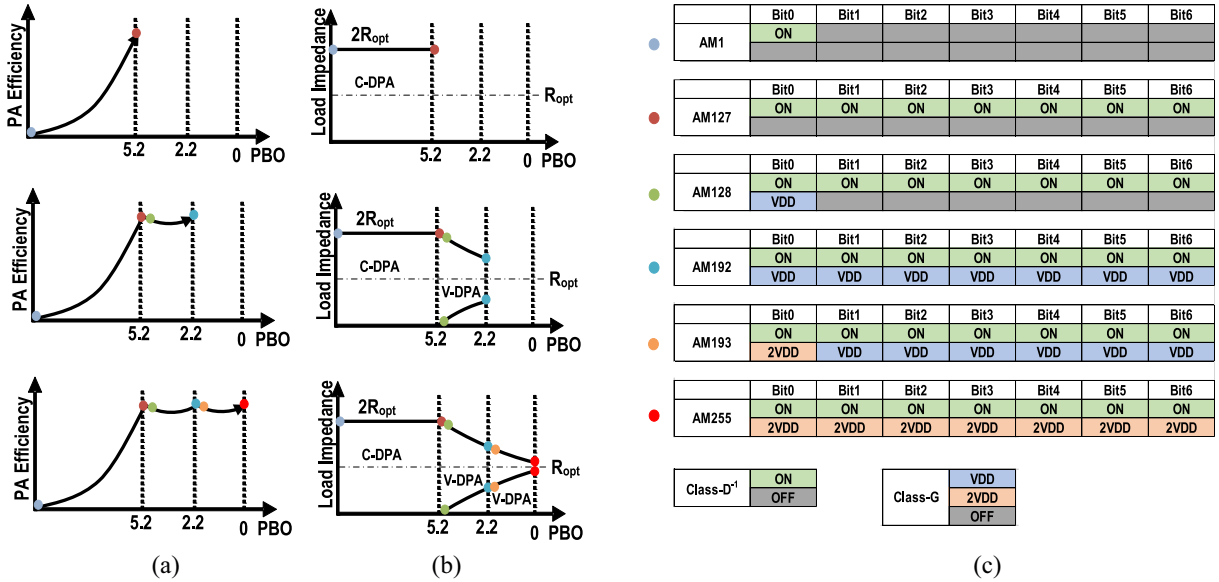


FIGURE 4. Simulated results of (a) PA efficiency, (b) load impedance, and (c) example of operation sequence.

architecture does not need a large switch in the Aux path to provide a short, because the voltage-mode PA used in Aux path provides a low impedance when turned off, supporting a very compact formfactor. However, if a current-mode PA is used in the Aux path, when the current-mode PA is turned off, a switch is then required, because the current-mode DPA shows high impedance when turned off, which will load the PA output passive network and degrade its efficiency. To the author's knowledge, this is the first demonstration of power combining current-mode and voltage-mode DPAs in a single-transformer footprint by using a single-transformer-based parallel combining network. Note this output passive network is not designed to realize any impedance inverter properties to ensure its broadband operation, since the turning-on sequence of the voltage/current-mode PAs performs effective Doherty active load modulations.

This is detailed as follows. The output voltage swing in the differential current-mode [28] and voltage-mode [26] PAs, with n out of N unit cells turned on are as follows:

$$V_{\text{out\_Current\_mode}} = \pi\left(\frac{n}{N}\right) \times V_{\text{DD}}, \tag{1}$$

$$V_{\text{out\_Voltage\_mode}} = \frac{4}{\pi}\left(\frac{n}{N}\right) \times V_{\text{DD}}. \tag{2}$$

The impedance at the main and aux PA output for a Doherty PA can be derived as

$$Z_{\text{Main}} = \frac{R_L}{1 + \frac{V_{\text{Aux}}}{V_{\text{Main}}}} \tag{3}$$

$$Z_{\text{Aux}} = \frac{R_L}{1 + \frac{V_{\text{Main}}}{V_{\text{Aux}}}} \tag{4}$$

where V_{Main} and V_{Aux} are the Main and Aux amplifier voltages, respectively. Replacing (1) and (2) into (3) and (4), the impedance presented to each PA can be derived as

$$Z_{\text{Main}} = R_L \frac{1}{\left(1 + \frac{4}{\pi^2} \times \frac{2n+m}{2^M-1}\right)} \tag{5}$$

$$Z_{\text{Aux}} = R_L \frac{1}{\left(1 + \frac{\pi^2}{4} \times \frac{2^M-1}{2n+m}\right)} \tag{6}$$

where M is total number of bits for VDPA, and m and n are the number of "ON" power cells of VDD mode and 2VDD mode in VDPA, respectively. Thus, depending on the AM turn-on sequence, each PA experiences proper active load modulation, achieving deep PBO efficiency enhancement.

B. OVERALL OPERATION OF PROPOSED DPA ARCHITECTURE

The proposed hybrid single-footprint transformer digital PA combines one main path C-DPA and one Aux path V-DPA, Class-G DPA, to achieve built-in AM–PM compensation and PBO efficiency enhancement. In the low-power region, as the output power increases, current DPA cells sequentially turn on until 5.2-dB PBO. At this time, if the output voltage of Main and Aux. path is equal, it would be 6-dB PBO after all the cells of Main path are turned on like conventional Doherty structure, however, the proposed architecture has different output voltages and impedances between main path and Aux path as shown in (1) and (4), thus when all the cells of Main path are turned on, theoretically, it achieves an efficiency peak at 5.2-dB PBO due to Doherty load modulation. After all the cells of the main path are turned on, the unit cells of the Aux path are gradually turned on in VDD mode. When the Aux path is fully turned on to VDD mode, the overall PA achieves an additional efficiency peak by class-G operation at 2.2-dB PBO, and then the Aux PA cells are gradually turned on to 2VDD mode as well. Fig. 4

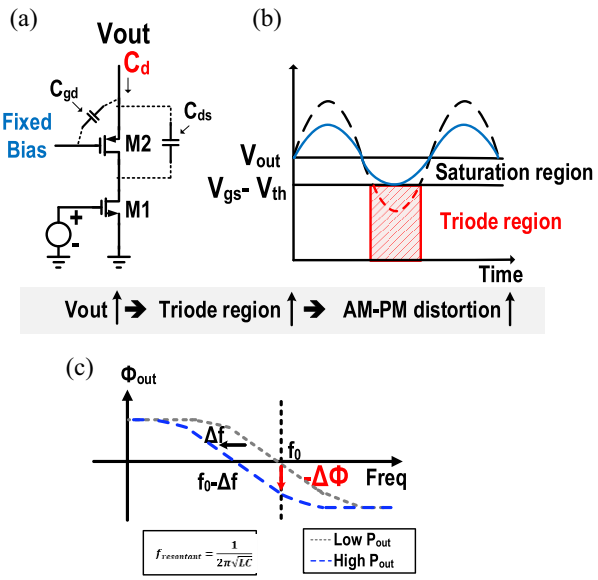


FIGURE 5. (a) Conventional current-mode DPA schematic. (b) Output voltage swings according to each region. (c) Phase nonlinearity behavior of conventional current-mode DPA.

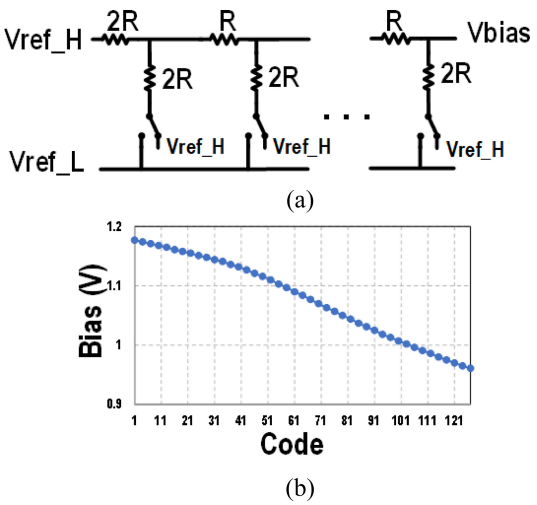


FIGURE 6. (a) Schematic of R2R DAC. (b) Simulated results of adaptive biasing.

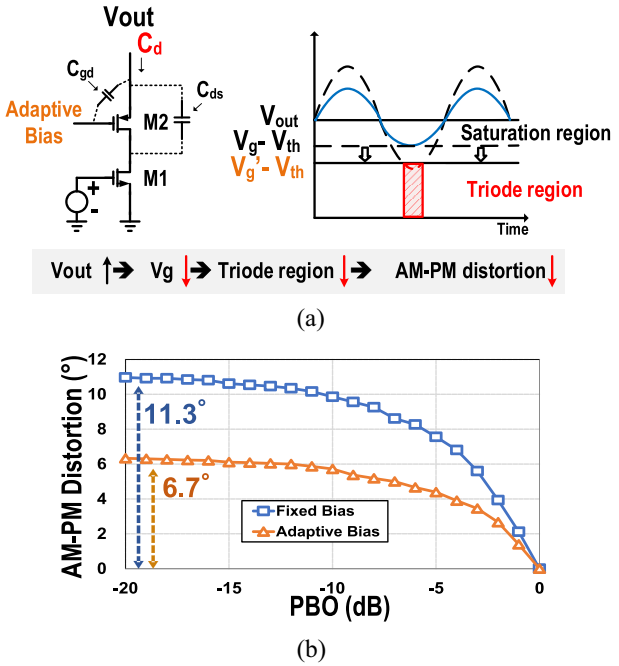


FIGURE 7. (a) Schematic of the proposed current-mode DPA with adaptive biasing. (b) Simulated AM–PM distortion results.

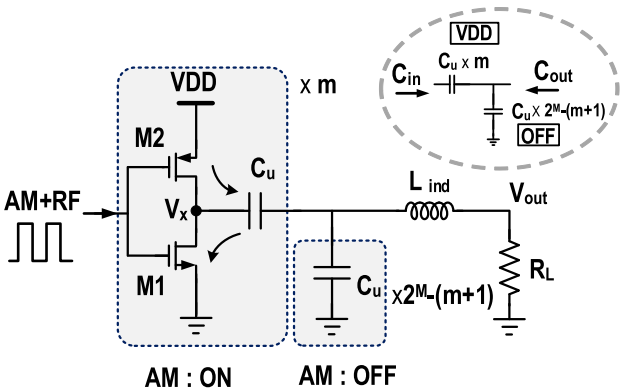


FIGURE 8. Schematic of conventional SCPA.

illustrates the efficiency, load impedance, and overall turn-on sequence of each PA operation.

III. THEORY OF AM–PM DISTORTION OF DIGITAL PA

There are two main sources of linearity distortion for PAs, AM–AM and AM–PM [42]. Since AM–AM distortion can be compensated through proper selection of the AM control code [30], we will focus on AM–PM distortion. The principles for the occurrence of AM–PM distortion and the methods to improve/compensate for it regarding the current-mode DPA and the voltage-mode DPA, respectively, are described below.

A. CURRENT-MODE AM–PM COMPENSATION

We will first review the behavior of conventional current mode, class-D^{-1} PA, and its main causes of AM–PM distortion [27], [30]. Fig. 5 shows the schematic for class-D^{-1} PA composed of N-bit segment binary-weighted cells. The nonlinearity of the current-mode DPA is mainly caused by the output capacitance C_d variations against output power level [30]. C_d can be derived as $C_{\text{gd}} + (1 - 1/|A|) \times C_{\text{ds}}$, where C_{ds} is the total effective capacitance between the drain and the source of M_2 and A is the voltage gain of the cascode transistor (M_2) [43]. First, the C_{gd} of the cascode transistor (M_2 in Fig. 5) is varied according to the device operation region as [44]

$$C_{\text{gd\_triode}} = \frac{WLC_{ox}}{2} + WC_{OV} \tag{7}$$

$$C_{\text{gd\_saturation}} = WC_{OV} \tag{8}$$

$$C_{\text{gd\_off}} = WLC_{OV} \tag{9}$$

where W is the cascode transistor gate width; L is the gate effective length; C_{ov} is the drain–gate overlap capacitance;

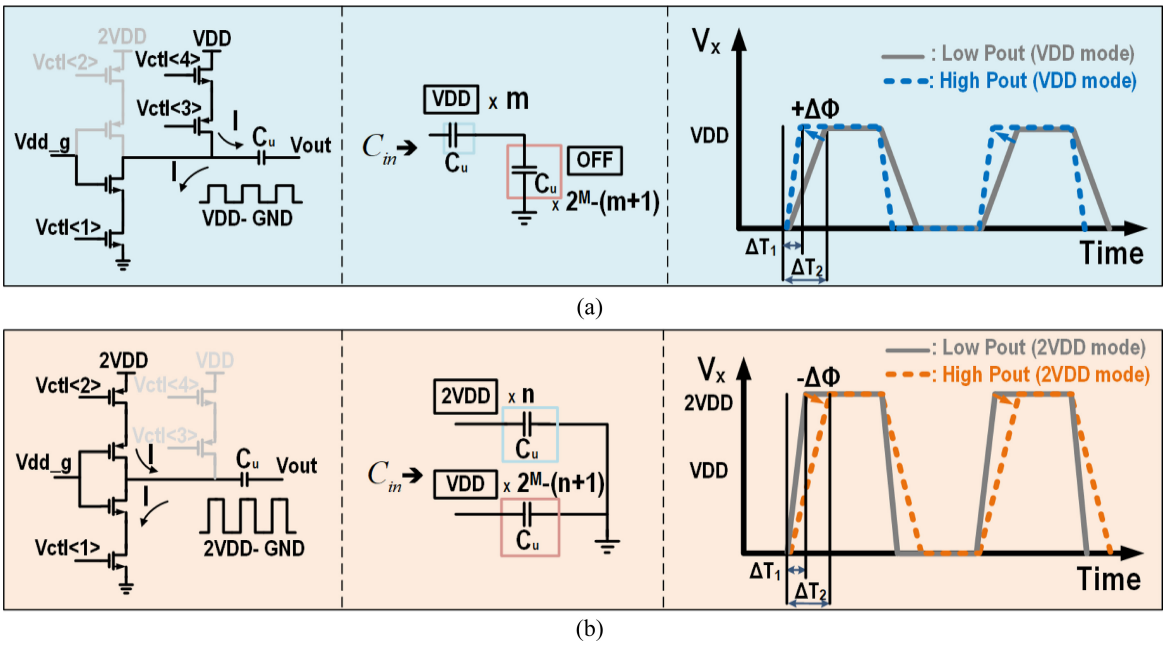


FIGURE 9. Class-G AM–PM distortion operation. (a) VDD mode. (b) 2VDD mode.

and C_{ox} is the gate-oxide capacitance. As more digital cells are turned on, the output voltage swing of V_{out} node increases. At this time, since the gate bias is fixed, as V_{out} increases, M_2 operates in the triode region for a longer period, which increases C_d. In addition, when the power cell is turned off, $C_d = C_{gd\_off}$, since C_{ds} is terminated with high impedance, providing low capacitance. In summary, as more cells are turned on in the conventional current-mode DPA, more cells operate in triode for longer periods, hence the total PA output capacitance increases as a function of output power. This modulated capacitance shifts the resonance frequency, which causes AM–PM distortion as shown in Fig. 5(c). As the output power increases, the AM–PM goes increasingly negative and we call it as lagging AM–PM [34].

To reduce the time period during the triode region, we use adaptive biasing on the cascode device. As more cells are turned on, the bias voltage is decreased as shown in Fig. 6(b). This operation shortens the interval in the triode region, which reduces the capacitance variation over output power. As shown in Fig. 7, employing adaptive biasing reduced the total AM–PM distortion from 11.3° to 6.7° at 2.4 GHz.

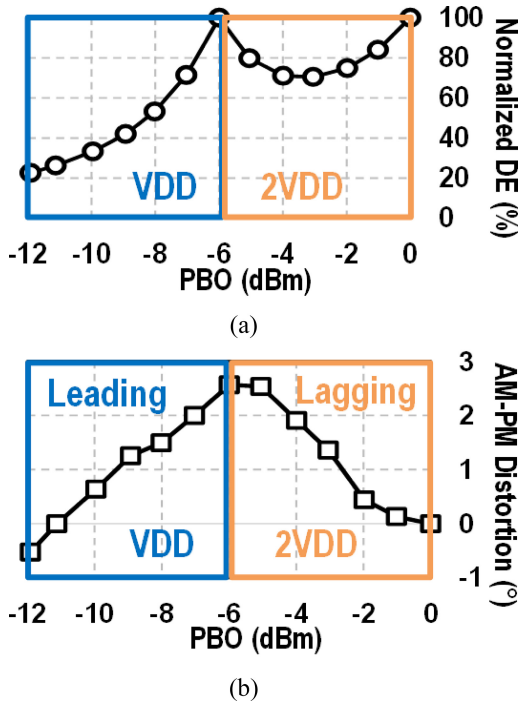


FIGURE 10. Simulated results of class-G about (a) DE and (b) AM–PM distortion.

B. VOLTAGE-MODE AM–PM COMPENSATION

In this section, we analyze and show the AM–PM distortion behavior of voltage-mode digital PA, conventional SCPA [26], and class-G [40]. As shown in Fig. 8, the conventional single-ended SCPA consists of an M-bit binary weighted unit cell and a bandpass matching network [26]. The output power level is determined according to the number of cells turned on by the AM code selected (m), whose bottom plates are switched between V_{DD} and GND at the carrier frequency. The capacitance of the unswitched cells $(2^M - (m+1)) \times C_u$ is shorted to ground, while the capacitance looking into the switched-on cells is $m \times C_u$. Hence, the equivalent capacitance (C_{out}) looking into the PA continues to be $(2^M - 1) \times C_u$ regardless of the number of cells turned ON. Hence, the inductance (L_{ind}) continues to resonate at the same frequency, and we can assume there is the same phase between V_x and V_{out}. On the other hand, the

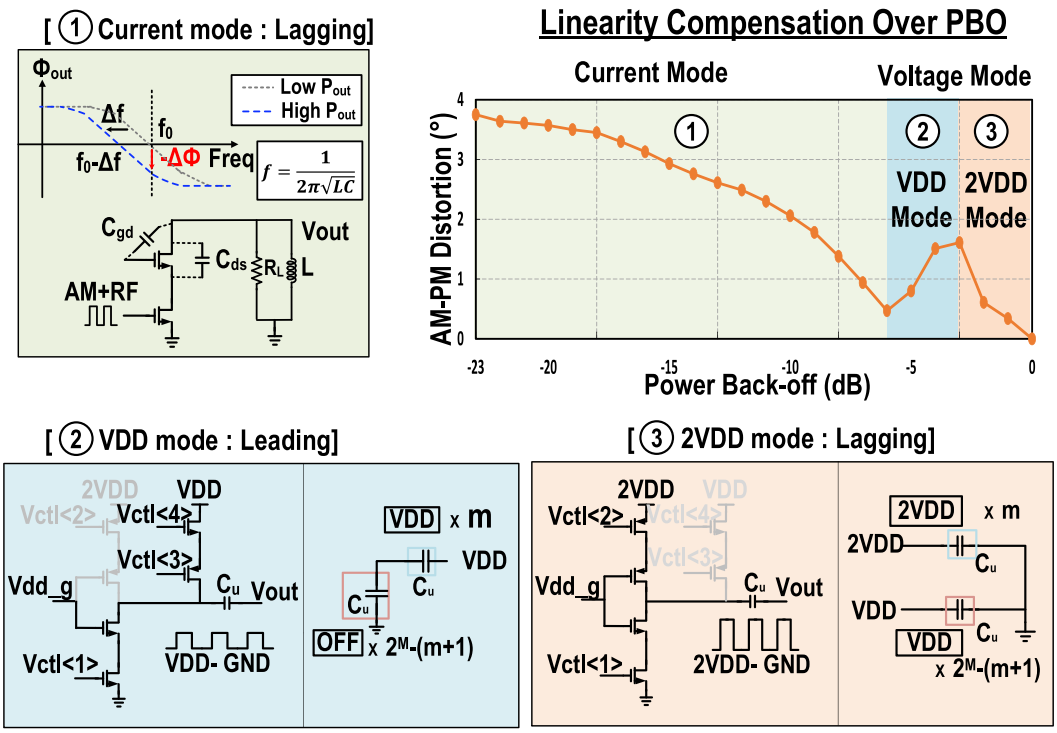


FIGURE 11. Simulated results of AM–PM distortion according to their operation region.

equivalent capacitance C_{in} observed by the PA cells changes as a function of the number of cells turned on as follows:

$$c_{\text{in}} = \frac{m(2^M - (1+m))}{2^M - 1} \times C_u \tag{10}$$

where M is the total number of bits of the SCPA, and m is the number of "ON" SCPA power cells. The charging/discharging time (Δt) of C_{in} can be expressed as follows:

$$\Delta t = C_{\text{in}} \times \frac{V_x}{mI} \tag{11}$$

where I is the current driving strength of the SCPA unit power cell. C_{in} is substituted in (11) and as a result, the transition charging/discharging time (Δt) at V_x can be further derived as [34]

$$\Delta t = C_u \times \left(1 - \frac{m}{2^M - 1}\right) \frac{V_{\text{DD}}}{I}. \tag{12}$$

As shown in this equation, the larger the number of unit cells (m) turned on, the shorter the transient time, corresponding to a positive frequency shift, and a corresponding leading behavior, which is inverse from the current-mode DPA AM–PM distortion. We can expand this concept to the class-G DPA. A voltage-mode amplifier can be represented as a capacitive divider, and Fig. 9 shows the VDD mode and 2VDD mode of class-G operation. In class-G VDD mode, AM–PM distortion demonstrates a leading behavior, the same as the conventional SCPA. However, when operating in the 2VDD mode, it can be expressed as a capacitive divider with two input sources as shown in Fig. 9(b) and it can be expressed by the following charging/discharging equation:

$$C_{\text{in}} = C_{\text{VDD}} + C_{\text{2VDD}} \tag{13}$$

$$\Delta t = C_u \times \left(\frac{2^M + n + 1}{2^M - 1}\right) \frac{V_{\text{DD}}}{I} \tag{14}$$

where n is the number of tuned on unit cells as 2VDD. As summarized in Fig. 9, for VDD mode, as the number of VDD cells (m) turned on increases, the charging/discharging time becomes shorter, which illustrates the leading AM–PM distortion behavior. However, in the case of the 2VDD mode, as the number of unit cells (n) transitioning from VDD to 2VDD is increased, the output power increases, the charging/discharging time becomes longer, and lagging AM–PM distortion behavior occurs. Looking at the simulation results of class-G operation, as shown in Fig. 10, the efficiency improves at 6-dB PBO thanks to class-G operation [40], and at the same time, the AM–PM distortion direction transitions from leading to lagging, and hence compensates itself. The magnitude of leading AM–PM distortion of the V-DPA can be manipulated by the driving strength of the SCPA power cells and the size of C_u, which is a direct tradeoff with the efficiency and output power [34].

C. AM–PM OPERATION OF PROPOSED ARCHITECTURE

The AM–PM nonlinearity as a function of the output power level is self-compensated by the proposed architecture. First, the AM–PM distortion of current-mode DPA has a lagging (negative) behavior according to output capacitance. However, it is mitigated by adaptive biasing. Second, as the

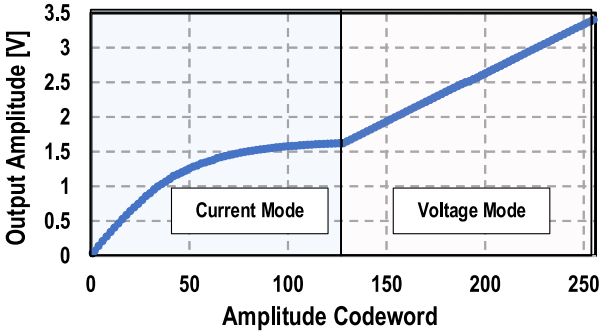


FIGURE 12. Simulated result of AM–AM response.

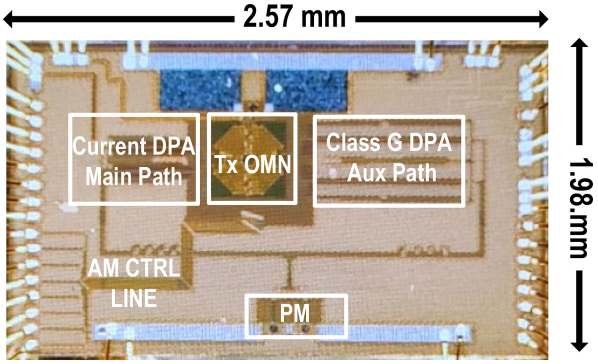
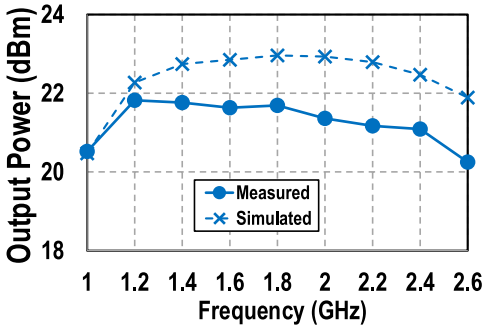
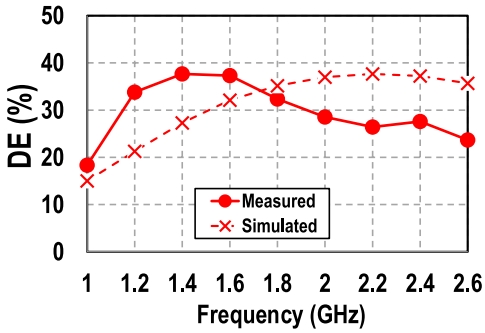


FIGURE 13. Chip microphotograph.



(a)



(b)

FIGURE 14. CW simulated and measurement results. (a) Output power. (b) DE according to frequency.

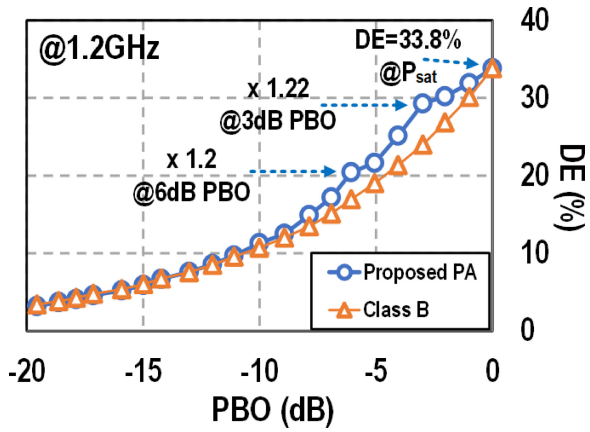


FIGURE 15. CW measurement DE results at 1.2 GHz.

DPA in the voltage-mode DPA is turned on in the VDD mode, the direction of AM–PM distortion is changed to the leading (positive) behavior, opposite to the previous current mode, which is a characteristic of the hybrid (current/voltage) operation. Third, the AM–PM distortion behavior changes its direction back to lagging as the cells in the Aux path change to the 2VDD mode. Fig. 11 illustrates the simulation results of the AM–PM distortion, and Fig. 12 shows the simulated results of the AM–AM response that changes as each mode is operated in the proposed architecture.

IV. MEASUREMENT RESULTS

A proof-of-concept hybrid polar Doherty DPA is implemented in the Globalfoundries 45-nm CMOS SOI process with a chip size of 2.57 mm × 1.98 mm, including all decoupling capacitors and electrostatic discharge (ESD) I/O pads (Fig. 13). This is a fully integrated DPA design with C-DPA and V-DPA power cells, adaptive bias, output passive network, and AM and PM drivers. The chip is mounted on an FR4 PCB board and wire-bonded to facilitate the probing-based testing. The dc supplies are 1.1 and 2.2 V for class-G operation.

We first characterize the DPA using continuous wave (CW) signals with a 50-Ω standard load. A single-ended PM signal is first converted by an off-chip balun (Krytar4010180) to generate the differential signals and fed to an input PM driver. The AM sequence is controlled using a USB-1024LS with a custom LabVIEW code. The amplified single-ended output signal is measured by an RF power meter (Keysight N1913A). Fig. 14 summarizes the CW measurement results. The measured Peak P_{out} is 21.8 dBm at 1.2 GHz and 1-dB BW is 1.2–2.4 GHz, which fractional BW of 66%. The peak DE is 37.8% at 1.4 GHz and DE is 33.8%/29.3%/20/4% for the peak/3 dB/6 dB/PBO at 1.2 GHz, which demonstrates 1.2×/1.22× PBO efficiency enhancement, compared to the ideal class-B as shown in Fig. 15.

The PA is then characterized with modulations. Desired complex modulation signals are synthesized in an advanced design system (ADS) and decomposed into their corresponding AM and PM signals for polar operation. The memoryless 1-D AM–AM lookup table (LUT) for each PA is made

TABLE 1. Comparison of state-of-the-art DPAs at GHz RF frequencies.

	This work	RFIC 2017 [36]	JSSC 2017 [24]	ISSCC 2018 [41]	JSSC 2020 [34]	VLSI 2021 [25]
Architecture	Hybrid Current/Voltage Mode Digitial Doherty PA	Current-Mode Digital Doherty PA	Polar Class-G VMD	Voltage-Mode Digital Doherty PA	Three-way Hybrid Current/Voltage mode Digital Doherty PA	Single-Core Inverse Class-D PA
Process [nm]	45	40	45	55	45	65
Number of Matching Networks	1	2	2	1	3	1
Passive Network Area [mm^2]	0.185	0.504*	-	0.166*	0.461	0.146*
Supply [V]	1.1 / 2.2	0.7	1.2/2.4	1.2/2.4	1.2	1.4
Frequency [GHz]	1.2	2.5	3.5	1.7	2.3	2
1dB RF BW [GHz]	1.2 - 2.4 (66%)	2.3 - 2.8 (21%)	2.9 - 4.3 (38%)	1.7 - 2 * (16%)	2.1 - 2.5 (17%)	-
Peak Power [dBm]	21.8	21.4	25.3	27	22.4	23.3
PEAK DE/PAE [%]	37.6	49.4	30.4 (PAE)	25.4 (PAE)	38.5	34.9
Number of η peaks	2	1	2	1	2	1
Modulation	64 QAM 20MHz	64 QAM 20MHz	1024 QAM 10MHz 32 Carrier	QPSK NB-IoT 180KHz	64 QAM 40MHz	64 QAM 10MHz
Avg. Power [dBm]	14.8	13.9	14.8	23*	15.3	16.7
Avg. efficiency [%]	22.8	24	18 (PAE)	17.9 (PAE)	24.7	25.2
EVM [dB]	-23.5	-30	-40.3	-21.6	-32	-28.5
DPD	No	Yes	Yes	No	No	Yes

*Estimate from figure

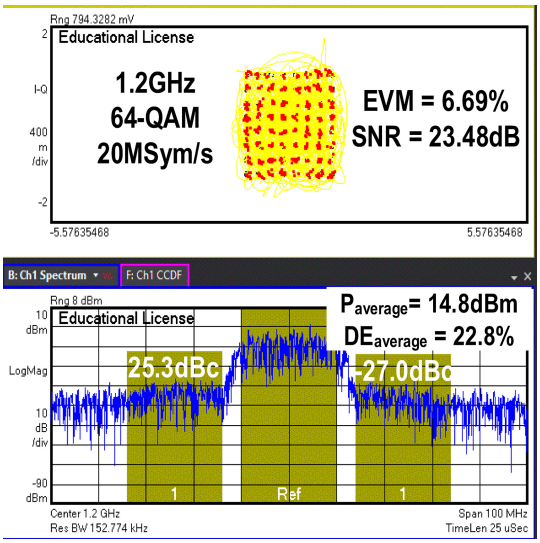


FIGURE 16. Modulation measurement with 20 Msys/s 64 QAM at 1.2 GHz.

based on the characterized CW test, and a pattern generator (Keysight 16822A) generated the 8-bit AM control LUT. The PM signals are generated by the arbitrary waveform generator (AWG) (Tektronix AWG7002A). Since the timing alignment between AM path and PM path is very critical for the modulation performance [45], we use a pulse function generator (Agilent 81160A) to generate the trigger pulses for AWG and pattern generator to synchronize the AM and PM signal with a fine control delay. The output signals from the PA are demodulated by a real-time oscilloscope (Keysight MSO840A).

Fig. 16 shows the demodulated 20-MSym/s single-carrier 64-QAM signal at 1.2 GHz without any phase predistortion. It achieves 14.8-dBm average P_{out} and 22.8% average DE, 23.48-dB EVM and −25.36-dBc ACLR. Table 1 shows the comparison of the proposed hybrid single transformer with state-of-the-art RF CMOS digital PAs. This proposed the single-transformer footprint hybrid current–voltage digital Doherty PA achieves broadband operation compared to the state of the art.

V. CONCLUSION

This article presents a compact broadband hybrid current-/voltage-mode digital Doherty PA with a single three-coil transformer as its output network and built-in large-single AM–PM distortion compensation, which is capable of supporting large-PAPR high-speed modulation signals without any phase predistortion. An adaptive biasing scheme is proposed to minimize the current-mode DPA's inherent AM–PM nonlinearity. Class-G operation within the voltage-mode PA is introduced to achieve efficiency enhancement and AM–PM nonlinearity reduction. A current-/voltage-mode DPA architecture is proposed to support AM–PM cancelation, removal of unnecessary switches, and support load modulation within a single-transformer network.

REFERENCES

[1] S.-W. Yoo, S.-C. Hung, and S.-M. Yoo, "A watt-level quadrature class-G switched-capacitor power amplifier with linearization techniques," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1274–1287, May 2019.

[2] Y. Li et al., "A 15-bit quadrature digital power amplifier with transformer-based complex-domain efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1610–1622, Jun. 2022.

[3] A. Zhang and M. S.-W. Chen, "A subharmonic switching digital power amplifier for power back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1017–1028, Apr. 2019.

[4] F. Wang, T.-W. Li, S. Hu, and H. Wang, "A super-resolution mixed-signal Doherty power amplifier for simultaneous linearity and efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3421–3436, Dec. 2019.

[5] Y. Yin et al., "A broadband switched-transformer digital power amplifier for deep back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2997–3008, Nov. 2020.

[6] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.

[7] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng.*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[8] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[9] Y. Cho, K. Moon, B. Park, J. Kim, and B. Kim, "Voltage-combined CMOS Doherty power amplifier based on transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3612–3622, Nov. 2016.

[10] S. Li, T. Chi, J.-S. Park, H. T. Nguyen, and H. Wang, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1243–1253, May 2019.
[11] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 6, pp. 2129–2138, Jun. 2005.
[12] Z. Hu, L. C. de Vreede, M. S. Alavi, D. A. Calvillo-Cortes, R. B. Staszewski, and S. He, "A 5.9 GHz RFDAC-based outphasing power amplifier in 40-nm CMOS with 49% efficiency and 22.2 dBm power," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2016, pp. 206–209.
[13] F. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. 33, no. 10, pp. 1094–1099, Oct. 1985.
[14] E. McCune, *Dynamic Power Supply Transmitters: Envelope Tracking, Direct Polar, and Hybrid Combinations*. Cambridge, U.K.: Cambridge Univ. Press, 2015.
[15] Z. Popovic, "Amping up the PA for 5G: Efficient GaN power amplifiers with dynamic supplies," *IEEE Microw. Mag.*, vol. 18, no. 3, pp. 137–149, May 2017.
[16] W. Tai et al., "A transformer-combined 31.5 dBm outphasing power amplifier in 45 nm LP CMOS with dynamic power control for back-off power efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1646–1658, Jul. 2012.
[17] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and B. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1787–1795, Jul. 2011.
[18] H. Wang et al., "A highly-efficient multi-band multi-mode all-digital quadrature transmitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1321–1330, May 2014.
[19] A. Azam, Z. Bai, and J. S. Walling, "Leveraging programmable capacitor arrays for frequency-tunable digital power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 6, pp. 1983–1994, Jun. 2020.
[20] Z. Bai, W. Yuan, A. Azam, and J. S. Walling, "Multiphase interpolating digital power amplifiers for TX beamforming," *Chips*, vol. 1, no. 1, pp. 30–50, 2022.
[21] A. Zhang, C. Yang, M. Ayesh, and M. S.-W. Chen, "26.6 A 5-to-6GHz current-mode subharmonic switching digital power amplifier for enhancing power back-off efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 364–366.
[22] J. Lee, D. Jung, D. Munzer, and H. Wang, "A compact CMOS broadband bidirectional digital transceiver frontend with capacitor bank and transformer matching network reuse," *IEEE Access*, vol. 10, pp. 117093–117104, 2022.
[23] Z. Bai, A. Azam, D. Johnson, W. Yuan, and J. S. Walling, "Split-array, C-2C switched-capacitor power amplifiers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1666–1677, Jun. 2018.
[24] V. Vorapipat, C. S. Levy, and P. M. AsbeckIEEE, "A class-G voltage-mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, Dec. 2017.
[25] K.-S. Choi, J. Ko, and S.-G. Lee, "A single-supply single-core inverse class-D digital power amplifier with enhanced power back-off efficiency adopting output power scaling technique," in *Proc. Symp. VLSI Circuits*, 2021, pp. 1–2.
[26] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
[27] D. Chowdhury, S. V. Thyagarajan, L. Ye, E. Alon, and A. M. Niknejad, "A fully-integrated efficient CMOS inverse class-D power amplifier for digital polar transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1113–1122, May 2012.
[28] H. Kobayashi, J. M. Hinrichs, and P. M. Asbeck, "Current-mode class-D power amplifiers for high-efficiency RF applications," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2480–2485, Dec. 2001.
[29] S. Hu, S. Kousai, and H. Wang, "2.8 A broadband CMOS digital power amplifier with hybrid class-G Doherty efficiency enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 1–3.
[30] J. S. Park, Y. Wang, S. Pellerano, C. Hull, and H. Wang, "A CMOS wideband current-mode digital polar power amplifier with built-in AM–PM distortion self-compensation," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 340–356, Feb. 2018.
[31] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. S. Walling, "A quadrature switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1200–1209, May 2016.
[32] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "Voltage mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1295–1304, May 2017.
[33] W. Yuan and J. S. Walling, "A multiphase switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1320–1330, May 2017.
[34] D. Jung, S. Li, J.-S. Park, T.-Y. Huang, H. Zhao, and H. Wang, "A CMOS 1.2-V hybrid current-and voltage-mode three-way digital Doherty PA with built-in phase nonlinearity compensation," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 525–535, Mar. 2020.
[35] B. Yang, H. J. Qian, and X. Luo, "Quadrature switched/floated capacitor power amplifier with reconfigurable self-coupling canceling transformer for deep back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3715–3727, Dec. 2021.
[36] Y. Shen et al., "A fully-integrated digital-intensive polar Doherty transmitter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2017, pp. 196–199.
[37] A. Zhang and M. S.-W. Chen, "A watt-level phase-interleaved multi-subharmonic switching digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3452–3465, Dec. 2019.
[38] E. Zenteno, M. Isaksson, and P. Händel, "Output impedance mismatch effects on the linearity performance of digitally predistorted power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 754–765, Feb. 2015.
[39] J. Lee, D. Jung, D. Munzer, and H. Wang, "A compact single transformer footprint hybrid current–voltage digital Doherty power amplifier," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2022, pp. 247–250.
[40] S.-M. Yoo et al., "A class-G switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1212–1224, May 2013.
[41] Y. Yin, L. Xiong, Y. Zhu, B. Chen, H. Min, and H. Xu, "A compact dual-band digital polar Doherty power amplifier using parallel-combining transformer," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1575–1585, Jun. 2019.
[42] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, Dec. 2017.
[43] B. Razavi and R. Behzad, *RF Microelectronics*. New York, NY, USA: Prentice Hall, 2012.
[44] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2005.
[45] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.

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