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Synergistic Distributed Thermal Regulation for On-CMOS High-Throughput Multimodal Amperometric DNA-Array Analysis

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(Invited Paper)

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ABSTRACT Accurate temperature regulation is critical for amperometric DNA analysis to achieve high fidelity, reliability, and throughput. In this work, a 9 × 6 cell array of mixed-signal CMOS distributed temperature regulators for on-CMOS multimodal amperometric DNA analysis is presented. Three DNA analysis methods are supported, including constant potential amperometry (CPA), cyclic voltammetry (CV), and impedance spectroscopy (IS). In-cell heating and temperature-sensing elements are implemented in standard CMOS technology without post-processing. Using proportional–integral–derivative (PID) control, the local temperature can be regulated to within ±0.5 °C of any desired value between 20 °C and 90 °C. To allow the in-cell integration of independent PID control, a new mixed-signal design is proposed, where the two computationally intensive operations in the PID algorithm, multiplication and subtraction, are performed by an in-cell dual-slope multiplying ADC, resulting in a small area and low power consumption. Over 95% of the circuit blocks are synergistically shared among the four operating modes, including CPA, CV, IS, and the proposed temperature regulation mode. A 3 mm × 3 mm CMOS prototype fabricated in a 0.13-μm CMOS technology has been fully experimentally characterized. The proposed distributed temperature regulation design and the mixed-signal PID implementation can be applied to a wide range of sensory and other applications.

INDEX TERMS Circuit sharing, mixed-signal IC, on-CMOS DNA analysis, proportional–integral–derivative (PID) control, temperature regulation.

I. INTRODUCTION

CONVENTIONAL optical DNA analysis methods typically require sample flushing, and thus they cannot be implemented in real time [1]. Amperometric electrochemical DNA analysis is performed with in situ samples, and therefore supports real-time operation [2]. Recently, several CMOS system-on-chip (SoC) designs for amperometric electrochemical DNA analysis have been developed [3], [4], [5], [6], [7], [8], [9], [10]. On-CMOS DNA array-based analysis also allows for advantageous high-density, low-noise, and low-cost monolithic integration of various modules for sensing, signal processing, communication, and power management.

Fig. 1 illustrates the operating principle of three most common amperometric DNA analysis methods. As depicted in Fig. 1(a), the surface of the working electrode (WE) is functionalized with probe DNA [3]. The hybridization of the probe DNA with the target DNA alters the surface properties of the WE, such as the impedance or the surface charges. As shown in Fig. 1(b), a voltage is then applied between the

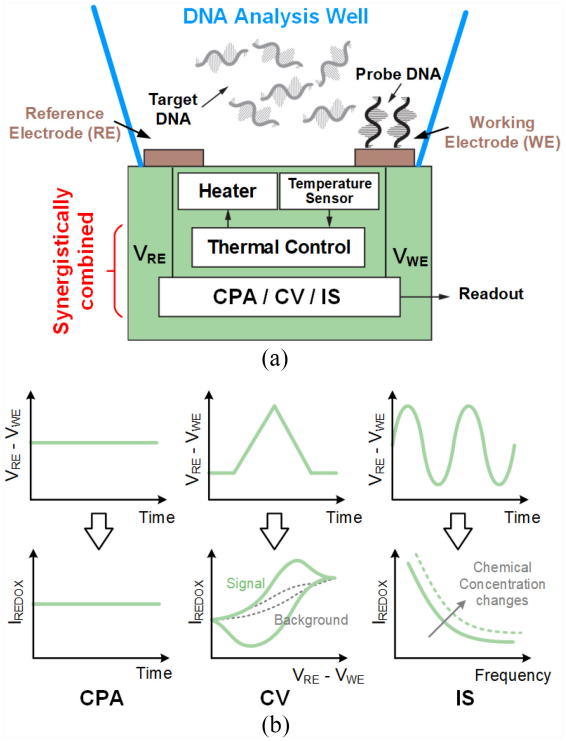


FIGURE 1. **(a) Conceptual block diagram of one channel of the temperature-regulated amperometric DNA analysis array. (b) Illustration of the basic operations of the three amperometric DNA analysis modes supported in this work: CPA, CV, and IS.**

reference electrode (RE) and the WE. The voltage waveform is set to be a constant voltage in order to implement constant potential amperometry (CPA), a bidirectional ramp to implement cyclic voltammetry (CV), and a sinusoid to implement impedance spectroscopy (IS). The surface property variation will result in a change of the read out redox current waveform that indicates the kinetics and thermodynamics of the chemical reactions and is used to identify if the unknown target DNA matches the known probe DNA [11]. Temperature of the sample is typically monitored and controlled near the sensor location.

Temperature is a key control parameter in all DNA analysis methods. Studies have shown that DNA hybridization is highly dependent on the temperature [12], [13], [14]. For a temperature increase of 10 °C, the redox current will drop by approximately 10% [14]. Additionally, time-varying temperature control in the range of 20 °C–90 °C is required for DNA multiplication through polymerase chain reaction (PCR). Therefore, a temperature regulation system is of great benefit for DNA sensing applications. In practice, on-chip peripheral CMOS processing modules often cause temperature variation across a DNA analysis array and do not scale well to large arrays. Thus, distributed in-channel temperature sensing and regulation are necessary. In addition, a channel-level thermal regulation scheme allows for the generation of spatial temperature gradients for advanced nonuniform DNA analysis [15], [16].

Several temperature regulation designs for chemical sensing applications have been reported [4], [6], [7], [8], [17], [18], [19]. These designs typically use resistive heating and sensing elements. The work in [17] presents a temperature sensing and regulation microsystem for biological applications that achieves a single fixed temperature of 37 °C on the backside of the chip, with an off-chip digital proportional–integral–derivative (PID) controller. The work in [18] presents a 3×3 microhotplate array for a protein-sensing application. In that design, the temperature of the chip is regulated up to 45 °C with an off-chip digital PID controller. The work in [4] presents a 16-channel, frequency-shift CMOS magnetic biosensor array for a protein-sensing application. This design consists of an array of in-channel heaters, with a single temperature sensor and an off-chip analog PID controller. The work in [19] presents a digital CMOS microhotplate array architecture for a gas-sensing application. The array consists of 3×3 gas-sensing sites. Each site consists of a heater, a temperature sensor, and a delta–sigma-modulated PID controller. The microhotplate achieves an operating temperature of up to 350 °C. A 40-channel DNA analysis SoC based on ISFET sensors for rapid point-of-care DNA detection is reported in [5]. This design includes in-channel heaters, temperature-sensing elements, and a dedicated ADC. A fully digital on-chip PID controller is utilized for temperature regulation at the cost of area and power. In summary, most existing closed-loop temperature regulation microsystems use off-chip controllers, with few exceptions [5], [7]. Conventional on-chip controller designs often require a large silicon area along with high power consumption, which can be prohibitive for most on-chip electrochemical sensing applications.

In this work, we present a compact, distributed temperature regulator design implemented in 0.13-μm standard CMOS technology. Fig. 1(a) illustrates the high-level block diagram of the proposed temperature-regulated electrochemical cell. It consists of a temperature sensor, a heater, a closed-loop regulator, a WE, an RE, and a potentiostat. We chose the PID algorithm for the closed-loop regulation because of its high efficacy in temperature control systems [20], [21]. PID controllers have been implemented on-chip but at the cost of large silicon area [22], [23] or have limited operational range and programmability [24], [25]. Here, we introduced a new design using mixed-signal circuits that yield a compact integration with low power dissipation. This design permits distributed temperature regulation in large-scale parallel DNA array sensing applications.

The presented temperature controller is a part of a highly integrated multifunctional SoC that performs on-chip amperometric electrochemical DNA analysis. The overall SoC consists of 54 sensing channels which share 600 on-chip gold microelectrodes. It performs label-free DNA analysis and pH sensing for applications, such as prostate cancer detection. In the design, we synergistically share the circuits among different operation modes to achieve high integration and low resource overhead. This work builds on our previous brief

(two-page) report on DNA sensing and temperature control circuits that can be integrated together with low resource overhead [26]. We also previously reported on the CV DNA sensing modality independently, on its own, when utilized with nano-structured gold electrodes grown directly on CMOS in [27]. The impedance modality low-power implementation was explored by us also independently, on its own, with a focus on implementing energy-efficient frequency-response analysis (FRA) computation in [28] and [29]. Key low-noise current-acquisition circuit design techniques, such as transimpedance amplifier and current conveyor (CC) using chopping stabilization, have been compared in [31] and [32] and are omitted from the material presented herein.

In this article, we present a unified review of how all of these sensing modalities and thermal regulation are implemented on the same IC with minimal resource overhead and focus on presenting the details of the distributed mixed-signal temperature regulator, including the system architecture, algorithm design, circuit implementation, and experimental results. The key contributions of this article include the following.

1) We present the first distributed temperature regulation design with on-chip PID control for individual DNA array cells. The distributed thermal regulation permits accurate temperature control across a large DNA analysis array and potentially enables the generation of advanced spatial profiles of temperature gradients. This is important for the three sensory modalities we implemented (i.e., CPA, CA, and IS) and are required not only by DNA analysis but also used in a wide range of applications, including lab-on-chip designs and implantable medical devices (e.g., a retinal prosthesis array). For example, such arbitrary programmable spatial thermal profiles enable the implementation of different DNA analysis protocols in different on-chip wells at the same time.
2) We offer a unified overview and experimental results for all methods needed for versatile on-chip DNA analysis (CPA, CA, IS, and thermal regulation), which is expanded beyond the initial coverage in [26], demonstrating only a very small 5% area overhead when the same mixed-signal circuits are synergistically reused for all four modes.
3) We have developed a new way of implementing PID control synergistically reusing mixed-signal circuits [e.g., multiplying ADC (MADC)], which avoids the computationally intensive multiplications of the PID algorithm in the digital domain, rendering compact silicon area and low power consumption.
4) We implemented a compact temperature sensor design where the currents proportional and complementary to temperature are directly used as the reference and input to the dual-slope MADC, which allows us to minimize the silicon area (95% of the in-cell circuits are reused between different modes).
5) We conducted a comprehensive characterization of the developed temperature regulation system, reported the experimental results, and compared it with the state-of-the-art designs.

The remainder of this article is organized as follows. Section II overviews the multimodal DNA analysis SoC. Section III provides background on temperature regulation principles. Section IV presents the VLSI architecture of the temperature controller. Section V details the circuit implementation. Section VI shows the experimental results obtained from the fabricated 0.13-μm CMOS prototype. Finally, Section VII concludes this article.

II. MULTIMODAL DNA ANALYSIS SOC WITH SYNERGISTIC CIRCUIT SHARING

Fig. 2 shows an overview of the presented multimodal DNA analysis SoC, which can be configured to perform CPA (Fig. 2(a) [26]), CV (Fig. 2(b) [27]), IS (Fig. 2(c) [29]), and temperature regulation [Fig. 2(d)].

The SoC includes a 9×6 array of low-power low-noise sensory circuit cells, a programmable waveform generator, on-chip SRAM memories, a shared digital pulse-width modulator (PWM), an all-digital ultrawideband (UWB) transmitter, and on-chip biasing and clock generation circuits. Each sensory cell includes a current-to-digital conversion channel, an array of: DNA sensors, a pH sensor, several BJTs to generate the complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) currents, and a heater for temperature regulation. Each cell also integrates a bias voltage generator, clock generation circuitry, and SRAM memory that can be programmed individually.

Each current-to-digital conversion channel consists of a CC and a dual-slope MADC. The dual-slope MADC multiplies the sensor's response with a set of digital coefficients and outputs the corresponding digital result. The digital output of each channel is serialized on the chip and then wirelessly transmitted using the all-digital UWB transmitter [27].

The SoC reuses a number of the same blocks (denoted by bold outlines and light green color in Fig. 2) in different configurations. The circuit-sharing design yields a significant saving in the integration area. Specifically, the circuits that occupy 95% of the in-cell area are shared with other modes of operation. For completeness, all key functionalities of the SoC are summarized in this section.

A. CONSTANT POTENTIAL AMPEROMETRY MODE

Fig. 2(a) shows the functional blocks for pH sensing using CPA analysis [30]. Sensing pH is required as a part of DNA analysis. The in-channel pH sensor is implemented by a floating-gate PFET, with the gate connected to the top metal layer in order to form a floating-gate electrode. The CMOS passivation layer is used as the pH-sensitive membrane, which gives a linear pH response with a sensitivity of about 56 mV/pH, depending on the stoichiometry. The pH sensors are directly interfaced to the current-recording

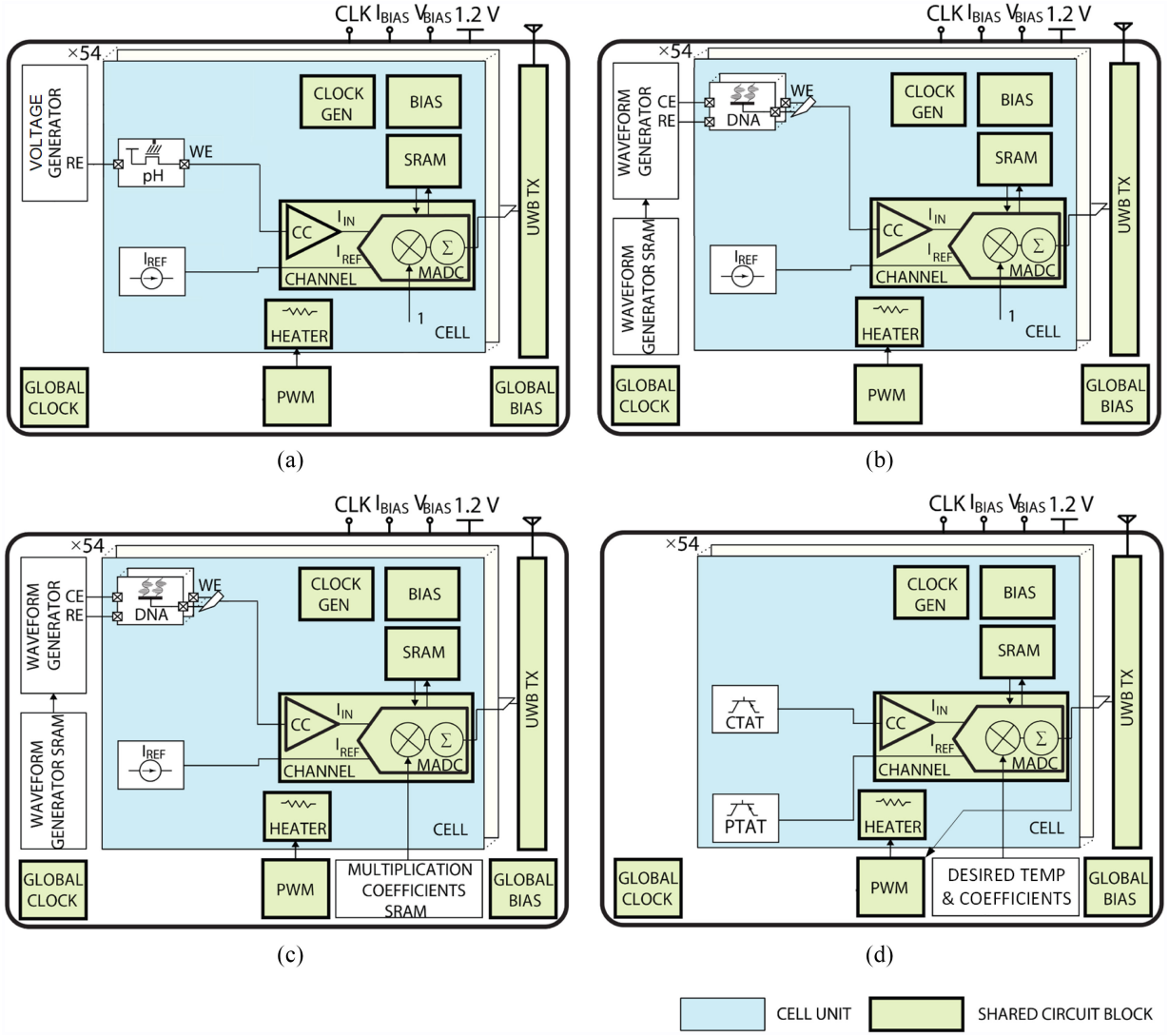


FIGURE 2. **Four modes of operation of the proposed multimodal DNA analysis SoC. (a) CPA configuration [26], (b) CV configuration [27], (c) IS configuration [29], and (d) temperature regulation configuration (the focus of this work). The blocks with a thick outline and highlighted in light green are synergistically shared in all modes, with over 95% of all areas reused in each operating mode.**

channels, with the gate voltage set by the on-chip RE. In this configuration, both Vgs and Vds of the pH sensors are fixed. Changes in the pH level will affect the pMOS threshold voltage, resulting in the changes in the drain current, which is digitized by the recording channel. For the detailed circuit implementation, please refer to our previous publication in [26]. In this mode, the cell temperature needs to be held at a constant value within ±0.5 °C.

B. CYCLIC VOLTAMMETRY MODE

Fig. 2(b) shows the functional blocks for CV analysis. In this mode, each channel is multiplexed among a bank of in-cell DNA sensors. The sensors are interrogated by the on-chip programmable waveform generator that is time-shared among all cells. The digital data representing the stimulation waveform properties are stored in the on-chip SRAM. The current-to-digital channel quantizes the input current and outputs the corresponding digital result. No computation is required in this case and the MADC digital multiplication coefficient is set to 1. For the detailed circuit implementation, please refer to our previous publication in [27]. In this mode, the cell temperature is required to be held at a constant value within ±0.5 °C.

C. IMPEDANCE SPECTROSCOPY MODE

Fig. 2(c) shows the functional blocks for IS analysis. In this mode, a frequency response analysis (FRA) algorithm is used to extract the real and imaginary components of the biosensor impedance [29]. The computationally intensive operations required by the FRA algorithm are performed by the in-channel MADC in the mixed-signal domain. The waveform generator produces a variable-frequency sinusoidal interrogation waveform for driving the RE, and the front-end current amplifier acquires the DNA sensor's response. The

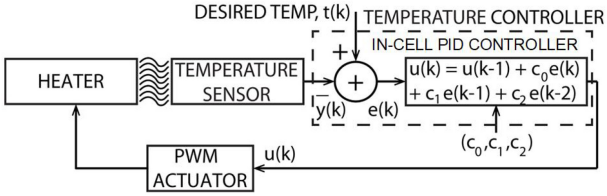


FIGURE 3. Block diagram of the PID control of the temperature regulation loop.

MADC multiplies the sensor's response with a set of digital FRA algorithm coefficients (stored in the multiplication coefficient SRAM). Next, the MADC accumulates the results over one period of the interrogation signal (integration) for extracting the impedance. For the detailed circuit implementation, please refer to our previous publication in [29]. In this mode, the cell temperature is also required to be held constant within ±0.5 °C.

D. TEMPERATURE REGULATION MODE

It is clear that each of the three sensory modes requires accurate temperature control. In order to support this, we have developed a new low-power low-area-overhead circuit for in-cell PID-based thermal control, which is the main focus of this article. Fig. 2(d) shows its functional blocks. In this mode, the SoC utilizes the same current-to-digital channels to measure temperature. The on-chip PID controller is used to regulate each cell's temperature and updates it in a time-multiplexed fashion. On-chip SRAMs are utilized to store PID coefficients and multiplication coefficients. The channel measures temperature by taking the ratio of a CTAT to PTAT currents as described in Sections III and IV. The measured temperature is fed to the on-chip PID controller. The PID controller regulates the 2-D chip temperature profile by modulating the in-cell heaters. The multiplication and subtraction operations required by the PID algorithm are performed by the in-channel MADC in the mixed-signal domain, yielding a small silicon area and low power consumption.

III. TEMPERATURE CONTROL PRINCIPLES

A. TEMPERATURE REGULATION

The block diagram of the temperature regulation loop is shown in Fig. 3. It consists of a heater, a temperature sensor, a PID controller, and an actuator. The actuator uses digital PWM for controlling the heater.

The continuous-time representation of a PID controller is given by

$$u(t) = K_p e(t) + K_i \int_0^t e(t)dt + K_d \frac{d}{dt} e(t) \tag{1}$$

where K_p is the proportional gain, K_i is the integral gain, K_d is the derivative gain, $e(t)$ is the error value, and $u(t)$ is the actuation value. A discrete-time representation of (1) in Z-domain is given by

$$D(z) = \frac{u(z)}{e(z)} = K_p + K_i \frac{T_s}{2} \frac{z+1}{z-1} + \frac{K_d}{T_s} \frac{z-1}{z} \tag{2}$$

where T_s is the sampling period. Equation (2) can be implemented numerically as follows:

$$u(k) = u(k-1) + c_0 e(k) + c_1 e(k-1) + c_2 e(k-2) \tag{3}$$

where k is the discrete time index, and c_0, c_1, and c_2 are the PID control coefficients.

During the operation, the PID controller calculates the error value $e(k)$ and attempts to minimize it by adjusting $u(k)$, which sets the PWM duty cycle of the actuator.

B. TEMPERATURE SENSING

Temperature can be measured by taking the ratio of two signals that are linearly dependent on it. In CMOS technologies, these signals can be derived from the base–emitter voltage of substrate pnp transistors [33]. These transistors use the p-substrate as the collector, the p^+-diffusion as the emitter, and an N-well as the base. Fig. 4(a) shows the generation of two linearly temperature-dependent signals. One is generated from the base–emitter voltage (V_{BE}) of a single pnp transistor, the other is generated from the difference between the base–emitter voltages (ΔV_{BE}) of two pnp transistors biased at different collector current levels.

The temperature dependence of the V_{BE} can be derived from the exponential relation between the collector current I_C and the base–emitter voltage as follows:

$$\begin{aligned} V_{BE}(T) = {} & V_{g0}\left(1 - \frac{T}{T_r}\right) + \frac{T}{T_r} V_{BE} T_r \\ & - n\frac{KT}{q} \ln \frac{T}{T_r} + \frac{KT}{q} \ln \frac{I_C T}{I_C T_r} \end{aligned} \tag{4}$$

where V_{g0} is the extrapolated bandgap voltage at 0 K, n is a process-dependent constant, K is a Boltzmann constant, q is the electron charge, and T_r is an arbitrary reference temperature [34]. As illustrated in Fig. 4(b), V_{BE} is CTAT with a typical slope of 2 mV/K. The nonlinearity is represented by the last two terms of (4), which is negligible in the temperature range of 20 °C to 90 °C required by DNA analysis.

The slope of the base–emitter voltage depends on the absolute value of the collector current. This dependence can be used to generate a voltage that is PTAT. The difference between the base–emitter voltages of two pnp transistors biased at two different collector currents can be expressed as follows:

$$\begin{aligned} \Delta V_{BE}(T) &= V_{BE2}(T) - V_{BE1}(T) \\ &= \frac{KT}{q} \ln \left(\frac{I_{C2}}{I_{C1}}\right) \end{aligned} \tag{5}$$

where I_{C1} and I_{C2} are the collector currents of the two pnp transistors.

Conventional temperature sensors measure the ratio of the PTAT signal to a temperature-independent reference signal. The temperature-independent reference signal can be generated by adding V_{BE} to a scaled version of ΔV_{BE} [33], [34], [35], [36], [37]. The scaling factor α is

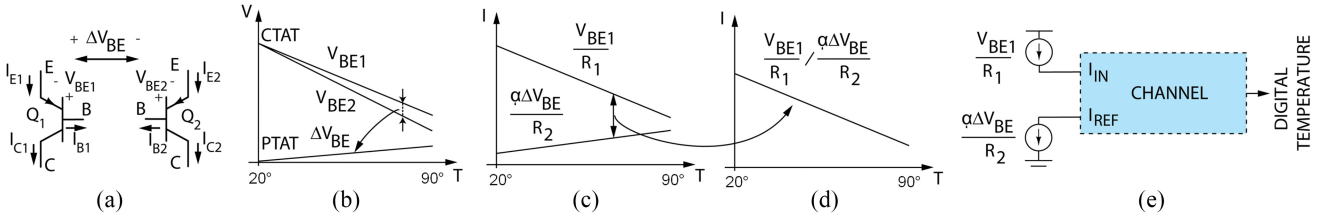


FIGURE 4. (a) Pair of BJTs for generating ΔV_{BE} and V_{BE}, (b) temperature dependence of the base–emitter voltage, (c) generation of PTAT and CTAT current, (d) conceptual plot of the proposed temperature-dependent current generation, and (e) utilization of a current-to-digital channel for temperature measurements.

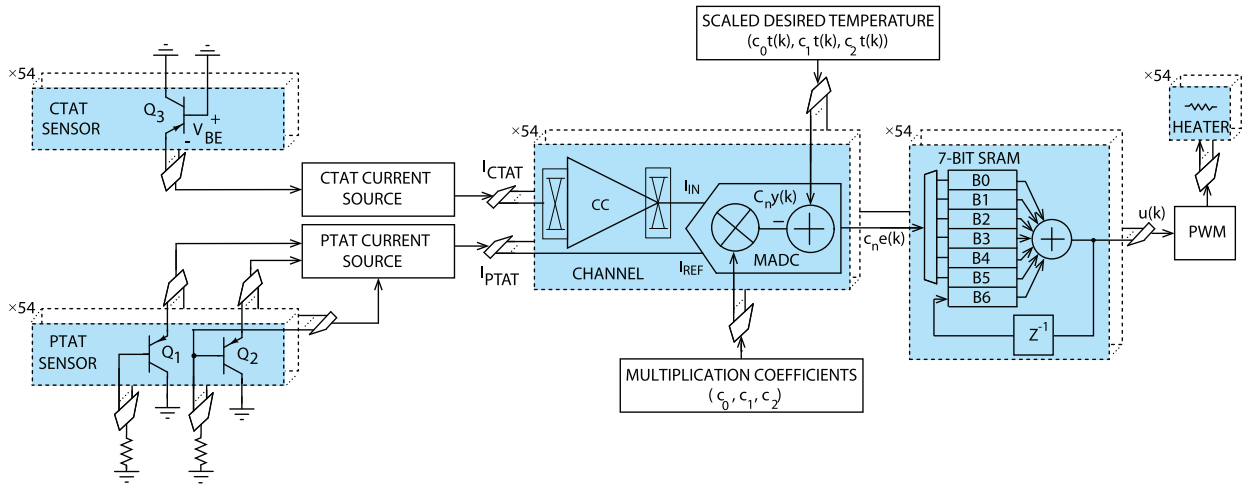


FIGURE 5. Top-level VLSI architecture of temperature regulation loop (shaded boxes are in-cell).

used to match the temperature dependence (with an opposite sign) of V_{BE} and ΔV_{BE}. However, the generation of the temperature-independent reference signal adds complexity to the circuit implementation, which is not suitable for a channel-level implementation. Although distributing a global temperature-independent signal is feasible, it places challenges in the signal routing if a voltage signal is used and requires accurate matching or time multiplexing if a current signal is used. In this work, we eliminate these issues by directly taking the ratio of PTAT and CTAT signals, which have an approximately linear relationship with temperature within the range of 20 °C–90 °C. The PTAT and CTAT voltages are converted to currents using resistors R_1 and R_2. $\alpha\Delta V_{BE}/R_2$ is used as the reference to the dual-slope MADC and V_{BE}/R_1 is used as the input signal, as illustrated in Fig. 4(e). As a result, the dual-slope MADC inherently digitizes the ratio of $\alpha\Delta V_{BE}/R_2$ to V_{BE}/R_1 [27]. The digitized output number represents the temperature. The factor α and the resistance R_1 and R_2 are set such that both the input and the reference currents utilize the full dynamic range of the channel over the operating temperature range.

IV. VLSI ARCHITECTURE

The top-level VLSI architecture of the temperature regulation loop is shown in Fig. 5. The regulation loop consists of CTAT and PTAT BJTs, PTAT and CTAT current sources, a current-to-digital channel, a 7-bit SRAM bank with an adder, a 12-bit digital PWM, and an in-cell heater. The in-cell BJTs are interfaced sequentially to the current sources that generate I_{PTAT} and I_{CTAT}. I_{CTAT} is used as the input to the channel, and I_{PTAT} is used as the reference current. The channel determines the ratio of I_{CTAT} to I_{PTAT}. Both currents are scaled such that their magnitude fits within the channel dynamic range over the operating temperature range. The ratio of I_{CTAT} to I_{PTAT} results in a linear transfer characteristic (versus temperature) [33]. The channel dual-slope MADC performs three tasks. First, it computes the ratio of I_{CTAT} to I_{PTAT}. Next, it multiplies this ratio by the PID coefficients (c_0, c_1, and c_2), and finally it subtracts the results from the scaled version of the desired temperature [$c_0t(k)$, $c_1t(k)$, and $c_2t(k)$]. The result of these three operations is the computation of $c_ne(k)$, as shown in Fig. 5. Next, these values are stored in the on-chip 7-bit SRAM bank. An on-chip adder adds the appropriate values according to (3) and computes $u(k)$, which sets the duty cycle of the signal generated by the digital PWM. The duty cycle of this signal sets the amount of time that the in-cell heater is on, thus regulating the temperature. The in-cell heater was implemented by a pMOS transistor with a width and length of 100 and 0.13 μm, respectively, and a 15-Ω load.

The timing diagram of the PID regulation loop is shown in Fig. 6. The channel dual-slope MADC performs three conversion cycles during one cycle of the PID controller, thus eliminating the need for three parallel ADCs. As shown

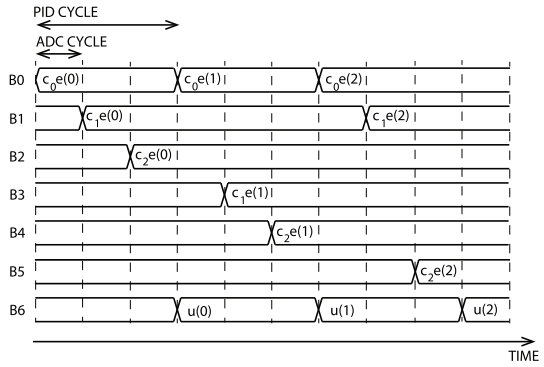


FIGURE 6. Timing diagram of the temperature regulation loop.

in Fig. 6, in the first conversion cycle of the PID controller, the ADC computes $c_0e(0)$, $c_1e(0)$, and $c_2e(0)$. Next, $u(0)$ is calculated from these values, and the duty cycle of the digital PWM is set accordingly. Consecutive values of $c_0e(n)$, $c_1e(n)$, $c_2e(n)$, and $u(n)$ are generated in the same manner.

V. CIRCUIT IMPLEMENTATION

A. CURRENT-TO-DIGITAL CONVERSION CHANNEL

The top-level VLSI architecture of the current-to-digital conversion channel is shown in Fig. 7(a). Each channel consists of a chopper-stabilized CC [31], a dual-slope MADC [28], control logic, on-chip memories, and a counter. The dual-slope MADC performs both multiplication and subtraction, as required by the PID algorithm.

The timing diagram of the MADC for a typical conversion cycle is shown in Fig. 7(b). The dual-slope MADC digitizes the input signal in two phases: 1) charging phase T_1 and 2) discharging phase T_2. The ratio of the duration of the charging phase to the discharging phase represents the input signal level. As shown in Fig. 7, to implement multiplication of the input current by a digital PID coefficient c_n, the duration of the charging phase is scaled with a constant coefficient $c_n<1$ [28]. In this case, by counting the time c_nT_2, a digital representation of c_nI_{CTAT} can be obtained.

As shown in Fig. 7, the counter is first reset. At the same time, the PID multiplication coefficient, c_n, is loaded into the in-channel latch ($S_3 = 1$). There is a large channel-to-channel variation between the BJT current output. To compensate for this variation, the channel counter is preloaded with a digital calibration value (stored in the in-channel calibration SRAM) at the rising edge of the RESET signal. Next, the in-channel counter counts up from this value to time c_nT_1, and the input current I_{CTAT} is integrated onto the capacitor C_{INT}. After time c_nT_1, the voltage on the capacitor is held constant for a fixed time interval T_{RD}. During this time, the digital representation of the desired temperature that is scaled by the PID coefficients $c_nt(k)$ is loaded into the counter. During time c_nT_2, the integrating capacitor is discharged with the PTAT current source. During time c_nT_2, the counter counts down, and the final value of the counter is available at the falling edge of S_2 signal. By counting down from $c_nt(k)$ in the second phase of the conversion cycle, the MADC performs

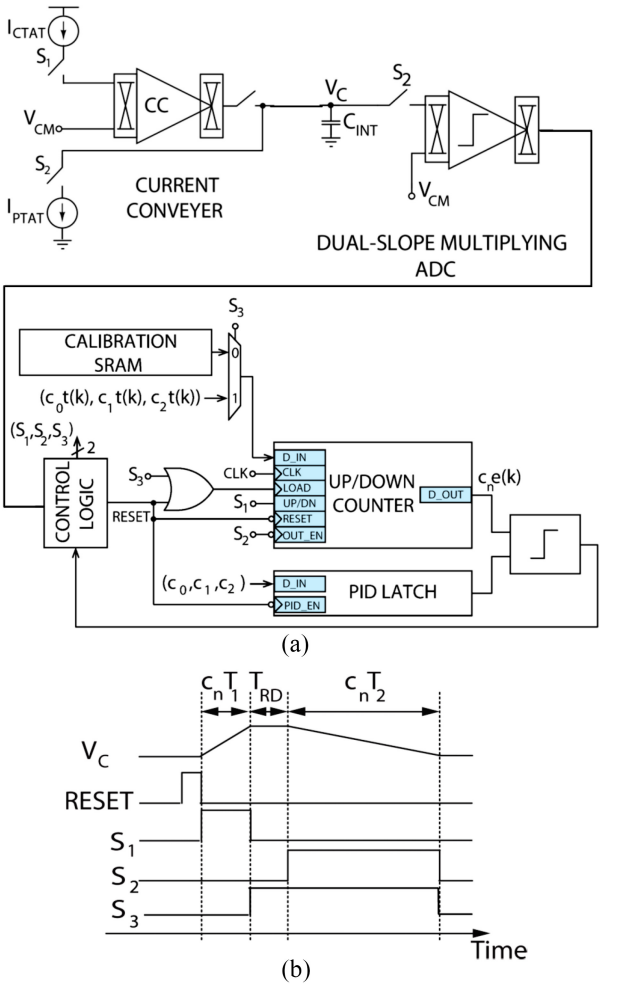


FIGURE 7. (a) Top-level VLSI architecture of one temperature-sensing channel and (b) timing diagram of the dual-slope MADC.

subtraction of $c_ny(k)$ from $c_nt(k)$ (as shown in Fig. 5) thus computing the error signal $c_ne(k)$.

The front-end bidirectional CC is implemented by a pMOS and an nMOS transistor connected in the feedback of an OTA [32]. The negative feedback ensures a known potential at the WE is set by the voltage at the noninverting input of the OTA. It also enables the CC to source and sink an input current without the need for a dc offset current. The OTA is implemented as a folded-cascode amplifier with a pMOS input pair. Chopper stabilization is utilized to reduce the OTA flicker noise and offset and dynamic element matching (DEM) is utilized to reduce the output current mirrors mismatch [32].

The ADC comparator is implemented with three stages of preamplifiers with a total gain of 60 dB, and a high-speed latch as the last stage. The first stage of the comparator is implemented as a cross-coupled diode-connected gain stage to provide a moderate gain with high bandwidth. Chopper stabilization suppresses the input offset and ensures a 9-bit accuracy. The second and third stages are identical to the first one but with no chopping. The high-speed latch is implemented with an nMOS input pair gain stage and an

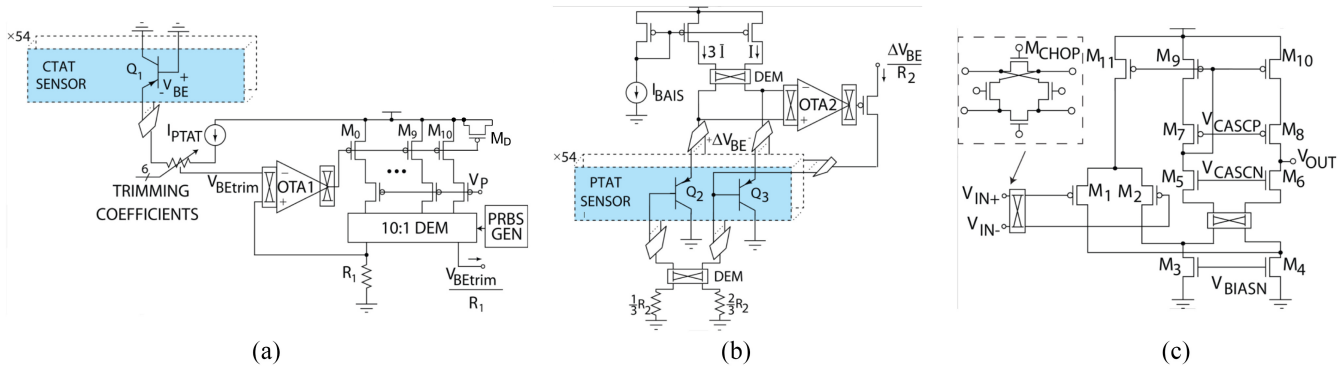


FIGURE 8. Circuit diagrams of (a) CTAT sensor and current source, (b) PTAT sensor and current source, and (c) chopper-stabilized folded-cascode OTA in the CTAT (OTA1) and PTAT (OTA2) current sources.

nMOS–pMOS cross-coupled load to provide high accuracy, low offset, and a high bandwidth [29].

B. CTAT AND PTAT CURRENT SOURCES

A simplified circuit diagram of the CTAT current source is shown in Fig. 8(a). To generate a digitally programmable base–emitter voltage V_{BEtrim} (compensating for chip-to-chip variations), a PTAT current (generated by a separate on-chip biasing circuit) is passed through a 6-bit programmable resistor connected in series with the diode-connected pnp transistor Q_1. The current V_{BEtrim}/R_1 is generated by a voltage-to-current converter, as shown in Fig. 8(a). A large resistor ($R_1 > 100$ MΩ) is required to ensure that the CTAT current is kept relatively low (20 nA) and stays within the dynamic range of the ADC. This would result in a large integration area. To reduce the size of the resistor, a current mirror with a 10:1 ratio is utilized. A 10:1 DEM is used to reduce the effect of the current mirror mismatch. In this work, R_1 is set to 1.5 MΩ.

A simplified circuit diagram of the PTAT current source is shown in Fig. 8(b). ΔV_{BE} is generated by determining the difference between V_{BE} of the two substrate pnp transistors that are biased at 3:1 collector current ratio. The voltage-to-current converter consisting of OTA2 and the nMOS feedback transistor generates ΔV_{BE} across R_2 (split into $R_2/3$ and $2R_2/3$). In this work, R_2 is set to 100 kΩ. This results in the desired output current $\Delta V_{BE}/R_2$. The resistor $R_2/3$ is added in series with the base of the Q_3 transistor in order to ensure that the base current of the Q_3 does not affect the output current.

The main causes of inaccuracy in the current sources are the input offset and the flicker noise of OTAs and the mismatch of the bias current mirror. Internal OTA chopping is utilized to reduce the effect of flicker noise and input offset voltage. OTA1 and OTA2 adopt the same circuit topology, as shown in Fig. 8(c). The transistor sizes are given in Table 1. The chopper switches are placed at the input of the OTA and below the cascoded nMOS transistors in the current mirror. This placement reduces the flicker noise and dc offsets caused by the input pair transistors and the nMOS current

TABLE 1. OTA transistor sizing.

Transistor	W/L (μm)
$M_{1,2}$	$9 \times 4/1$
$M_{3,4}$	$4 \times 1.5/4$
$M_{5,6}$	$5 \times 1.5/1$
$M_{7,8}$	$10 \times 1.5/1$
$M_{9,10}$	$4 \times 1.5/4$
M_{11}	$11 \times 1.5/2$

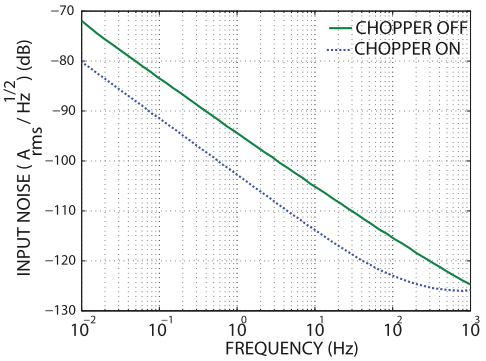


FIGURE 9. Simulated input-referred noise spectrum of the OTA with chopper enabled and disabled from 0.01 Hz to 1 kHz.

mirror transistors. The ripples introduced by chopping are filtered out by the capacitors connected to the gate of M0–M10. pMOS transistors same as the mirror devices were used as the filtering capacitors. DEM at 100 Hz, by the means of the chopper switches in series between the current sources and the resistors, is utilized to improve the matching.

The simulated input-referred noise of OTA1 in cases where the chopper is disabled and enabled is shown in Fig. 9. The integrated input-referred noise from 0.01 Hz to 1 kHz is 0.11 pA when the chopper is disabled and 0.06 pA when the chopper is enabled. The contribution of each transistor to the total input-referred noise is shown in Fig. 10. When the chopper is disabled, the main contributions to the input-referred flicker noise are from the OTA current mirror transistors M_3 and M_4, and from the input pair transistors

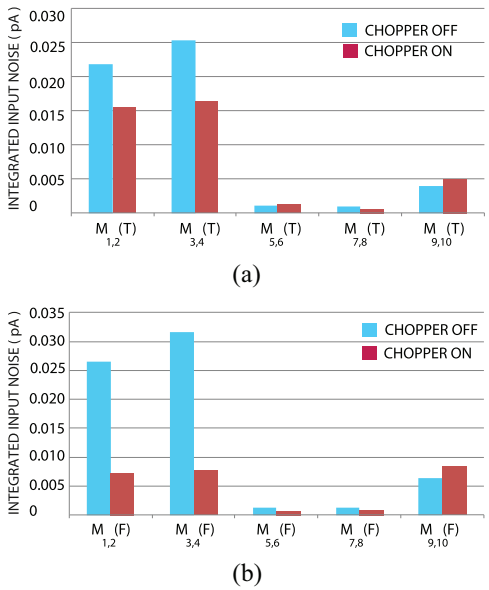


FIGURE 10. Simulated OTA noise. (a) Thermal noise contribution and (b) flicker noise contribution.

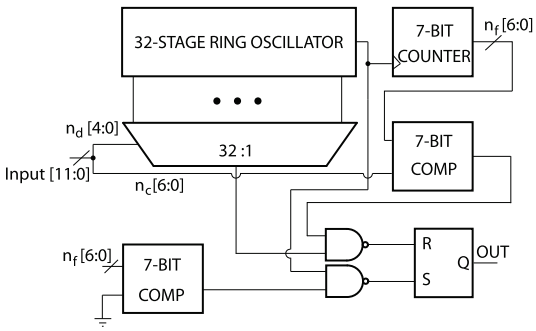


FIGURE 11. Block diagram of the digital PWM.

M_1 and M_2. When the chopper is enabled, the current mirror transistors M_9 and M_{10} are the main contributors to the input-referred flicker noise.

C. DIGITAL PULSE-WIDTH MODULATOR

In the temperature regulation loop, a digital PWM sets the duty cycle of the pulse for controlling the in-channel heater. The achievable discrete set of the duty cycle settings of the pulse depends on the digital PWM resolution. In this work, a 12-bit digital PWM architecture is selected. The design is based on a hybrid delay-line/counter architecture in [38]. The block diagram of the PWM is shown in Fig. 11. In this architecture, a 7-bit counter and 32-stage ring oscillator are used to achieve the 12-bit resolution. At the beginning of a switching cycle, the output set-reset (SR) flip-flop is set, and the PWM output pulse goes high. The pulse that propagates through the ring at the oscillation frequency serves as the clock for the counter. At the time when the counter output matches the top most significant bits of the digital input (n_c), and a pulse reaches the tap selected by the least significant bits (n_d), the output flip-flop is reset, and the output pulse goes low [38].

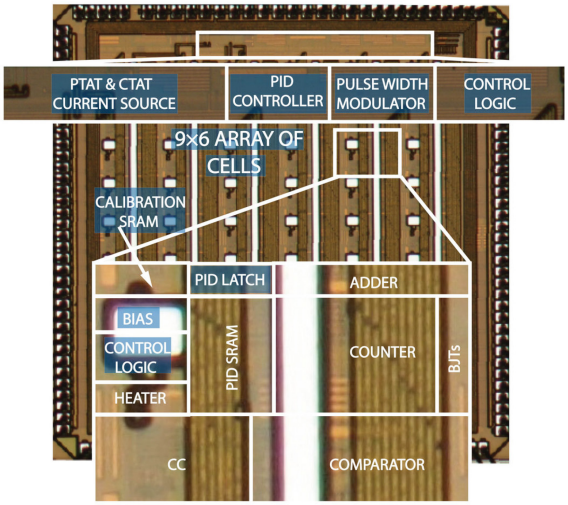


FIGURE 12. Micrograph of the wireless temperature-regulated DNA analysis SoC fabricated in 0.13-μm CMOS technology.

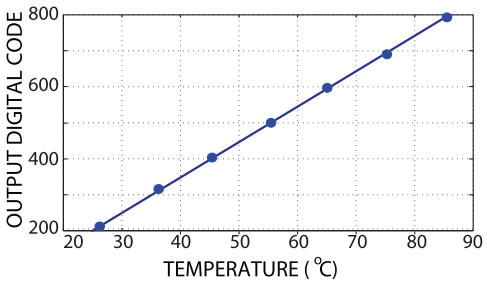


FIGURE 13. Experimentally measured digital output of the ADC versus temperature.

VI. EXPERIMENTAL RESULTS

A. CHIP MICROGRAPH

The micrograph of the fabricated multimodal amperometric DNA analysis SoC is shown in Fig. 12. The 54 cells are arranged in a 9 × 6 array on a 3 mm × 3 mm CMOS die. Each cell consists of a CC, a dual-slope MADC, an in-cell bias and clock generator, a pH sensor, a heater, and temperature-sensing BJTs. The PID controller, CTAT and PTAT current sources, and the digital PWM are located in the top section of the die. The electrodes are postprocessed with 2-D and 3-D Au top layers and several metal underlayers [27].

B. TEMPERATURE REGULATION TESTING RESULTS

The output digital code of the ADC versus temperature, from 20 °C to 90 °C, is shown in Fig. 13. The temperature sensor archives a linear transfer function over the operating temperature range. Fig. 14 shows the measured temperature error of seven dies randomly selected from one wafer, which operated at a supply voltage of 1.2 V. After a one-point calibration for compensating for the BJT variation across channels, as

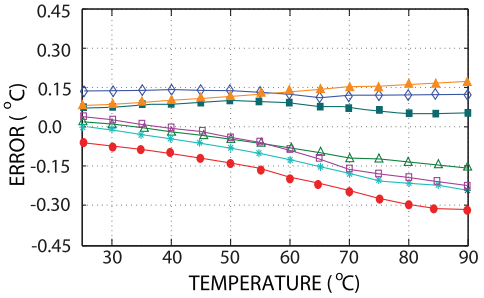


FIGURE 14. Temperature regulation error experimentally measured on seven dies from one wafer.

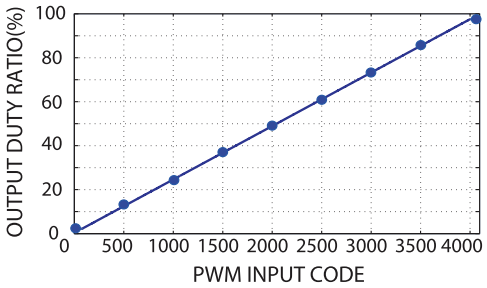


FIGURE 15. Experimentally measured transfer function of the PWM.

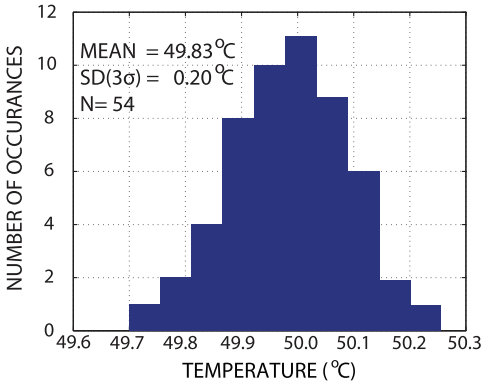


FIGURE 16. Experimentally measured temperature from 54 channels in one chip.

discussed in Section V-A, the temperature error across the seven dies was less than ±0.5 °C over the temperature range of 20 °C to 90 °C. As opposed to just sensing the absolute temperature, the main focus of this work is PID control to regulate the temperature to a certain accuracy. This process depends on the thermodynamics of the die (and the sample) and may not be well modeled by IC CAD simulations, so these experimental results are included rather than Monte-Carlo simulation results. It can be observed in Fig. 14 that there are seemingly two clusters of dies with slightly diverging error as the temperature increases. We hypothesize that this may be due to the fact that the seven tested dies were chosen from a larger population of dies fabricated across a wafer with local or global mismatch having such an effect on the performance. The number of dies tested is not sufficient to draw further statistically significant conclusions. The error range obtained is well within the specification for this application.

The digital PWM is characterized by sweeping the digital input code from 0 to 4095 and clocking the digital PWM at 2.5 MHz. This maximum PWM frequency was chosen to enable us to explore various design configurations (e.g., various PCR protocols) and various use cases (e.g., various number of wells, the same or different DNA types). The choice of the frequency is driven in part by the temporal response time constants of the thermal processes within the CMOS substrate and of those in the fluids, materials, and structures placed in contact with the die, especially on its top surface, closest to the heat generators. As this circuit may be used in different configurations, it was deemed best to allow for a wide range of clock tuning without adding a high energy penalty for overclocking. The design allows for clock speed reduction for power savings which is typically validated by thermal imaging and other means in each applications-specific experimental phase. The experimental results of Fig. 15 show the measured duty ratio of the output pulses as a function of the 12-bit digital input. The minimum (4%) and the maximum (96%) duty ratios are set by design. The digital PWM achieves a linear transfer function over the programmable digital input code with a 0.82% maximum error. The digital PWM achieves a minimum duty cycle resolution of 0.1 μs.

Besides the on-chip resistive heaters, all other on-chip circuits also generate a certain amount of heat. However, the amount of power dissipated by the other circuits is small compared to the heater's maximum power, namely, 0.35 versus 270 mW, respectively. Therefore, this additional small amount of heat does not significantly affect the temperature of the sample, even in the no-heating mode, as the temperature increase due to these circuits' power dissipation is well below the required 0.5 °C tolerance, based on power density considerations. When the temperature is regulated, once the steady state is reached, any increase in the temperature and any nonuniformity in the spatial profile of heat generated by these circuits are compensated for by the distributed PID temperature control. This is, in fact, another advantage of the proposed thermal regulation method.

An external heater was utilized to set the chip temperature at 50 °C and the temperature at each channel was recorded to study the effect of channel-to-channel mismatch. Experimentally measured temperature from 54 channels in one chip is shown in Fig. 16. The mean digital output temperature and the corresponding standard deviation are 49.83 °C and 0.20 °C, respectively.

An example of the temperature regulation cycle in liquid (5-mL 1-M potassium phosphate buffer solution), with steps at 35 °C, 45 °C, 55 °C, and 65 °C, is shown in Fig. 17. The solid line is the chip temperature and the dashed line is the desired temperature. It takes roughly 10 s to achieve an increase of 5 °C in the chip. The measured absolute value of

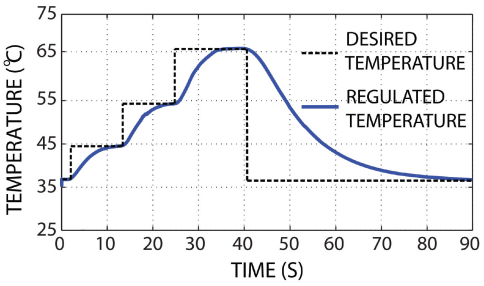


FIGURE 17. Transient responses of temperature regulation with target temperatures at 35 °C, 45 °C, 55 °C, and 65 °C.

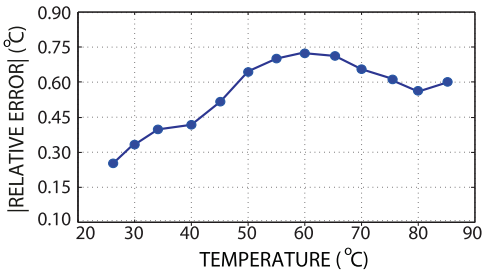


FIGURE 18. Experimentally measured absolute value of the relative error of the PID regulation loop.

TABLE 2. Experimentally measured characteristics.

Technology	0.13μm CMOS
Supply Voltage	1.2V
Area	3mm×3mm
Array Dimensions	9×6 channels
Channel Size	300μm×200μm
Sensitivity	8.6pA
Power during temperature regulation (System level)	
SRAM	1.3μW
PID Controller	21μW
Temperature Core	12μW
Heater	270mW @ 90°C
Power during temperature regulation (Channel level)	
Current conveyor	8μW
Comparator	19μW
Biasing	4μW
Digital	11μW
Total (Channel)	42μW

the relative error of the PID regulation loop over the operating temperature range is shown in Fig. 18. The absolute value of the error stays below 0.75 °C over the operating temperature range. The absolute temperature regulation error is an accumulation of the error of the temperature sensor and the PID controller. The nonlinearity of the curve is mainly introduced by the temperature sensor, which can be calibrated if needed.

Table 2 provides a summary of the experimentally measured characteristics of the system for temperature regulation. The power consumption of 42 μW per channel was measured during the temperature regulation operation. The channel area is 0.06 mm^2, where over 95% of the area is reused

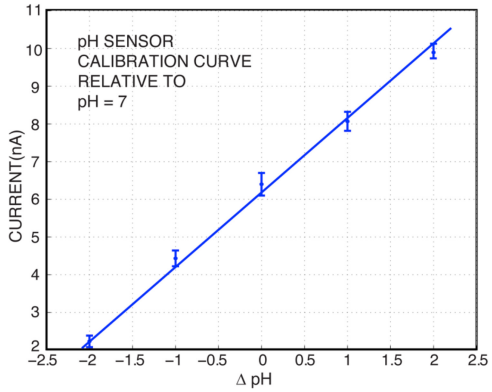


FIGURE 19. Experimental characterization of pH sensing in the CPA mode. The 3σ error bars from 20 measurements are shown.

for multiple functions. The power and area are significantly better than prior digital implementations of PID controllers, for example, 1 mW and 0.15 mm^2 in [22] using 180-nm CMOS, and 331.7 μW and 0.152 mm^2 in [23] using 65-nm CMOS.

C. MULTIMODAL AMPEROMETRIC DNA ANALYSIS RESULTS

The dynamic performance of the cell was measured with a 15-Hz sinusoidal input current at a full-scale current of 400 nA. The ADC was clocked at 10 MHz. An SNR of 56.9 dB was measured, leading to an effective number of bits (ENOBs) of 9.3. The distortion was limited by a −58.7-dB HD2 due to the single-ended architecture of the ADC.

Fig. 19 shows the experimental characterization of pH sensing in the CPA mode. The 3σ error bars from 20 measurements are shown in the figure. The measured current leads to a linear response of 1.8 nA/pH within ±2 relative to a pH of 7.

Fig. 20 shows the experimental measurements of prostate cancer DNA in the CV mode. On-chip gold electrodes were used for the CV scans, which were performed in a 20-μM potassium ferrocyanide solution. Oxidation and reduction peaks are clearly visible in the CV scans using 5-μM single-stranded DNA-modified electrodes. This is because of the negatively charged film created by thiolated DNA probes when they repel the negatively charged electrochemical reporter. Adding a 5-μM noncomplementary DNA target does not change the CV signal, which indicates that nonspecific adsorption is negligible. On the other hand, adding a 5-μM complementary target to the chip leads to the creation of double-stranded DNA on the biosensing electrode, which indicates additional negative charge and elimination of ferrocyanide's redox peak. The error bars (from three chips) in the figure show a detection noise margin of around 4 nA.

Fig. 21 shows the experimental measurements of prostate cancer DNA using the IS mode. The IS frequency was from 0.1 Hz to 10 kHz. The recordings of 20-μM potassium ferrocyanide in the cases of 5-μM single-stranded DNA, the

TABLE 3. Comparative analysis of temperature-regulated biosensory microsystems.

		ISSCC 2010 [4]	JSSC 2017 [10]	JSSC 2019 [6]	TBioCAS 2020 [7]	TBioCAS 2020 [8]	This Work
Modes	CPA	No	No	No	No	Yes	Yes
	CV	No	No	Yes	No	Yes	Yes
	IS	No	No	Yes	No	Yes	Yes
	Temp. Reg.	Yes	Yes	Yes	Yes	Yes	Yes
Process	CMOS Process	0.13µm	0.25µm	0.25µm	0.18µm	0.6µm	0.13µm
	System power*	165mW	118mW	256mW	2.7mW	1.242mW	0.35mW
	Supply Voltage	1.2V	2.5V	2.5V	3.3V	5V	1.2V
	Chip Area	7.5mm^2	63mm^2	10.24mm^2	15mm^2	361mm^2	9mm^2
Channel	Electrode Count	16	1,024	1,024	1,225	16,064	600
	Electrode Type	2D	2D	2D	2D	2D	3D
	Dynamic Range	55dB	116dB	93dB	N/A	N/A	128dB
	Conversion Rate	N/A	50Hz	50Hz	17.06Hz	100kHz	10kHz
	Sensitivity	0.3Hz	20fA	280fA	N/A	42.8pA	8.6pA
	Signal Generator	Yes	No	Yes	Yes	Yes	Yes
	Signal Frequency	1GHz	N/A	50Hz	N/A	N/A	10kHz
	Wireless	No	No	No	No	No	UWB
Temp. Regul.	Channel	1	13	13	49	2	54
	Control Method	PID	N/A	N/A	On/off	N/A	PID
	Implementation	Off-chip	Off-chip	Off-chip	On-chip	Off-chip	On-chip
	Signal Domain	Analog	N/A	N/A	Digital	N/A	Mixed-signal
	Accuracy	1°C	0.3°C	N/A	1°C	0.5°C	±0.5°C

*The system power numbers cited are for measurement operation, not dedicated to temperature regulation.

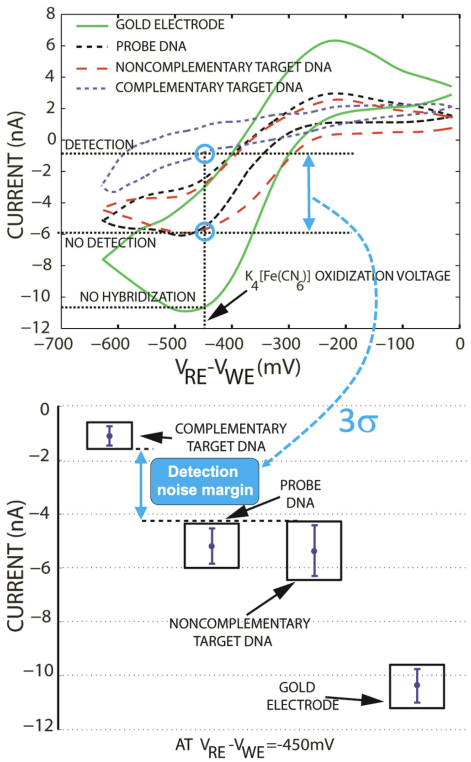


FIGURE 20. Experimental measurements of 5-μM prostate cancer DNA using CV from 0 to −700 mV at a scan rate of 100 mV/s. The 3σ error bars show 20 measurements from three chips.

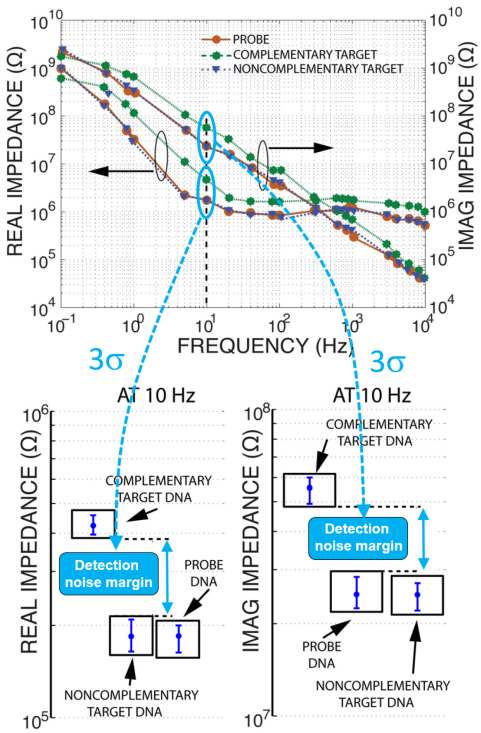


FIGURE 21. Experimental measurements of 5-μM prostate cancer DNA using IS from 0.1 Hz to 10 kHz. The 3σ error bars show 20 measurements from three chips.

addition of 5-μM noncomplementary DNA, and the addition of 5-μM complementary DNA target are shown. The 3σ error bars show 20 measurements from three chips. The impedance spectrum of the DNA probe and the noncomplementary target is fairly similar as expected. The addition of the complementary DNA probe results in a change in the impedance spectrum.

Table 3 provides a comparative analysis of the presented design and existing temperature-regulated biochemical sensory microsystems. The presented work supports advantageous multimodal DNA analysis with the most flexible temperature regulation scheme. Our design also achieves a compact channel area, thanks to the synergistic circuit-sharing design.

VII. CONCLUSION

A 9 × 6 cell array (54-channel) mixed-signal CMOS temperature-regulated distributed DNA-sensing SoC was developed. The SoC reuses circuitry to perform CPA, CA, IS, and temperature regulation. The on-chip, in-channel heating and temperature-sensing elements were implemented in standard CMOS without any post-processing. Local temperature can be regulated to within ±0.5 °C of any desired point between 20 °C and 90 °C using PID control. The overall design achieved a very low power consumption at 42 μW per channel from a 1.2-V supply during temperature regulation. Each channel occupies a silicon area of only 0.06 mm^2. This design can be used in a wide range of applications where temperature regulation is desirable. The proposed circuit-sharing methodology can also be beneficial for future highly integrated SoC designs.

REFERENCES

[1] B. Jang, P. Cao, A. Chevalier, A. Ellington, and A. Hassibi, "A CMOS fluorescence-based biosensor microarray," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2009, pp. 436–437.

[2] P. M. Levine, P. Gong, R. Levicky, and K. L. Shepard, "Active CMOS sensor array for electrochemical biomolecular detection," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1859–1871, Aug. 2008.

[3] F. Heer, M. Keller, G. Yu, J. Janata, M. Josowicz, and A. Hierlemann, "CMOS electro-chemical DNA-detection array with on-chip ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 168–169.

[4] H. Wang, Y. Chen, A. Hassibi, A. Scherer, and A. Hajimiri, "A frequency-shift CMOS magnetic biosensor array with single-bead sensitivity and no external magnet," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 438–439.

[5] D. M. Garner et al., "A multichannel DNA SoC for rapid point-of-care gene detection," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 492–493.

[6] A. Manickam et al., "A CMOS electrochemical biochip with 32 × 32 three-electrode voltammetry pixels," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 2980–2990, Nov. 2019.

[7] J. H. Park, J. S. Y. Tan, H. Wu, Y. Dong, and J. Yoo, "1225-channel neuromorphic retinal-prosthesis SoC with localized temperature-regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1230–1240, Dec. 2020.

[8] W. Tedjo and T. Chen, "An integrated biosensor system with a high-density microelectrode array for real-time electrochemical imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 1, pp. 20–35, Feb. 2020.

[9] M. Zhang, Z. Tang, X. Liu, and J. Van der Spiegel, "Electronic neural interfaces," *Nat. Electron*, vol. 3, no. 4, pp. 191–200, Apr. 2020.

[10] A. Manickam et al., "A fully integrated CMOS fluorescence biochip for DNA and RNA testing," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2857–2870, Nov. 2017.

[11] T. G. Drummond, M. G. Hill, and J. K. Barton, "Electrochemical DNA sensors," *Nat. Biotechnol.*, vol. 21, no. 10, pp. 1192–1199, Oct. 2003.

[12] B. Malorny, C. Bunge, and R. Helmuth, "A real-time PCR for the detection of salmonella enteritidis in poultry meat and consumption eggs," *J. Microbiol. Methods*, vol. 70, no. 2, pp. 245–251, 2007.

[13] G. Liu et al., "An enzyme-based E-DNA sensor for sequence-specific detection of femtomolar DNA targets," *J. Amer. Chem. Soc.*, vol. 130, no. 21, pp. 6820–6825, 2008.

[14] A. Sassolas, B. D. Leca-Bouvier, and L. J. Blum, "DNA biosensors and microarrays," *Chem. Rev.*, vol. 108, no. 1, pp. 109–139, 2008.

[15] G. Harper et al., "Evaluation of temperature gradient gel electrophoresis for the analysis of prey DNA within the guts of invertebrate predators," *Bull. Entomol. Res.*, vol. 96, no. 3, pp. 295–304, 2007.

[16] V. L. Kopparthy and N. D. Crews, "A versatile oscillating-flow microfluidic PCR system utilizing a thermal gradient for nucleic acid analysis," *Biotechnol. Bioeng.*, vol. 117, no. 5, pp. 1525–1532, 2020.

[17] J. B. Christen and A. G. Andreou, "Design, fabrication, and testing of a hybrid CMOS/PDMS microsystem for cell culture and incubation," *IEEE Trans. Biomed. Circuits Syst.* vol. 1, no. 1, pp. 3–18, Mar. 2007.

[18] X. Liu, L. Li, and A. J. Mason, "Thermal control microsystem for protein characterization and sensing," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2009, pp. 277–280.

[19] U. Frey, M. Graf, S. Taschini, K.-U. Kirstein, and A. Hierlemann, "A digital CMOS architecture for a micro-hotplate array," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 441–450, Feb. 2007.

[20] J. Wang and N. Zhang, "Proportional-integral-differential controller for polymerase chain reaction," in *Proc. Int. Conf. Bioinformat. Biomed. Eng.*, 2008, pp. 1584–1587.

[21] Z. Q. Niu, W. Y. Chen, S. Y. Shao, X. Y. Jia, and W. P. Zhang, "DNA amplification on a PDMS-glass hybrid microchip," *J. Micromech. Microeng.*, vol. 16, no. 2, pp. 425–433, 2006.

[22] T. Talaska and R. Dlugosz, "Low power, low chip area, programmable PID controller realized in the CMOS technology," in *Proc. Int. Conf. Mixed Design Integr. Circuits Syst. (MIXDES)*, Jun. 2018, pp. 169–172.

[23] S. John, A. I. Rasheed, and V. K. Reddy, "ASIC implementation of fuzzy-PID controller for aircraft roll control," in *Proc. Int. Conf. Circuits, Controls Commun. (CCUBE)*, 2013, pp. 1–6.

[24] X. Liu, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel, "Design of a closed-loop, bidirectional brain machine interface system with energy efficient neural feature extraction and PID control," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 729–742, Aug 2017.

[25] X. Liu, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel, "A 12-channel bidirectional neural interface chip with integrated channel-level feature extraction and PID controller for closed-loop operation," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, 2015, pp. 1–4.

[26] H. M. Jafari, L. Soleymani, K. Abdelhalim, E. H. Sargent, S. O. Kelley, and R. Genov, "Nanostructured CMOS wireless ultra-wideband label-free DNA analysis SoC," in *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, Jun. 2012, pp. 122–123.

[27] H. M. Jafari, K. Abdelhalim, L. Soleymani, E. H. Sargent, S. O. Kelley, and R. Genov, "Nanostructured CMOS wireless ultra-wideband label-free PCR-free DNA analysis SoC," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1223–1241, May 2014.

[28] H. M. Jafari and R. Genov, "CMOS impedance spectrum analyzer with dual-slope multiplying ADC," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Nov. 2011, pp. 361–364.

[29] H. Jafari, L. Soleymani, and R. Genov, "16-channel CMOS impedance spectroscopy DNA analyzer with dual-slope multiplying ADC," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 5, pp. 468–478, Oct. 2012.

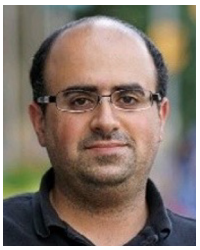
[30] Y. Ma et al., "A review of electrochemical electrodes and readout interface designs for biosensors," *IEEE Open J. Solid-State Circuits Soc.*, early access, Nov. 14, 2022, doi: 10.1109/OJSSCS.2022.3221924.

[31] H. M. Jafari and R. Genov, "Bidirectional current conveyor with chopper stabilization and dynamic element matching," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2012, pp. 1079–1082.

[32] H. M. Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1149–1157, May 2013.

[33] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from −55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[34] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.
[35] K. Souri, Y. Chae, and K. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of $\pm 0.15^{\circ}$C (3σ) from -55 to 125°C," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2012, pp. 208–210.
[36] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of $\pm 0.1^{\circ}$C from -55 to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.
[37] X. Liu, M. Zhang, and J. Van der Spiegel, "A low-power multifunctional CMOS sensor node for an electronic facade," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2550–2559, Sep. 2014.
[38] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.



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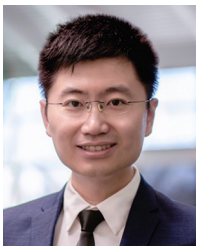

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