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CMOS Platform for Everyday Applications Using Submillimeter Electromagnetic Waves

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ABSTRACT Complementary Metal Oxide Semiconductor (CMOS) integrated circuits (IC's) technology is emerging as a means for realization of capable and affordable systems that operate at frequencies near 300 GHz and higher. This is lowering a key barrier for utilizing the submillimeter electromagnetic waves in everyday applications. Despite the fact that the unity maximum available gain frequency, $f_{\max}$ of N-channel MOS (nMOS) transistors (with connections to the top metal layer) has peaked at ~320 GHz, signal generation up to 1.33 THz, coherent detection up to 1.2 THz, and incoherent detection up to ~10 THz have been demonstrated using CMOS IC's. Furthermore, highly integrated rotational spectroscopy transceivers operating at frequencies up to near 300 GHz, and 400-GHz concurrent transceiver pixels and arrays for high-resolution radar imaging, and 300 and 390-GHz transmitters, and 300-GHz receivers for high data-rate communication have been demonstrated in CMOS. The performances of these CMOS circuits are sufficient or close to being sufficient to support electronic smelling using rotational spectroscopy that can detect and quantify concentrations of a wide variety of gases; imaging that can enable operation in a wide range of visually impaired conditions; and high-bandwidth communication. Finally, techniques for affordable packaging and testing submillimeter-wave systems are suggested based on experimental demonstrations.

INDEX TERMS Built-in self-test (BIST), Complementary Metal Oxide Semiconductor (CMOS), everyday applications, integrated circuits (IC's), interconnects, nonlinear devices, packaging, submillimeter wave.

I. INTRODUCTION

ELECTROMAGNETIC waves in the submillimeter (300 GHz–3 THz) region of the spectrum have a wide variety of potential everyday applications [1], [2], [3]. The waves can be used for real-time 3-D imaging through walls, fog, clouds, dusts, sands, and others [4], [5], These waves can also be utilized for electronic smelling using rotational spectroscopy [6]. Additionally, the wide bandwidth available in this frequency range can be used for high data-rate wireline [7] and wireless communication [8], [9]. Advances of the high-frequency performance for the complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology are starting to open the paths to affordably fabricate the necessary devices for these applications by leveraging the cost and scale of CMOS manufacturing. This in turn should make uses of these applications in daily life feasible and practical [10], [11], [12]. This article expands and updates the discussions originally published in [2] and [3], and also combines other previously published contents [13], [14], [15] to provide a more complete discussion of the challenges, opportunities, and state of the art. More specifically, in Section II, the devices and interconnects in CMOS, and the challenges they pose, as well as the opportunities they provide toward implementing submillimeter-wave circuits, are described. This section was originally published in [2] and [3]. Additionally, this article in Sections III and IV present the state-of-the-art performance of CMOS submillimeter-wave circuits, their

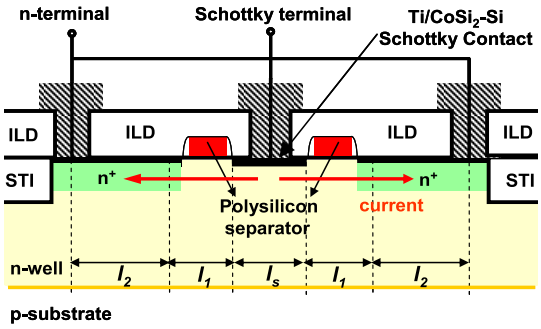

FIGURE 1. Schottky diode structure in CMOS [15].

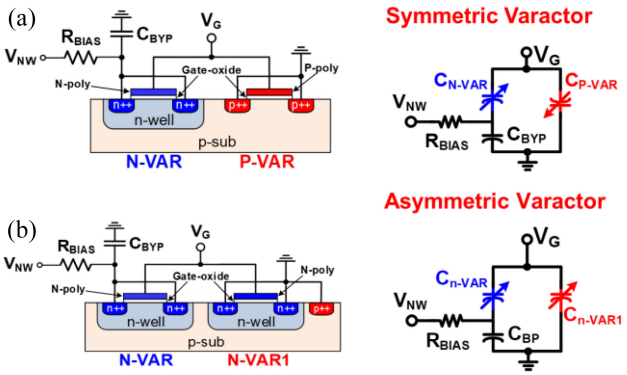

FIGURE 2. (a) Symmetric [20], [21] and (b) asymmetric MOS varactors [22].

applications and expected advances that will help to expand the application opportunities. These sections expand and update the discussions once again in [2] and [3], and also include updated contents from [13]. Finally, approaches for affordable packaging and testing submillimeter-wave systems are suggested based on the experimental demonstrations in [14] and [15] that are partially reproduced here.

II. CMOS TECHNOLOGY FOR SUBMILLIMETER-WAVE CIRCUITS

Demonstrations of submillimeter-wave circuits in CMOS are in part enabled by the advances of high-frequency capabilities of the active and passive devices in the technology. The highest unity current gain frequency, f_T and unity maximum available power gain frequency, $f_{\max}$ of N-channel MOS (nMOS) transistors fabricated in CMOS are 280 and 320 GHz, respectively [16]. These are for transistors including the interconnects to the top metal layer that increase parasitic capacitance, resistance, and inductance. The highest $f_{\max}$ was achieved using a transistor in 32-nm CMOS [16]. The $f_{\max}$ of the latest technology node is no longer the highest [16]. Amplification at frequencies up to ~80 % of $f_{\max}$ has been demonstrated [17]. These limit the maximum frequency for linear amplification using transistors in CMOS to ~300 GHz or less [12]. Additionally, the decrease of supply voltage with the technology scaling is making generation of a sufficient power level in amplifiers and local oscillators (LOs) needed for mixing operation more difficult.

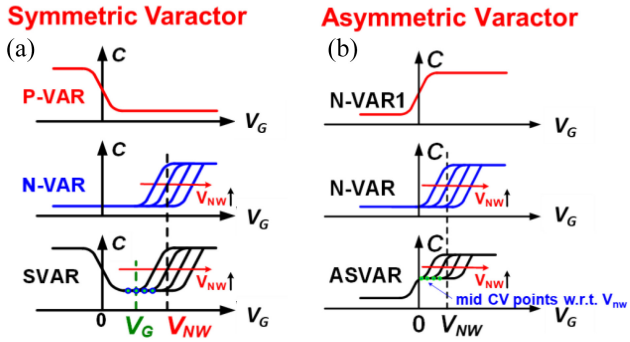

FIGURE 3. (a) Symmetric and (b) asymmetric MOS varactor C-V characteristics [22].

Despite these limitations, it is possible to operate CMOS circuits and systems at frequencies above 300 GHz. Similar to what the terahertz community has done for many years using III–V devices and photonic crystals, the nonlinearity of components in CMOS can be utilized to accomplish this. In fact, Schottky diodes [18], [19] shown in Fig. 1 with a cut-off frequency $(2\pi RC)^{-1}$ and MOS varactor diodes [20], [21], [22] shown in Fig. 2 with a dynamic cut-off frequency, $f_{cd} = (2\pi R)^{-1}\,(1/C_{\min} - 1/C_{\max})$ of over 2 THz have been reported using CMOS. With increasing cut-off frequencies, responsivity (output voltage/input power) of Schottky diode detectors, and conversion efficiency of varactor frequency multipliers and mixers are improved at a given operating frequency. Increasing the cut-off frequencies also raises the maximum operating frequency at which given performance can be achieved. Theoretically, amplification using varactors is possible up to $f_{cd}/2$ [23] which is higher than $f_{\max}$ of transistors. These nonlinear devices are realized without any modifications to the fabrication processes.

The Schottky diode structure shown in Fig. 1 [19] utilizes a metal-silicide-to-n-well contact. The shapes of voltage dependence of MOS varactor capacitance can be almost freely controlled by connecting multiple n- and p-type varactors with varying cathode bias voltages in parallel. Exploiting this, both symmetric MOS varactors [Fig. 2(a)] that suppress even-order nonlinearity [20], [21] and asymmetric MOS varactors that suppress odd-order nonlinearity [Fig. 2(b)] [22] have been demonstrated. Fig. 3 shows C-V characteristics of both symmetric [20], [21] and asymmetric [22] MOS varactors. These suppression properties simplify the harmonic termination requirements, which can lead to lower loss.

Fortunately, not all component characteristics degrade as the operation frequency is increased toward 1 THz. The efficiency of on-chip patch antenna that can be realized in a 130-nm CMOS process with a ~2-μm thick top metal layer and a total thickness of the dielectric layer between the silicon and aluminum bond pad layer of ~7 μm [24] improves to ~80 % at 1 THz from ~30 % at 300 GHz [Fig. 4(a)]. With increasing frequency, the patch height from the ground plane normalized to a wavelength and the perimeter-to-area ratio of resonant patch increase. These make patch antennas a better radiator and improve their efficiency.

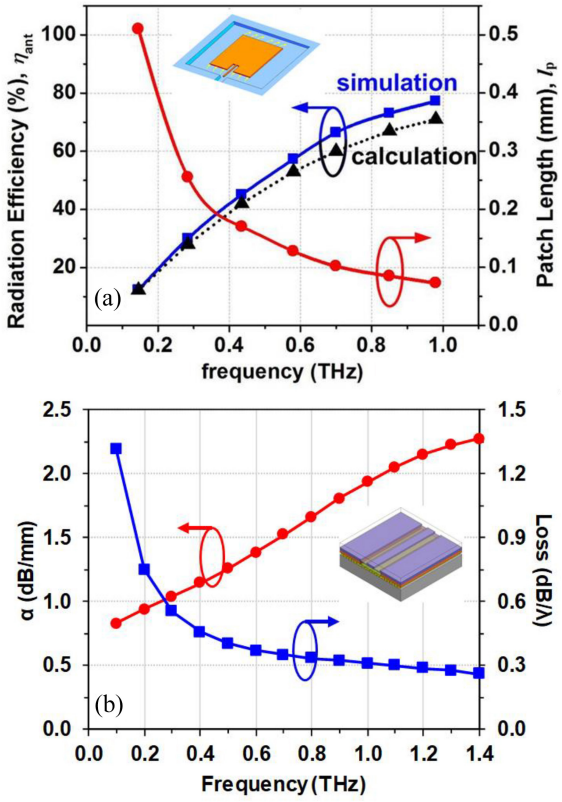

FIGURE 4. (a) Radiation efficiency of a patch antenna that can be achieved in CMOS versus frequency [24]. (b) Loss of a grounded coplanar waveguide that can be realized in CMOS versus frequency [3].

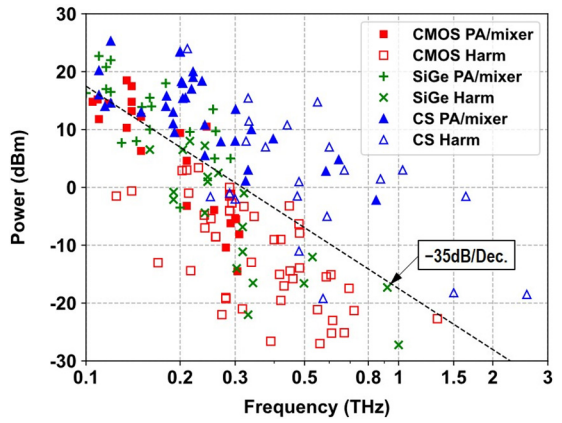

FIGURE 5. Output power (normalized to a single chain) versus frequency for signal generation circuits fabricated using nMOS transistors in CMOS, SiGe HBT's, and III–V devices (https://www.wchoi.net/thz).

The loss of grounded coplanar waveguides (65-nm CMOS process) widely used to form impedance matching components increases with frequency when a length is fixed. On the other hand, when the loss is normalized to a wavelength, it decreases from ∼0.6 dB/λ at 300 GHz to ∼0.3 dB/λ at 1 THz [3]. Because dimensions of matching components are normalized to a wavelength, their performance improves with operating frequency [Fig. 4(b)]. These and the reduction of nMOS f_T and f_{max} with the addition of interconnects illustrate the importance of a properly optimized interconnect process for improving the performance of CMOS submillimeter-wave circuits. As mentioned, this section was originally published in [2] and [3].

III. SUBMILLIMETER-WAVE CMOS CIRCUITS

The realization of capable submillimeter-wave CMOS circuits is also enabled by the advances in circuit techniques. The basic functional blocks of submillimeter-wave systems for everyday applications are a transmitter and a receiver, and two of the key performance metrics are transmitter output power and receiver noise figure.

A. OUTPUT POWER OF SIGNAL GENERATION CIRCUITS

Fig. 5 shows the output power from the literature versus operating frequency for signal generation circuits fabricated in CMOS. The results for arrays and multiple parallel chains have been normalized to that for a single chain. The highest output power level of CMOS anharmonic oscillators with a frequency multiplication circuit is ∼−1 dBm at 300 GHz [25], ∼−8 dBm at 482 GHz [26], and −18 dBm at 694 GHz [27]. A transistor frequency multiplier is used to generate 0 dBm at 288 GHz [28], and MOS varactor frequency multipliers are used to generate −3.2 dBm at 447 GHz [21], −8 dBm at 480 GHz [29], −21.3 dBm at 720 GHz [30], and −23 dBm at 1.33 THz [22]. The multipliers in addition to providing higher output power at higher frequencies also support a larger output frequency range for signal generation at 400 GHz and above. As discussed in Section V, these performance levels are sufficient to implement useful systems [2].

The 1.33-THz signal was generated using a cascade of a symmetric MOS varactor frequency quintupler and an asymmetric MOS varactor frequency doubler. The output power, P_{out} of −23 dBm at 1.33 THz is close to the simulated output power of −21 dBm at 1.4 THz. Since the simulated conversion loss of 700-GHz-to-1.4-THz frequency doubler is 18 dB, the power delivered to the input of doubler should be ∼−5 dBm. Accounting for the frequency mistuning, the circuit could be generating output power of ∼0 dBm near 650 GHz [22]. The highest normalized output power of CMOS signal generators using a frequency multiplier and an anharmonic oscillator falls with a slope of ∼−35 dB/decade as the operating frequency is increased. The total output power levels of CMOS sources without normalization are higher. By spatially combining outputs of anharmonic oscillators, total output power levels of 1 dBm (four elements) at 345 GHz [31], 0 dBm (36 elements) at 590 GHz [32], and −3 dBm (32 elements) at 694 GHz [27] have been demonstrated.

B. NOISE FIGURE OF RECEIVER RF FRONT-ENDS

Receivers can be categorized into two types: 1) incoherent receivers that detect only the amplitude of input signals and 2) coherent receivers that detect both the amplitude and

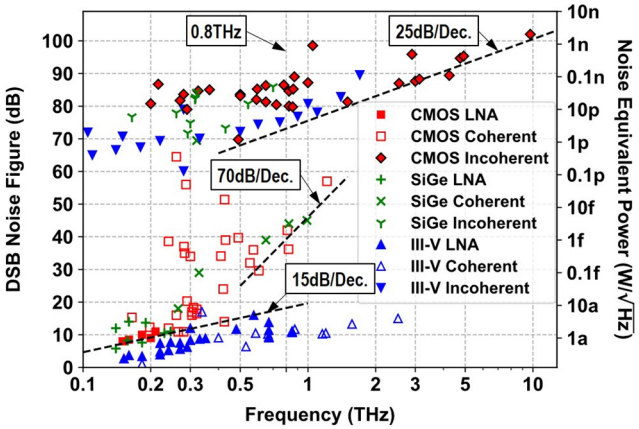

FIGURE 6. DSB noise figure versus operating frequency for coherent receivers, and NEP and effective noise figure (noise bandwidth of 1 kHz) versus operating frequency for terahertz incoherent detectors fabricated using devices in CMOS, SiGe HBT's, and III–V devices (https://www.wchoi.net/thz).

phase. Because an incoherent receiver detects by squaring input signals, its ability to detect small signals is severely limited compared to coherent receivers which rely on mixing of input signals with an LO signal with an amplitude many orders of magnitude higher than that of the input signals.

Fig. 6 shows the double-side-band (DSB) noise figures from the literature versus operating frequency for coherent receivers fabricated using nMOS transistors and MOS varactors in CMOS. Coherent detection up to 1.2 THz has been demonstrated in CMOS [33]. The lowest measured DSB noise figures for CMOS receivers are 11 dB at 260 GHz [34], 11.5 dB at 280 GHz [35], and 14 dB at 420 GHz [36]. The noise figure increases with a slope of ∼15 dB per decade as the output frequency is increased. This is significantly slower than that for the transmitter output power.

At frequencies above 420 GHz, noise figures of CMOS circuits increase with a slope of ∼70 dB/decade due to the use of higher order subharmonic mixing [33], [37], [38]. The amplitude of the frequency-multiplied LO signal is not sufficiently high to properly switch devices due to the increased loss of high-order frequency multiplication and operating frequency. This once again degrades conversion loss and noise figure. In addition, increased downconversion of noise due to the increased harmonic contents further degrades noise figure. These limitations can be mitigated using a separate frequency multiplier that is more efficient and can generate higher power, and by lowering the order of subharmonic mixing.

Fig. 6 also shows the noise equivalent power (NEP) and effective noise figure (noise bandwidth of 1 kHz) of incoherent detectors fabricated once again using nMOS transistors, and Schottky diodes in CMOS. The NEP is the input power at which the signal to noise ratio is unity over a 1-Hz bandwidth. For a given noise bandwidth (BW), an NEP can be converted to an effective noise figure ($NEP/(kT\sqrt{BW})$). The highest operating frequency for incoherent detectors fabricated in CMOS is ∼10 THz. It utilizes a Schottky diode detector [39]. The effective noise figures of the incoherent receivers vary from 70 to 100 dB which as expected are significantly higher than that of coherent receivers at frequencies below 1 THz. As discussed in Section V, these noise performance levels of coherent and incoherent receivers should be sufficient to support everyday applications. This section presented expanded and updated discussions originally published in [2] and [3].

IV. AFFORDABLE DEBUGGING AND TESTING

Affordable testing and easy debugging of circuits operating near 300 GHz or above are critical to lower cost and shorten development cycles. The cost of traditional high-frequency tests using probes and instruments in conjunction with sophisticated de-embedding techniques is prohibitive in high volume. Including ac test points for characterization of internal nodes for de-bugging is not practical because of loading of the nodes by the instruments and the parasitic capacitance and inductance added by the test points that alter or degrade the circuit characteristics. Furthermore, due to the use of components with smaller physical dimensions, the submillimeter-wave circuits are more sensitive to process variations. The testing and debugging challenges can be mitigated using a built-in self-test (BIST) that utilizes high-impedance, broadband, and compact root mean square (RMS) detectors [14], [40], [41], [42], [43]. The sensitivity to process variation can be reduced to improve circuit yield by post fabrication tuning using the measurements.

For high-impedance and broadband on-chip voltage measurements in CMOS at frequencies near 300 GHz or above, Schottky diodes [42], p-n diodes [44], and MOS transistors [40] can be utilized. Fig. 7 is a schematic of on-chip 300-GHz voltage measurement block that includes seven high impedance and broadband on-chip diode-connected nMOS detectors. The signals of interest are coupled to the detectors through a capacitor $C_{c\#}$, which dc isolates the detector dc bias from that of the node being measured. The detectors are biased from one current source and each of them is biased through a 5-kΩ resistor, $R_{F\#}$ and a selection transistor. The resistor in combination with a capacitor, C_F shared by all the detectors forms a low pass filter that attenuates high-frequency signals. Sharing C_F among the detectors reduces the overall area overhead of the voltage measurement circuits. The detector outputs are multiplexed to an analog-to-digital converter.

Fig. 7 also shows an equivalent ac circuit model of a diode. The detector gain is

$$\frac{V_o}{(v_{rms})^2} = \left(\frac{1}{2nV_T}\right)\left[\frac{1}{\left(\frac{f}{f_c}\right)^2 + \left(\frac{C_c + C_j}{C_c}\right)^2}\right], \qquad (1)$$

where V_o is the output dc voltage, $v_{\rm rms}$ is the RMS voltage of signal being measured, $f_c = 1/(2\pi R_s C_j)$ is the cut-off frequency of diode, n is the ideality factor, and V_T is the thermal voltage. At the operating frequencies of interest,

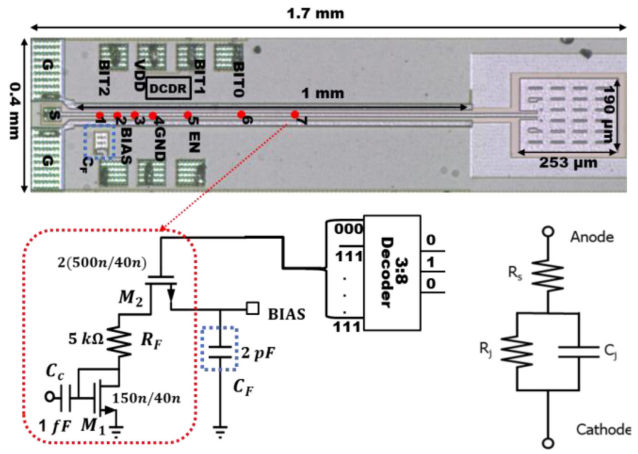

FIGURE 7. Structure for standing wave voltage measurements [37]. nMOS diode detectors with a decoder for selection and ac model of diode-connected nMOS transistors (bottom right).

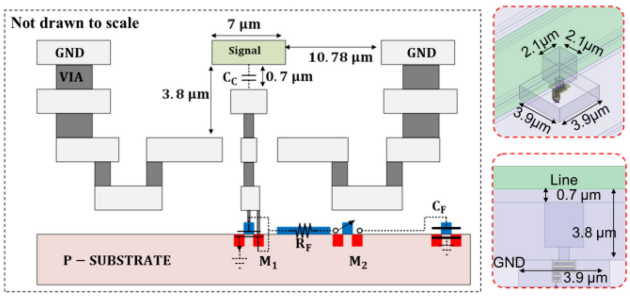

FIGURE 8. (Left) Cross section of a detector placed within a GCPW, (top right) 3-D perspective, and (bottom right) side view of signal coupling structure, C_c [14].

the magnitude of impedance of C_j is much less than that of R_j. If the signal frequency f is much less than f_c, the junction voltage V_j is $C_c V_{in}/(C_c + C_j)$ and is independent of frequency and makes the detectors broadband. The detector gain depends on temperature that must be compensated, n, C_c, and C_j. Variations of these ultimately limit the measurement accuracy.

The values of C_c and C_j are 1 to 0.2 fF with the corresponding reactance of $-j0.53$ kΩ and $-j2.6$ kΩ at 300 GHz and the series combination impedance is –j3.1 kΩ. This is sufficiently high for nodes with an impedance of 20–200 Ω to make the loading effect small. If necessary, the capacitances can be made even smaller. Fig. 8 shows how a diode connected nMOS transistor detector can be inserted into a grounded coplanar waveguide to detect 280–300-GHz signals. The diode and coupling capacitor occupy an area of $3.9 \times 3.9\ \mu m^2$. The other components needed including a switch transistor and a resistor are placed under the ground plane of GCPW to limit the area penalty [40]. The range of measured gains (25 measurements) is ∼12% of the mean for 25 300-GHz detectors [40].

Table 1 summarizes the measured performance of RMS detectors [40]. The insertion loss of detectors is less than 0.2 dB at 220–300 GHz. The loss is measured relative to a structure with 50-Ω source and load. These indicate that

TABLE 1. RMS detectors for mm-wave voltage measurements [40].

Detection device	NMOS
Technology	45-nm CMOS
Frequency (GHz)	270-300
Area (µm^2)	24
Dynamic range (dB)	41
Insertion loss (dB)	0.2

detectors with minimal loading or a high impedance can be realized. The measured detector gain is constant over a bandwidth of 30 GHz [40]. The bandwidth is limited by the instrumentation and should be higher. The dynamic range of detectors is 40 dB. This combination of high impedance, broadband and compact area allows the detectors to be almost freely utilized with small impact to circuit area and operation.

The seven RMS detectors placed in a GCPW connected to a patch antenna tuned for 280 GHz in Fig. 5 are used to measure standing wave voltages along the waveguide at 270–300 GHz to experimentally verify that the tuned frequency of patch is ∼280 GHz [40]. The measured input reflection coefficients, $|S_{11}|$'s of the structures with and without the seven detectors are almost the same indicating that the detectors can be added with negligible impact [40].

This type of detectors enables high-frequency voltage sensing using dc/low-frequency measurements which can be used to support BIST. Given the demonstration of signal detection up to 10 THz using devices in CMOS, it should be possible to utilize this technique over the entire submillimeter-wave frequency range. The measurements can also be used to improve the performance and yield through post fabrication tuning and selection [14]. The section presented shortened discussions in [14].

V. LOW-COST PACKAGING

Affordably packaging submillimeter-wave circuits is another critical requirement for supporting everyday applications. At frequencies near 300 GHz and above, on-chip antennas can have efficiency of ∼40%, and the resonant antennas can be significantly smaller than the IC's, while managing the losses of interconnection between the circuits and antennas in a package becomes increasingly difficult. For these, the case for use of on-chip antennas is stronger at the submillimeter-wave frequencies.

One of the last remaining questions for on-chip antennas has been the effects of encapsulation material used in packaging. Fortunately, encapsulation materials based on silica microparticles dispersed in an epoxy matrix can be sufficiently low loss even at 400 GHz. Loss tangents of ∼0.01 at 400 GHz have been measured [45]. Because of this, placing a 300-GHz on-chip patch antenna in a low-cost quad-flat-no-leads (QFNs) package using such encapsulation materials (Fig. 9) can in fact improve the antenna performance [15]. Full-wave simulations of a rectangular patch antenna, compliant with the metal stack and design rules of a 65-nm

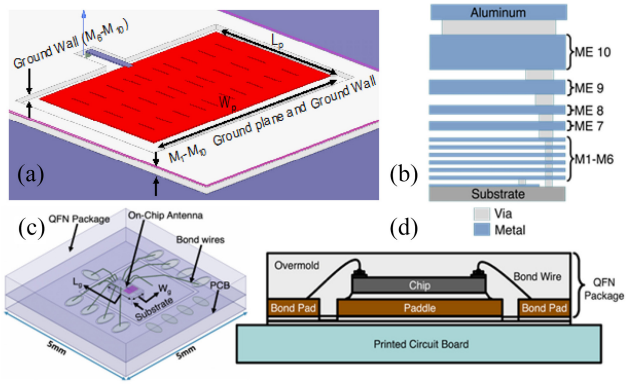

FIGURE 9. (a) Zoomed-in figure of a rectangular patch antenna. (b) Metal-via stack of 65-nm CMOS process used (not drawn to scale). (c) EM simulation structure with a QFN packaging material placed above an on-chip antenna. (d) IC packaging structure [15].

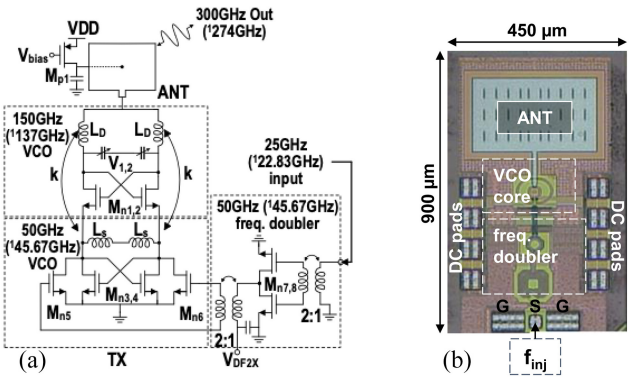

FIGURE 10. (a) Schematic and (b) die photograph of the signal generator [15].

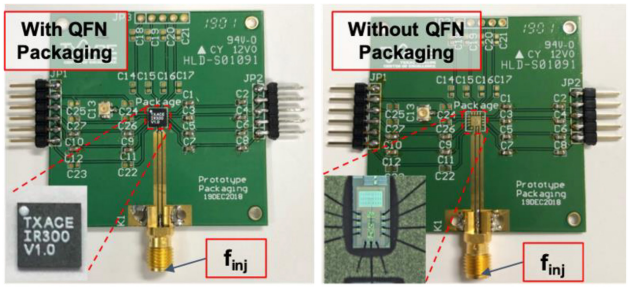

FIGURE 11. PCB with a 300-GHz signal generator in a low-cost QFN package and with a signal generator without packaging [15].

TABLE 2. Simulated and measured (with and without packaging) performance of 300-GHz signal generators [15].

Encapsulation Material	Simulation				Measurements	
	None		QFN (ε_r=3.55)[b]		QFN	None
			Loss Tangent			
			0.01	0.02		
f_o (GHz)	**300**	**276**	**274**	**274**	**274**	**276**
Pwr. Delivered to Ant. (dBm)	-13.2	-18.5	-16.4	-16.5		
Radiation Efficiency (%)	34.9	25.1	40.1	33.8		
Peak Gain at $\phi = 0°$(dB)	2.1	0	3.2	2.4		
[a]*EIRP* (dBm) (**with bond-wires**)	-11.1	**-18.5**	**-13.2**	-14.1	**-12.8**	-18.9
P_{DC} (mW)	24	24	24	24	26.3	26

[a]Effective isotropic radiated power [b]Simulated with a 400-µm thick material with ε_r=3.55 and loss tangents of 0.01 and 0.02, and with bond wires.

CMOS process, show 13-% radiation efficiency, 1-dB peak antenna gain and 7-GHz −10-dB $|S_{11}|$ bandwidth increases when the thickness of packaging encapsulation material over the antenna is $\sim \lambda/3$.

To experimentally corroborate these simulation studies based on measured packaging dielectric properties, a 300-GHz signal generation circuit (Fig. 10) is encapsulated in a QFN package using a commercial service. The size of the silica-based package is 4×4 mm^2 with 16 pins. The thickness of packaging material is ∼400 μm. The packaged IC is mounted on a 2-layer printed circuit board (PCB) using a low-cost FR-5 substrate as shown in Fig. 11. For proper comparison, the cases with and without an encapsulation material were both simulated and measured with the same PCB. The IC is wire bonded using gold wires to the pads of a QFN package (Figs. 9(c) and 11).

The measured characteristics of signal generation circuits with and without the encapsulation material on top of the antenna are summarized in Table 2. In addition, the simulated performance of on-chip antennas with two different dielectric properties ($\varepsilon_r = 3.55$ and loss tangent of 0.01 and 0.02) for the encapsulation materials is also shown in Table 2. Unfortunately, the measured data for the silica-based (SiO_2) material of the QFN package were not available. The permittivity of 3.55 corresponding that of one of the materials studied in [45] was used in simulations. The two values of loss tangent were utilized in order to bound the impact of the uncertainty. Bond wires are included in the simulation models.

The measured effective isotropic radiated power (EIRP) of the signal generation circuit with encapsulation at 274 GHz is ∼6 dB higher than that at 276 GHz without encapsulation. If ϵ_r of the packaging material were 3.55, then the power delivered to the antenna simulated using the circuit and S-parameter of antenna from EM simulation is ∼2.0-dB higher than the case without the packaging. This is mostly due to the improvement of power match between the circuit and antenna. In addition, the simulated peak gain in plane $\phi = 0°$(dB) is ∼3.2-dB higher for the case with encapsulation ($\varepsilon_r = 3.55$, loss tangent of 0.01) at 274 GHz than that for the no-encapsulation case at 276 GHz. This increase is due to an improvement of the power match between the antenna and its surroundings, and due to an increase of the energy of fringing fields responsible for the radiation which is proportional to the permittivity. The latter raises the gain by increasing the efficiency.

This combination of improvements of power match and gain can explain much of the measured difference (∼6.1 dB). The improved EIRP after encapsulation for packaging corroborates the fact that circuits with an on-chip antenna can

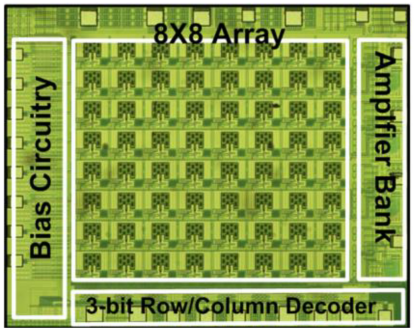

FIGURE 12. 8 × 8 array of 820-GHz diode-connected nMOS pixels with on-chip low-noise preamplifiers [54].

FIGURE 13. Examples of transmission mode images taken with CMOS detectors without using external optics [2].

indeed be packaged using a low-cost technique and packaging can actually improve the antenna performance. The section presented condensed discussions from [15].

VI. CMOS INTEGRATED SYSTEMS FOR SUBMILLIMETER-WAVE APPLICATIONS

The submillimeter-wave CMOS transmitter and receiver circuits discussed in Section II have been utilized to implement integrated systems for imaging [13], [24], [39], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], electronic smelling using rotational spectroscopy [34], [35], [67], [68], [69], [70], [71], and high data-rate wireless communication [8], [9], [72], [73], [74], [75], [76], [77], [78], [79], [80] and wireline communication over dielectric waveguides [7], [81], [82], [83], [84]. Examples of these systems are discussed in this section to illustrate that the necessary electronics for everyday applications in the submillimeter-wave band can be affordably realized.

A. IMAGING

Submillimeter-wave imaging has been one of the most widely studied and fascinating applications [13], [24], [39], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66]. An 820-GHz imaging array using diode connected nMOS detectors fabricated in 130-nm CMOS (Fig. 12) [54] has been demonstrated. It includes an 8 × 8 pixel array, analog multiplexers, an amplifier bank external to the pixel array, and column/row decoders. A pixel consists of a patch antenna, a diode-connected nMOS transistor for detection, a double-stub matching network and an access transistor [54]. Placing the amplifiers outside of pixels increases flexibility for optimizing their bandwidth and noise performance. This is critical for improving the overall NEP of imaging array. The average responsivity and NEP of the imaging array including the amplifiers is 2600 V/W and 37 pW/$\sqrt{}$Hz, respectively. The minimum NEP is 13 pW/$\sqrt{}$Hz. As seen in Fig. 6, the minimum (lowest filled diamond next to the 800-GHz line) is the same as that achieved using III–V Schottky diode detectors at the same frequency.

Fig. 13 shows transmission mode images formed with the array without using external optics (lens-less). The images are that of a floppy disk, an identification card with an embedded RFID, and a peanut butter cup with a molten spot (bright spot) in a wrapper [54]. The imaged objects are illuminated using a −5-dBm source 1.5-cm away and the waves which transmitted through the samples are detected using an array 1.5-cm away from the object. Absorption and reflection of submillimeter waves are highly material dependent and these dependencies provide the contrast in the images. The chocolate covered peanut butter cup is strongly absorbing while the metal structures are highly reflecting. Increasing the dynamic range of imaging system by lowering the noise figure/NEP and increasing the transmitted power will widen the variety of materials and range of thicknesses that can be imaged through. Drawings of the imaging pixel and lens-less transmission mode image setup can be found in [54].

A critically needed imaging capability is operation in all weather conditions. It has been suggested that a key factor limiting the use of autonomous vehicles is the operational challenges in visually impaired conditions [12]. A major goal for the submillimeter-wave community is realization of a power-efficient system that can image through rain, fog, dust and others while supporting a range of 200 m and an angular resolution less than 0.3°, as well as a practical form factor (∼10 cm × 20 cm × 5 cm). A significant step toward realizing this goal is the demonstration of an array of 430-GHz concurrent transceiver radar pixel with an area of 400 × 400 μm^2 or ∼λ/2 × λ/2 that works with an external 6-cm diameter reflector to support an angular resolution of ∼0.7° [13]. With a 15-cm diameter, it should be possible to achieve an angular resolution less than 0.3°. A substantial portion of this discussion was previously reported in [13].

The pixel in Fig. 14 consists of a 3rd-order anharmonic differential Colpitts oscillator, a pair of mixing devices using diode-connected nMOS transistors, and an inverter-based IF LNA. Due to the use of a differential patch antenna and

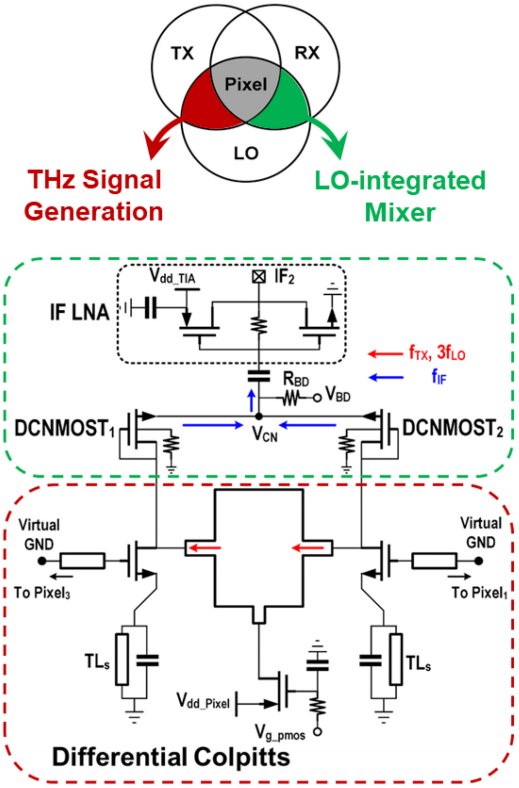

FIGURE 14. Concurrent transceiver pixel integrating a transmitter, receiver, on-chip antenna, and injection locking circuit for stabilization of operating frequency [13].

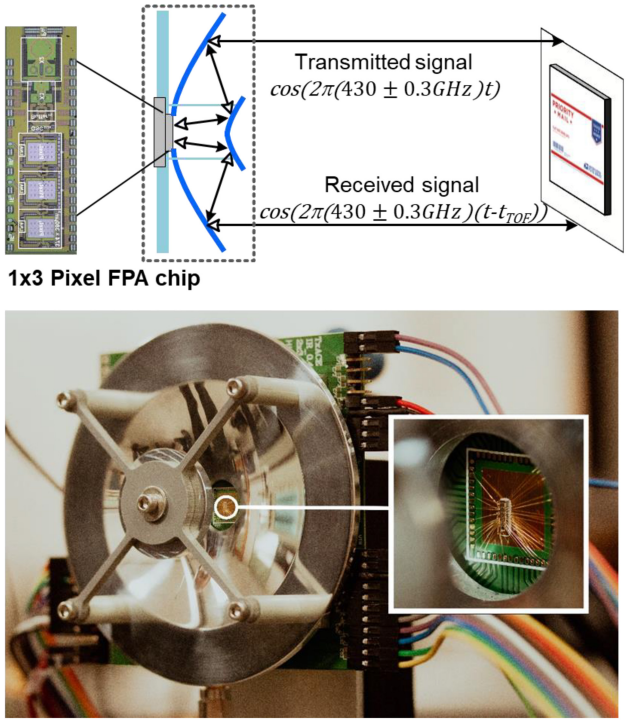

FIGURE 15. 1 × 3 pixel array integrated with a 6-cm diameter Cassegrain reflector to form a reflection mode imager.

a current source, the two single-ended Colpitts oscillators in the pixel are forced to operate in differential mode, and the 3rd harmonic signal generated by the nonlinearity of the differential Colpitts oscillator is radiated through the patch and works as a TX. In the RX mode, the signal picked up by the antenna is differentially delivered into the pixel. A pair of diode-connected triple-well nMOS transistors (DCNMOST's) is used for down conversion and IF signal extraction. The received differential RX signal is mixed with the differential 3rd harmonic signal of oscillator in the pixel to generate in-phase IF currents.

To stabilize oscillation and to better maintain the signal balance among pixels, an auxiliary oscillator (Osc_{AUX}) is employed. An FSK signal at ∼24 GHz from an external generator is frequency multiplied by 6 on chip and injected into Osc_{AUX} at the fundamental oscillation frequency through a coupled line at its drain nodes to FSK modulate the TX output. The transmission line TL_g in Fig. 14 sets the fundamental oscillation frequency and also functions as a coupling network for LO synchronization among pixels.

An 1 × 3 TRX pixel array is fabricated in 65-nm bulk CMOS and shown in Fig. 15. With a 10-dBm injection signal at ∼24 GHz, a locking range of 0.9 GHz is achieved with a peak EIRP of −4 dBm at 431.6 GHz. The minimum DSB NF is 38.5 dB at 431 GHz. The total power consumption of the array including the frequency multiplier chain for injection locking is 147 mW, among which only 28.6 mW is consumed by an individual pixel including the IF LNA (∼4 mW).

Fig. 15 also shows an imager prototype incorporating a Cassegrain reflector and an 1 × 3 TRX pixel array. A conventional parabolic profile with a diameter of 6 cm and a focal length of 3 cm is employed for the main reflector. The measured half-power beamwidth is ∼0.7°. With the reflector, an EIRP increase of ∼27 dB is observed. To demonstrate imaging in a visually impaired condition, images are captured with and without heavy fog as shown in Fig. 16. A 6 × 6-cm^2 PCB is used as a target and placed on a 2-D linear scanner at 3 m from the imager. The modulation rate and deviation of the FSK TX signals are 5 and 360 MHz. The amplitude of the tone at $f_{IF} + f_m$ (365 MHz) is used to form images. There is no significant difference between the images. Both images clearly show the PCB and the SNR's in both cases are over 30 dB (resolution bandwidth = 100 Hz). There SNR's indicate the imager module can be used to image objects at larger stand-off distances. With a 15-cm diameter reflector, it should be possible to increase the distance close to 100 m. Since the IF output also includes the phase information, use of advanced image processing to improve image quality should be possible.

The transmitter and receiver of the concurrent transceivers can also be used to incorporate reflection mode imaging on smartphones (Fig. 17) for seeing through packages to detect contents without opening them; walls to locate wires and pipes; decorative pieces to detect air voids and cracks, and

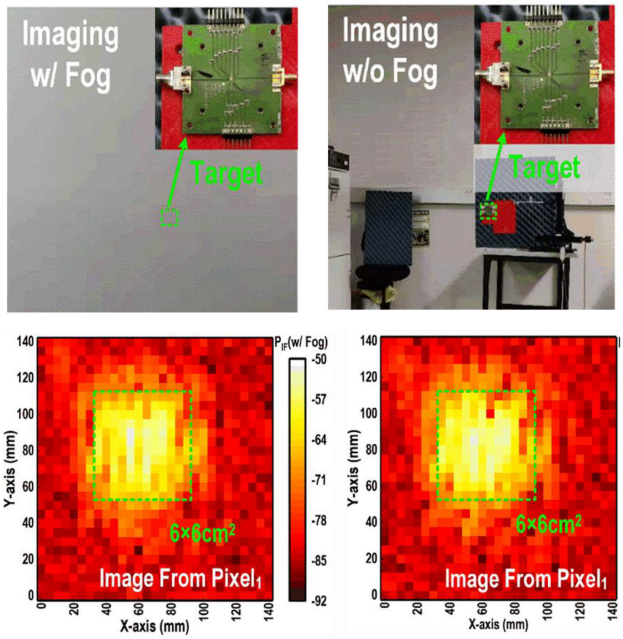

FIGURE 16. Images of a 6 cm × 6 cm PCB 3-m away with and without fog [13].

FIGURE 17. Reflection mode imager using arrays of TX and RX pixels incorporated on a smartphone.

TABLE 3. Link margin analyses for a reflection mode imaging system operating at 400 GHz for a range of 5 cm and a 2-mm² imaged object size (radar cross section, σ).

Short Range Imaging at Range of 50 mm (3 x 3 TX pixels and 1 RX pixel)			
Frequency	400 GHz	Noise figure	40 dB
Transmitted power (P_t)	-18 + 9.5 dBm	B (Bandwidth)	30 dB-Hz
Antenna gain (G^2)	3.5 + 9.5 + 3.5 dB	Noise floor	-104 dBm
Radar cross section (σ)	3 dB-mm²	R^{-4} @50 mm	-68 dB/mm⁴
$\lambda^2/(4\pi)^3$ @400 GHz	-35.5 dB-mm²	Received power (P_r)	-92.5 dBm
kT	-174 dBm/Hz	SNR	11.5 dB

many others. However, this see-through technology poses significant privacy risks since this capability is that used for security screening at airports. Because of this, for the use on smartphones, the range should be limited to ∼10 cm or less. Table 3 summarizes a link analysis for a simple lens-less reflection mode imaging system operating at 400 GHz with a range of 5 cm and an imaged object size of 2-mm² (radar cross section, σ). With 3 × 3 transmitters and a receiver, an SNR of 11.5 dB can be provided. These transmitters can also be made to beam steer [65].

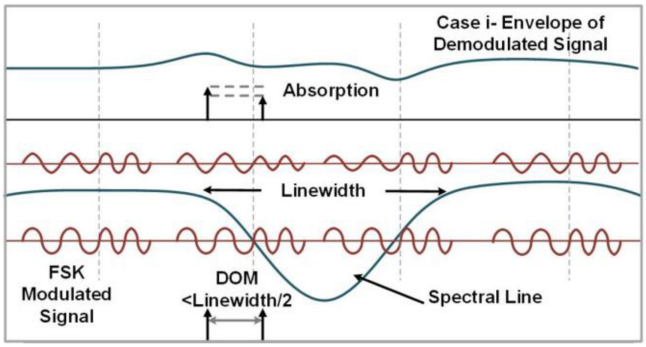

FIGURE 18. Interaction of an FM signal with a molecular line [2].

B. ELECTRONIC SMELLING

Electronic smelling can be emulated by gas sensing utilizing rotational spectroscopy [6], which can be used to identify a wide variety of gases and to quantify their concentrations. Considering how smell is used in daily life, the application opportunities should be almost limitless. A 225–280-GHz receiver and a 205–255-GHz transmitter for rotational spectroscopy have been demonstrated using a 65-nm CMOS technology [34], [67]. The width of spectral lines is ∼1 MHz or Q of the lines is more than 200,000. Because of this, the lines of different gases do not overlap. Additionally, often there are multiple lines for a given molecule, which allows multiple checks for identification. These make the specificity of technique almost absolute [6].

The requirements of a receiver for rotational spectroscopy differ from those for communication. The receiver needs to detect weak energy absorption in the presence of much larger (10^6 times larger) baseline variations [6] instead of detecting small signals in the presence of noise. The baseline variations are due to standing waves in a sample cell and other phenomena. A frequency-modulated (FM) transmitted signal is used to enable detection of small absorption dips. The modulation is also used to mitigate the impact of the RF output power variations with frequency.

The two tones of an FM signal in Fig. 18 are absorbed differently depending on its relative position to a molecular absorption line and results an FM-to-AM conversion of the transmitted signal. The difference of absorption also depends on the depth of modulation (DOM) and is maximized when the two tones are separated by a half of the linewidth. The widths of spectral lines for different molecules are not the same. Hence, an ability to vary DOM is desired. The AM signal resulting from the interaction with a molecular spectral line is typically amplified and filtered using a lock-in technique after detection. A lock-in amplifier is a homodyne receiver using the source for frequency modulation as the LO. The receiver includes a narrow band low-pass filter to reduce output noise.

A block diagram of a receiver for rotational spectroscopy is shown in Fig. 19, which includes a 210–305-GHz RF front-end composed of an on-chip dipole antenna [34],

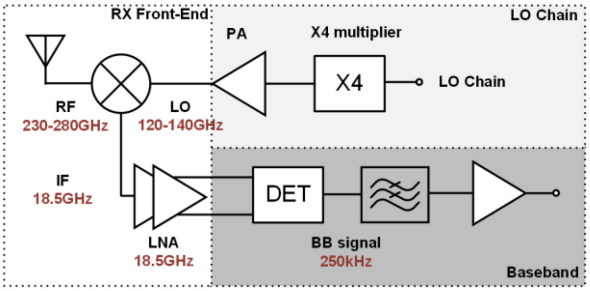

FIGURE 19. Receiver for electronic smelling using rotational spectroscopy [68].

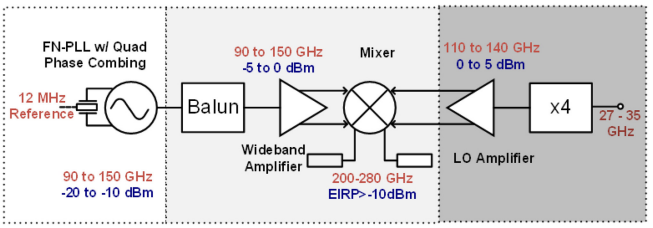

FIGURE 20. Transmitter for electronic smelling using rotational spectroscopy [67].

a 2nd-order subharmonic mixer and a 20-GHz low-noise Intermediate Frequency amplifier [6]. The RF front-end achieves a minimum DSB noise figure of 11 dB. The receiver also includes an AM detector, a baseband amplifier and a frequency-multiply-by-4 circuit for generation of LO around 130 GHz. It employs both lower and upper side LO injections to increase the operating frequency range.

The transmitter shown in Fig. 20 [67] includes a 200–280-GHz RF front-end composed of an on-chip dipole antenna, a broadband amplifier and an upconversion mixer. The RF front-end can deliver a peak output power of −1 dBm. When the input power is −20 dBm, the output power is −8 dBm. The incident power to a sample cell of a rotational spectrometer should be −30 to −20 dBm to avoid saturation of molecule, which limits the dynamic range for concentration measurements. This moderate incident power requirement makes the electronic smelling application well suited for CMOS realization. The transmitter also includes a fractional-N synthesizer with an RF step of less than 1 kHz and a frequency-multiply-by-4 circuit for generation of LO around 130 GHz. Once again, both lower and upper side LO injections are used to increase the operating frequency range.

Because of the high Q of molecular lines, rotational spectroscopy systems need an accurate frequency reference which can be costly. Fortunately, this can be circumvented by using the lines of known molecules in the system such as H_2O as a frequency reference. A frequency stability below 1 part per billion has been demonstrated for a rotational line [70]. A spectroscopy setup incorporating the CMOS transmitter and receiver IC's in Fig. 21 used the line at 242.626 GHz [67] to detect Ethanol in a human breath sample, demonstrating that highly integrated CMOS systems can support important and practical applications at 200–300 GHz.

C. COMMUNICATION

High data-rate wireless communication [8], [9], [72], [73], [74], [75], [76], [77], [78], [79], [80] and wireline communication over dielectric waveguides [7], [81], [82], [83], [84] are also key submillimeter-wave applications. The ever-increasing need for a higher data communication capacity is fueling the interest for communication at millimeter and submillimeter-wave frequencies [85] due to the availability of wide frequency bands that could be allocated for communication. A 240-GHz highly integrated QPSK transceiver for 16-Gb/s [8] wireless communication, a 300-GHz RF transmitter front-end that can support 105-Gb/s (32-QAM) communication [9], and a 390-GHz transmitter for 28-Gb/s BPOOK communication [80] and many others [72], [73], [74], [75], [76], [77], [78], [79] have been demonstrated in CMOS.

The challenges that are limiting deployment of submillimeter-wave communication systems are degradation of the circuit performance and increasing power consumption with operation frequency. These challenges however could be tolerated if the capacity power efficiency (CPE) of a link [bits/Joule] or capacity/power consumption can be improved. CPE for wireless communication based on Shannon's Capacity is

$$\frac{\text{Capacity}}{P_{DC}}\left[\frac{\text{bits}}{J}\right]=\frac{B}{P_{DC}}\log_2\left[1+\left(\frac{P_{TX}}{FkTB\lambda^2}\right)\left(\frac{\eta_{TX}\eta_{RX}A_{TX}A_{RX}}{R^2}\right)\right], \tag{2}$$

where the bandwidth is B. The second term in the argument for $\log_2$ is the SNR at the receiver output, and λ is the wavelength, R is the link distance, P_{TX} is the power delivered to the transmitter antenna, F is the receiver noise factor, and η_{TX} and η_{RX} are the efficiencies of transmitter and receiver antennas while A_{TX} and A_{RX} are the transmitter and receiver antenna aperture areas. As the operating frequency is increased, λ decreases and because for a given fractional bandwidth, the absolute bandwidth increases, the required Q-factors of input and output matching networks to achieve a given bandwidth increase. These higher Q-factors can be used to reduce the matching network losses and to increase the gain per stage of amplifiers needed to generate and down convert RF signals. These in turn reduce the output power requirements of amplifiers as well as reducing the number of stages and helping to lower the power consumption increase. Both, the decreasing λ and increasing Q-factors (given bandwidth) mitigate the deleterious impact to CPE of the increasing noise figure and decreasing transmitter output power with the operating frequency. CPE is also the inverse of energy efficiency.

Table 4 summarizes the CPE of subset of CMOS transmitter-receiver combinations in the literature operating at 28 GHz to 300 GHz. For simplicity, the aperture efficiencies are assumed to be unity and the atmospheric loss is ignored. At ranges of 10 and 1000 m, CPE's when an aperture size is 10 cm^2 or 10-cm^2 CPE for a 315-GHz

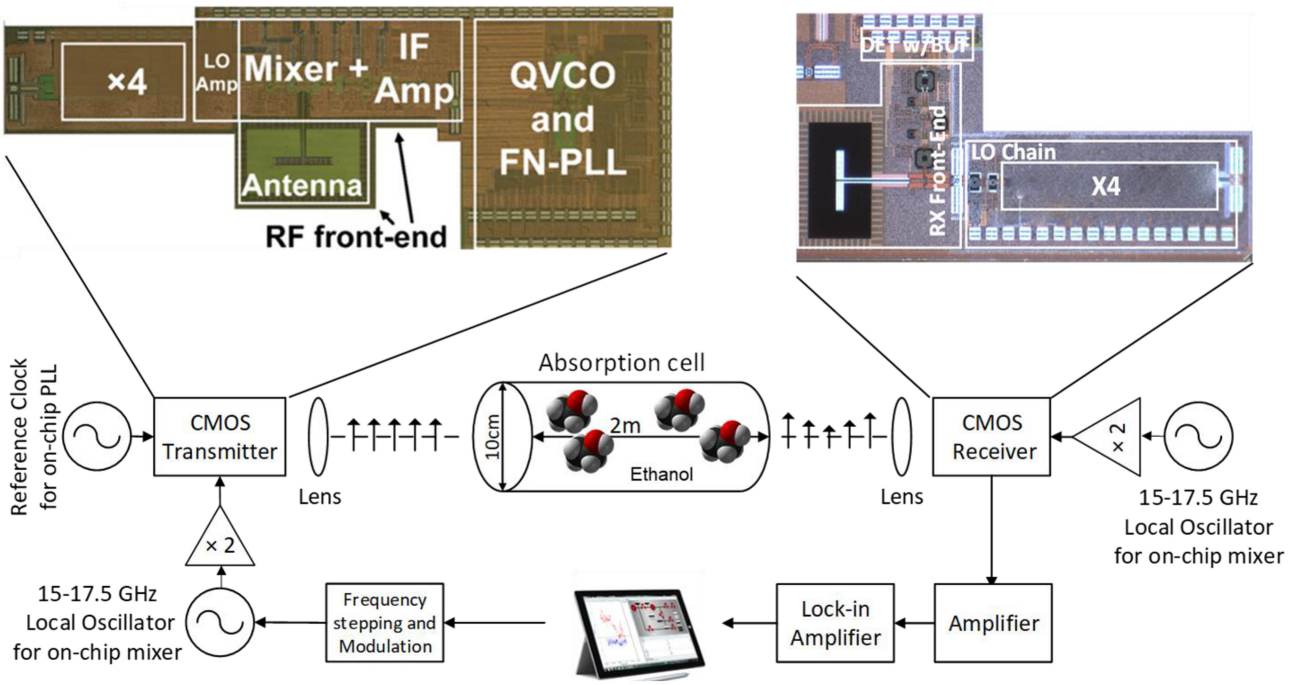

FIGURE 21. Rotational spectroscopy setup utilizing CMOS transmitter and receiver IC's [67].

TABLE 4. CPE [bits/joule] for CMOS transceivers in the literature.

TX/RX Parameters	[86]	[87]	[77]	[72]	[76]
Frequency (GHz)	28	73	180	265	300
Peak power (mW), P_{TX}	63	6.3	0.45	0.7	0.1
DC power, P_{DC} (mW)	(TX 299, RX 148)	(TX 148, RX168)	(TX 200, RX 126)	(TX 890,RX 897)	(TX 350, RX 195)
RF Bandwidth, B_{TX} (GHz)	2.5	10	40	20	40
l (mm)	10.7	4.1	1.67	1.1	1
DSB NF of RX (dB)	4.1	5.5	15.6	19.9	19
State of art DSB NF (dB)	2	4.5	9	11	12
Technology	65-nm CMOS	22-nm FinFET	65-nm CMOS	40-nm CMOS	65-nm CMOS
CPE 10 cm^2 at 10 m	$1.5x10^{11}$ ($1.5x10^{11}$)	$8.6x10^{11}$ ($8.8x10^{11}$)	$1.6x10^{12}$ ($2.0x10^{12}$)	$2.1x10^{11}$ ($2.8x10^{11}$)	$8.7x10^{11}$ ($1.1x10^{12}$)
CPE 10 cm^2 at 100 m	$9.2x10^{10}$ ($9.8x10^{10}$)	$4.1x10^{11}$ ($4.3x10^{11}$)	$3.8x10^{11}$ ($7.4x10^{11}$)	$6.8x10^{10}$ ($1.3x10^{11}$)	$1.8x10^{11}$ ($3.9x10^{11}$)
CPE 10 cm^2 at 1000 m	$3.7x10^{10}$ ($4.3x10^{10}$)	$4.9x10^{10}$ ($5.8x10^{10}$)	$7.6x10^{9}$ ($3.3x10^{10}$)	$2.2x10^{9}$ ($1.4x10^{10}$)	$3.1x10^{9}$ ($1.5x10^{10}$)
CPE 100 cm^2 at 1000 m	$9.2x10^{10}$ ($9.8x10^{10}$)	$4.1x10^{11}$ ($4.3x10^{11}$)	$3.8x10^{11}$ ($7.4x10^{11}$)	$6.8x10^{10}$ ($1.3x10^{11}$)	$1.8x10^{11}$ ($3.9x10^{11}$)

( ) CPE's calculated using the state-of-the-art NF

transceiver [76] are 4.8×10^{11} and 9.0×10^{8} bits/J while that for a 5G transceiver operating at 28 GHz [86] are 9.9×10^{10} and 2.5×10^{10} bits/J, respectively. Surprisingly, at a range of 10 m, the 10-cm^2 CPE for the 315-GHz is $\sim 5\times$ higher. This is primarily due to the fact that the bandwidth of 315-GHz circuit is $\sim 10\times$ wider. At 1000 m, 10-cm^2 CPE for the 315-GHz transceiver is more than $25\times$ lower than that of the 28-GHz transceiver. When the second term or the argument of the $\log_2$ is reduced to much less than 1 due to an increase of R, then CPE becomes approximately proportional to $P_{Tx}/(P_{DC}FkT\lambda^2)$. The higher power and lower receiver noise at 28 GHz [86] overcome the higher B and $1/\lambda^2$ at 315 GHz, and the 28-GHz link has a higher CPE. When the aperture is increased to 100 cm^2, the 100-cm^2 CPE for the 315-GHz transceiver at R of 100 m is once again $\sim 5\times$ higher.

This means the CMOS circuits operating near 300 GHz already in the literature can be used to implement significantly more capacity power-efficient wireless links than 5G links. This in combination with a larger capacity and expected performance improvements should make submillimeter-wave wireless communication an important part of the future interconnected world. The main reasons for this counterintuitive conclusion about CPE are it

is proportional to B while it is logarithmically dependent on the other parameters, and the assumption for a constant antenna aperture area at varying operating frequencies which increases the passive gain of antenna with the operating frequency. As a matter of fact, CPE's for the systems using an active gain with a phased array can be multiple orders of magnitude lower. Because of this, low profile, adaptive, steerable, and easy to use apertures are key to implementing practical submillimeter-wave wireless links.

Wireline communication using a dielectric waveguide using CMOS IC's over a short distance (∼1 m) has been proposed to mitigate the complexity of high data-rate communication over copper wires as well as the challenges for implementing optical communication systems [7], [81], [82], [83], [84]. The waveguide loss target at 300 GHz is ∼8 dB/m versus −82 dB propagation loss over 1 m for wireless communication at the same frequency. Frequency-division multiplexing (FDM) and polarization-division multiplexing (PDM) can be simultaneously used to increase the data rate over a given bandwidth [83]. The use of horizontal and vertical polarization communication modes in five 45-GHz frequency bands between 157.5 and 382.5 GHz provides a total of ten channels. An aggregate data rate of 300 Gb/s could be supported with a data rate of 30 Gb/s per channel. Signals from five frequency channels can be combined using a multiplexer/combiner and used to drive a feed for a horizontally polarized mode while signals from another set of five channels can be combined and used to drive a feed for a vertically polarized mode. On the receiver side, the horizontally polarized signals are picked up by a launch for the horizontal polarization and distributed to appropriate receivers tuned to the five frequency channels for demodulation. Similarly, the vertically polarized signals are picked up, distributed and demodulated. To reduce the interference among transmitted signals in different frequency bands, modulation techniques that reduces the out-of-band emission, such as MSK [76], [77] and CPFSK [81] are preferred.

A 1-m long dielectric waveguide communication system with a bit error rate of 1×10^{-12} can be realized utilizing a transmitter with an output power of −6 dBm and a demodulator with a DSB noise figure of 18 dB, which have already been demonstrated at ∼300 GHz using 65-nm CMOS [75], [83]. Once again, referring back to Figs. 5 and 6, the CMOS transmitter and receiver performance at ∼300 GHz can be better than that demonstrated thus far for dielectric waveguide communication, and 400-GHz transceivers with adequate performance should also be possible [36], [80]. This section presented expanded and updated discussions in [2] and [3], and additional contents from [13].

VII. FUTURE OF CMOS SUBMILLIMETER-WAVE CIRCUITS AND SYSTEMS

It is certain that further efforts will improve the performance of CMOS transmitters and receivers operating at 300–500 GHz. Multiple high-power sources using the MOS transistor nonlinearity for frequency multiplication [27], [28], [31], [32] and some receivers [38] rely on signal swings well above the limits recommended by the CMOS foundries. This is a major concern and studies are needed to better understand the lifetime implications.

Even at frequencies above 500 GHz, improvements are expected. As mentioned, using a frequency multiplier formed with a symmetric accumulation mode MOS varactor in CMOS, it should be possible to generate ∼0 dBm of power at ∼650 GHz [22]. Using reactive nonlinearity enables implementation of frequency multipliers with a greater efficiency than that using resistive nonlinearity including those of transistors [22]. Reactive nonlinearity in CMOS has been used to implement an upconversion mixer that generates the highest linear output power over a 30-GHz bandwidth near 300 GHz. It provides a promising approach for generating wideband modulated signals at even higher frequencies [78]. The ∼0-dBm signal at ∼650 GHz can be used as an LO signal for fundamental downconversion mixers operating up to ∼700 GHz and 2^{nd}-order harmonic mixers operating up to 1.4 THz to reduce their noise figures.

This improved noise performance, along with the output power approaching 0 dBm, will enable implementation of high-performance CMOS-integrated systems operating up to 1 THz. Area and power efficiency of submillimeter-wave circuits and integrated systems should be improved in order to expand the application opportunities. A necessary approach for improving the energy efficiency of systems and also for relaxing the efficiency and other performance requirements of circuits is better control of EM energy propagation using external passive optics, including electronically steerable reflectarrays [88], [89], [90], [91] and waveguiding structures [7], [81], [82], [92]. Improving their performance, and making them easy to use, adaptable, steerable, and affordable are critical research opportunities and challenges. For the optics using steerable electronic reflectarrays, because of the dimensional controls and the number of elements needed to form the arrays for submillimeter-wave applications, solutions utilizing microelectronic and solid-state circuit design techniques [88], [89] should be of great interest.

VIII. CONCLUSION

The CMOS circuits discussed in Section II have been used to demonstrate highly integrated transmitters and receivers operating up to ∼300 GHz for rotational spectroscopy [34], [67], a 230-GHz molecular frequency reference that exhibits stability approaching that of atomic clocks [70], wireless communication at 240–390 GHz [8], [9], [72], [73], [74], [75], [76], [77], [78], [79], [80], radar imaging at 200–430 GHz [13], [59], [60], [61], [62], and incoherent detector arrays for transmission mode imaging at frequencies up to 1 THz [52], [53], [54]. In addition, techniques for high-impedance broadband on-chip voltage measurements needed for BIST [14], [40] and packaging of circuits with on-chip antennas operating up to 300 GHz in a low-cost QFN package [15] are demonstrated. These

mean all the key technologies needed to produce affordable submillimeter-wave CMOS microsystems for everyday applications have already been demonstrated.

It is certain that further efforts will improve the performance, including power efficiency of CMOS transmitters and receivers operating at 300–500 GHz. Even at frequencies above 500 GHz, improvements are expected. Additionally, the BiCMOS technologies with SiGe-HBT $f_{\max}$ of greater than 500 GHz being developed should also provide an alternate means to further improve the output power and power efficiency of submillimeter-wave circuits while leveraging the manufacturing capabilities of the Silicon IC industry. More significant improvements of the system performance are expected from better controlling EM energy propagation using external passive optics and waveguiding structures. Improving their performance, and making them easy to use, adaptable. steerable, and affordable are critical research opportunities and challenges. These efforts will enable implementation of CMOS-integrated systems operating up to 1 THz that have an improved imaging resolution at a given form factor; can image through materials with greater ranges of absorption and thicknesses; can detect a wider variety of molecules; and can support even higher communication capacity with an improved energy efficiency.

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