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Flexible Interlinking Converter With Enhanced FRT Capability for On-Board DC Microgrids

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ABSTRACT In this paper, a flexible interlinking dc/dc converter with enhanced FRTC is proposed to satisfy the advanced requirements of modern on-board DC MGs; the topology uses a non-isolated switched capacitor-type multilevel converter in combination with a cascaded step up/down converter to facilitate the incorporation of various types of energy storage and/or production units in a DC MG. Overall, a high voltage conversion ratio between the dc bus of the MG and the power unit is achieved. The proposed configuration facilitates the CCM operation of both the power unit and the DC MG and it is characterized by bidirectional power flow capability, enhanced FRTC, zero switching losses for the multilevel converter, limited complexity of the control scheme (compared to the counterpart multilevel solutions) and low real-time communication demands, corresponding so to the increasing flexibility needs of the EMS of modern MGs. The mathematical analysis and the dynamic performance of the control scheme of the proposed topology concept are evaluated via MATLAB/Simulink simulations and real-time CHIL tests, with the use of a 1202 dSPACE platform and an external dsPIC30F4011 microcontroller.

INDEX TERMS Control hardware-in-the-loop, dc microgrids, high step-up/down voltage ratio, multilevel dc/dc converter, switched capacitors.

NOMENCLATURE

(E)TM(s)	(electrified) transport mean(s).
MG(s)	microgrid(s).
RES	renewable energy source(s).
DG(s)	distributed generator(s).
ESS(s)	energy storage system(s).
BES	battery energy storage.
SCs	supercapacitors.
dc (DC)	direct current (A).
M/AEA(S)	more/all electric aircraft(ship).
H/M/LVDC	high/medium/low voltage dc (V).
λ	voltage conversion ratio.
DAB	isolated dual active bridge.
ZVS/ZCS	zero voltage/current switching.
MMC	modular multilevel converter.
FRTC	fault ride-through capability.
SAF	series active filter.
APU(s)	auxiliary power unit(s).
EMS	energy management system/strategy.
n	number of capacitive components.
CCM, DCM	continuous, discontinuous conduction mode.
CHIL	control hardware-in-the-loop.
DSP	digital signal processor.
C	capacitance (F).
$C_0 \div {}_{n\text{-}1}$	capacitance of 0÷n-1 component (F).
HBC	full bridge converter.
G_1–G_4	HBC switches.
D_1–D_4	HBC diodes.
G_p	switches for the parallel connection of $C_0 \div C_{n-1}$.
G_s	switches for the series connection of $C_0 \div C_{n-1}$.
G_L	switches for the connection of n-1 cells.
G_{s1}, G_{s2}	step up, step-down operation switch.
D_{s1}, D_{s2}	step up, step-down operation freewheeling diode.
$S_0 \div S_5$	switching states of the topology.

H	hysteresis zone (A).
i_{bus}, I_{bus}	instantaneous, average dc-link current (A).
i_s, I_s	instantaneous, average current of the power unit (A).
i_c	instantaneous capacitor current (A).
$i_{c0 \div 5}$	instantaneous capacitor current at $S_0 \div S_5$ (A).
V_{bus}	dc bus voltage (V).
V_s	power unit voltage (V).
v_c, V_c	instantaneous, average capacitor voltage (V).
$v_{c0 \div 5}$	instantaneous capacitor voltage at $S_0 \div S_5$ (V).
L_{bus}, L_s	dc bus, power unit inductance (H).
v_{Lbus}, V_{Lbus}	instantaneous, average dc bus inductor voltage (V).
v_{Ls}, V_{Ls}	instantaneous, average inductor voltage of the power unit (V).
d	duty cycle.
T_{sw}, f_{sw}, ω_{sw}	switching period (s), frequency (Hz) angular frequency (rad/s).
TF(s)	transfer function(s).
T(s)	TF of the step-up operation.
F(s)	TF of the step-down operation.
G_{do}	open-loop gain of the TFs (s).
ω_0	$L_{bus}C$ resonance angular frequency of the TFs (rad/s).
ω_r	$L_{bus}C$ resonance angular frequency (rad/s).
k	L_{bus} to L_s ratio.
Λ	factor of the numerator of the TF ($1/s^2$).
M, N	factors of the numerator of the TF (1/s).
A	I_{bus} to $I_{c,rms}$ ratio.
$I_{c,rms}$	rms capacitor current (A).
MOP	maximum operating point.
$I_{ref(max)}$	(maximum) i_{bus} reference (A).
$P_{sw,loss(,max)}$	(maximum) switching losses (W).
V_{DD}, I_D	base values for drain-source voltage (V), drain current (A).
E_{on}, E_{off}	turn on, off switching energy loss (mJ).
ΔI_{bus}	steady-state peak to peak variation of i_{bus} (A).
$\Delta I_{s(max)}$	(maximum) steady-state peak to peak variation of i_s (A).
δ_1, δ_2, δ_3	percentage values.
$L_{bus,max/min}$	maximum/minimum L_{bus} (H).
$L_{s,max/min}$	maximum/minimum L_s (H).
C_{min}	minimum C (F).
$k_{max/min}$	maximum/minimum k.
$\omega_{r,max/min}$	maximum/minimum ω_r (rad/s).
$\omega_{sw,max/min}$	maximum/minimum ω_{sw} (rad/s).
$V_{c,ref,max/min}$	(maximum/minimum) v_c reference (V).
x, X	instantaneous, average input variable.
u, U	instantaneous, average independent input variable.
y, Y	instantaneous, average output variable.
A_1, A_2, A_{avg}	3×3 algebraic matrixes.
B_1, B_2, B_{avg}	3×2 algebraic matrixes.
C_1, C_2, C_{avg}	1×3 algebraic matrixes.
D_1, D_2, D_{avg}	1×2 algebraic matrixes.
sI	unity (identity) Laplace matrix.

I. INTRODUCTION

A. MOTIVATION AND APPLICATION UNDER STUDY

Nowadays, the more the electrification level of the TMs' increases, the more the electrical system of a modern ETM becomes comparable to a land-based autonomous MG [1]; in light of this, the incorporation of various RES (e.g., photovoltaics, DGs) and alternative energy sources (e.g., fuel cells), other energy harvesters (such as thermoelectric generators) as well as multiple buses of different voltage levels in the ETM's powertrain has become a trend in research community and automotive industry, aiming at the reduction of the use of fossil fuels and green-house gases' emissions, consequently. On the other hand, the incremental penetration of RES, ESSs (e.g., BES, SCs) and energy harvesters with inherent DC operation, as well as the growing ratio of DC loads in ETMs' on-board power systems, seems to pave the way for further utilization of DC systems or even for the adoption of pure DC onboard MGs [1]. For example, in M/AEA a purely HVDC distribution architecture, utilizing 270 V or 540 V (±270 V) main DC buses, has been widely investigated and proposed [2]. Furthermore, in recent M/AES concepts, a wide range of voltage levels of the main DC distribution architecture has been proposed, using 1-35 kV MVDC [3] – depending on the different types/classes of the vessels – as well as lower DC buses, such as 690 V [1], [4].

B. LITERATURE REVIEW

Several voltage step-up topologies have been proposed in the literature, regarding the appropriate interlinking of the previously mentioned DGs and/or loads in a modern DC MG, dealing in particular with the case of the high/medium power ones, where high voltages are usually utilized at the MG side [5], [6], [7], [8]. As regards the state-of-the-art bidirectional converters that are proposed for the dc/dc high power conversion in DC MGs, these are characterized by high λ capability, good dynamic performance (thanks to direct current control) and modularity (in system/cell lever or in both). In more detail, the isolated dual active bridge (DAB) constitutes the most promising candidate so far [9], [10], [11], [12], [13] providing advantages such as galvanic isolation, high-power density, fast power flow reversal, step-up and step-down operation (with high λ), applicability of synchronous rectification, inherent fault isolation capability. In addition, some other isolated converter topologies based on the DAB, such as the resonant type DAB [14], [15], have been proposed with the prospect of expanding the soft-switching region (realizing both ZVS and ZCS), where a capacitor and/or an inductor can be placed in series with the transformer. However, these converters suffer from well-known disadvantages regarding the magnetically coupled circuit (i.e., incorporation of a high-frequency – though relatively bulky – transformer which moderates power density and raises saturation issues) and the complexity of the control scheme to achieve soft/zero switching operation. On the other hand, a non-isolated multilevel converter topology [16], [17], such as the MMC, is an alternative attractive

solution for high-power conversion in modern DC MGs [18], [19], [20]. The merits of this converter over conventional ones are the inherent redundancy, the current-fed control that facilitates self-balancing of the capacitors, the low device ratings, the very low output harmonic distortion, the scalability and the possibility of common dc-bus configuration for multidrive applications; on the contrary, the practical bottlenecks that may prohibit the use of the MMC for higher voltage and power levels (as reported in [18]) are: the voltage stresses across the flying capacitors that may lead to a bulky capacitor bank, the operational limitations due to the complex charging pattern and the hard switching characteristics (that limit the increase of the switching frequency in practice). It is worth noting that the common characteristic of interest, regarding the above-mentioned solutions, is their default inability of providing FRTC (due to the magnetic coupling of the transformer-based converters and the voltage fed circuitry/configuration in combination with the different state of charge of the capacitors in each sub-module of the multilevel topologies); however, FRTC constitutes a critical/important feature of the contemporary standards regarding the power quality in DC MGs [20], [21].

C. CONTRIBUTION OF THE PRESENT PAPER

Under this light and with respect to the recently published/introduced SAF concept regarding the connection of a dynamic power unit to a DC MG via an appropriate interlinking converter (facilitating the energy flow between the DC MG and an electric machine [22], [23]), this paper aims to further extend that circuitry analysis to similar DC MG applications. Specifically, the present study proposes the series connection of various types of power units (e.g., APU, DG, BES, SCs, fuel cells, etc.) and a DC MG, being a configuration which has already proved its enhanced FRTC [22], [23]; the basic scope of the proposed circuitry concept is the facilitation of the energy transactions between the power unit (being the DC port/input of the interlinking topology) and the DC MG, as well as between DC buses with different voltage levels (as depicted in Fig. 1), through the development of a flexible EMS (serving as a modern electrical energy hub in essence). It is noted that, any converter that enables bidirectional power flow can be used in the proposed interlinking topology (which constitutes a current-fed converter in essence); the present work proposes the incorporation of a switched capacitor-type multilevel (n-level) converter [24] in combination with a cascaded step-up/down converter [25], as Fig. 2 illustrates; an appropriate (dis)charging pattern is implemented at the multilevel converter (utilizing the basic idea of a charge pump circuitry [26]), allowing for the CCM operation at each side connected to the interlinking topology, under high λ, as it will be discussed.

The advantages of the proposed concept (that will be demonstrated by the theoretical analysis and the presented results) are the following: 1) elimination of the narrow λ range of the traditional step-up/down converters (via the switched-type pattern of the capacitor-based circuit), 2) coherent design

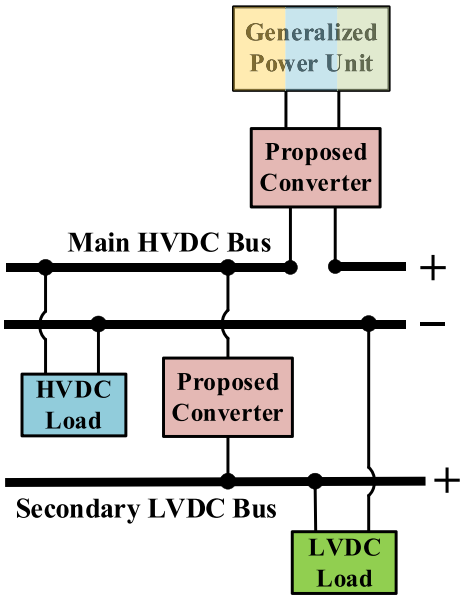

FIGURE 1. Proposed interlinking topology for DC MGs.

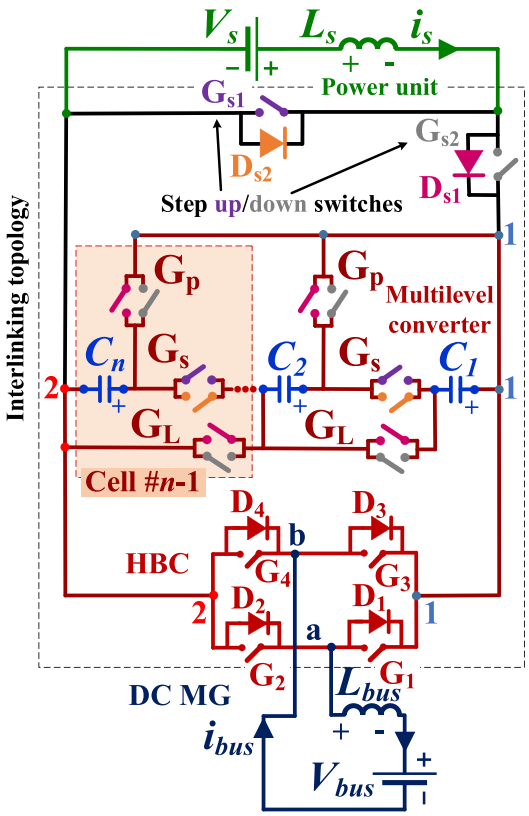

FIGURE 2. Proposed interlinking switched capacitor-type multilevel dc/dc converter for bidirectional power flow between a power unit and a DC MG.

methodology, ensuring the optimal performance of the converter (in terms of the practical components' selection) and facilitating CCM at both sides (i.e., the power unit and the DC MG), 3) flexibility feature; step-up and step-down operation, facilitating the bidirectional power flow in the interlinking

topology, enabling so a) the incorporation of various types of power units, such as energy storage and/or production ones (energy hub in essence) in the DC MG, b) the interconnection of dc buses of different voltage levels (e.g., interconnection of an HVDC and an LVDC of the MEA), c) modularity via the multiport feature of the circuitry configuration, which can be considered as a building block (comprising of any type of bidirectional power components' cells, such as BES and SCs), d) implementation of various energy management strategies, with simple real-time communication demands among the system's units (i.e., incorporated power units, multiple interlinking converter blocks and DC MG buses), 4) zero switching losses (ZCS) of the multilevel converter, 5) reliability and redundancy of the proposed topology, thanks to the availability of identical components' cells/building blocks of the interlinking converter and 6) enhanced FRTC (thanks to the current-fed configuration of the interlinking topology and the self-balancing ability of the multilevel converter's switching pattern), which is neither inherent nor practical for the common dc/dc cascaded configuration (voltage-fed converters).

It is worth noting that the main scope of this work is to introduce the basic concept/idea of this flexible interlinking topology (by proposing a series connected dc/dc converter configuration) and its circuit analysis, as well as to validate its EMS control feasibility; practical issues (such as the capacitors' health monitoring and DGs' and ESSs' actual control loops) are excluded from this – initial – study, being some interesting points for further work. The dynamic performance of the proposed switched capacitor-type multilevel converter is enhanced via the developed design algorithm, while the theoretical analysis of the proposed EMS control scheme has been verified through both MATLAB/Simulink simulations and a CHIL test-bench via a dSPACE MicroLabBox platform and an external DSP, i.e., the 16-bit dsPIC30F4011 microcontroller.

II. CIRCUIT ANALYSIS OF THE PROPOSED INTERLINKING TOPOLOGY

The basic concept of the proposed interlinking topology lies on the incorporation of a switched capacitor-type multilevel dc/dc converter between a power unit (in this study the power unit circuit is modeled as a voltage source connected in series with an inductor, as depicted in Fig. 2) and the DC MG under study (in this study the DC MG is modeled as a voltage source, whereas the series inductance is set in accordance with the desired switching frequency – as it will be discussed in Section III); a dual-mode (dis)charging pattern is implemented at the multilevel converter, facilitating so different charging and discharging rates of the capacitive unit, as it will be thoroughly explained. It is noted that for the presentation of the basic concept of the proposed charge pump pattern [25], ideal capacitors (of the same C-capacitance value per capacitor) are employed.

A. PROPOSED SWITCHED CAPACITOR-TYPE MULTILEVEL DC/DC CONVERTER

For the implementation of the proposed topology, a n-level capacitive unit along with an HBC is employed in the circuitry, as shown in Fig. 2. The input of the HBC is the capacitive unit (which is also connected to the power unit circuit), while the output of the HBC is connected to the DC MG under study. For the sake of the present analysis, the power unit is considered as the low voltage side, while the DC MG is considered as the high voltage side (thus $\lambda \geq 1$).

The operating principle of the proposed topology regarding the interlinking of a power unit (it can be considered both as a power source and a sink) and a DC MG lies on the implementation of a dual-mode (dis)charging pattern of the intermediate n-capacitors' matrix that is incorporated in the multilevel circuitry ($C_1 \div C_n$); as Fig. 2 depicts, $n-1$ capacitor cells are needed for the construction of a n-level capacitor matrix. For the implementation of the bidirectional power flow, i.e., from the power unit to the dc bus (voltage step-up operation) and vice versa (voltage step-down operation), each capacitor cell must be comprised of three (3) bidirectional switches that facilitate the parallel and series connection of the capacitors of the $n-1$ cells.

Specifically, as Fig. 2 illustrates, a pair of bidirectional switches allows for the parallel connection of the capacitors (G_p, G_L) while one bidirectional switch (G_s) serves their series connection, so that a n-level topology is constructed. Moreover, at the power unit side, the step-up operation is achieved by the using G_{s1} and D_{s1}, while the step-down operation is achieved by using G_{s2} and D_{s2}.

As it will be analytically explained, the number of levels (n) that facilitate the bidirectional power flow in CCM operation of the power unit circuit, depends on λ. The step-up operation of the proposed topology is analytically described in the following subsection (the mathematical description of the step-down operation can be derived accordingly).

B. SWITCHING OPERATION OF THE CIRCUITRY

Table 1 presents the status of the variables of the total topology, including the power unit circuit, the interlinking circuit and the DC MG of Fig. 2, according to the switching states ($S_0 \div S_5$) of Fig. 3(the switching states during step-down operation are also included). It is noted that the basic states of operation are S_0 and S_3, while S_1, S_2, S_4 and S_5 are used for the zero current switching (ZCS) of the capacitor cells' switches (transition states). In addition, the power flow regulation is imposed via the hysteresis current control that is implemented on i_{bus}, keeping it so at a constant value (I_{ref}) within a constant hysteresis zone (H). It is noted that the selection of a specific current controller type (i.e., hysteresis or peak current or average current mode control) has no effect on the operating principles of the proposed scheme.

Fig. 3 presents the switching states during the step-up operation of Fig. 2, in which the power flows from the power unit to the DC MG. During S_0, G_{s1} is on and i_s increases in

TABLE 1. Bidirectional Power Flow: Voltage Step-up/Down Modes. Switching States of the Power Unit, Multilevel Converter and DC Bus (Fig. 3)

State	Power Flow: Power Unit (PU) → DC bus (Voltage Step-up)								Power Flow: DC bus → Power unit (Voltage Step-down)							
	Active Switch(es)/Diode(s)			v_{Ls}	v_{Lbus}	i_s	i_{bus}	v_c	Active Switch(es)/Diode(s)			v_{Ls}	v_{Lbus}	i_s	i_{bus}	v_c
	HBC	PU	Cell						HBC	PU	Cell					
S_0	G_1, G_4	G_{s1}	G_s[1]	V_s	v_{c0}-V_{bus}	↑	↑	↓	G_2, G_3	G_{s2}	G_p[1], G_L[3]	v_{c0}-V_s	V_{bus}+v_{c0}	↑	↑	↓
S_1	G_1, D_3	G_{s1}	G_s[1]	V_s	-V_{bus}	↑	↓	=	G_2, D_4	D_{s2}	G_p[1], G_L[3]	-V_s	V_{bus}	↓	↑	=
S_2	G_1, D_3	G_{s1}	G_p[2], G_L[3]	V_s	-V_{bus}	↑	↓	=	G_2, D_4	D_{s2}	G_s[2]	-V_s	V_{bus}	↓	↑	=
S_3	D_2, D_3	D_{s1}	G_p[2], G_L[3]	V_s-v_{c3}	-V_{bus}-v_{c3}	↓	↓	↑	D_1, D_4	D_{s2}	G_s[2]	-V_s	V_{bus}-v_{c3}	↓	↓	↑
S_4	G_1, D_3	G_{s1}	G_p[2], G_L[3]	V_s	-V_{bus}	↑	↓	=	G_2, D_4	D_{s2}	G_s[2]	-V_s	V_{bus}	↓	↑	=
S_5	G_1, D_3	G_{s1}	G_s[1]	V_s	-V_{bus}	↑	↓	=	G_2, D_4	D_{s2}	G_p[1], G_L[3]	-V_s	V_{bus}	↓	↑	=

[1] ZCS: zero current turn on (S_5) and zero current turn off (from S_1 to S_2).
[2] ZCS: zero current turn on (S_2) and zero current turn off (from S_4 to S_5).
[3] G_L: cell n-1 must be activated in all states (S_0-S_5) in order to activate n-1 levels of the topology of Fig. 2.

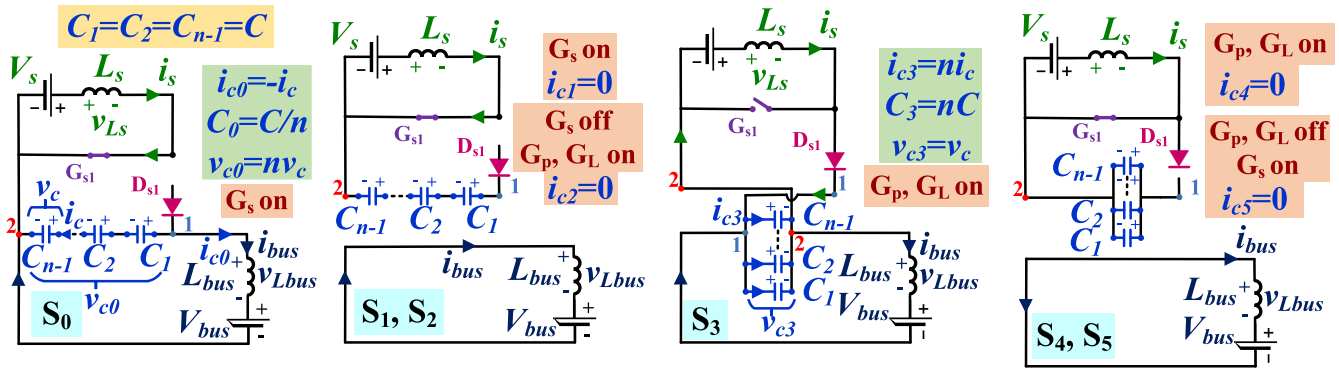

FIGURE 3. Switching states (S_0÷S_5) of the proposed interlinking topology for step-up operation.

the face of V_s. At the same time, G_{p1}, G_{p2} are off, G_s, G_{n-1}, G_1 and G_4 are on, so that i_{bus} increases in the face of nv_c-V_{bus} while the capacitors discharge. Regarding S_0, the following equations are derived:

$$\left.\frac{di_s}{dt}\right|_{S_0} = \frac{v_{Ls}}{L_s} = \frac{V_s}{L_s} \tag{1}$$

$$\left.\frac{di_{bus}}{dt}\right|_{S_0} = \frac{v_{Lbus}}{L_{bus}} = \frac{v_{c0} - V_{bus}}{L_{bus}} = \frac{nv_c - V_{bus}}{L_{bus}} \tag{2}$$

$$\left.\frac{dv_c}{dt}\right|_{S_0} = \frac{i_c}{C} = -\frac{i_{bus}}{C} \tag{3}$$

S_0 ends when i_{bus} reaches the upper limit of the hysteresis zone (I_{ref} +H/2). At this point, G_4 turns off (S_1 begins) and i_{bus} decreases in the face of -V_{bus}, while i_c becomes zero. Following that, G_s turns off (zero current switch) and S_2 begins, while i_{bus} keeps decreasing.

Next, at the time spot when i_c reaches zero (according to Table 1) S_3 starts; G_{s1} turns off, i_s decreases in the face of V_s-v_c and the capacitors charge. At the same time, G_{p1}, G_{p2}, G_{n-1} are on, G_s is off and G_1 turns off, so that i_{bus} decreases in the face of -v_c-V_{bus} and the capacitors charge. As regards S_3, the following equations are derived:

$$\left.\frac{di_s}{dt}\right|_{S_3} = \frac{v_{Ls}}{L_s} = \frac{V_s - v_{c3}}{L_s} = \frac{V_s - v_c}{L_s} \tag{4}$$

$$\left.\frac{di_{bus}}{dt}\right|_{S_3} = \frac{v_{Lbus}}{L_{bus}} = \frac{-v_{c3} - V_{bus}}{L_{bus}} = \frac{-v_c - V_{bus}}{L_{bus}} \tag{5}$$

$$\left.\frac{dv_c}{dt}\right|_{S_3} = \frac{i_c}{C} = \frac{i_s + i_{bus}}{nC} \tag{6}$$

S_3 ends when i_{bus} reaches the lower limit of the hysteresis zone (I_{ref} -H/2). At this point, G_1 turns on, S_4 begins and i_{bus} keeps decreasing in the face of -V_{bus}, while i_c becomes zero. Following that, G_{p1}, G_{p2} turn off at S_5 (zero current switch), while i_{bus} keeps decreasing.

Equations (1)–(6) are used for the average model analysis of the following section.

III. AVERAGE MODEL AND PERFORMANCE ANALYSIS

The average modeling of the circuitry in Fig. 3 is presented in Fig. 4; for the derivation of d, only the basic states, i.e., S_0 and S_3 of Fig. 3, are used. In addition, it is noted that a high capacitance value (C) facilitates the mathematical analysis approach, accounting for the constant capacitor voltage assumption throughout the development of the theoretical equations. Moreover, it is noted that for the sake of the simplicity of the analysis of the present section, the parasitic components of L_{bus}, L_s and C have been omitted.

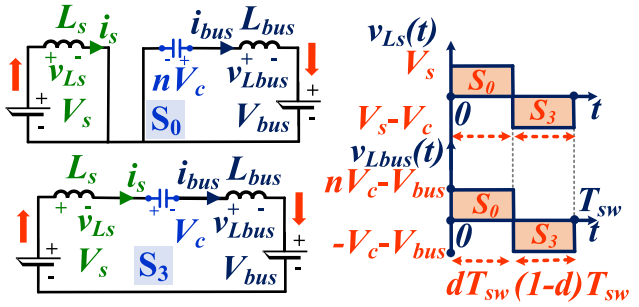

FIGURE 4. Switching states' equivalent circuit for the step-up operation of Fig. 3.

A. AVERAGE MODEL IN STEP-UP AND STEP-DOWN OPERATION

The analysis of the steady state operation ($V_{Ls} = V_{Lbus} = 0$) of Fig. 4 leads to the following set of equations:

$$V_{Ls} = 0 \Rightarrow V_s d + (V_s - V_c)(1-d) = 0 \Rightarrow V_c = \frac{V_s}{1-d} \tag{7}$$

$$V_{Lbus} = 0 \Rightarrow (nV_c - V_{bus})\, d + (-V_c - V_{bus})(1-d) = 0$$

$$\Rightarrow d = \frac{V_c + V_{bus}}{(n+1)V_c} \tag{8}$$

Taking (7) and (8) into account, d in step-up operation can be defined as follows:

$$d = \frac{1 + \overbrace{V_{bus}/V_s}^{\lambda}}{n + 1 + V_{bus}/V_s} = \frac{1+\lambda}{n+1+\lambda} \tag{9}$$

From (9) it is obvious that as n increases, d decreases, facilitating so the stable step-up operation of the proposed topology for a wide practical d range (i.e., $0.2 \div 0.8$), as λ increases. As a result, a wide λ range can be satisfied under CCM operation of the power unit's circuit.

The steady state analysis of Fig. 4 regarding the step-down operation leads to the following expression (derived in the same manner as for the step-up operation):

$$d = \frac{1}{1 + \frac{1+\lambda}{n}} \tag{10}$$

From (10) it is obvious that, as in step-up operation, a wide λ range can be satisfied under CCM operation of the power unit's circuit.

Moreover, from (7) and (8) regarding the step-up operation, the following expression can be extracted (which is also valid for the step-down operation):

$$V_c = V_s \frac{(n+1+\lambda)}{n} \tag{11}$$

B. PERFORMANCE ANALYSIS AND DESIGN OF THE PROPOSED TOPOLOGY

The circuit design (passive components and semiconductors) of the proposed topology of Fig. 2 must ensure the optimal performance at both sides of the topology (i.e., the power unit and the DC MG) during the implementation of the control scheme/pattern (according to the switching states of Table 1) under load, voltage and power supply variations. The basic feature of the proposed circuitry is the implementation of the energy transactions between two independent sources (i.e., the DC MG and the power unit) with the aid of a series-connected converter; the latter acts as a controllable voltage source (regulated by i_{bus}), facilitating the imposition of the desired level of the transferred power. Since the hysteresis current control of i_{bus} directly affects d (which is common to the total circuitry of Fig. 2) and d is regulated for the CCM of i_s, the open-loop TF $i_s/I_{ref,\max}$ to d of the proposed topology is used for designing the system's parameters that result in the enhancement of the power transfer capability of the topology – regarding both step-up and step-down operations.

As regards the step-up operation, (1)–(6) that formulate the switching model of Figs. 3 and (9), (11) that formulate the average model of Fig. 4 are used along with (A8)–(A11) of the Appendix, so that the following TF is derived:

$$T(s) = \frac{i_s(s)/I_{ref,\max}}{d(s)} = G_{do} \frac{-s^2 - Ms + \Lambda}{s\left(\frac{1}{\omega_0^2}s^2 + 1\right)} \tag{12}$$

In (12):

$$G_{do} = \frac{1}{A \cdot \omega_{sw}} \cdot \frac{(n+1+\lambda)^2}{n\left(1 + \frac{\lambda^2}{k}\right)} \tag{13}$$

$$\omega_0 = \omega_r \cdot \frac{\sqrt{n \cdot \left(k + \lambda^2\right)}}{(n+1+\lambda)} \tag{14}$$

$$M = A \cdot \omega_{sw} \cdot \frac{(\lambda - 1 - n)}{(n+1+\lambda)} \tag{15}$$

$$\Lambda = \omega_r^2 \cdot \frac{n \cdot \lambda \cdot (n - \lambda - 1)}{(n+1+\lambda)^2} \tag{16}$$

$$k = \frac{L_{bus}}{L_s} \tag{17}$$

$$A = \frac{I_{bus}}{V_c \cdot C \cdot \omega_{sw}} = \frac{I_{bus}}{I_{c,rms}} = \sqrt{\frac{n+1+\lambda}{1+\lambda+n\cdot(1+\lambda)^2}} \tag{18}$$

$$\omega_r = \frac{1}{\sqrt{CL_{bus}}} \tag{19}$$

Working similarly for the step-down operation, the following TF is derived:

$$F(s) = \frac{i_s(s)/I_{ref,\max}}{d(s)} = G_{do} \frac{s^2 - Ns - \Lambda}{s\left(\frac{1}{\omega_0^2}s^2 + 1\right)} \tag{20}$$

In (20):

$$N = \frac{A \cdot \omega_{sw}}{n} \tag{21}$$

Equations (12)–(21) clarify that:

i) The open-loop gain (G_{do}) in (13) constitutes a current amplifier at the power unit's side in essence; in light of this, a high G_{do}-value ensures a wide margin for a wide range of d-values.
ii) From (12) and (20) it turns out that G_{do} is common for both step-up and step-down operations.

The assumptions i and ii can be used to develop a rigorous design procedure that allows for the selection of the appropriate parameters' values of the proposed topology in Fig. 2, facilitating the bidirectional power flow (i.e., step-up and down operation) between the power unit and the DC MG, on the basis of the following criteria:

a) The design is oriented upon the MOP($I_{ref,\max}$), according to the specifications/inputs of the system under study – i.e., λ (V_s, V_{bus}).
b) The selected n-value facilitates the optimal dynamic response of the power unit's side for operation in CCM, in both step-up and step-down modes – dictated by the selected d from (9) and (10).
c) The expression of the open-loop gain (G_{do}) is used for the selection of the optimal components of the topology (i.e., L_{bus}, L_s, C) that facilitate its best performance. From (13) it turns out that, for fixed λ and n, G_{do} is directly increased by a large k-value and decreased by a large ω_{sw}-value. Moreover, (14) suggests that ω_0 is proportional to k and ω_r, while a large ω_{sw}-value increases M in (15) and N in (21); Λ in (16) increases with ω_r. These observations/conclusions constitute the basic tool for the design of the optimal/desired performance of the system – in terms of the frequency domain response analysis [27] of the TFs in (12) and (20).

Considering a–c, the design procedure of the proposed topology can be summarized in the following steps:

1) Define the system's specifications as inputs: MOP ($I_{ref,\max}$), λ (V_s, V_{bus}) – practically, λ is rounded up to the next integer number. Move to step 2.
2) Select d from (9), (10); e.g., setting $d = 0.5$ (optimal choice in terms of dynamics for practical converters [28]), the following is derived:

$$n = \lambda + 1 \tag{22}$$

In (22), $\lambda \geq 1$ (initial assumption, Section II, Subsection A), thus $n \geq 2$. Define n from (22) and move to step 3.
3) Define the maximum ω_{sw} ($\omega_{sw,\max}$) which results in acceptable $P_{sw,loss}$ ($P_{sw,loss,\max}$) of the interlinking HBC (with respect to commercial HBC modules for the application under study), according to the following formula [22]:

$$P_{sw,loss} \approx \frac{2}{\lambda} \cdot \frac{\omega_{sw}}{\pi} \cdot \frac{V_{bus} \cdot I_{ref}}{V_{DD} \cdot I_D} \left(n \cdot E_{on} + E_{off}\right) \tag{23}$$

Define $\omega_{sw,\max}$ from (23), for $P_{sw,loss,\max}$. Move to step 4.
4) Minimize ΔI_{bus} (in the present control implementation, $\Delta I_{bus} = H$) according to the power quality specifications of the system under study, through an appropriate H-value ($H = \delta_1 \cdot I_{ref,\max}$, e.g., $\delta_1 = 5\%$). L_{bus}-value can be calculated via the following equation (which is derived for $n = \lambda + 1$ at step 2 – $d = 0.5$), with the use of (2), (11) for the step-up operation (accordingly for the step-down operation):

$$H = \frac{V_{bus} \cdot (2+\lambda) \cdot \pi}{L_{bus} \cdot \lambda \cdot \omega_{sw,\max}} < \delta_1 \cdot I_{ref,\max} \Rightarrow L_{bus} > \frac{V_{bus} \cdot (2+\lambda) \cdot \pi}{\lambda \cdot \omega_{sw,\max} \cdot \delta_1 \cdot I_{ref,\max}} \tag{24}$$

Define $L_{bus,\min}$ from (24) and $L_{bus,\max}$ according to practical design/components' limitations, such as the inductors' costs [28]. It is noted that the $L_{bus,\max}$-value results in the minimum ω_{sw}-value ($\omega_{sw,\min}$) of the converter. Move to step 5.
5) Ensure CCM operation of the power unit, via the following condition (which is derived for $n = \lambda + 1$ at step 2, $d = 0.5$, with respect to (1) and (11) for the step-up operation and accordingly for the step-down operation):

$$L_s > \frac{V_{bus} \cdot \pi}{\lambda \cdot \omega_{sw} \cdot \Delta I_{s,\max}}, \Delta I_{s,\max} = \delta_2 \cdot \overbrace{\lambda \cdot I_{ref,\max}}^{I_{s,\max}} \tag{25}$$

Define $L_{s,min}$ from (25) and $L_{s,\max}$ according to practical design/components' limitations, such as the inductors' costs [28]. Move to step 6.
6) Define the maximum acceptable ΔV_c from the following equation (which is derived for $n = \lambda + 1$ at step 2):

$$\Delta V_c = \frac{I_{ref,\max} \cdot \pi}{C \cdot \omega_{sw}} < \delta_3 \cdot V_c \Rightarrow C > \frac{I_{ref,\max} \cdot \pi}{\omega_{sw} \cdot \delta_3 \cdot V_c} \tag{26}$$

Define $C_{,min}$ from (26). End of the design process.

Finally, the outputs of the 6-step design algorithm are: n-value (for the desired d that facilitates the optimal dynamic response of the topology; usually $d = 0.5$ is considered), $\omega_{sw,\max}$ (resulting in acceptable switching losses of the interlinking converter), acceptable range of L_{bus}, L_s values – the final choice of k value facilitates $G_{d0} >> 1$ in (13) – and $C_{\min}$-value (resulting in the optimal ω_r that leads to the optimal performance and power quality of the system, with respect to the Bode plot analysis). Specifically, with respect to the analysis of Subsection B of the present section, for the selected values of λ (step 1) and n (step 2), the maximum k-value ($L_{bus,\max}$, $L_{s,min}$) along with $\omega_{sw,\min}$ facilitate the wide open-loop gain margin as regards the response of the TFs expressions in (12) and (20) – it is evaluated with the use of the Bode plots. On the other hand, the C-value (with reference to the optimal value, $C_{\min}$) can be used for the determination of the appropriate ω_r, with respect to the frequency domain analysis of the TFs in (12) and (20), as it is highlighted in the presented results of the following section (Section IV).

It is noted that the simplified analysis (with the use of ideal components in the circuitry of Fig. 4) that yields (12)–(26)

TABLE 2. Proposed EMS; Operating Modes of the Energy Sources (DG, DC MG) and Interlinking Circuitry

Mode	power unit energy flow	power unit switches	interlinking converter operation (Table I)	DC MG energy flow
1	Supply	G_{s1} on (Table I)	Step-up	Absorption
2	Not connected	G_{s1}, G_{s2} off	Step-down	Provision
3	Storage	G_{s2} on (Table I)	Step-down	Provision
4	Not connected	G_{s1}, G_{s2} off	Step-up	Absorption

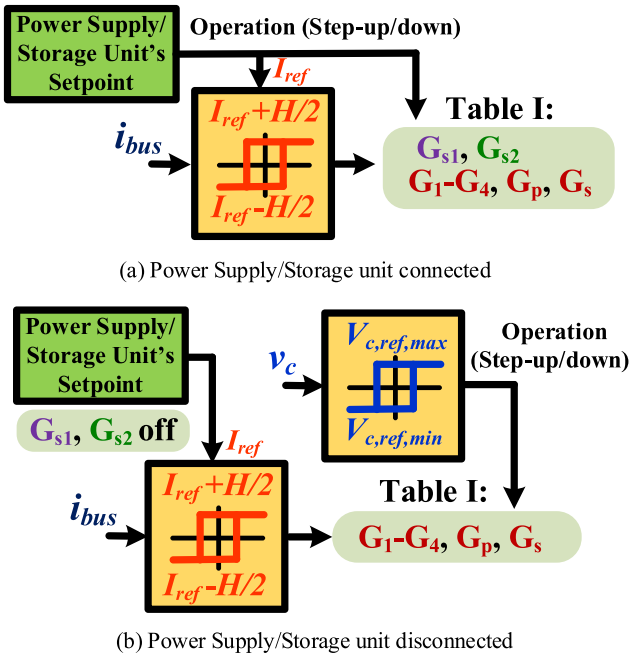

FIGURE 5. Control implementation of the proposed EMS: (a) Power supply/storage unit connected, (b) Power supply/storage unit disconnected.

does not cancel the rational of the proposed design procedure; the latter can be used in practical cases, including more detailed/accurate design parameters, such as the parasitic elements of the passive components and the bidirectional switches, that lead to a more complex system description.

C. DEVELOPMENT OF THE EMS CONTROL SCHEME

In the present subsection, the EMS scheme of the proposed topology of Fig. 2 is developed according to the energy flow schedule of the DC MG (i.e., from/to the power unit); Table 2 presents the possible operating modes of the energy sources (i.e., the power unit and the DC MG) attached to the interlinking circuitry for the proposed EMS, while Fig. 5 illustrates the block diagram of the EMS.

As regards the proposed EMS, the power unit can either provide (mode 1 of Table 2) or store (mode 3 of Table 2) energy to / from the DC MG, according to the control implementation of Fig. 5(a); in case of disconnection of the

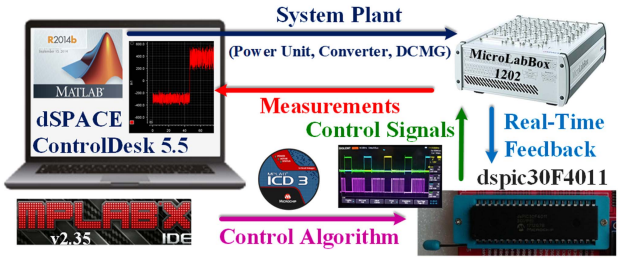

FIGURE 6. Block diagram of the CHIL set-up for the real-time validation of the proposed control scheme [22].

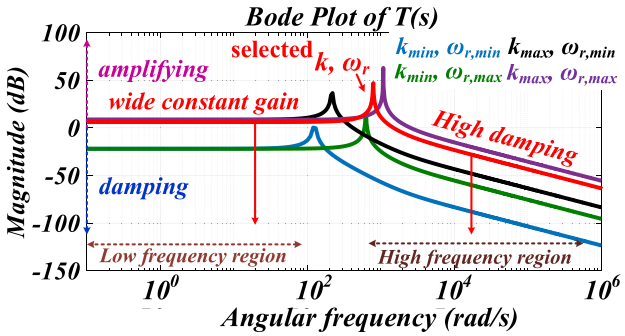

FIGURE 7. Performance optimization of the converter, with the implementation of the design algorithm on $T(s)$. Bode plots (step-up operation, $\lambda = 7$, $n = 8$) for various k and ω_r values' combinations (constant ω_{sw}).

power unit from the circuitry of Fig. 2, the multilevel converter toggles between modes 2 and 4 according to the control implementation of Fig. 5(b), so that the capacitors charge and discharge between $V_{c,ref,\max}$ and $V_{c,ref,\min}$ (hysteresis control implementation on v_c); the latter results in zero average power transfer between the DC MG and the interlinking converter during the disconnection time interval of the power unit, enforcing so the operation of the proposed topology as a flexible bond that facilitates energy transactions between the (various voltage level) buses of the MG.

On the other hand, in the case of a short circuit fault at the main DC bus side (i.e., $V_{bus} = 0$), the EMS control scheme continues its operation for $n = 1$, which in this case ensures the circuitry's operation with $d = 0.5$. In more detail, for $n = 1$ and $V_{bus} = 0$, (2) and (5) suggest that $d = 0.5$, while f_{sw} is reduced (T_{sw} is increased). At the same time, the capacitor bank continues its (dis)charging pattern, with positive average charge during each cycle of the control implementation – as it can be derived from (3) and (6); thus, constant current flow (uninterrupted hysteresis current control on i_{bus}) is provided to the DC MG during the fault, ensuring so the enhanced FRTC of the proposed scheme. However, it is worth noting that, under this condition, the power unit operates in DCM – which is dictated by (25).

IV. PERFORMANCE VALIDATION VIA SIMULATIONS & REAL-TIME CHIL IMPLEMENTATION

The performance of the developed EMS scheme of the proposed circuitry (as described in detail in Sections II and III)

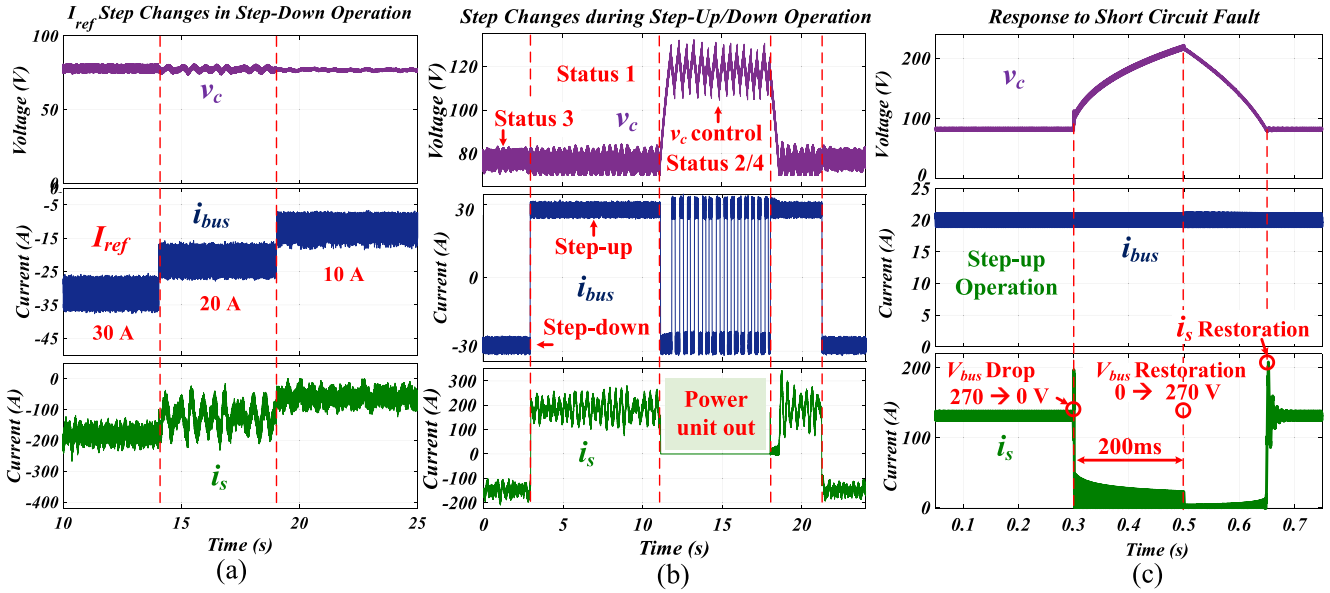

FIGURE 8. Implementation of the proposed EMS scheme: (a) I_{ref} step changes in step-down operation (real-time CHIL results, Table 3), (b) Step changes of operating mode, from step-up to step-down and vice versa (real-time CHIL results, Table 3), (c) Control response to short circuit fault (simulation results, sampling frequency 10 MHz, f_{sw} = 13.5 kHz, L_{bus} = 1 mH, L_s = 20 uH, C = 5 mF).

TABLE 3. Real-Time Model Parameters of the Proposed Circuitry

Simulink Real-Time Model Parameters
DC MG[1]: V_{bus}=270 V, $I_{ref,max}$=30 A, L_{bus}=50 mH (step 4)
Power unit: V_s=48 V, L_s=1 mH (step 5), k=50 (step 5)
Multilevel converter: λ=7 (step 1), n=8 (step 2), C=200 mF (step 6)
Control parameters: H =5 A (step 3), $V_{c,ref,max}$=130 V, $V_{c,ref,min}$=110 V f_{sw}=1kHz (step 4)
MicroLabBox 1202 sampling frequency: 25 kHz
dsPIC30f4011 frequency: 7.37 MHz

[1] It is noted that the proposed range of power rating of the developed topology (approximately 8 kW) is in alignment with dc/dc converter topologies regarding the MEA microgrid under study [13].

is validated via simulations in Simulink (MATLAB R2018b software) and real-time control implementation; Fig. 6 illustrates the block diagram of the CHIL set-up.

The dSPACE MicroLabBox 1202 platform (combined with MATLAB R2014b software) has been employed, in cooperation with an external dsPIC30f4011 DSP controller hardware; the latter receives the real-time feedback signals (i.e., i_{bus} and v_c are the microcontroller's inputs) from the simulation model (i.e., the circuitry of Fig. 2 is built in MicroLabBox 1202), implements the proposed control algorithm and sends the appropriate control signals (i.e., the on/off commands of the switches of the power unit and the multilevel converter are the microcontroller's outputs) back to the MicroLabBox 1202.

The parameters of the CHIL tests are given in Table 3 and they have been selected according to the 6-step design algorithm of Section III, Subsection B (considering the real-time sampling frequency restriction of the MicroLabBox 1202 hardware [22]). The CHIL tests of the present subsection are used as a proof of concept of the developed control method under real-time implementation, considering the influence of second order effects such as computational and PWM delays, quantization errors of the embedded ADCs in the microcontroller, deadtime of the inverter, etc. [22], [29], [30].

Fig. 7 exhibits the Bode plot of the TF in (12) – the response of the TF in (20) is similar, for various combinations of k and ω_r values (with respect to the maximum and minimum boundaries that are defined with the use of the 6-step design algorithm of Subsection B, Section III); this figure verifies that a high k-value satisfies the wide gain margin requirement of the topology, while ensuring that this constant gain is oriented at the low frequency range (which is desirable for the stable operation of the circuitry). Furthermore, the selection of an appropriate ω_r value (through C-value) facilitates the wide range of the gain damping at the high frequency region (close to switching frequency), which is another significant requirement (noise damping).

Fig. 8(a) illustrates the step-down operation of the developed control algorithm in real-time implementation, under step changes of I_{ref}, highlighting the good dynamic performance of the proposed control scheme. Moreover, Fig. 8(b) confirms the robustness of the proposed system and control algorithm during operating mode changes, dictated by the proposed EMS. Finally, Fig. 8(c) verifies the FRTC, under a 200 ms short circuit fault at the DC MG side. The dSPACE CHIL results in Fig. 8(a) and (b) show that the proposed EMS control strategy is effective under various scenarios in real time, while the high sampling frequency of the simulations in Fig. 8(c) is used for better accuracy of the presented results.

V. CONCLUSION

In the present work, a dc/dc switched-type multilevel converter is combined with a cascaded step up/down converter to

form a flexible interlinking topology, which can be incorporated in modern DC MGs, enabling the flexible connection of various power units; the proposed circuitry facilitates the wide λ range and high-power range requirements in CCM, with relatively low semiconductor switches/components count (with respect to similar counterpart multilevel topologies), while achieving zero current switching operation and reduced real-time communication demands.

The most significant advantages of the developed current-fed topology are its enhanced FRTC (which is not an inherent feature of the counterpart converters of similar high λ capability), the high dynamic performance (thanks to the current mode control) and the modularity (in cell level) that are favorable for the DC MG application under study.

The theoretical analysis has been verified by both simulations and real-time (CHIL) test results, highlighting the good dynamic response of the converter and the effectiveness of the EMS control scheme that is implemented during step changes. In summary, this work has successfully introduced the concept of this flexible interlinking topology and its control/operational principles and validated its feasibility.

APPENDIX

The state-space realization (linearized state-space model) of the proposed topology of Figs. 3 and 4 is given as follows:

$$x = [i_s\ i_{bus}\ v_c]\,,\ y = [i_s] \tag{A1}$$

$$\frac{dx}{dt} = A_{avg}\cdot x + B_{avg}\cdot u \tag{A2}$$

$$y = C_{avg}\cdot x + D_{avg}\cdot u \tag{A3}$$

$$\frac{y(s)}{d(s)} = C_{avg}\left[sI - A_{avg}\right]^{-1}\cdot\left[(A_1 - A_2)\cdot X + (B_1 - B_2)\cdot U\right] + \left[(C_1 - C_2)\cdot X + (D_1 - D_2)\cdot U\right] \tag{A4}$$

$$X = [I_s I_{bus} V_c]\,,\ U = [V_s, V_{bus}] \tag{A5}$$

$$A_{avg} = A_1\cdot d + A_2\cdot(1-d) \tag{A6}$$

$$C_{avg} = C_1\cdot d + C_2\cdot(1-d) \tag{A7}$$

As regards the step-up operation, using (A1)–(A7), (9) and (11), the state-space average model of Fig. 4 can be expressed by the following equations:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & n/L_{bus} \\ 0 & -1/C & 0 \end{bmatrix},\ A_2 = \begin{bmatrix} 0 & 0 & -1/L_s \\ 0 & 0 & -1/L_{bus} \\ 1/nC & 1/nC & 0 \end{bmatrix} \tag{A8}$$

$$B_1 = B_2 = \begin{bmatrix} 1/L_s & 0 \\ 0 & -1/L_{bus} \\ 0 & 0 \end{bmatrix} \tag{A9}$$

$$C_1 = C_2 = [1 \quad 0 \quad 0] \tag{A10}$$

$$D_1 = D_2 = [0 \quad 0] \tag{A11}$$

REFERENCES

[1] Z. Jin, L. Meng, J. M. Guerrero, and R. Han, "Hierarchical control design for a shipboard power system with dc distribution and energy storage aboard future more-electric ships," *IEEE Trans. Ind. Inform.*, vol. 14, no. 2, pp. 703–714, Feb. 2018.

[2] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft—Technology review," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5588–5599, Jul. 2019.

[3] *IEEE Recommended Practice for 1 kV to 35 kV medium-voltage dc power systems on ships*, IEEE Standard 1709-2010, 2010.

[4] J. Hou, Z. Song, H. F. Hofmann, and J. Sun, "Control strategy for battery/flywheel hybrid energy storage in electric shipboard microgrids," *IEEE Trans. Ind. Inform.*, vol. 17, no. 2, pp. 1089–1099, Feb. 2021.

[5] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[6] C. G. Zogogianni, E. C. Tatakis, and V. Porobic, "Investigation of a non-isolated reduced redundant power processing dc/dc converter for high-power high step-up applications," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5229–5242, Jun. 2019.

[7] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-power bidirectional DC–DC converter for aerospace applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4366–4379, Nov. 2012.

[8] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[9] N. Hou and Y. Li, "Communication-free power management strategy for the multiple DAB-based energy storage system in islanded dc microgrid," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4828–4838, Apr. 2021.

[10] T. Yang, F. Gao, S. Bozhko, and P. Wheeler, "Power electronic systems for aircraft," in *Control of Power Electronic Converters and Systems*, vol. 2, F. Blaabjerg Ed. Orlando, FL, USA: Academic, 2018, pp. 333–368.

[11] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[12] S. Chakraborty and S. Chattopadhyay, "Minimum-RMS-current operation of asymmetric dual active half-bridge converters with and without ZVS," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5132–5145, Jul. 2017.

[13] L. Tarisciotti, A. Costabeber, L. Chen, A. Walker, and M. Galea, "Current-fed isolated DC/DC converter for future aerospace microgrids," *IEEE Trans. Ind. App.*, vol. 55, no. 3, pp. 2823–2832, May/Jun. 2019.

[14] A. V. Mirtchev and E. C. Tatakis, "Design methodology based on dual control of a resonant dual active bridge converter for electric vehicle battery charging," *IEEE Trans. Veh. Techn.*, vol. 71, no. 3, pp. 2691–2705, Mar. 2022.

[15] H. Wu, S. Ding, K. Sun, L. Zhang, Y. Li, and Y. Xing, "Bidirectional soft-switching series-resonant converter with simple PWM control and load-independent voltage-gain characteristics for energy storage system in DC microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 995–1007, Sep. 2017.

[16] X. Li, X. Zhang, W. Jiang, J. Wang, P. Wang, and X. Wu, "A novel assorted nonlinear stabilizer for DC–DC multilevel boost converter with constant power load in DC microgrid," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11181–11192, Oct. 2020.

[17] Y. Lu, H. Wu, B. Tu, M. Li, Y. Xia, and Y. Xing, "Ultra-wide output voltage range power supply based on modular switched-converter principle," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 94–106, Jan. 2020.

[18] M. V. Soares and Y. R. de Novaes, "MMC based hybrid switched capacitor dc-dc converter," *IEEE Open J. Power Electron.*, vol. 3, pp. 142–152, 2022.

[19] X. Xiang, X. Zhang, Y. Gu, G. P. Chaffey, and T. C. Green, "Analysis and investigation of internal ac frequency to minimize ac current magnitude and reactive power circulation in chain-link modular multilevel direct dc–dc converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5586–5599, Dec. 2020.

[20] F. Zhang, W. Li, and G. Joós, "A transformerless hybrid modular multilevel DC–DC converter with DC fault ride-through capability," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2217–2226, Mar. 2019.
[21] C. Balasundar, C. K. Sundarabalan, J. Sharma, N. S. Srinath, and J. M. Guerrero, "Effect of fault ride through capability on electric vehicle charging station under critical voltage conditions," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 2, pp. 2469–2478, Jun. 2022, doi: 10.1109/TTE.2022.3145864.
[22] N. Apostolidou and N. Papanikolaou, "Active power control of switched reluctance generator in more electric aircraft," *IEEE Trans. Veh. Techn.*, vol. 70, no. 12, pp. 12604–12616, Dec. 2021.
[23] N. Apostolidou and N. Papanikolaou, "Vector control-based energy management system for switched reluctance starter/generators," *IEEE Trans. Veh. Techn.*, early access, Jul. 21, 2022, doi: 10.1109/TVT.2022.3192982.
[24] Y. Wang, Y. Yuan, G. Li, Y. Ye, K. Wang, and J. Liang, "A T-type switched-capacitor multilevel inverter with low voltage stress and self-balancing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 5, pp. 2257–2270, May 2021.
[25] B. Axelrod, Y. Berkovich, and A. Ioinovici, "A cascade boost-switched-capacitor-converter - two level inverter with an optimized multilevel output waveform," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2763–2770, Dec. 2005.
[26] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.
[27] W. Jiang, S. H. Chincholkar, and C.-Y. Chan, "Investigation of a voltage-mode controller for a dc-dc multilevel boost converter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 7, pp. 908–912, Jul. 2018.
[28] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Boston, MA, USA: Kluwer Academic, 2001.
[29] M. A. A. Mohamed, S. S. Yeoh, J. Atkin, H. Hussaini, and S. Bozhko, "Efficiency focused energy management strategy based on optimal droop gain design for more electric aircraft," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 4, pp. 4205–4218, Dec. 2022, doi: 10.1109/TTE.2022.3159731.
[30] W. Hu, Z. Wu, X. Lv, and V. Dinavahi, "Robust secondary frequency control for virtual synchronous machine-based microgrid cluster using equivalent modeling," *IEEE Trans. Smart Grid*, vol. 12, no. 4, pp. 2879–2889, Jul. 2021.

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