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Novel Electric Vehicle Traction Architecture With 48 V Battery and Multi-Input, High Conversion Ratio Converter for High and Variable DC-Link Voltage

ANKUL GUPTA [1] (Student Member, IEEE), RAJAPANDIAN AYYANAR [1] (Senior Member, IEEE), AND SOMBUDDHA CHAKRABORTY [2] (Member, IEEE)

[1]School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85287 USA
[2]Kilby Labs, Texas Instruments Inc, Santa Clara, CA 95051 USA

CORRESPONDING AUTHOR: ANKUL GUPTA (e-mail: agupt164@asu.edu).

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ABSTRACT A new architecture for electric vehicle (EV) traction system with multiple low-voltage battery packs and high conversion ratio DC-DC converters is proposed here. In EV traction systems, higher voltage motors offer improved efficiency and power density. High power DC fast charging also favors charging at high DC voltages to limit the charging cable current to manageable levels. However, the optimum battery voltage is relatively low considering factors such as issues with large number of cells in series and safety. The proposed architecture with multiple 48 V battery packs and integrated, multi-input, high conversion ratio converters (HCRC), can reduce the maximum voltage in the vehicle during emergencies to 48 V and provide a variable, high voltage DC link. It enables independent charging/discharging control of the different low-voltage battery modules ensuring cell balancing and enhancing reliability. The proposed topology significantly reduces the voltage stress and peak/RMS current stress of the switches. It features seamless bi-directional power flow characteristics, which supports regenerative braking and high voltage DC fast charging. Four distinct configurations are analyzed and the configurations with interleaving are shown to improve performance and significantly reduce the filter inductor size. The proposed HCRC operation for EV application is verified experimentally through a 4-phase multi-input, 4 kW hardware prototype. With the nominal input fixed to 48 V, the output voltage is controlled to vary between 200 V to 800 V. The converter achieves a peak efficiency of 98.36% and a full-load efficiency of 97.3% at 50 kHz switching frequency for the interleaved configuration.

INDEX TERMS Bi-directional DC-DC converter, electric vehicle traction system, high gain, non-isolated boost, variable DC link voltage, wide conversion ratio.

I. INTRODUCTION

Due to multiple environmental, societal and health benefits, there has been a steady growth in the demand of hybrid electric vehicles (HEV) and electric vehicles (EV) [1], [2]. Compared to conventional internal combustion engine (ICE) vehicles, EVs are more energy efficient and have zero exhaust emissions which provides an ideal solution to reduce increasing environmental pollution. However, the industry still faces challenges in terms of high capacity battery manufacturing, fast battery charging and improved powertrain performance [2]–[4]. A typical EV powertrain does not include a DC-DC converter and the voltage of the battery stack is the input voltage to the motor inverter. In this case, the battery voltage is unregulated and can result in voltage drops during operation. In recent times, addition of an intermediate DC-DC converter is proposed in literature to improve the overall performance of powertrain [5]–[8]. With this, the motor can be optimized for improved efficiency

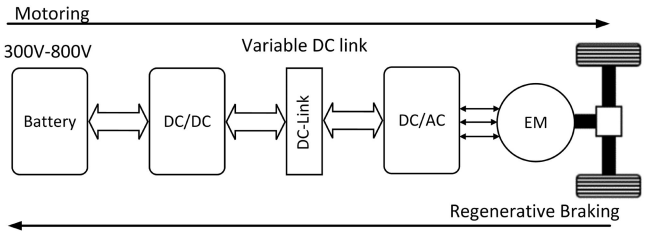


FIGURE 1. EV traction system architecture with an intermediate DC-DC converter.

operation, independent of the minimum battery stack voltage [5]. It also helps in regulating the DC link voltage while reducing the common mode noise for a wide range of operating conditions [6]. Another big advantage of this intermediate boost converter is the ability to have variable DC link voltage. With the variation in motor speed, the DC link voltage varies providing an improved system operation [7]. The DC-DC converter ensures a stable and controllable voltage level at the input of the motor drive inverter as well as reduces the losses in the DC-AC conversion stage [8], [9]. The motor core losses are also reduced as a result of variable DC link voltage. Even though additional losses occur in the DC-DC converter, the net reduction in losses due to variable DC link voltage is higher resulting in improved overall efficiency of the system. The architecture of the powertrain with an intermediate DC-DC converter is shown in Fig. 1. The DC-DC converter has bidirectional power flow capability to ensure the power is fed back to the battery during regenerative braking and to support charging through the high voltage DC link.

In the existing EV powertrain, the battery stack output voltage is in the range of 300 V–800 V [10], [11]. The nominal output voltage of a Lithium-ion cell is 3.6 V. These cells are stacked in different series and parallel combinations to form a module. These modules are then connected in series to achieve the required high output voltage from the battery. When connecting multiple cells in series, it is very important to continually monitor and balance the cell voltages [3]. With unbalance in cell voltages, the battery performance deteriorates. Also, if a cell became open-circuit in series connected module, the entire module containing the failing cell can be detached from the circuit which is not the case in parallel connected cells. Thus, parallel connection of battery modules have some advantages compared to series connection [12], [13]. However, the best solution would be to have multiple converters interfacing low-voltage battery packs to a common, high voltage DC bus. Another issue with the existing battery pack is the presence of high voltage in the car at all times. This increases the risk of shock for personnel working on repair and first responders in case of accidents. Also, it can result in increased chances of fire in case of accidents. In recent times, 48 V battery system has been introduced for its implementation for traction system [14], [15]. However, its implementation is limited to only hybrid electric vehicles with low voltage and low power electric motor. The EV traction motor and inverter performance with 800 V battery system has been presented in [16] and it has shown to improve motor and inverter efficiency. However, battery management system (BMS) cost increases in this case as it becomes more challenging to monitor individual cell performance with large number of cells in series. This paper proposes a new configuration with 48 V battery pack while providing DC link voltage greater than 800 V which combines the advantages of both low voltage battery pack and high voltage motor.

A number of DC-DC converter topologies have been discussed in literature for their implementation in EV traction system and a review of these topologies is presented in [6]. In [17], [18], high gain DC-DC converter for EV traction system has been proposed. In [19], [20], wide input voltage range, high gain DC-DC converter for EV traction system have been proposed. However, these converter do not have bidirectional power flow capability and can be suitable only for fuel cell based EV. In [21], a flying capacitor bidirectional DC-DC converter with variable output voltage is presented but the maximum variation in output voltage is limited to 3 times the input voltage. In [22], conventional interleaved boost in discontinuous mode operation with variable switching frequency is discussed with limited voltage gain range and single input. Also, all of these converters do not have multiple input capability to be connected to different battery packs. A review of the DC-DC converter topologies with multiple-input capability for EV application has been presented in [23]. In [24]–[27], high gain multi-input DC-DC converters are presented for low and medium power applications requiring multiple input sources. The converter in [24] does not have bi-directional power flow whereas [25]–[27] have limited bi-directional operation, which is essential for EV traction application. Even though there are multiple inputs, these converters do not have interleaving among the different inductors, as well as have limited output voltage range operation. In [28], a multi-input DC-DC converter for hybrid electric vehicles with multiple input energy sources is proposed. Similarly, a bi-directional multiple input DC-DC converter for fuel cell based electric vehicles is presented in [29]. All of these converter have low voltage gain which makes them unsuitable for application with low voltage battery packs.

This paper proposes a novel architecture for EV traction system with multi-input, high conversion ratio DC-DC converter with low voltage battery pack and variable DC link voltage, which can overcome the drawbacks mentioned above. The proposed multi-input high conversion ratio converter (HCRC) is a combination of interleaved inductor and switched capacitor configuration. The operation of single input version of the converter for photovoltaic (PV) application with fixed output voltage has been discussed in [30], [31]. The converter operation for equal current sharing over wide range of operation without current control implementation with single input is discussed in [32]. The single input version of the converter can achieve wide input and output voltage range

through phase shedding operation [33], but this is not possible for all the configurations of multi-input case as all the phases need to remain active to ensure equal battery charge status. One of the multi-input configurations of the converter has been discussed in [34] for grid connected PV systems. The converter operation for fixed output voltage has been presented in that paper with a duty limitation ($D > 0.5$), thus, restricting the converter in achieving wide output voltage range. Also, there is no interleaving among the different phase inductors resulting in need of large inductors. There is no discussion on the converter capability to operate in buck mode as well as converter control implementation. This paper proposes a new architecture with four different multi-input HCRC configurations for their implementation in EV traction system.

The main contribution of this paper are summarized as follows:

1) *Novel Architecture for Battery Electric Vehicles:*
   - A novel architecture for a battery electric vehicle (BEV) traction system with 48 V battery modules with high-gain DC-DC converters in multiple configurations for an optimally variable, high voltage DC link (200 V to >800 V) is proposed and shown to be a viable solution for commercial BEV specifications for the first time. The same bi-directional, high gain DC-DC converters also support high voltage (>800 V) DC fast charging.
   - The proposed architecture combines the advantages of low-voltage battery packs with the advantages of high voltage electric motor and high voltage fast charging. The compelling benefits of the architecture in terms of system-level performance, cost of BMS, reliability and safety are described in Section II. It may be noted that with module-level converters and with a choice of multiple configurations introduced here, the size of wiring to connect to inverter terminals and fast charging terminals is as low as that of an 800 V system.
2) *HCRC Topology, Configurations and Optimal Design for 48 V/800 V EV Traction Application:*
   - Multi-Input HCRC is proposed as the intermediate DC-DC converter which is able to achieve high voltage gain with low device current and voltage stress.
   - Multiple configurations of the multi-input HCRC in parallel are presented with different interleaving patterns to minimize the filter inductor size.
   - Detailed analysis of converter operation over wide range of duty ratio and multiple zones of operation, to be able to achieve a smooth transition over wide variable DC link voltage specific to the EV application.
   - Converter operation for both equal and unequal current sharing (as required to support cell balancing) among the different input battery modules over wide range of converter operation.
3) *Extensive Experimental Validation:*
   - Experimental validation of two different HCRC configurations corresponding to the full voltage range of the proposed EV architecture with both equal and unequal current sharing among different input sources and with efficiencies (over a wide range of operating conditions) that are among the highest reported in the literature for high gain converters.
   - Experimental results corresponding to dynamic wide variations in DC link voltage (200 V to 800 V) with 48 V input sources are presented showing converter transitioning between different zones maintaining low device stress under all operating conditions.
   - Buck mode operation experimental results presented to highlight bi-directional power flow capability of the converter.

The rest of the paper is organized as follows: In Section II, the proposed architecture advantages and implementation is discussed in detail. Section III includes the converter operation analysis in detail for both zones of operation. In Section IV, the converter operation in closed loop control is discussed whereas the converter comparison with different multi-input DC-DC converters has been presented in Section V. The converter design considerations are specified in Section VI and the simulation results for parallel HCRC operation is presented in Section VII. Finally, the experimental verification of the proposed system along with efficiency results and loss breakdown is presented in Section VIII.

II. PROPOSED ARCHITECTURE

One of the configurations of the proposed EV traction system architecture with multi-input high gain DC-DC converter is shown in Fig. 2. Here, the maximum battery voltage in multiple modules is designed to be 48 V. A multi-input configuration of HCRC converts it to a significantly higher magnitude DC link voltage with a very wide range of variation. Each battery module is connected to a separate phase of the multi-input HCRC, where the charging and discharging of each battery module can be individually controlled. Each phase of HCRC can be further divided into a sub-module consisting of a single inductor, single capacitor and two switches except for Phase 1 of HCRC. The first phase does not have an intermediate capacitor.

The major advantages of the proposed architecture include:

- Combines the advantages of low-voltage battery packs with the advantages of high voltage electric motor and high voltage fast charging.
- The battery management system at 48 V is significantly simpler and less expensive than an 800 V battery system. [16] shows that the BMS for even a 400 V battery system is 1.3 times less expensive than the BMS at 800 V, and the reliability with 400 V battery pack is significantly higher compared to 800 V battery (1000 cycles vs. 800 cycles). Hence, the advantages are expected to be even more significant when 48 V battery pack is compared with 800 V pack. Besides, the charging and

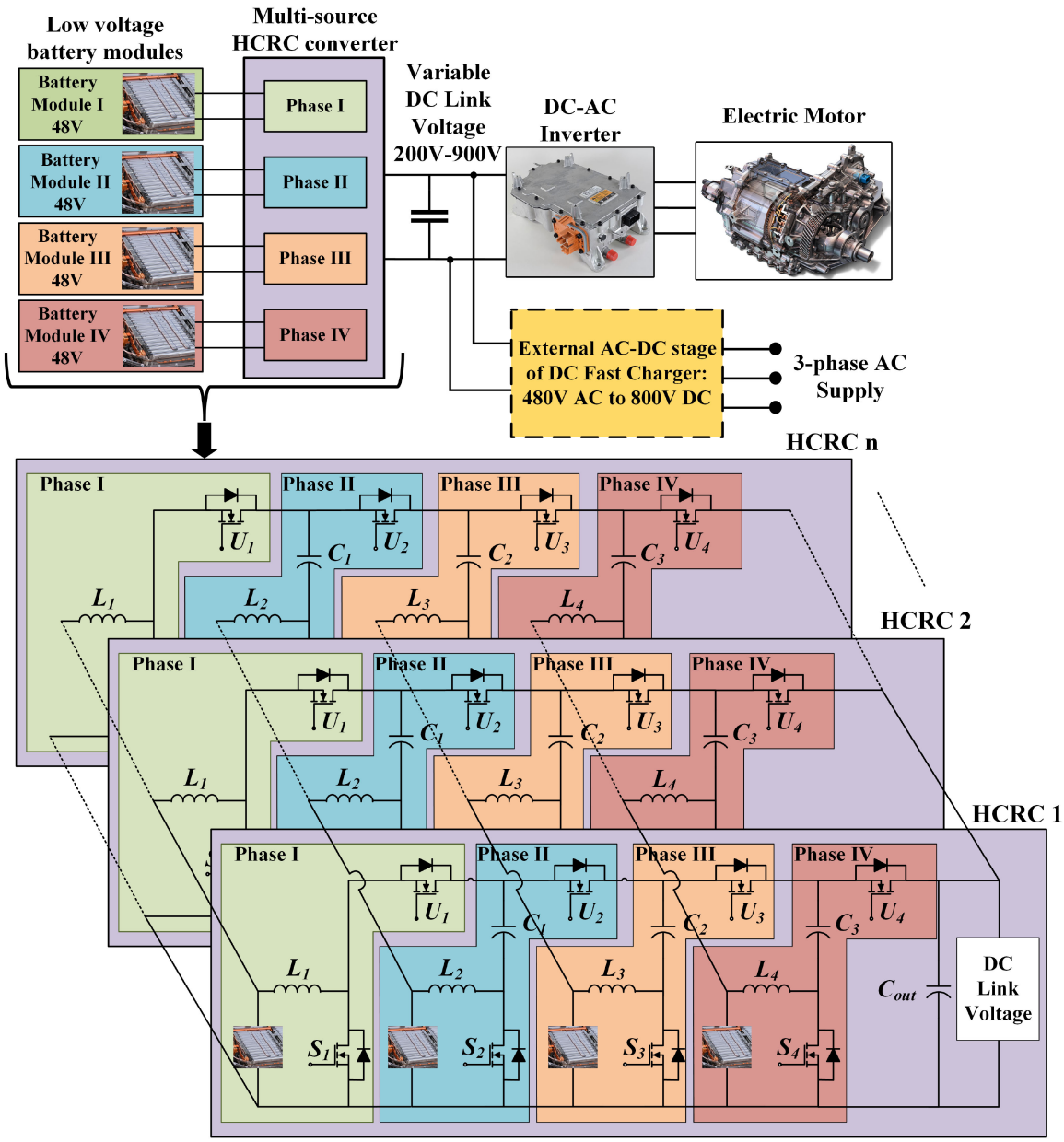


FIGURE 2. An example configuration of the proposed EV traction system architecture with 4-phase multi-input high conversion ratio converter. It can be extended to *n* number of phases to accommodate different specifications.

discharging of each battery module can be independently controlled with its corresponding converter.

- Proposed solution offers a significant safety advantage with the highest voltage present in the vehicle during emergency or repair/maintenance being 48 V (with DC-DC converters turned off), widely accepted as a safe voltage for automotive systems.
- Enables DC fast charging at >800 V (which is recently a main motivation for the move towards higher voltage battery systems) through the same high-gain, bidirectional DC-DC stage in the buck mode operation. Need for a separate DC-DC converter in DC fast charging system can be eliminated as the output of the AC-DC stage of the fast-charging system can be directly connected to EV's DC link, with the battery management performed by the on-board high gain converter.
- Enables use of more compact and efficient high-voltage motors with improved torque-speed performance.
- Variable DC-link voltage enhances the efficiency of the inverter stage and allows use of novel space vector PWM methods such as 240 CPWM with low switching loss and low common mode voltages [35].
- Potentially eliminates the need for a separate high voltage to 48 V auxiliary power unit at multi-kW power levels to support growing 48 V loads in EVs.

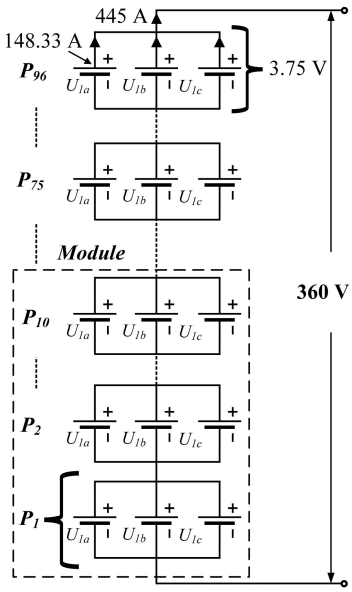


FIGURE 3. Basic schematic showing cell connection in the current Chevrolet Bolt battery pack.

- With integrated high-gain converters and with a choice of multiple configurations introduced here, the size of wiring to connect to inverter terminals and charging terminals is as low as that of an 800 V system.
- Distributed, modular, scalable and fault-tolerant EV architecture when implemented using the proposed HCRC configurations.

A. EXAMPLE DESIGN CORRESPONDING TO CHEVROLET BOLT

Here, the low-voltage EV architecture with proposed high gain converter corresponding to the specifications of Chevrolet Bolt is described. The existing battery pack structure is presented and an example of the reconfigured system with the proposed architecture is shown. The battery pack in Chevrolet Bolt is rated for 60 kWh energy with a peak power of 160 kW [11]. A basic schematic of the cells connection in bolt battery pack is shown in Fig. 3. Three cells are connected in parallel to form a pouch, with 96 pouch in series connection. The detailed specifications of the currently employed battery pack are as follows:

- 60 kWh battery pack with a total of 288 battery cells divided unequally among 10 modules
- 8 modules with 30 cells and 2 modules with 24 cells
- 96 cells in series configuration with 3 groups in parallel
- Individual cell voltage of 3.75 V with nominal battery voltage of 360 V
- Maximum power of the battery system is 160 kW with peak battery output current close to 445 A

Corresponding to the battery specifications given above, different configurations ranging from four phases to eight phases of the high conversion ratio converter are possible. With 48 V battery system, the input current will be very high corresponding to power level of hundreds of kW. To ensure the current output of each battery module does not exceed that of the existing, multiple HCRC can be connected in parallel. In the example shown in Fig. 4. Here, four 48 V battery modules with four HCRC modules are connected to form a stack. There are two stacks connected in parallel resulting in a total of 8 battery modules and 8 HCRC converters in the reconfigured system. Each battery module is connected to the same phase of each HCRC module. For example, phase 1 of all the four HCRC modules is connected to battery module I in stack I. This enables interleaving among the different phase inductors, thus, reducing the inductance value and inductor size. Also, there is interleaving at the output capacitor resulting in smaller DC link capacitor. The Chevrolet Bolt battery pack needs to be modified slightly to fit to the proposed low battery voltage converter structure. The total number of cells are increased from 288 cells to 312 cells with the battery energy increasing to 64.4 kWh. The total number of cells in series in the battery pack is reduced from 96 to 13, which eases the battery management system (BMS) operation and safety issues related to high battery pack voltage. The specifications of the proposed system are given below:

- 64.4 kWh battery pack with total 312 battery cells divided equally in 8 modules
- Each module contains 39 cells with 13 cells in series configuration and 3 sets in parallel (13 s/3p)
- Maximum voltage of each module is 48.75 V with each battery module rated for peak energy of 8.05 kWh and maximum power of 21.5 kW
- Maximum current output from each battery module remains the same (445 A) as that of existing architecture. Each HCRC converter is rated for 22 kW for a total of 176 kW

From the above example design, it can be seen that the existing battery pack of Bolt can be easily reconfigured with minimal modifications to fit the proposed system. The work described in this paper is also equally suitable for another configuration with just one stack, 4 modules 78 cells each in 13 series, 6 parallel (13 s/6p) arrangement and with four, 4-phase, 44 kW HCRC converters. The second configuration will need fewer voltage sensors for BMS leading to even lower BMS cost [16]. With changing power of the battery pack, the number of phases can be accordingly modified to keep the net output from each battery module constant. The proposed structure has an advantage of increased safety due to low battery voltage and decreases cell balancing issues as there are less battery cells in series configuration. The number of battery modules and HCRC converters in parallel can be varied accordingly for implementation with different power level battery packs.

B. PHASE OPTIMIZATION OF HCRC

Deciding the number of phases of HCRC is the first step when designing it for EV traction application. With change in

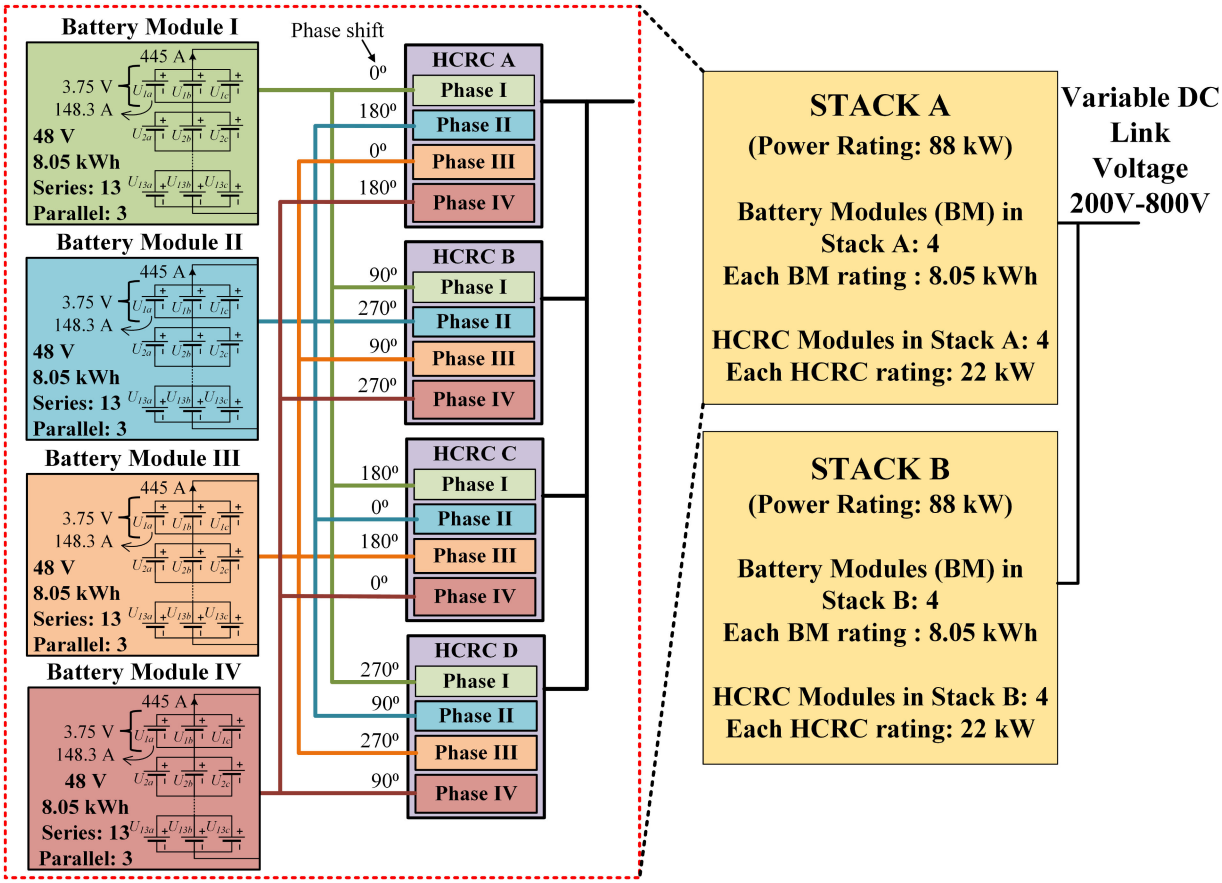


FIGURE 4. Proposed parallel HCRC configuration with modified 48 V battery pack to closely match the conventional 360 V configuration of Chevrolet Bolt battery pack shown in Fig. 3. A single stack structure with 13 s/6p cell configuration for each battery module is also possible.

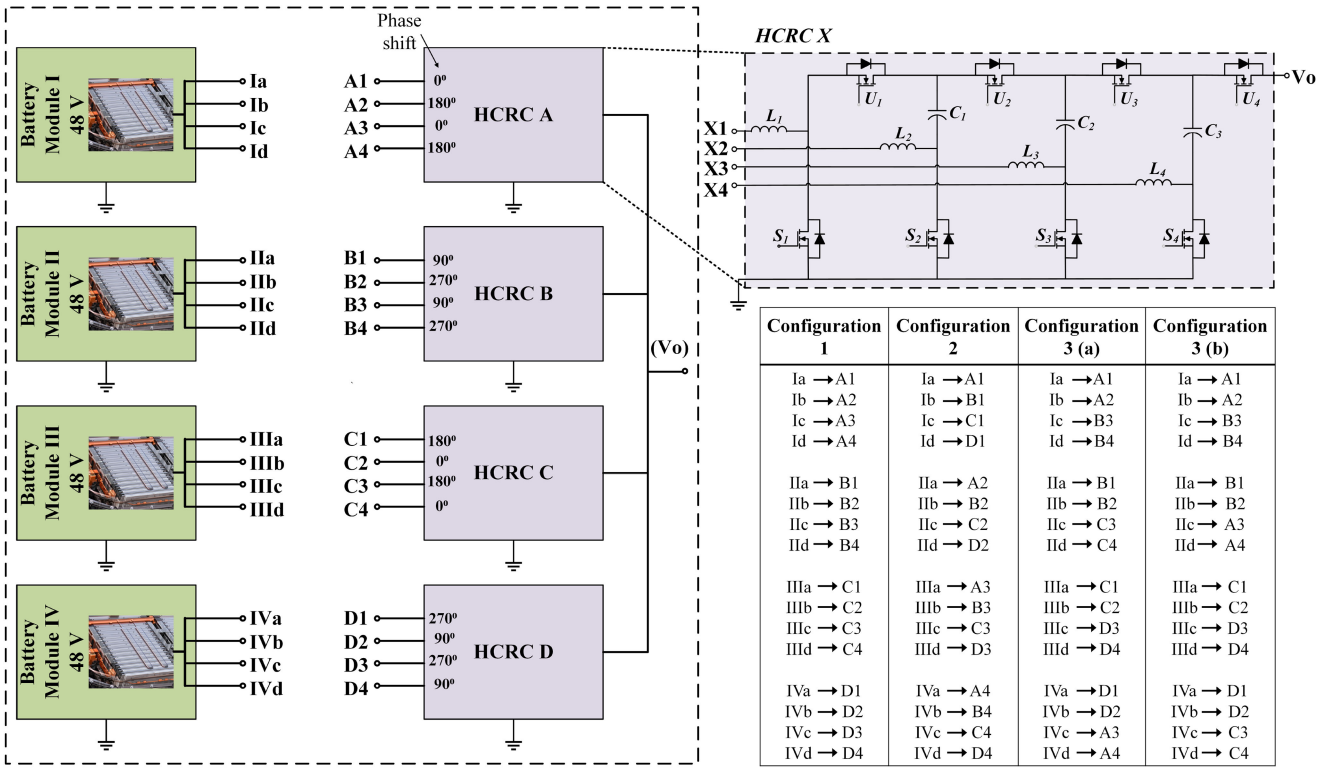
number of phases, the operation and control characteristics of the converter also changes. The major factors that contribute towards this optimization are:

- **Gain:** Compared to conventional interleaved boost converter, adding a phase in HCRC leads to increase in the gain achieved by the converter. The application gain requirement is one of the major factors in choosing the number of phases of the converter.
- **Semiconductor device stress:** Based on the available device voltage and current ratings, the number of phases can be chosen. With increase in number of phases, the voltage and current stress of the semiconductor device decreases.
- **Output voltage range:** Increasing the number of phases also results in the increase of the minimum conversion ratio possible in the converter. This places a limit on the lower range of the variable DC link voltage, which is an important consideration. However, in the configurations that allow phase shedding this may be less significant.
- **Converter control:** Similar to conventional boost converter, HCRC also has a right half plane (RHP) zero. With increase in the number of phases, the RHP zero frequency decreases, thus, reducing the converter control bandwidth. Thus, increasing the number of phases impact the dynamic response of the converter.

Based on all these factors, the converter phases can be optimized accordingly. However, even number of phases possesses the advantage of symmetrical converter structure which makes the interleaving of different phases possible as discussed in next section. In addition to this, the converter component count and efficiency will also vary based on the number of phases which needs to be taken in account when choosing the number of phases. A 4-phase multi-input HCRC is chosen here based on the factors discussed above. The converter has the advantage of lower component count while easily able to achieve a conversion ratio ranging from 4 to above 20.

C. POSSIBLE CONVERTER CONFIGURATIONS

For EV traction application, the rating of DC-DC converter is in hundreds of kW. The HCRC modules can be stacked in parallel to meet this requirement as well as to regulate the maximum current from each battery module to a desired value. As discussed in the previous section, a stack consists

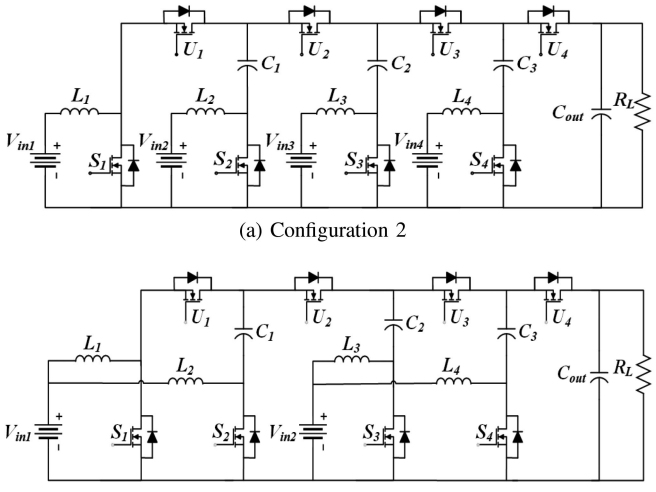


Configuration 1	Configuration 2	Configuration 3 (a)	Configuration 3 (b)
Ia → A1	Ia → A1	Ia → A1	Ia → A1
Ib → A2	Ib → B1	Ib → A2	Ib → A2
Ic → A3	Ic → C1	Ic → B3	Ic → B3
Id → A4	Id → D1	Id → B4	Id → B4
IIa → B1	IIa → A2	IIa → B1	IIa → B1
IIb → B2	IIb → B2	IIb → B2	IIb → B2
IIc → B3	IIc → C2	IIc → C3	IIc → A3
IId → B4	IId → D2	IId → C4	IId → A4
IIIa → C1	IIIa → A3	IIIa → C1	IIIa → C1
IIIb → C2	IIIb → B3	IIIb → C2	IIIb → C2
IIIc → C3	IIIc → C3	IIIc → D3	IIIc → D3
IIId → C4	IIId → D3	IIId → D4	IIId → D4
IVa → D1	IVa → A4	IVa → D1	IVa → D1
IVb → D2	IVb → B4	IVb → D2	IVb → D2
IVc → D3	IVc → C4	IVc → A3	IVc → C3
IVd → D4	IVd → D4	IVd → A4	IVd → C4

FIGURE 5. Possible battery-HCRC module configurations.

of four battery modules and four HCRC module. Each HCRC module has four input terminals which can be connected either to the same battery module or different battery modules resulting in a possibility of multiple configurations, each having it's own advantage.

The different possible battery-HCRC module connection configurations are shown in Fig. 5. Only four configurations with the most advantages are discussed here. Configuration 1 is the basic configuration where each HCRC module is connected to an individual battery pack. In configuration 2, each battery pack is connected to a respective phase of different HCRC. In configuration 3(a) and 3(b), first two phases of each HCRC are connected to particular battery module whereas last two HCRC phases are connected to a different battery module. The sequence of battery module connection is only different in these configurations. The presented configurations provide an advantage of interleaving among different HCRC phase inductors. This results in reduction of input current ripple which in turn decreases the inductor size. Similarly, there is interleaving at the output side of HCRC resulting in lower rms current through output capacitor. Apart from this, certain parallel configurations have an added advantage in cases of fault occurring in the HCRC modules. HCRC also the capability of achieving wide range of output voltage through phase shedding operation [33], which is possible for only certain configurations. A comparison between the different configurations is shown in Table 1. The configuration 2 presented here corresponds to the Chevrolet Bolt architecture shown in Fig. 4.



(a) Configuration 2

(b) Configuration 3(a)

FIGURE 6. Schematics of a 4-phase, multi-input, bidirectional HCRC used for experimental validation. (a) Configuration 2 with 4 input sources, and (b) Configuration 3a with 2 input sources.

D. SCALED HARDWARE PROTOTYPE CONFIGURATIONS

For experimental verification of HCRC proposed for EV application, a scaled hardware prototype is built. Single HCRC operation with each phase connected to a separate input voltage source is tested for the rated EV traction system DC link voltage range. The schematic of a single 4-phase HCRC in configuration 2 is shown in Fig. 6(a). As, this configuration does not have interleaving among the different phases and

TABLE 1. Comparison Between Different Parallel HCRC Configurations for EV Traction System

Configuration	Inductor Interleaving	Input current ripple	Output Capacitor Interleaving	Battery-HCRC Module connection	Fault Tolerance	Phase Shedding
1	180^o Phase shift	Relatively higher	90^o Phase shift	Individual battery connected to corresponding HCRC module	Faulty HCRC module can result in removal of corresponding battery pack	Yes
2	90^o Phase shift	Low	90^o Phase shift	Each battery connected to all HCRC modules	Faulty HCRC module can be easily isolated	No
3 (a)	90^o Phase shift	Low	90^o Phase shift	Each battery connected to two HCRC modules which are further interconnected	Faulty HCRC module can be isolated	Limited
3 (b)	90^o Phase shift	Low	90^o Phase shift	Two battery modules connected to corresponding two HCRC modules	Faulty HCRC module can be isolated	Limited

the inductor ripple is equal to the input current ripple. This won't be the actual case when multiple HCRC are connected in parallel. To present the advantages of interleaving, single HCRC converter operation in configuration 3(a) is also verified experimentally and the schematic is shown in Fig. 6(b). In the interleaved configuration, two input sources are connected to the converter instead of four. As the alternate phases in the converter are 180° out of phase, phase 1 and 2 as well as phase 3 and 4 are interleaved. This results in significant decrease in input current ripple while reducing the inductor size and inductance value. With additional HCRC in parallel, the inductor value and size will further reduce due to 90° phase shift among different phase inductors. The converter operation in all these configurations remains the same. Hence, moving forward converter operation for configuration 2 is discussed in detail.

III. CONVERTER OPERATION

In this section, the operation of the 4-phase HCRC with four input sources in boost mode is discussed. The alternate phase switches of HCRC are switched 180° out of phase. The converter operation can be divided into two zones based on the duty ratio of operation. The converter device characteristics as well as gain varies in each zone. The converter operation in each zone is discussed as well as detailed equations for device voltage and current stress are presented in this section. The device characteristics in buck mode remain the same as boost mode and hence, the buck mode operation is not provided here to avoid repetition.

A. ZONE I OPERATION

Zone I corresponds to highest gain zone, where all the phases are simultaneously ON for a certain interval of time in one switching cycle. In Zone I, the alternate phases of the converter are phase shifted by 180° and the duty ratio of operation is greater than 0.5 for all phases. The converter possesses inherent current sharing among its different phases in this zone with equal duty ratio for all phases. This can be verified with the basic capacitor charge balance principle applied to the intermediate as well as output capacitor and is already discussed in [32] for the single input version of the converter. For a 4-phase converter with 48 V input voltage, the output voltage range of the converter in this zone is between 384 V to 900 V. As a high DC link voltage is desirable for EV traction system, this would be the main zone of operation.

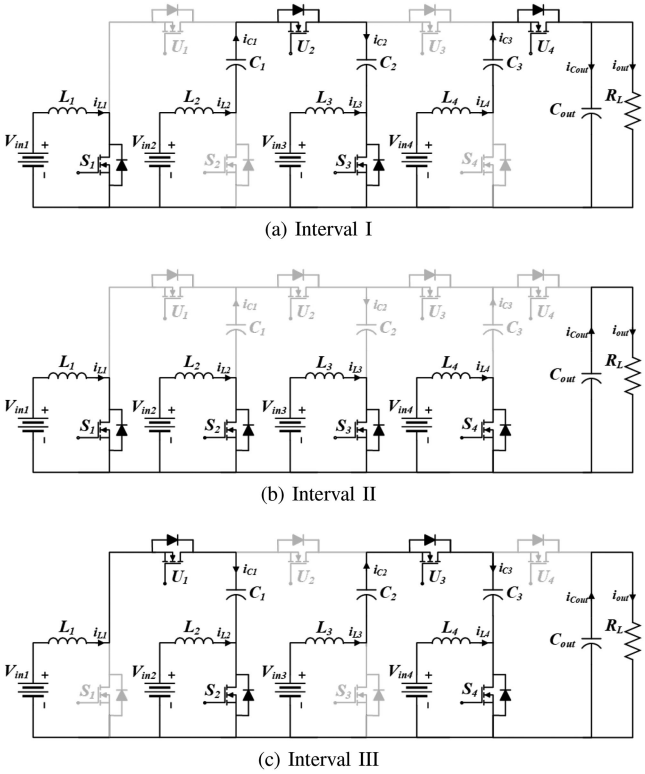
With 180° phase shift in alternate phase switching and equal duty ratio for all the four phases, the converter operation can be divided into three intervals in this zone. The current path and corresponding conducting devices in the three intervals are shown in Fig. 7. The ideal current and voltage waveforms for different devices corresponding to Zone I operation are shown in Fig. 8. The converter operation in each of these intervals is given below.

- **Interval I** [t_1–t_2] (Fig. 7(a)): In this interval, only S_1 and S_3 are in ON-state. The intermediate capacitor C_2 is charged in this interval through discharging of capacitor C_1. This results in higher current flow through phase 3 bottom switch in this interval, which is equal to twice the individual phase current. Also, C_3 discharges in this interval to provide the load current as well as to charge the output capacitor.
- **Interval II** [t_0–t_1, t_2–t_3] (Fig. 7(b)): In this interval all the four switches are ON simultaneously (as the duty is higher than 0.5 in this zone). All the four phase inductors are charged in this interval with no current flow through any intermediate capacitors. The output capacitor supports the load current in this interval.
- **Interval III** (Fig. 7(c)): In this interval, S_2 and S_4 are in ON-state. Intermediate capacitor C_1 charges through phase 1 inductor current while C_3 charges through discharging of C_2. The current in phase 2 and phase 4 bottom switch are higher in this interval. Similar to Interval II, the output capacitor supports the load current in this interval.

The converter gain corresponding to equal input voltage and equal duty for all phase switches is equal to 4 times that of conventional boost converter and is specified by (1). The current carried by the different phases is equal in this

TABLE 2. Zone I: Device Voltage and Current Stress

	Equal Input Voltage & Current $(D_1 = D_2 = D_3 = D_4 = D)$	Unequal Input Voltage & Current $(D_1 \neq D_2 \neq D_3 \neq D_4)$
Bottom Switch Voltage	$V_{S1,2,3,4} = \frac{V_o}{4}$	$V_{Sm} = \frac{V_{inm}}{(1-D_m)}; \quad m \in [1,4]$
Top Switch Voltage	$V_{U1,2,3} = \frac{V_o}{2}; \quad V_{U4} = \frac{V_o}{4}$	$V_{U1} = V_{C2}\ ; V_{U2} = V_{C3} - V_{C1}\ ; V_{U3} = V_o - V_{C2}\ ; V_{U4} = V_o - V_{C3}$
Capacitor Voltage	$V_{C1} = \frac{V_o}{4}\ ; V_{C2} = \frac{V_o}{2}\ ; V_{C1} = \frac{3V_o}{4}$	$V_{Cm} = \sum_{n=1}^{m} \frac{V_{inm}}{(1-D_m)}; \quad m \in [1,3]$
Bottom Switch Current (Peak & RMS)	$I_{S1(pk)} = I_{ph}\ ; I_{S2,3,4(pk)} = 2I_{ph}$ $I_{S1(rms)} = I_{ph}\sqrt{D}$ $I_{S2,3,4(rms)} = I_{ph}\sqrt{3-2D}$	$I_{S1(pk)} = I_{L1}\ ; I_{S2(pk)} = I_{L1} + I_{L2}\ ; I_{S3(pk)} = I_{L2} + I_{L3}\ ; I_{S4(pk)} = I_{L3} + I_{L4}$ $I_{S1(rms)} = I_{L1}\sqrt{D_1}$ $I_{RMS(Sm)} = \sqrt{I_{Lm}^2(D_m + D_{m-1} - 1) + (I_{Lm} + I_{L(m-1)})^2(1 - D_{m-1})};\ m \in [2,4]$
Top Switch Current (Peak & RMS)	$I_{U1,2,3,4(pk)} = I_{ph}$ $I_{U1,2,3,4(rms)} = I_{ph}\sqrt{1-D}$	$I_{Sm(pk)} = I_{Lm}\ ; \quad m \in [1,4]$ $I_{RMS(Um)} = I_{Lm}\sqrt{(1-D_m)}\ ; \quad m \in [1,4]$
Capacitor Current (RMS)	$I_{C1,2,3(rms)} = I_{ph}\sqrt{2(1-D)}$ $I_{Cout(rms)} = I_{out}\sqrt{\frac{D}{1-D}}$	$I_{RMS(Cm)} = \sqrt{I_{Lm}^2(1-D_m) + I_{L(m+1)}^2(1-D_{m+1})}\ ; \quad m \in [1,3]$ $I_{RMS(Cout)} = I_{out}\sqrt{\frac{D_4}{1-D_4}}$



(a) Interval I

(b) Interval II

(c) Interval III

FIGURE 7. Current path and conducting devices at various intervals corresponding to Zone I operation of HCRC.

case and is given by (2). The voltage and current stresses of different devices corresponding to equal input voltage and current operation are given in Table 2.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{4}{(1-D)} \tag{1}$$

$$i_{L1,2,3,4} = \frac{i_{out}}{(1-D)} = I_{ph} \tag{2}$$

The discharging/charging current requirement of different battery modules can be slightly different depending on the operating conditions such as state of charge of individual cells and need for cell balancing. This is achieved by applying slightly different duty to the different phases based on the current requirement, and ensuring that the duty is always higher than 0.5. There is an extra converter operating state added in this case apart from the three states for equal current sharing discussed above. The extra converter operation state corresponds to three switches being simultaneously ON. Any three of the four switches can be ON based on the duty of each phase. The device voltage and current stress varies only slightly with un-equal current sharing.

Here, converter operation equation corresponding to different input voltage and different duty for all phases is discussed in detail. The converter output voltage in terms of input voltage and duty ratio of different phases is given in (3). The average inductor current for each phase in terms of the output current is given by (4).

$$V_{out} = \frac{V_{in1}}{(1-D_1)} + \frac{V_{in2}}{(1-D_2)} + \frac{V_{in3}}{(1-D_3)} + \frac{V_{in4}}{(1-D_4)} \tag{3}$$

$$i_{Lm} = \frac{i_{out}}{(1-D_m)};\ m \in [1,4] \tag{4}$$

The different devices voltage and current stresses with unequal input voltage and duty operation are summarized in Table 2. In this case, the voltage stress across the MOSFET is not same and is defined by the duty ratio of that respective phase. The converter still has the advantage of low voltage stress across devices as the voltage stress varies slightly compared to equal duty ratio operation case. The voltage stress across intermediate capacitor is still a fraction of the output voltage and is given in terms of input voltage. The upper switches still see a higher voltage stress compared to the bottom switches except the last phase switch of the converter. In

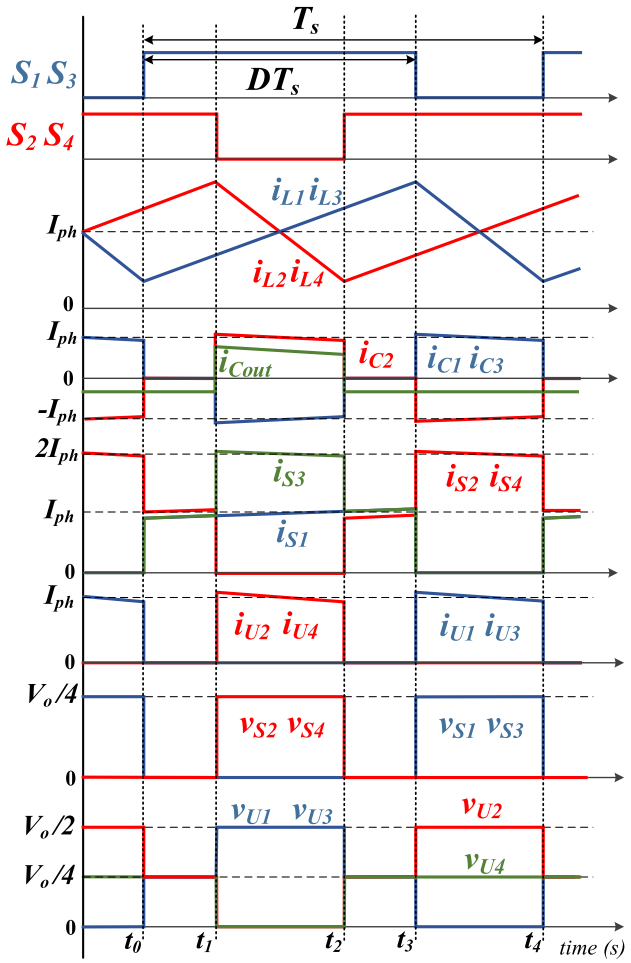


FIGURE 8. Converter operation waveform for equal current sharing in Zone I.

this case, the upper switch voltage can be expressed in terms of intermediate capacitor voltages to avoid lengthy repetition.

In case of equal current sharing among the different phases, the peak current stress across bottom switches of all the phases, except for phase 1, is twice the output current of individual battery module. As the duty of each phase can be slightly different, the peak and rms current flowing through different phases can be correspondingly different. Neglecting the ripple in switch current, the peak and rms currents for both top and bottom switches are presented in the Table 2. Here I_L is the average inductor current of that particular phase. Similarly, the rms currents through the intermediate capacitors and output capacitor also vary with varying duty of each phase.

B. ZONE II OPERATION

This zone II operation of the converter is defined when duty ratio of all the phases is less than 0.5. The converter gain as well as device voltage and current stress varies in this zone compared to Zone I operation. For the chosen specifications, the output voltage attained in this zone varies between 192 V to 384 V for 48 V input voltage. In this zone, the converter does not inherit the equal current sharing among the different phases with same duty ratio. The converter can still have equal current flowing through all phases with modified duty for different phases. However, with implementation of a current controller, the current sharing between the different phases will be automatically taken care of without manually changing the duty. The converter still inherits the flexibility of having different inductor phase currents in this zone for same output voltage and output power.

For simplicity in explanation, only the analysis and equations corresponding to equal input voltage and equal current sharing condition are discussed here as this would be the nominal operating condition. The condition for equal current sharing among different phases with equal input voltage is given by (5). This is derived by applying the capacitor charge balance across the intermediate and output capacitor [32]. For easy representation, the duty of the phase 1 can be considered the defining duty of the converter and phase 3 duty is calculated accordingly.

$$D_3 = \frac{1 + D_1}{3};\ D_2 = D_4 = 0.5;\ (0 < D_1 < 0.5) \quad (5)$$

In Zone II and with unequal duty ratios, the converter operation can be divided into four main intervals during one switching cycle. The devices have significantly different voltage and current stress in each of these intervals of operation. The current path and conducting devices in the four intervals are shown in Fig. 9. The ideal current and voltage waveforms for different devices corresponding to Zone II operation are shown in Fig. 10. As each phase has different duty, the inductor ripple in each phase is different here but the average current flowing through each inductor is equal. The converter operation in each of these intervals is discussed below.

- **Interval I** [t_0–t_1, t_2–t_3] (Fig. 9(a)): In this interval, only S_3 is in ON-state. C_2 is charged through phase 1 and phase 2 current in this interval while current through C_3 supports the output current. S_3 has a peak current equal to 3 times the average input current in this interval.
- **Interval II** [t_1–t_2] (Fig. 9(b)): This is same as the interval I of Zone I operation with S_1 and S_3 in ON-state and C_2 in charging state. C_3 discharges to charge the output capacitor as well as provide the load current.
- **Interval III** [t_3–t_4, t_5–t_6] (Fig. 9(c)): In this interval, all bottom switches are in OFF state. All intermediate capacitors discharge in this interval. This results in high current flowing through the top switches, with current through U_4 equal to the sum of all the individual input phase currents. Also, the voltage across S_1 equals the output voltage in this interval.
- **Interval IV** [t_4–t_5] (Fig. 9(d)): This interval is same as the interval III in Zone I operation with S_2 and S_4 in ON-state. C_1 and C_3 are charged in this interval with output capacitor providing the load current.

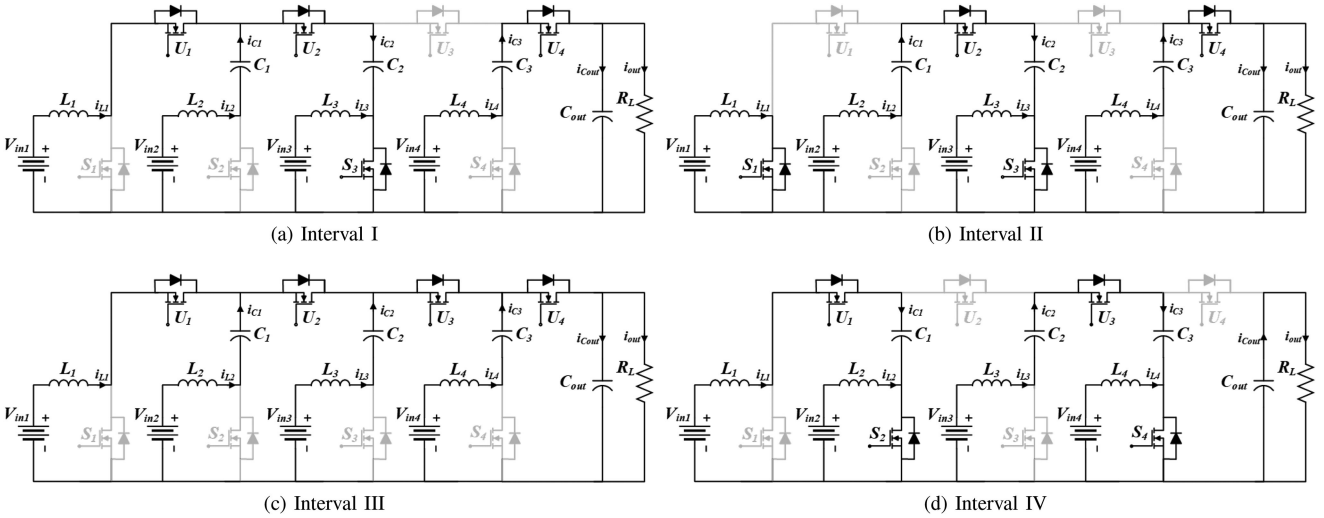


FIGURE 9. Current path and conducting devices at various intervals corresponding to Zone II operation of HCRC.

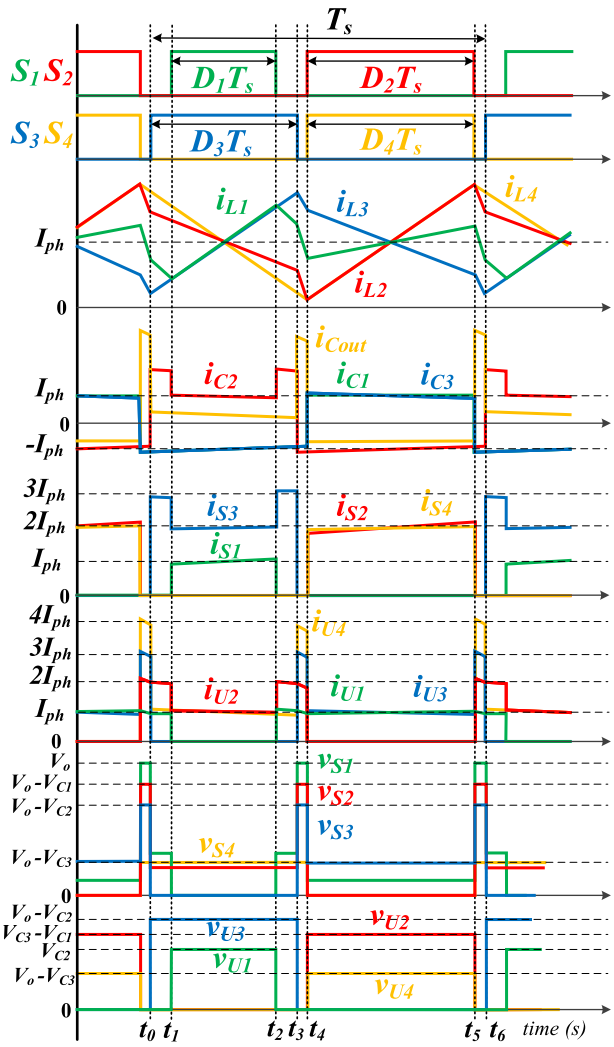


FIGURE 10. Converter operation waveform for equal current sharing in Zone II.

For case with varying duty for the four phases with unequal voltages for different phases, the converter operation may have more sub intervals in addition to those given in Fig. 9. The converter device voltage and current stress will deviate slightly with different input voltage and duty ratio for different phases. The converter gain in this zone for equal current sharing case is given by (6). The inductor current for all phases is equal and defined by (7) and is denoted as I_{ph} for simple representation.

$$k_{II} = \frac{V_o}{V_{in}} = \frac{4}{(1 - D_1)} \tag{6}$$

$$i_{L1} = i_{L2} = i_{L3} = i_{L4} = \frac{i_{out}}{1 - D_1} = I_{ph} \tag{7}$$

The different devices voltage and current stress with unequal input voltage and duty operation is summarized in Table 3. The voltage stress of the intermediate capacitors is still a fraction of output voltage. Compared to Zone I, this zone has a drawback of high voltage stress across the main switches. As the converter enters this zone of operation only at a lower output voltage, the maximum voltage stress across the switches is less than half the maximum output voltage rating of the converter. The voltage stress across the main switches is expressed in terms of intermediate capacitor voltage for easy representation. All switches have different voltage stress in this zone. Contrary to Zone I operation, the voltage stress across upper switches is lower compared to the bottom switches. All upper switches have different voltage stress across them represented in terms of capacitor voltages.

The peak current stress of the bottom switches is not as uniform as in the case of the Zone I operation. Phase 3 sees the highest peak current among all the phases, while phase 1 has the lowest peak current. The upper switches have a much higher peak current stress compared to Zone I operation. The peak current for the phase 4 upper switch is equal to the total

TABLE 3. Zone II: Device Voltage and Current Stress

	Equal Input Voltage & Current ($D_3 = \frac{1+D_1}{3}, D_2 = D_4 = 0.5$)
Bottom Switch Voltage	$V_{S1} = V_o$; $V_{S2} = V_o - V_{C1}$; $V_{S3} = V_o - V_{C2}$; $V_{U4} = V_o - V_{C3}$
Top Switch Voltage	$V_{U1} = V_{C2}$; $V_{U2} = V_{C3} - V_{C1}$; $V_{U3} = V_o - V_{C2}$; $V_{U4} = V_o - V_{C3}$
Capacitor Voltage	$V_{C1} = \frac{3V_oD_1D_3}{2(2-D_1)}$; $V_{C2} = \frac{3V_oD_3}{2(2-D_1)}$; $V_{C3} = \frac{3V_oD_3}{2}$
Bottom Switch Current (Peak & RMS)	$I_{S1(pk)} = I_{ph}$; $I_{S2(pk)} = i_{S4(pk)} = 2I_{ph}$; $i_{S3(pk)} = 3I_{ph}$ $I_{S1(rms)} = I_{ph}\sqrt{D_1}$; $I_{S2,4(rms)} = 2I_{ph}\sqrt{D_2}$; $I_{S3(rms)} = I_{ph}\sqrt{9D_3 - 5D_1}$
Top Switch Current (Peak & RMS)	$I_{U1,2,3,4(pk)} = mI_{ph}$; $m \in [1,4]$ $I_{U1(rms)} = I_{ph}\sqrt{1-D_1}$; $I_{U2(rms)} = I_{ph}\sqrt{4D_2 - 3D_1}$ $I_{U3(rms)} = I_{ph}\sqrt{10D_1 - D_3}$; $I_{U4(rms)} = I_{ph}\sqrt{16D_2 - 15D_3}$
Capacitor Current (RMS)	$I_{C1,C3(rms)} = I_{ph}\sqrt{2D_2}$; $I_{C2(RMS)} = I_{ph}\sqrt{3D_3 - 3D_1 + 1}$ $I_{Co(rms)} = \sqrt{I_o^2 + I_{ph}^2(16D_2 - 15D_3) - I_oI_{ph}(8D_2 - 6D_3)}$

input current to the converter. Even though the peak current stress across the top and bottom switches is high, the time interval of peak current flow is very small compared to the time period of the switching cycle. This results in relatively lower rms current resulting in low conduction loss penalty. The rms current rating for S_1 is same as that of zone I. The rms current ratings for S_2 and S_4 are equal as both phases are operated with equal duty. For the remaining switches, the rms current rating varies depending on the duty of different switches. The rms current rating for intermediate capacitors also varies for different phases. C_1 and C_3 have the same rms current rating as phases 2 and 4 have the same duty ratio of operation. The inductor current ripple is not considered in computing the peak current rating of different devices for easy representation.

IV. CLOSED LOOP CONTROL

As boost mode is the major mode of operation, detailed analysis of converter control in this mode is presented. An overview of the converter transfer function in boost mode operation along with the implementation of voltage and current controller for closed loop operation is presented.

Similar to a conventional boost converter, the high conversion ratio converter also has a right half plane (RHP) zero in the plant transfer function. As Zone I is the main zone of operation, the converter transfer function is discussed for this zone for equal duty ratio operation of all phases. As a 4-phase converter results in a 8th order system, the transfer function equations are very lengthy and only relevant equations are presented. The duty to output voltage transfer function ($G_{vd}(s)$) and duty to phase 1 current transfer function ($G_{iL1d}(s)$) of the converter are derived through state space modeling of the converter in MATLAB. The derived analytical transfer function is compared with the corresponding switching model transfer function in PLECS. In Fig. 11, the transfer function Bode plots from analytical and simulation models are shown. It can be seen that there is a good match between the two models. There is a difference in the phase plot visible in $G_{vd}(s)$ transfer

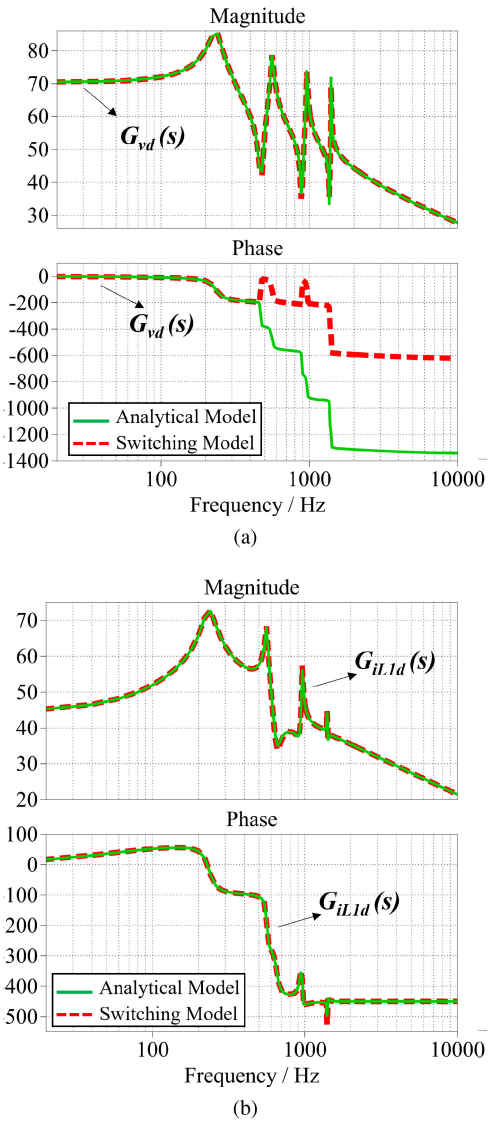


FIGURE 11. Converter magnitude and phase bode plot of analytical and switching model of converter for (a) Duty to output voltage transfer function ($G_{vd}(s)$) (b) duty to phase 1 current transfer function ($G_{iL1d}(s)$).

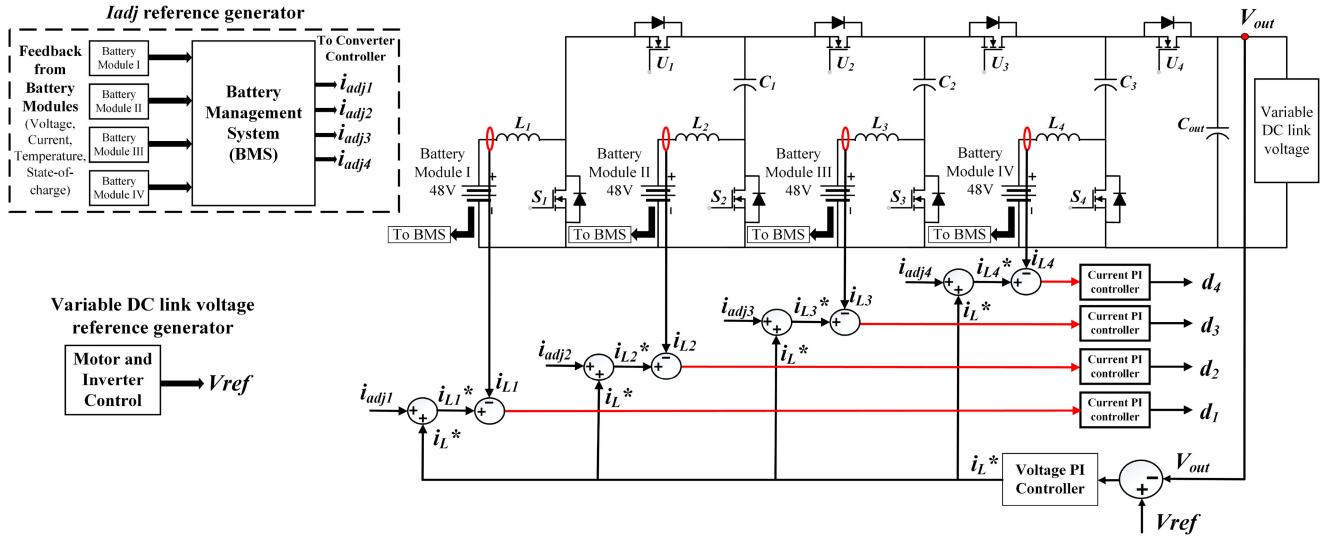


FIGURE 12. Dual loop control implementation for a 4-Input high conversion ratio converter.

function which is actually just a 360° phase shift in the two model plots and is theoretically the same. It has been observed that the transfer function of the multi-input HCRC remains the same as that of single input case, which has been discussed in detail in [36], [37].

The HCRC has additional pole pair and zero pair in its duty to output voltage transfer function when compared to the conventional boost transfer function. With each additional phase of the converter, an additional pole and zero pair is added in this transfer function. For a 4-phase converter, the converter has four pole pairs and three zero pairs as shown in Fig. 11(a). The first pole pair is dominated by the output capacitor which is also the dominant pole pair of the converter. The converter exhibits one RHP zero which is given by (8). Compared to the RHP zero frequency of conventional single-phase boost, there is an additional factor of 4 due to the number of phases. As RHP zero plays a major role in defining the controller bandwidth of the boost converter, the converter control bandwidth significantly decreases with increasing number of phases. Hence, the number of phases of the converter needs to be optimized for the required dynamic response.

$$f_{RHPzero} = \frac{R_{load}(1-D)^2}{4 * 2\pi * L} \tag{8}$$

As both the DC link voltage as well as the input current of the converter needs to be regulated, a dual loop control has been proposed here. There is an outer voltage loop that regulates the output voltage which generates the current reference for the inner current loop. The inner current loop is responsible for regulating the inductor current. The proposed dual loop control implementation for 4-input HCRC is shown in Fig. 12. Here, there is one outer voltage loop and four inner current loops, one for each phase. A voltage PI controller regulates the output voltage to the set reference voltage (Vref). This reference voltage is set by the motor and inverter control, which is dependent on multiple factors such as vehicle speed, required torque, etc., and are beyond the scope of this work. Here, an additional i_{adj} term is introduced to the current reference generated by voltage controller. In EV traction systems, BMS is employed which ensures proper battery operation by monitoring the battery module voltage, current, state-of-charge, etc. The idea here of introducing the i_{adj} control term is to regulate the current from each battery module based on the charge status of the battery sensed by the BMS. Based on this additional term, the current from each of these battery modules can be regulated independently of each other based on the battery charge status. Each phase current is sensed and compared with its respective current reference to generate the duty of that phase.

The proposed controller design is initially implemented in PLECS with C-script blocks to emulate the implementation of the controller in hardware with Digital Signal Processor (DSP). As RHP zero plays a major role in defining the controller bandwidth of the boost converter, the converter control bandwidth significantly decreases with increasing number of phases. Hence, the number of phases of the converter need to be optimized for the required dynamic response. Keeping in mind the RHP zero frequency of the converter, the control bandwidth is decided. To ensure smooth converter control for wide range of output voltage and power, controller is designed for the lowest bandwidth condition. In boost converter with RHP zero, a thumb rule for defining the controller bandwidth is set the control bandwidth less than $\frac{1}{5}$ of the RHP zero frequency. For the proposed HCRC, the minimum RHP zero frequency condition occurs at rated power and maximum output voltage (maximum duty). For the designed hardware prototype, the worst RHP zero frequency (8) is 1666 Hz ($R_{load} = 160\,\Omega, D = 0.76, L = 220\,\mu H$). The RHP zero frequency will be higher than this for all other operating conditions. Prior to hardware implementation, the controller PI values are tuned in PLECS by observing the open loop gain ($G_{OL}(s)$) plot

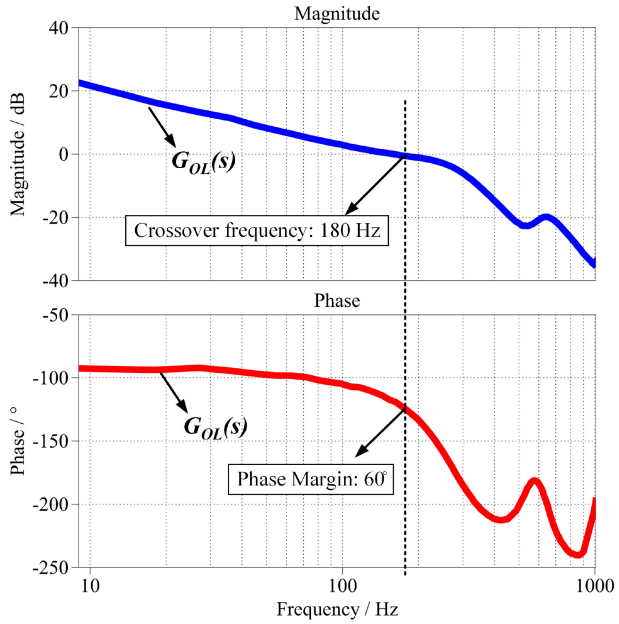


FIGURE 13. Magnitude and phase bode plot of converter open loop gain ($G_{OL}(s)$) with dual loop control implementation.

of the converter. The crossover frequency and phase margin of the converter with implemented controller is observed to ensure controller stability. For the worst-case condition, the open loop gain plot of the converter with the tuned PI values is shown in Fig. 13. For this controller design, the control bandwidth is 180 Hz with a phase margin of 60°. As for EV application the response time for variation in output voltage is in hundreds of milliseconds, the bandwidth is sufficient to provide the desired transient response. As for other voltage and power conditions, the RHP zero frequency is going to be higher than at worst case condition, the designed controller is going to be stable. The dual loop PI controller is implemented in hardware through Texas Instruments TSM320F28379 DSP.

V. COMPARISON WITH OTHER MULTI-INPUT HIGH GAIN DC-DC CONVERTER TOPOLOGIES

In order to evaluate the merits of the proposed structure, it is compared with other multi-input non-isolated high gain DC-DC converter topologies. For a better comparison overview, the proposed structure is compared in terms of different parameters relevant for EV application specification and is presented in Table 4. All the converters are simulated in detail in PLECS under identical input/output conditions. Comparison is made in terms of bidirectional power flow (BPF) capability, interleaving, input current, inductor design, semiconductor device ratings and limitations in duty. All the topologies under consideration are simulated in PLECS for 48 V input to 800 V output at 4 kW, 50 kHz operation. Both the maximum voltage and current stress among all devices as well as the sum of voltage and current stress of semiconductor devices is specified. The I^2_{RMS} is an important metric that determines the total conduction losses in the converter, and hence, it is included for a complete comparison.

Converter in [24] does not has the capability to support bi-directional power whereas [25]–[27] have limited bi-directional operation where only the n^{th} input stage has bi-directional capabilities. All of these converters are capable of achieving high gain but have a limitation on the minimum duty of operation ($D > 0.5$). This results in limited output voltage range operation of these converters and thus, are not able to achieve low output voltage in the range of 200 V. Even though the structure is multi-input involving multiple inductors, there is no interleaving among different inductors leading to very large filter inductor requirement. It can be seen in the table that for the same input current ripple specifications, the inductance value required for other topologies is quite large. Also, for a n-input converters in [25]–[27], the current from different input sources is not equal which is not desired for EV application involving multiple battery modules. Most of these multi-input converters are recommended for low/medium power application due to the presence of multiple diodes and thus, are not suited for low voltage high current application. The proposed structure provides an overall optimization for EV application as it has bi-directional power flow, interleaving among different phases resulting in smaller inductor requirement and wide output voltage range operation. The proposed converter has the capability of independent current control from different battery modules based on charge status of the battery, which is not discussed for other topologies. Also, low voltage semiconductor device with lower on-state resistance can be used as the voltage stress across devices remains low over the entire range of operation. The proposed converter also has the lowest I^2_{RMS} value making it highly suitable for high power applications.

VI. CONVERTER DESIGN CONSIDERATIONS

The selection and design of all the components of the single multi-input HCRC hardware prototype with varying DC link voltage operation are presented in this section.

A. INDUCTOR SELECTION

In configuration 2, as each phase of the converter is connected to a separate battery module, the maximum battery current is the maximum input current for each phase inductor. The inductor ripple current in Zone I operation for equal phase currents case is given by (9). In Zone II operation, as duty of each phase is different, the inductor current ripple for different phases is different even though the average current is equal. The inductor current ripple in Zone II operation is given by (10). As the converter power varies with output voltage, the inductor is designed for the maximum current and maximum desired ripple at rated voltage at rated power which corresponds to Zone I operation.

$$\Delta I_{Lz1(config.2)} = \frac{V_{out}(1-D)D}{4f_{sw}L} \tag{9}$$

$$\Delta I_{Lz2(config.2)} = \frac{V_{out}(1-D_1)D_m}{4f_{sw}L};\ m \in [1,4] \tag{10}$$

TABLE 4. PERFORMANCE COMPARISON of PROPOSED STRUCTURE WITH OTHER MULTI-INPUT HIGH GAIN DC-DC CONVERTERS (All Converters are Simulated Under Identical Conditions Of: $V_{in} = 48\,V$, $V_o = 800\,V$, $P_o = 4\,kW$, $f_s = 50\,kHz$)

Ref.	Limitations (Bidirectional Power Flow (BPF) /Interleaving /Minimum Output Voltage)	Duty	Current from different Input Sources*	Inductor Value+/ Net Inductance Current Product@	Maximum Device Voltage/Current Stress ($V_o = 800\,V$)	Sum of All Devices Voltage Stress**	Sum of All Devices Current Stress##	Sum of All Devices Mean Square Current++	Total Devices#
[24] (3 VM Stage)	No BPF/ No Interleaving/ Cannot achieve $V_{o,min}$ of 200 V	0.76	Equal current (2 Inputs) 42 A each	$330\mu H, 42\,A$ (x2) 1.16424 HA^2	400 V / 84 A	1800 V	300 A	4968 A^2	L: 2 S: 2 D: 4 C: 4
[25]	Limited BPF/ No Interleaving/ Cannot achieve $V_{o,min}$ of 200 V	0.623	Unequal current (2 Inputs) $I_{in1} = 48.5\,A$ $I_{in2} = 35.5\,A$	$500\mu H, 35.5\,A$ $2\,mH, 13.5\,A$ $260\mu H, 35.5\,A$ $800\mu H, 13.5\,A$ 1.46809 HA^2	800 V / 62 A	2321 V	250 A	4954 A^2	L: 4 S: 6 D: 2 C: 4
[26]	Limited BPF/ No Interleaving/ Cannot achieve $V_{o,min}$ of 200 V	0.688	Unequal current (2 Inputs) $I_{in1} = 68\,A$ $I_{in2} = 16\,A$	$560\mu H, 52\,A$ $2.6\,mH, 16\,A$ $300\mu H, 16\,A$ 2.25664 HA^2	800 V / 84 A	2412 V	216 A	5445 A^2	L: 3 S: 5 D: 1 C: 3
[27]	Limited BPF/ No Interleaving/ Cannot achieve $V_{o,min}$ of 200 V	0.623	Unequal current (2 Inputs) $I_{in1} = 48.5\,A$ $I_{in2} = 35.5\,A$	$500\mu H, 35.5\,A$ $2\,mH, 13.5\,A$ $500\mu H, 22\,A$ $2mH, 13.5\,A$ 1.601125 HA^2	927 V / 62 A	2568 V	223 A	4004 A^2	L: 4 S: 7 D: 1 C: 4
Proposed HCRC Config. 3(a)	No Limitation	0.76	Equal current (2 Inputs) 42 A each	$220\mu H, 21\,A$ (x4) 0.417648 HA^2	400 V / 42 A	2200 V	231 A	2705 A^2	L: 4 S: 8 C: 4

*Equal duty operation is considered for topologies with multiple phases

+For fair comparison, inductors for each converter are designed to ensure equal input current ripple ($\Delta I_{in} = 2.2A$) from different input sources which is close to 2.5% of the net input current to the converter (84 A). The inductance value and current rating of each inductor are specified.

@This is defined as the summation of the product of the inductance value, peak inductor current and rms inductor current of different inductors in the converter ($\sum LI_{pk}I_{rms}$), which is a measure of the size of the inductors.

**This is the summation of the peak voltage across all switches and diodes in the converter ($\sum V_{sw,pk} + \sum V_{D,pk}$)

##This is the summation of the peak current across all switches and diodes in the converter ($\sum I_{sw,pk} + \sum I_{D,pk}$)

++This is the summation of the square of the rms current of all switches and diodes in the converter ($\sum I^2_{sw,rms} + \sum I^2_{D,rms}$). This metric is related to the conduction losses in the switches for a bidirectional converter.

#L: Inductor, S: Switches, D: Diodes, C: Capacitors

In configuration 3(a), the input current ripple from each voltage source is reduced due to interleaving between the two phases. Similar to configuration 2, the inductor is designed for maximum current through each phase inductor and maximum input current ripple at rated power and voltage of the converter. The input current ripple in this configuration is given by (11). Inductor with smaller inductance value can be used with configuration 3(a) to ensure same input current ripple as configuration 2. This results in significant reduction in inductor size as well.

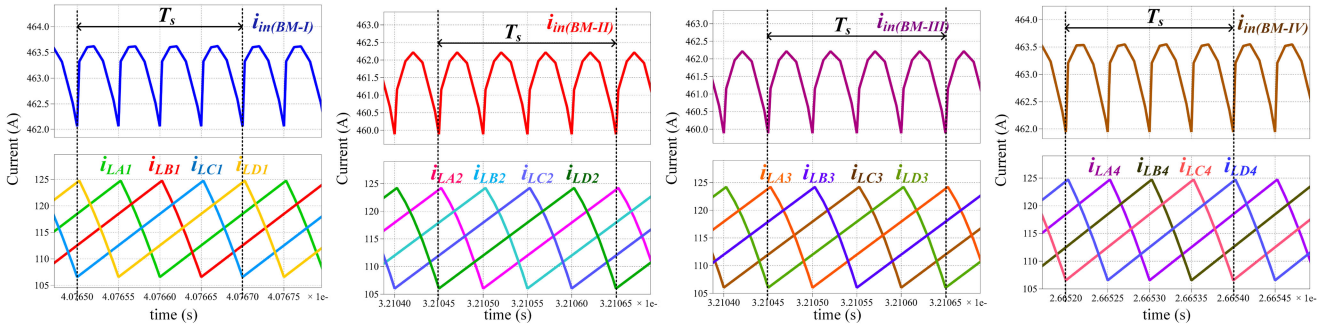
$$\Delta I_{inz1(config.3(a))} = \frac{V_{out}(1-D)(2D-1)}{4 f_{sw} L} \tag{11}$$

B. CAPACITOR SELECTION

The intermediate capacitor design depends on the maximum voltage stress and the maximum rms current flowing through it at maximum rated power and voltage. These are already specified in Table 2. The voltage ripple across C_2 or C_3 does not affect the converter operation but for C_1, the capacitance should meet the voltage ripple criteria. When the converter is operating at the lowest possible output voltage (200 V in this case), the voltage across C_1 is significantly low. With high ripple across C_1, this voltage can become negative, which is not desired for normal converter operation. Hence, C_1 needs to be designed accordingly to ensure the voltage ripple across it does not become negative. The desired capacitance value for C_1 can be calculated by (12). Here, I_ph is the maximum phase current and $D_{2,zoneII}$ is the duty of phase 2 switch in Zone II corresponding to converter operation at 200 V output voltage. $V_{C1,max}$ is the maximum allowed voltage ripple which is twice the maximum steady state value of C_1.

$$C_I = \frac{I_{ph,max}(1 - D_{2,zoneII})}{f_{sw}\Delta V_{C1,max}} \tag{12}$$

The output capacitor should meet both the maximum voltage ripple as well as rms current requirement. The maximum



(a) Battery Module I (b) Battery Module II (c) Battery Module III (d) Battery Module IV

FIGURE 14. PLECS simulation waveform showing battery current and inductor current of different parallel HCRC modules in a stack for configuration 2.

rms current is at maximum rated power in Zone I operation and is given in Table 2. The voltage ripple across the output capacitor is same as that for conventional boost converter and can be designed accordingly.

C. SWITCH SELECTION

The maximum voltage across the bottom switch is equal to the maximum output voltage of the converter in Zone II. For the proposed 4-phase HCR, the maximum output voltage in Zone II with 48 V input voltage is 384 V. For top side switches, the maximum voltage stress is equal to half the maximum output voltage in Zone I operation. In this case, the maximum voltage across top switches is 400 V. The current in the switches varies with zone of operation. The bottom switch current rating is specified corresponding to maximum output voltage and maximum rated power in Zone I. The maximum current in the bottom switches (neglecting the inductor ripple) is equal to twice the maximum input current for each phase as given in Table 2. For the top switches, U_4 sees the maximum current stress equal to four times the maximum individual phase current(neglecting the inductor ripple) in Zone II operation. The current rating of the top switches is specified in Table 3.

VII. SIMULATION RESULTS

The parallel operation of different HCRC modules discussed in Section II. C. is verified through simulations carried out in PLECS. Simulation results for only configuration 2 (shown in Fig. 4) are presented here as a proof of concept. The simulated converter is designed to be rated for Chevrolet Bolt battery pack. Simulations are carried out with each HCRC module rated for 22 kW and all the battery modules have a nominal voltage of 48 V, whereas the output voltage of each HCRC module is set to 800 V. The switching frequency is set to 50 kHz. In Fig. 14, different battery module current as well as inductor currents are shown. The advantage of interleaving multiple HCRC modules in parallel can be observed here. A 40 μH inductor is chosen here for the HCRC modules. Even though the ripple across each inductor is 18 A, the net battery ripple current is close to 2 A which less than 0.5% of the net input current. With equal duty, inherent current sharing of HCRC is still retained in the parallel configuration. There is

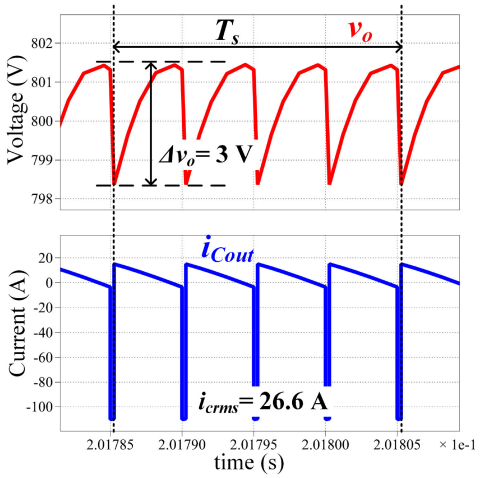


FIGURE 15. PLECS simulation waveforms showing output voltage and output capacitor current waveform of parallel HCRC in a stack for configuration 2.

no difference in the switch voltage and current stress of HCRC due to parallel operation and hence, the simulation waveforms are not presented here.

Another advantage with parallel HCRC operation is the interleaving at the output side of HCRC. The output voltage and output capacitor current waveform are shown in Fig. 15. Even for a small capacitance value of output capacitor (10 μF in this case), the voltage ripple across the output is less than 0.5% as shown in figure. Similarly, for the net output power of 88 kW (Four 22 kW HCRC modules in parallel), the rms current across the output capacitor is close to 26 A. Thus, with the proposed interleaving of multiple HCRC modules, the passive component value as well as size can be significantly reduced.

VIII. EXPERIMENTAL RESULTS

The proposed multi-input HCRC operation is verified experimentally through a single scaled hardware prototype. Due to limited testing facilities available, the parallel operation of HCRC is not verified experimentally. Also, experimental results of single HCRC corresponding to only configuration 2

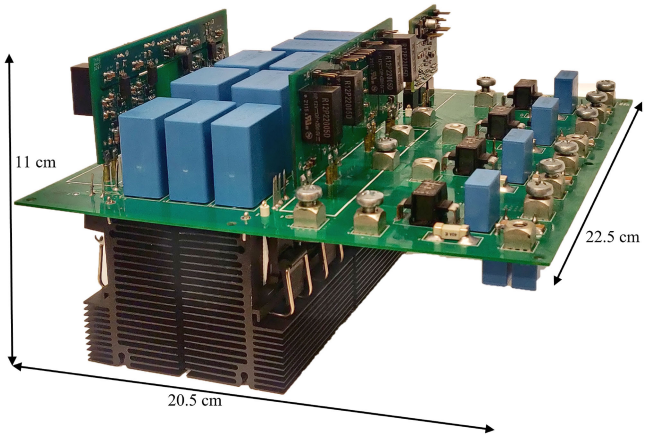


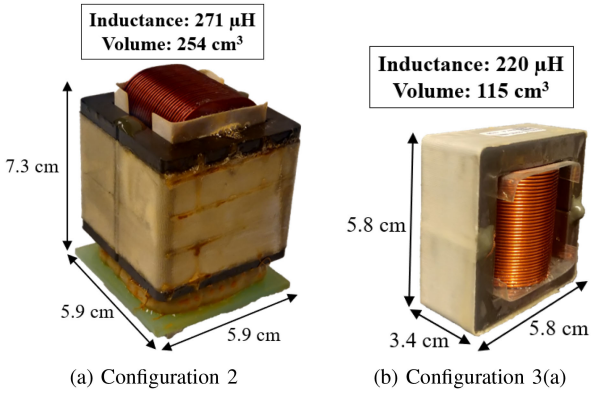
FIGURE 16. 48 V to 800 V, 4 kW 4-phase multi-input HCRC hardware prototype.

TABLE 5. Hardware Prototype Specifications

Parameters	Specifications
Rated Power(P_o)	4 kW
Input voltage(V_{in})	40 V – 50 V
Output voltage(V_o)	200 V–800 V
Switching Frequency(f_{sw})	50 kHz
Inductor for Configuration 2	271 μH
Inductor for Configuration 3(a)	220 μH
Intermediate capacitor 1(C_1)	24 μF/ 300 V
Intermediate capacitor 2(C_2)	10 μF/ 630 V
Intermediate capacitor 3(C_3)	8 μF/ 750 V
Output capacitor(C_o)	14 μF/920 V
Switch	C3M0015065K(CREE)

and 3(a) operation are presented here. Configuration 1 corresponds to single input operation of HCRC which has already been previously discussed whereas configuration 3(b) is a slightly modified version of configuration 3(a). The developed 4-phase multi-input HCRC hardware prototype is shown in Fig. 16. To minimize noise in the gate driver and sensor circuitry, separate boards are designed and mounted on the power board as shown in figure. The four phase inductors are placed outside the board which allows us to test the converter for both the interleaved and non-interleaved cases. The final specifications of the hardware prototype are shown in Table 5. The nominal input voltage to the converter is 48 V and the output voltage can vary between 200 V to 800 V. The components selected for the hardware prototype meet all the design requirements as discussed in the previous section. 650 V SiC MOSFET (C3M0015065 K) from CREE are used for all the switches.

Two different off-the-shelf inductors are chosen for obtaining the experimental results as shown in Fig. 17 which meet the design requirement. As there is no interleaving in the four-input supply configuration, inductor with high inductance value is chosen to minimize the input current ripple. The inductance for this case is 271 μH. The required inductance decreases in case of two-input supply configuration due to



(a) Configuration 2 (b) Configuration 3(a)

FIGURE 17. Inductor selected for (a) Configuration with four input sources (b) Interleaved configuration with two input sources .

interleaving. This enables to use an inductor with small inductance and smaller size. As seen from Fig. 17, the inductance for interleaved case reduces to 220 μH while the size reduces by 55% compared to the non-interleaved case. As there are four inductors used, the net reduction in size is significant due to interleaving. Also, the inductor used for configuration 3(a) has lower winding resistance which results in lower conduction losses in the inductor.

A. CONVERTER WAVEFORM FOR CONFIGURATION 2

The converter is operated with four different input power sources with each source connected to an individual phase. Experimental results corresponding to both zones of operation are presented here. In Fig. 18, inductor current and input voltage waveforms corresponding to both zones of operation are shown. The current is equally shared among the four phases in both zones. In Zone II operation, as each phase has different duty of operation, the inductor current ripple in each phase is different but the average value is the same. Similarly, experimental waveform for intermediate and output capacitor voltage in both zones of operation are shown in Fig. 19. The intermediate capacitor voltage is a fraction of output voltage in both zones and matches well with the analytical value. The voltage stress across switches for the two zones of operation are shown in Fig. 20. The switch voltage stress in Zone I operation is low for bottom switches compared to Zone II operation.

The converter operation with unequal current among different phases for both zones of operation is shown in Fig. 21. Here, the four input sources are providing different current based on the voltage of the input source. The input source with the lowest voltage supplies the least current while the source with the highest voltage supplies the maximum current. This would be similar to the case where differently charged battery packs are connected to the converter where the current from each one is drawn based on their charge status. It is ensured that the net input power to the converter remains same and the output voltage is regulated to the desired value

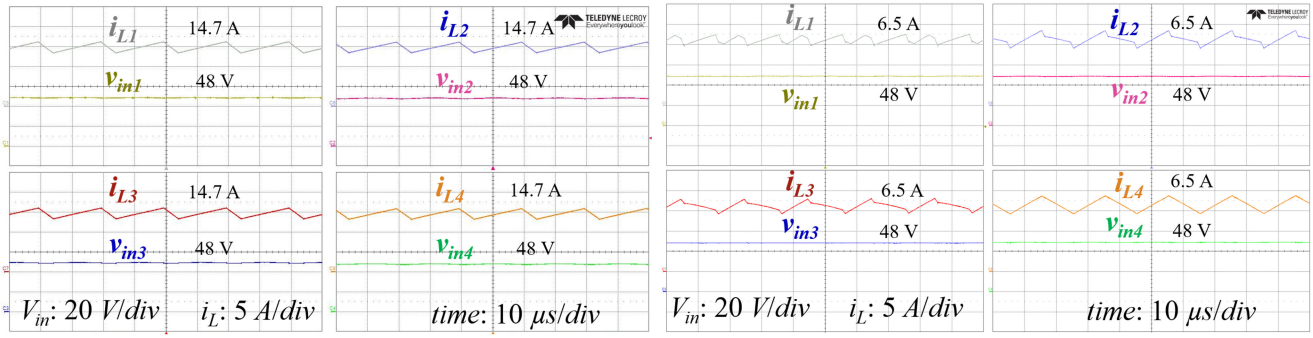


FIGURE 18. Input voltage and inductor current waveform for HCRC configuration 2 in (a) Zone I: 48 V to 800 V (b) Zone II: 48 V to 250 V.

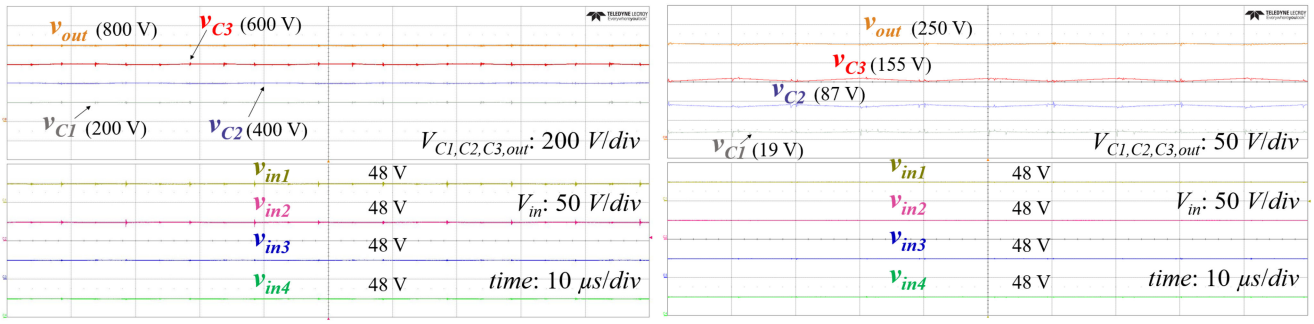


FIGURE 19. Intermediate and output capacitor voltage for HCRC configuration 2 in (a) Zone I: 48 V to 800 V (b) Zone II: 48 V to 250 V.

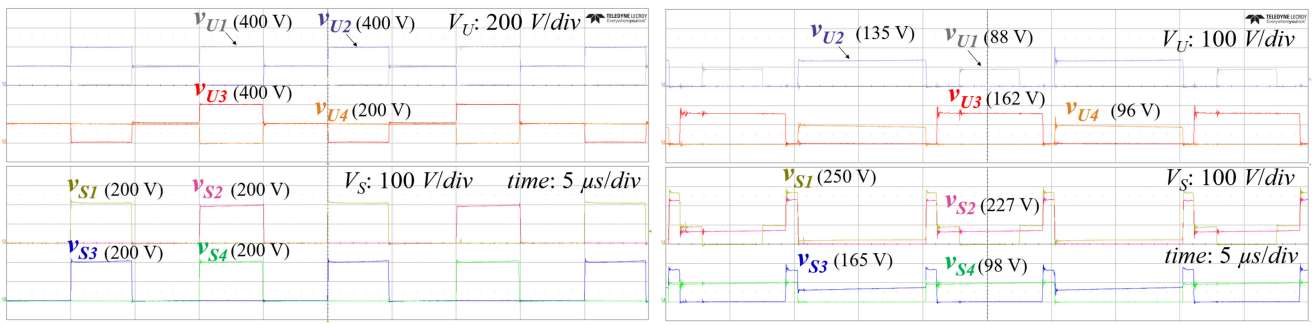


FIGURE 20. Top and bottom switch voltage for HCRC configuration 2 in (a) Zone I: 48 V to 800 V (b) Zone II: 48 V to 250 V.

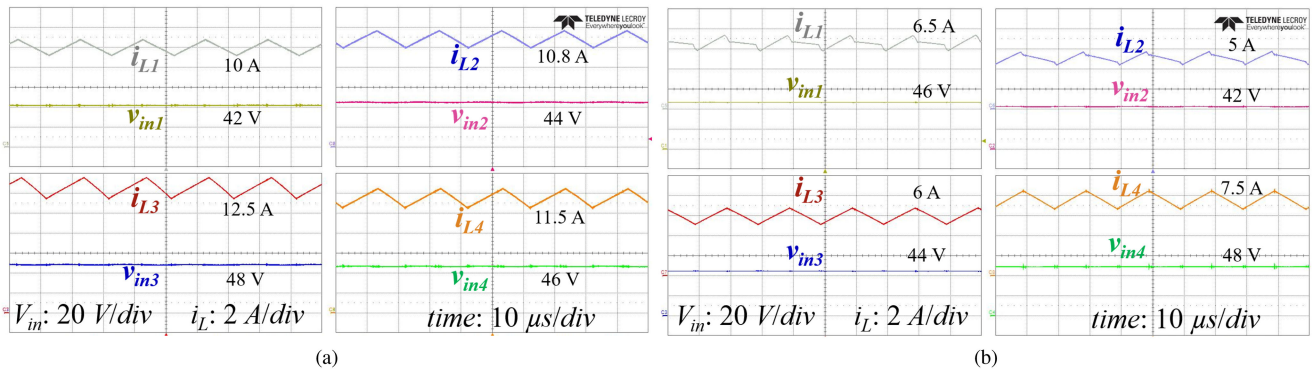
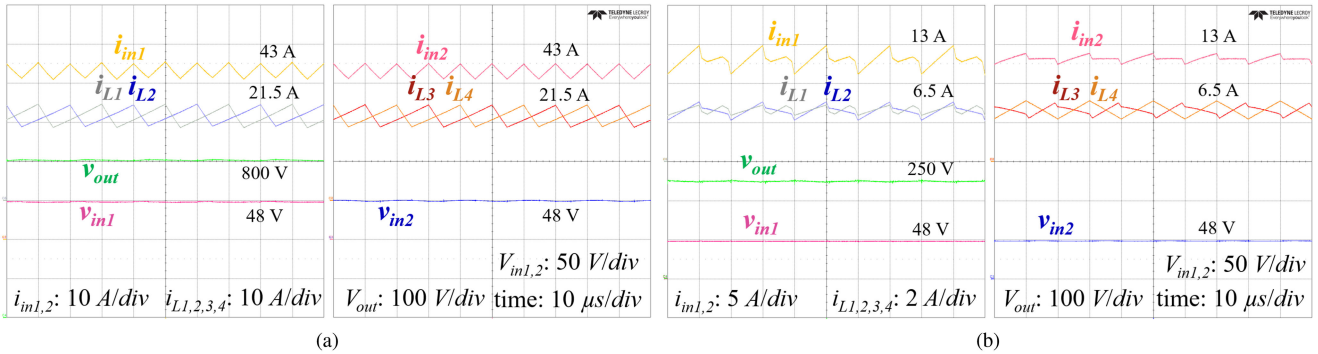
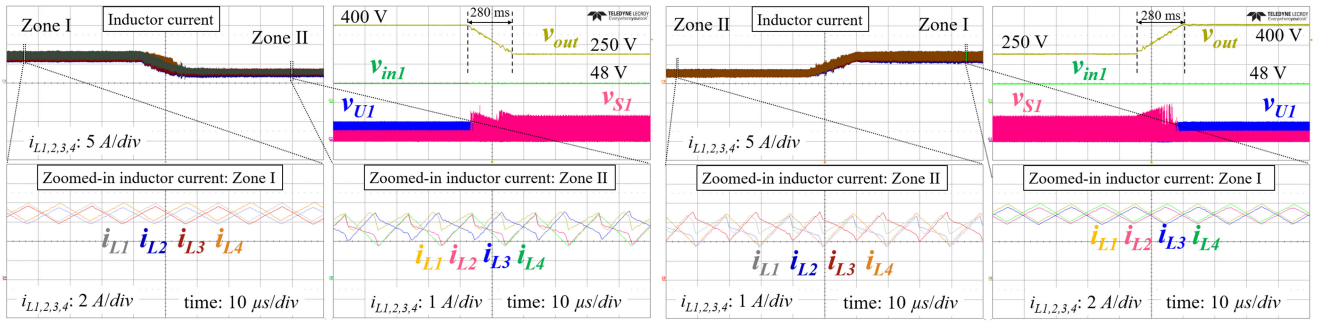


FIGURE 21. Unequal input voltage and current operation of HCRC configuration 2 in (a) Zone I: 48 V to 400 V (b) Zone II: 48 V to 300 V.



(a) (b)

FIGURE 22. Input voltage, output voltage and inductor current for HCRC configuration 3(a) in (a) Zone I: 48 V to 800 V, 4 kW (b) Zone II: 48 V to 250 V, 1.25 kW.



(a) (b)

FIGURE 23. Experimental waveform for converter operation with varying DC link voltage (v_{in} : 50 V/div, v_{out} : 100 V/div,v_S, v_U : 200 V/div, time : 200 *ms*/div) (a) Ramp-down in output voltage from 400 V to 250 V (Zone I to Zone II transition) (b) Ramp-up in output voltage from 250 V to 400 V (Zone II to Zone I transition).

with unequal current sharing. There is only a slight variation in the voltage and current stress of the devices compared to equal current sharing case and is not presented here to prevent redundancy.

B. CONVERTER WAVEFORM FOR CONFIGURATION 3(A)

In this case, the converter is operated with two input sources with interleaving among the first two phases and the last two phases. Experimental waveforms for inductor and input current corresponding to converter operation in Zone I at rated power and rated voltage are shown in Fig. 22(a). It can be seen that the current is equally shared among the four inductor phases as well as the two input sources. The inductance value reduces to 120 μH under full load condition. The input current ripple is 4.3 A in this case which is 10% of the input current ripple. Similarly, experimental waveform for converter operation in Zone II is shown in Fig. 22(b). As each phase has different duty of operation, the inductor current ripple for each phase is different in this case. This results in different input current ripple for the two sources. The input current ripple of source 1 is 3.8 A and of source 2 is 1.6 A. The voltage stress across different devices in the converter remain the same as that for configuration 2 and hence, are not presented here.

C. VARIABLE DC LINK VOLTAGE

Experimental waveforms with output voltage varying from 250 V to 800 V are presented here for configuration 2 with input voltage set to 48 V for all four input sources. The converter is operated in closed loop with an inner current control loop and outer voltage control loop with a resistive load. A ramp change in output voltage reference is provided to emulate varying DC link voltage.

In Fig. 23, the output voltage is ramped-up from 250 V to 400 V with converter transitioning from Zone II to Zone I operation and vice-versa, without any transient spikes. The zoomed-in inductor current waveforms before and after the transition are shown in the figure which shows equal current sharing ensured by closed loop control. Due to limited channel availability, only the input voltage of source 1 is shown in the results. The bottom switch voltage is high in Zone II operation (equal to output voltage) which becomes low as the converter transitions to Zone I operation.

The converter operation with output voltage ramping down from 800 V to 400 V and vice- versa, is shown in Fig. 24. The converter is operating in Zone I operation over the entire range with no transient spikes during transition. The switch voltages increase gradually with the increase in output voltage and the input current is equally shared among different phases. Thus, the converter can operate with wide

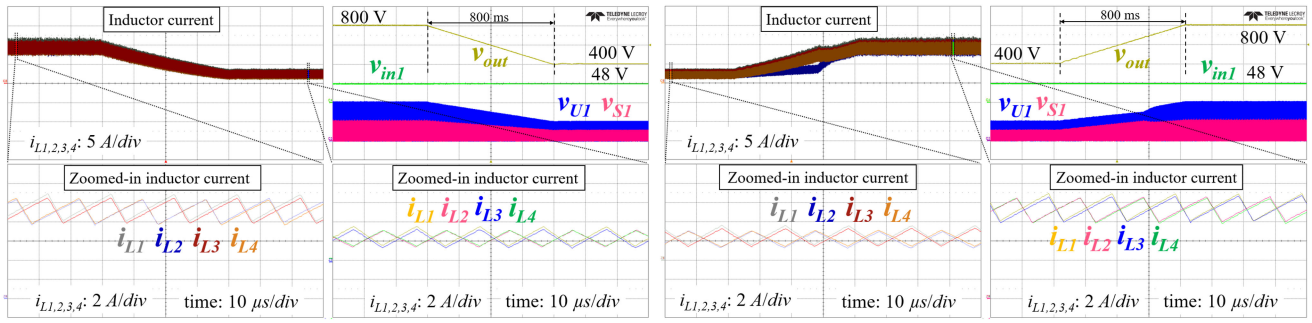


FIGURE 24. Experimental waveform for converter operation with varying DC link voltage in Zone I (v_{in} : 50 V/div, v_S, v_U, v_{out} : 200 V/div, time : 200 ms/div) (a) Ramp-down in output voltage from 800 V to 400 V (b) Ramp-up in output voltage from 400 V to 800 V.

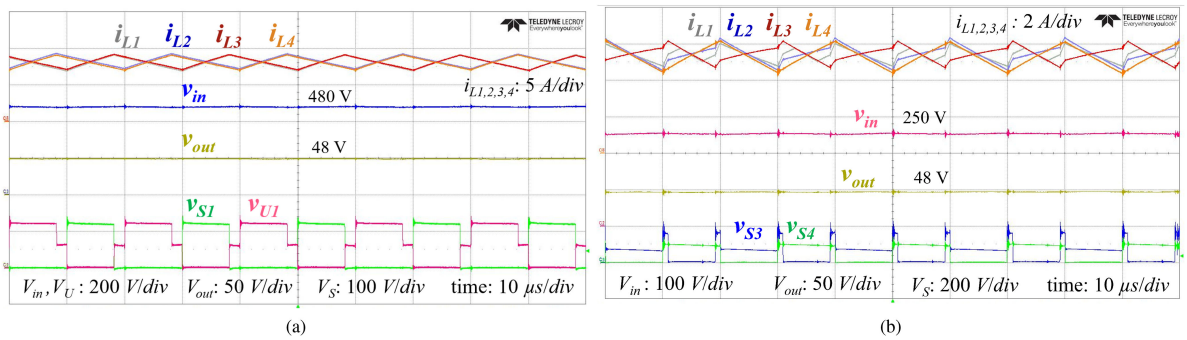


FIGURE 25. Experimental waveform for converter operation in buck mode with equal current sharing in (a) Zone I: 480 V to 48 V (b) Zone II: 250 V to 48 V.

variation in DC link voltage which is desired for EV application.

D. CONVERTER WAVEFORM IN BUCK MODE

The converter can operate in buck mode during regenerative braking as well as during charging from onboard charger or external DC fast charger through the DC link. For the verification of the buck mode of operation of the converter, the high voltage side is replaced with a DC voltage source and the low voltage side is connected to a resistive load. Due to limited electronic load availability in the lab, all the four input phases are connected to the same resistive load for obtaining the experimental results. The inductor used for obtaining buck mode operation results is 271 μH. The input voltage in case of buck mode is limited to a maximum of 480 V due to the voltage rating limit of the DC source available. The converter operation in both zones of operation is shown in Fig. 25. It can be seen that the current among different phases is shared equally. Same as boost mode, Zone II buck mode operation has different phases operating at different duty. The voltage and current rating of different devices in buck mode remain the same as in boost mode. In case of batteries connected to each individual phase, the charging current can be individually controlled in each phase based on the charge status of the battery of that particular phase. This has been shown here by having unequal current sharing among the different inductors while regulating the output voltage to 48 V and is shown in Fig. 26.

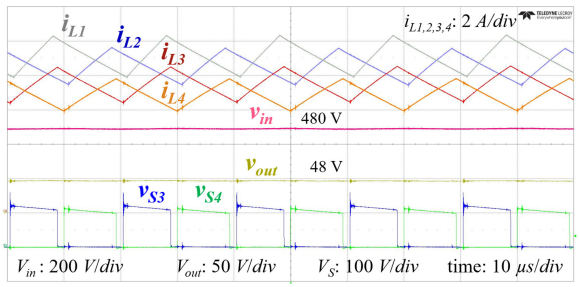


FIGURE 26. Experimental waveform for converter operation in buck mode with unequal current sharing (as commanded) in Zone I from 480 V to 48 V.

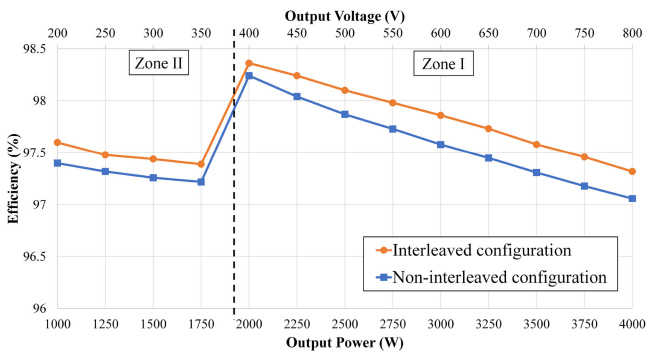


FIGURE 27. Converter experimental efficiency with varying output power and output voltage with input voltage fixed to 48 V at 50 kHz switching frequency.

TABLE 6. Comparison With Other Non-Isolated DC-DC Converter Topologies for EV Traction System

Ref.	Multiple-Input	Soft-switching	Voltage Gain	Main Switch	Specifications	Peak η	Rated Power η
Proposed (HCRC)	Yes	No	$\frac{4}{(1-D)}$	SiC	V_{in}: 48 V V_{out}: 200 V-800 V 4 kW, 50 kHz	98.36 % @ 2 kW	97.3 %
[17] (2020)	No	No	$\frac{2(1-D)}{(1-2D)}$	Si	V_{in}: 25 V-80 V V_{out}: 200 V 100 W, 20 kHz	95.4 % @ 50 W	93.1 %
[18] (2021)	No	Yes	$\frac{1}{(Q+0.5-D)}$	Si	V_{in}: 50 V V_{out}: 400 V 1 kW, 50 kHz	94.5 % @ 320 W	93.1 %
[19] (2017)	No	No	$\frac{2}{(1-D)}$	Si	V_{in}: 50 V-120 V V_{out}: 400 V 1.6 kW, 20 kHz	96.62 % 1.6 kW	96.62 %
[20] (2020)	No	No	$\frac{2+D}{2-D}$	GaN	V_{in}: 90 V-300 V V_{out}: 800 V 1.3 kW, 100 kHz	97.8 % @ 500 W	95.7 %
[21] (2012)	No	No	$\frac{1}{1-D}$	IGBT	V_{in}: 220 V V_{out}: 220 V-660 V 55 kW, 20 kHz	97.8 % @ 5 kW	96.3 %
[22] (2021)	No	Yes	$\frac{D_A}{D_A-D}$	SiC	V_{in}: 250 V-400 V V_{out}: 800 V 80 kW, 50 kHz	96.5 % @ 80 kW	96.5 %
[28] (2017)	Yes	No	$\frac{1-D_1}{(1-D_2)(D_2-D_1)}$	Si	V_{in}: 20 V V_{out}: 120 V 80 W, 30 kHz	92 % @ 40 W	91 %
[29] (2015)	Yes	No	$\frac{D}{(1-D)}$	IGBT	V_{in}: 130 V V_{out}: 300 V 5 kW, 20 kHz	95 % @ 5 kW	95 %

E. LOSS BREAKDOWN AND EFFICIENCY

The converter is operated for a wide range of output voltage with the input voltage fixed to 48 V. Experimental efficiency of the converter operating in boost mode with varying output power and output voltage is shown in Fig. 27. Here, the load varies proportionally to the varying output voltage, keeping the output current fixed to emulate the EV operation. The output power is shown in the bottom x-axis and the output voltage is specified in the top x-axis in the plot. The converter is able to achieve peak efficiency of 98.36% in configuration 3(a) and 98.24% peak efficiency in configuration 2 corresponding to 400 V, 2 kW operation. For the whole range of operation, the converter efficiency is above 97%. The interleaved configuration has better efficiency as the inductor losses are lower when compared to non-interleaved case. With multiple HCRC in parallel connection, there will be 90° phase shift among the 4-phase inductors which will further reduce the inductor value and size while reducing the series DC resistance and is expected to yield further improvement in efficiency. There is a sudden drop in converter efficiency when the converter transitions from Zone I to Zone II operation. This is because the voltage and current stress across the bottom switches increases significantly in Zone II, resulting in higher switching losses. The peak efficiency at rated voltage and rated power is 97.32% achieved for the interleaved configuration case.

The converter analytical loss breakdown for both zones of operation for the configuration 2 is presented in Fig. 28. The loss calculation is carried out in PLECS simulation. It can be seen that the dominant component of losses in Zone I operation is the switch conduction loss due to high input current. In Zone II operation, the MOSFET switching loss is dominant due to higher voltage and current stress in devices. The converter has similar loss breakdown in configuration 3(a) with difference only in the inductor losses and hence, is not presented here to keep the paper concise. The buck mode of operation is expected to have similar efficiency results over the wide range of converter operation. Experimental efficiency of the converter in buck mode with configuration 2 inductor is 98.15%, operating at 400 V to 48 V at 2 kW at 50 kHz switching frequency. This is similar to boost mode efficiency in configuration 2.

In Table 6, the proposed converter is compared with other DC-DC converter topologies in literature proposed specifically for EV traction system discussed. The proposed converter configuration has higher gain enabling it to be implemented with low voltage battery packs. The proposed converter also has the widest output voltage range. Also, the converter has highest efficiency among the different topologies discussed here.

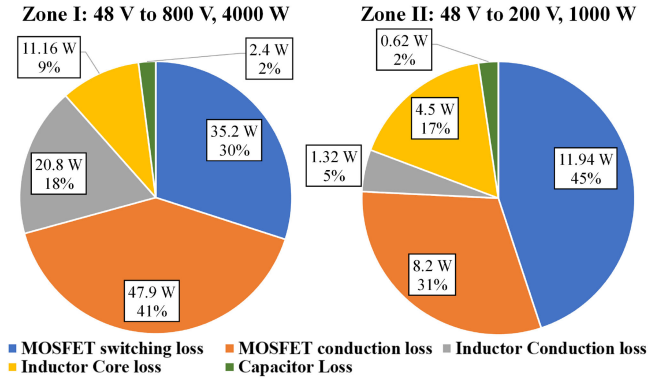


FIGURE 28. Converter loss breakdown in configuration 2.

IX. CONCLUSION

In this paper, a new architecture for EV traction system with 48 V battery pack and multi-input high conversion ratio converters is proposed. The topology achieves high gain and supports wide variation in output voltage as required for variable DC link applications, while keeping the device voltage and current stresses low. It also has the capability to control the currents in the different phases to be unequal in order to allow charging and discharging of battery modules independent of each other. Multiple possible configurations of HCRC in parallel are also presented along with simulation verification. A sample design of the proposed system corresponding to Chevrolet Bolt battery pack is also discussed. The HCRC operation is verified experimentally through a scaled hardware prototype for both interleaved and non-interleaved configurations. In case of interleaved configuration, the net inductor size reduces by 55% for with slight increase in overall efficiency for the whole range of converter operation. The converter can achieve a output voltage varying from 200 V to 800 V without any transient spikes. The converter is able to achieve high efficiency over the entire range of operation with a peak efficiency of 98.36% corresponding to 400 V output voltage at 2 kW for interleaved configuration.

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ANKUL GUPTA (Student Member, IEEE) received the bachelor's degree from the Maulana Azad National Institute of Technology, Bhopal, India, in 2015, and the M.S. degree in electrical engineering in 2019 from Arizona State University, Tempe, AZ, USA, where he is currently working toward the Ph.D. degree with the School of Electrical, Computer and Energy Engineering.

His research interests include topologies and control methods for dc-dc converters, soft-switching techniques for switched mode power converters, and wide bandgap (WBG) devices based power electronic interfaces.

RAJAPANDIAN AYYANAR (Senior Member, IEEE) received the M.S. degree in power electronics from the Indian Institute of Science Bangalore, Bengaluru, India, in 1995, and the Ph.D. degree in power electronics from the University of Minnesota, Minneapolis, MN, USA, in 2000. He is currently a Professor with Arizona State University, Tempe, AZ, USA.

SOMBUDDHA CHAKRABORTY (Member, IEEE) received the M.S and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2003 and 2006, respectively. He is currently the Design Manager of power technology with Kilby Labs, Texas Instruments, Santa Clara, CA, USA. Prior to his current position, he was a Design Engineer with General Electric, where he worked on new product development for electronic ballast. Later, he was a System Design Manager with Volterra Semiconductors, Fremont, CA, USA, designing multiphase VR solutions for Datacenter applications.

His research and product development interests include high density AC/DC and DC/DC power management system for computing, automotive, and industrial applications using leading edge process, package, integration and circuit techniques to enhance power delivery efficiency.