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A Review of Current-Limiting Control of Grid-Forming Inverters Under Symmetrical Disturbances

BO FAN [1] (Member, IEEE), TENG LIU [1] (Member, IEEE), FANGZHOU ZHAO [1], HENG WU [1] (Member, IEEE), AND XIONGFEI WANG [1,2] (Fellow, IEEE)

[1]Department of Energy (AAU Energy), Aalborg University, 9220 Aalborg, Denmark
[2]Division of Electric Power and Energy Systems, KTH Royal Institute of Technology, 11428 Stockholm, Sweden

CORRESPONDING AUTHOR: XIONGFEI WANG (e-mail: xwa@energy.aau.dk)

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ABSTRACT Grid-forming (GFM) inverters are recognized as a viable solution to increase the penetration of renewable energy in bulk power systems. However, they are physically different from synchronous generators in terms of overcurrent capability. To protect the power semiconductor devices and support the power grid under severe symmetrical disturbances, the GFM control systems should be able to achieve the following requirements: current magnitude limitation, fault current contribution, and fault recovery capability. Various current-limiting control methods are reported in the literature to fulfill these goals, including current limiters, virtual impedance, and voltage limiters. This paper presents an overview of those methods. Emerging challenges that need to be addressed, including temporary overcurrent, unspecified output current vector angle, undesired current saturation, and transient overvoltage, are pointed out. Comparative simulations are conducted to demonstrate the performance of different methods under grid voltage drops and phase jumps. Finally, open issues of current-limiting control methods for GFM inverters, including transient stability assessment, voltage source behavior under overcurrent conditions, and windup of voltage controllers, are shared.

INDEX TERMS Grid-forming (GFM) inverter, current-limiting control, current magnitude limitation, fault current contribution, fault recovery capability.

NOMENCLATURE

θ	phase angle generated by outer-loop control, in rad.
E	voltage magnitude generated by outer-loop control, in p.u.
i	inverter output current, in p.u.
I	inverter phase current magnitude, $I = \|i\|$, in p.u.
I_M	maximum allowed phase current magnitude, in p.u.
i_p	inverter output active current, in p.u.
i_q	inverter output reactive current, in p.u.
i_{ref}	output current reference, in p.u.
$\bar{i}_{ref}$	saturated output current reference, in p.u.
P	inverter output active power, in p.u.
P_{ref}	inverter output active power reference, in p.u.
Q	inverter output reactive power, in p.u.
Q_{ref}	inverter output reactive power reference, in p.u.
v_e	equivalent internal voltage, in p.u.
v_g	grid voltage, in p.u.
v_{ref}	voltage reference generated by outer-loop control, in p.u.
v_t	inverter terminal voltage, in p.u.
V_t	inverter terminal voltage magnitude, $V_t = \|v_t\|$, in p.u.
v_{PCC}	PCC voltage, in p.u.
V_{PCC}	PCC voltage magnitude, $V_{PCC} = \|v_{PCC}\|$, in p.u.
v_{PWM}	voltage modulation reference, in p.u.
V_{ref}	voltage magnitude reference, in p.u.
ω_{ref}	angular frequency reference, in rad/s.
X_T	transformer reactance, in p.u.

Z_e equivalent output impedance, in p.u.
Z_{Fault} fault impedance between the cable and the ground, in p.u.
Z_f inverter filter impedance, in p.u.
Z_{g1} grid impedance between PCC and fault location, in p.u.
Z_{g2} grid impedance between fault location and grid, in p.u.

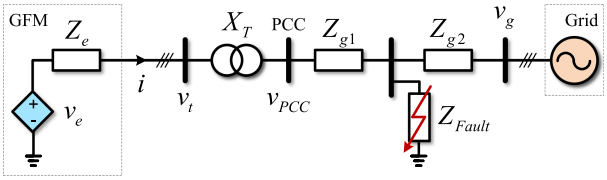

FIGURE 1. Simplified circuit model of a GFM inverter under fault.

I. INTRODUCTION

Grid-forming (GFM) inverter technology is treated as a promising solution for future bulk power systems with high penetration of renewable-energy power generation [1], [2]. Differing from conventional grid-following (GFL) inverters, GFM inverters are controlled as voltage sources behind impedance in normal operation [3], [4], and hence, they are able to establish system voltage and frequency autonomously [5], and have higher stability robustness in weak grid interconnections [6].

The voltage source behavior of GFM inverters makes their output currents highly dependent on external system conditions. Upon large disturbances such as voltage drops or phase jumps at the point of common coupling (PCC) [7], synchronous generators can, in general, supply 5–7 p.u. overcurrent [8], while semiconductor-based inverters can only handle 1.2–2 p.u. overcurrent typically [9], [10], which prevents them from maintaining the voltage profile as in normal operation [11]. To successfully ride through these disturbances, appropriate current-limiting control methods are required for GFM inverters, which need to satisfy the following requirements [7], [12], [13], [14]:

- *Current magnitude limitation:* The GFM inverter's phase current magnitude should be lower than its maximum allowed limit, e.g., 1.2–2 p.u., to protect the power semiconductor devices.
- *Fault current contribution:* The GFM inverter should supply required active/reactive currents to support the power grid during disturbances [13], e.g., supplying full reactive current when the PCC voltage falls below 0.5 p.u. [7].
- *Fault recovery capability:* The GFM inverter should be able to restore its normal operation when disturbances are cleared [13], e.g., restoring active power to 90% of its pre-fault value within 0.5 s after the disturbance clearance [14].

To meet these requirements, various current-limiting control methods for GFM inverters are reported in the literature, including current limiters, virtual impedance, and voltage limiters. The current limiters usually make the inverter behave as a current source during overcurrent conditions, which can facilitate the regulation of the output current vector angle to meet the fault current contribution requirement. In comparison, the virtual impedance methods and voltage limiters can maintain the voltage source behavior of the GFM inverter to some extent during severe disturbances, which may allow for automatic fault recovery. This paper reviews those methods and identifies the emerging challenges that need to be addressed, including temporary overcurrent, unspecified output current vector angle, undesired current saturation, and transient overvoltage. Further, the performance of different methods is demonstrated by simulations under grid voltage drops and phase jumps. Finally, open issues that need to be resolved, including transient stability assessment, voltage source behavior under overcurrent conditions, and windup of voltage controllers, are shared.

The remainder of this paper is organized as follows: Section II illustrates the basics of current-limiting control of GFM inverters. In Sections III-V, current limiters, virtual impedance methods, and voltage limiters are reviewed, respectively. Open issues are shared in Section VI. Finally, Section VII concludes this paper.

II. BASICS OF CURRENT-LIMITING CONTROL METHODS

Fig. 1 shows a simplified circuit model of a grid-tied GFM inverter. The GFM inverter consists of an internal voltage source v_e and equivalent output impedance. The filter impedance will be included in Z_e, if no inner-loop control is utilized. When inner-loop control is used, the filter impedance will not be included in Z_e [24].

According to the Kirchhoff's circuit laws, the phase current magnitude of the GFM inverter can be expressed as

$$I = \|i\| = \frac{\|v_e - v_{PCC}\|}{\|Z_e + \mathrm{j}X_T\|} \tag{1}$$

where $\|\cdot\|$ denotes the modulus of a complex variable, j is the unit imaginary number. When a disturbance causes PCC voltage drop or phase angle jumps, the voltage difference $\|v_e - v_{PCC}\|$ can increase. Consequently, I may exceed its maximum allowed value I_M of the GFM inverter.

To prevent the GFM inverters from overcurrent tripping, various current-limiting control strategies are reported in the literature [25], [26]. Based on how the current magnitude I is restricted, these strategies can be classified into three types:

- *Current limiter:* GFM control restricts the phase current magnitude I within the maximum allowed value I_M through closed-loop current control [27], [28], [29].
- *Virtual impedance:* GFM control adjusts the phase current magnitude I by increasing the total impedance $\|Z_e + \mathrm{j}X_T\|$ based on virtual impedance/admittance control methods [30], [31], [32].
- *Voltage limiter:* GFM control regulates the phase current magnitude I by reducing the voltage difference $\|v_e - v_{PCC}\|$ via voltage limiters [33], [34].

TABLE 1. Performance Comparisons of Different Current-Limiting Control Methods Under Symmetrical Disturbances

	Current limitation performance	Fault current controllability	Fault recovery capability
Current limiter	• Good in the steady state • Temporary overcurrent in transients	• Change to PLL-based GFL inverter and adjust current references [15] • Adjust power references [16]	May fail to recover due to the windup of voltage controllers [17]–[19]
Virtual impedance	• Tradeoff between current limitation and stability [20]–[22] • Temporary overcurrent in transients	• Depend on the virtual impedance and electrical network parameters • Adjust power references [23]	Good to restore normal operation automatically
Voltage limiter	• Good in the steady state • Temporary overcurrent in transients	Depend on the voltage limiter and electrical network parameters	Good to restore normal operation automatically

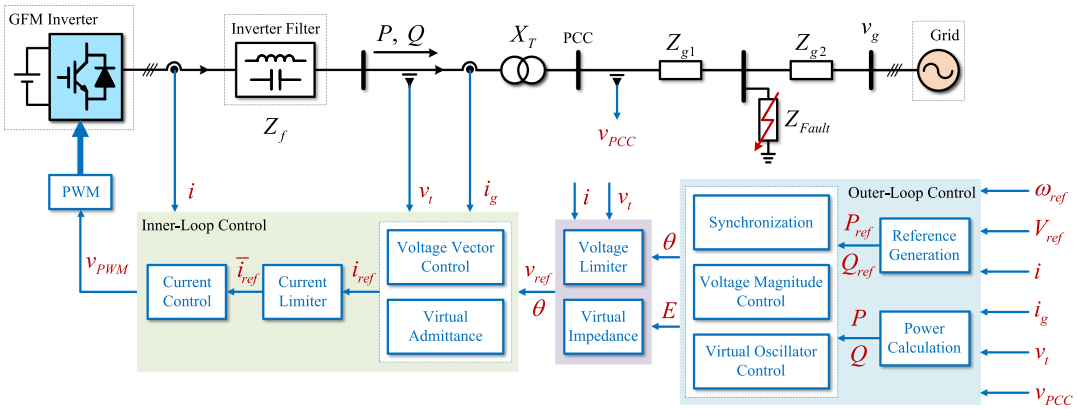

FIGURE 2. Control diagram of a GFM inverter with current-limiting control methods.

Comparisons of different methods in terms of current limitation performance, fault current controllability, and fault recovery capability are illustrated in Table 1, which will be discussed in detail in the following sections.

Fig. 2 illustrates a general control diagram of a GFM inverter furnished with current-limiting control methods. The control system is composed of two control layers, i.e., the outer-loop control layer and the inner-loop one. The main objective of the outer-loop control is to synchronize the GFM inverter with the power grid and regulate the terminal voltage magnitude. A voltage magnitude E and phase angle θ will be generated based on the active and reactive power references P_{ref}, Q_{ref}, voltage and angular frequency references V_{ref}, ω_{ref}, and the feedback variables i, i_g, v_t, v_{PCC}. The inner-loop control aims to produce the voltage modulation reference v_{PWM} from v_{ref} and θ generated by the outer-loop control. It is worth noting that the inner-loop control may not be always needed for GFM controls.

III. CURRENT LIMITER

The current limiter is usually embedded in the inner-loop control layer as noted in Fig. 2. Its principle is to restrict the original current reference i_{ref} generated from the voltage vector control or virtual admittance control to a saturated one $\bar{i}_{ref}$ satisfying $\|\bar{i}_{ref}\| \le I_M$. Thereafter, current controllers are utilized to realize $i = \bar{i}_{ref}$, and thus achieves $I \le I_M$.

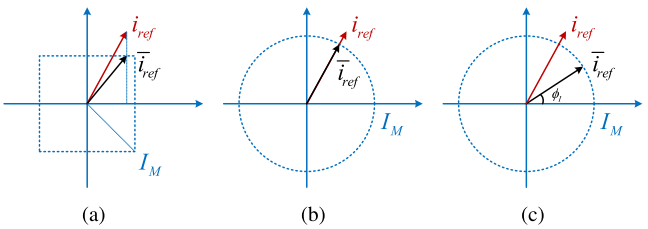

FIGURE 3. Illustration of different current limiters: (a) instantaneous limiter; (b) magnitude limiter; (c) priority-based limiter.

Based on how the saturated current reference $\bar{i}_{ref}$ is calculated, three current limiters are commonly utilized for GFM inverters, including the instantaneous limiter [17], [27], [35], [36], the magnitude limiter [28], [37], [38], [39], [40], and the priority-based limiter [15], [29], [41], [42].

A. INSTANTANEOUS LIMITER

The illustration of an instantaneous limiter is shown in Fig. 3(a), which utilizes an element-wise saturation function to achieve a saturated current reference $\bar{i}_{ref}$.

The instantaneous limiter can be implemented in different reference frames [17], [27], [35], [36], expressed as

$$\bar{i}_{ref,\mathrm{x}} = \begin{cases} I_{M,\mathrm{x}}\,\mathrm{sign}(i_{ref,\mathrm{x}}), & |i_{ref,\mathrm{x}}| > I_{M,\mathrm{x}} \\ i_{ref,\mathrm{x}}, & |i_{ref,\mathrm{x}}| \le I_{M,\mathrm{x}} \end{cases} \tag{2}$$

where x = a, b, c/d, q/α, β denotes the axis in the corresponding reference frame. In the natural reference frame (*abc*-frame), the current limit $I_{M,\mathrm{x}}$ is equal to I_M. In the stationary ($\alpha\beta$-frame) or synchronous (*dq*-frame) reference frame, the current limit $I_{M,\mathrm{x}}$ is usually selected as $I_M/\sqrt{2}$ to ensure that $\sqrt{\bar{i}^2_{ref,\mathrm{d}/\alpha} + \bar{i}^2_{ref,\mathrm{q}/\beta}} \le I_M$.

B. MAGNITUDE LIMITER

The illustration of a magnitude limiter is given in Fig. 3(b), which only decreases the magnitude of the original current reference i_{ref}. The angle of $\bar{i}_{ref}$ maintains the same as that of i_{ref}.

The magnitude limiter is originally designed in the $\alpha\beta$-frame or *dq*-frame [28], [37], [38] and further extended to a generalized one in the *abc*-frame [39], [40], which can be expressed as

$$\bar{i}_{ref,\mathrm{x}} = \begin{cases} i_{ref,\mathrm{x}}, & I_{ref,\mathrm{x}} \le I_M \\ \frac{I_M}{I_{ref,\mathrm{x}}} i_{ref,\mathrm{x}}, & I_{ref,\mathrm{x}} > I_M \end{cases} \tag{3}$$

with $I_{ref,\mathrm{x}}$ representing the magnitude of $i_{ref,\mathrm{x}}$, and x = a, b, c/d, q/α, β.

C. PRIORITY-BASED LIMITER

Fig. 3(c) shows the principle of the priority-based limiter, which not only decreases the magnitude of i_{ref} but also prioritizes its angle to a specific value ϕ_I. Notice that ϕ_I is a user-defined angle that represents the angle difference between $\bar{i}_{ref}$ and the d-axis oriented to θ.

The priority-based limiter implemented in the *dq*-frame is represented as [15], [29], [41], [42]

$$\bar{i}_{ref} = \begin{cases} i_{ref}, & \|i_{ref}\| \le I_M \\ I_M \mathrm{e}^{\mathrm{j}\phi_I}, & \|i_{ref}\| > I_M \end{cases}. \tag{4}$$

In [29], [41], $\phi_I = 0$ is selected. Further, $-\pi/2 < \phi_I \le 0$ is chosen in [42] based on an optimized method with improved transient stability. In [43], [44], ϕ_I is selected to be as close as possible to the pre-fault angle of i to mitigate current transients upon the disturbance inception.

D. PERFORMANCE COMPARISONS OF CURRENT LIMITERS

All these three current limiters can achieve satisfactory current magnitude limitation under severe disturbances. However, they can suffer from transient overcurrent caused by the current control loop dynamics. Among the three current limiters, the instantaneous limiter is the simplest one to achieve the overcurrent protection of GFM inverters. However, when it is implemented in the *abc*-frame and $\alpha\beta$-frame, the inverter output current i can become non-sinusoidal due to the clipping of the current reference [39]. Furthermore, as shown in (2), in the $\alpha\beta$-frame and *dq*-frame, conservative current limits may be needed, which can reduce the capacity utilization of the GFM inverter and requires the use of inverters with a relatively large I_M, e.g., 2 p.u. in [27], [36]. Compared with the instantaneous limiter, the magnitude limiter and the priority-based one can ensure a sinusoidal output current i with extra current magnitude calculations, and fully utilize the overcurrent capability of the inverter during severe symmetrical disturbances.

In addition to the current magnitude limitation, these current limiters generally have difficulties in meeting the fault current contribution objective required by grid codes. When the current limiter is triggered, the inverter terminal voltage may not be aligned with the d-axis oriented to θ. Consequently, the angle difference between i and v_t cannot be specified to meet the fault current contribution requirement [7], [13]. To deal with this issue, one method is to switch the GFM inverter to a phase-locked loop (PLL-)synchronized GFL inverter [15], [37], [45]. However, the PLL can suffer from small-signal or transient instability issues under weak grid conditions [46], [47]. An alternative solution that avoids switching the synchronization methods is to adjust the active and reactive power references based on grid codes [16], [48], [49], which are further tracked by power control loops to achieve the fault current contribution goal [50]. An example based on [7] is given as

$$Q_{ref} = \begin{cases} V_t I_Q, & 0.5\ \text{p.u.} < V_{PCC} < 0.9\ \text{p.u.} \\ V_t I_M, & 0 \le V_{PCC} \le 0.5\ \text{p.u.} \end{cases}, \tag{5}$$

and $P_{ref} \le \sqrt{V_t^2 I_M^2 - Q_{ref}^2}$, where $V_{PCC} = \|v_{PCC}\|$, I_Q denotes the reactive current requirement of the power grid when the PCC voltage is between 0.5 p.u. and 0.9 p.u.

Furthermore, as shown in Fig. 2, once these current limiters are triggered, the inverter phase current magnitude will be fixed at I_M. Therefore, the voltage vector controller and the voltage magnitude controller cannot adjust the inverter terminal voltage magnitude V_t to its reference value [11]. The windup of these voltage controllers may further result in a current reference i_{ref} whose magnitude is larger than I_M. Consequently, undesired current saturation occurs, which prevents the inverter from successful fault recovery [19]. Extra anti-windup designs are required for these voltage controllers to address this issue when current limiters are utilized.

E. CASE STUDY

Simulation tests of the magnitude limiter and the priority-based limiter with $\phi_I = 0$ are conducted to demonstrate their performance during severe symmetrical disturbances. The control structures in [19], [51] are utilized. During the disturbances, the power references are adjusted according to (5). The system and control parameters are given in Appendix. To test the fault current contribution performance of the current limiters, a 0.8 p.u. grid voltage drop is utilized. Further, a -60° grid voltage phase jump, i.e., the angle difference between the internal voltage source of the GFM inverter and the grid voltage increases by 60°, is simulated to test the disturbance ride-through capability of these current limiters.

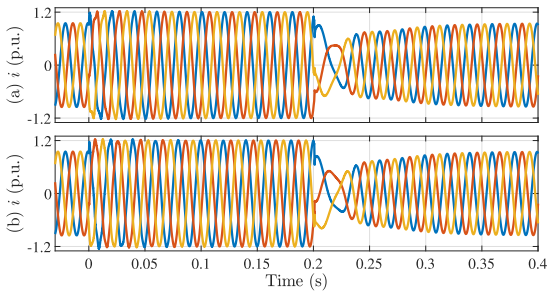

FIGURE 4. Inverter phase current when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s: (a) magnitude limiter; (b) priority-based limiter ($\phi_I = 0$).

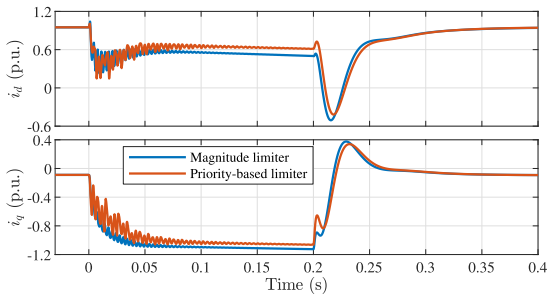

FIGURE 5. Fault current contribution with the current limiters when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s.

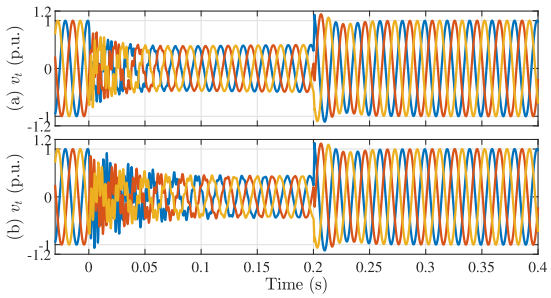

FIGURE 6. Inverter terminal voltage when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s: (a) magnitude limiter; (b) priority-based limiter ($\phi_I = 0$).

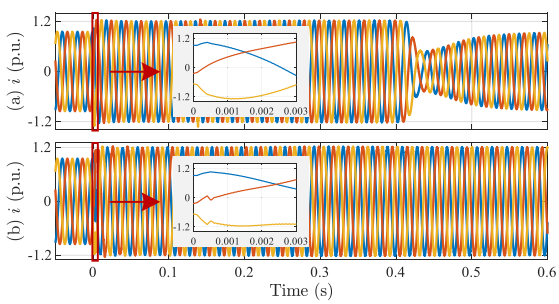

FIGURE 7. Inverter phase current when the grid voltage phase angle jumps by -60° at 0 s: (a) magnitude limiter; (b) priority-based limiter ($\phi_I = 0$).

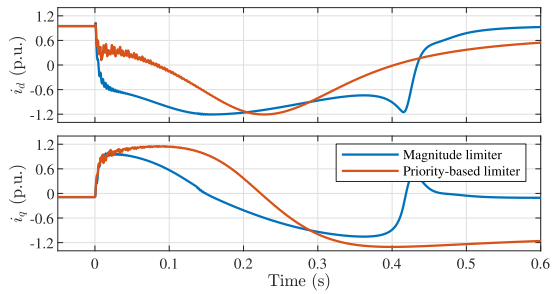

FIGURE 8. Fault current contribution with the current limiters when the grid voltage phase angle jumps by -60° at 0 s.

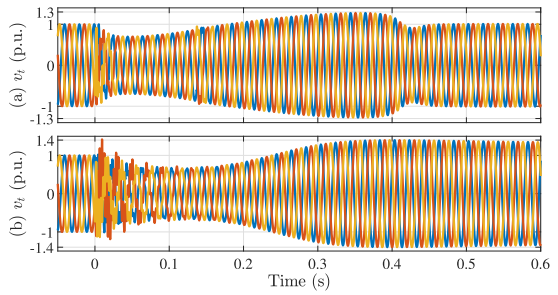

FIGURE 9. Inverter terminal voltage when the grid voltage phase angle jumps by -60° at 0 s: (a) magnitude limiter; (b) priority-based limiter ($\phi_I = 0$).

1) GRID VOLTAGE DROPS TO 0.2 P.U. FOR 200 MS

In Figs. 4–6, the performance of the two current limiters under the grid voltage drop disturbance is given. From Fig. 4, one can notice that both current limiters can restrict the inverter phase currents to 1.2 p.u. The active and reactive current responses are depicted in Fig. 5. One can see that the supplied reactive current amount (i_q) can meet the grid code requirement [7]. However, since the angle difference between i and v_t is regulated by the power control loop whose bandwidth is typically below 50 Hz [52], the inverter has difficulty in meeting the fault current response speed required by grid codes [7]. The inverter terminal voltage responses are shown in Fig. 6. When the grid voltage drop is cleared, transient overvoltage around 1.2 p.u. occurs since the inverter still injects a large amount of reactive current to the grid that lifts up the terminal voltage [53].

2) GRID VOLTAGE PHASE ANGLE JUMPS BY -60°

The results after the grid voltage phase angle jumps are shown in Figs. 7–9. As depicted in Fig. 7, both current limiters can quickly restrict the inverter phase current magnitude to 1.2 p.u. When the magnitude limiter is utilized, a temporary overcurrent with a peak value of 1.3 p.u. for about 1 ms occurs due to the severe phase jump disturbance and the current control loop dynamics. When the disturbance is cleared, unlike the magnitude limiter that can restore normal operation automatically, the priority-based limiter cannot successfully ride through the phase jump disturbance due to the windup

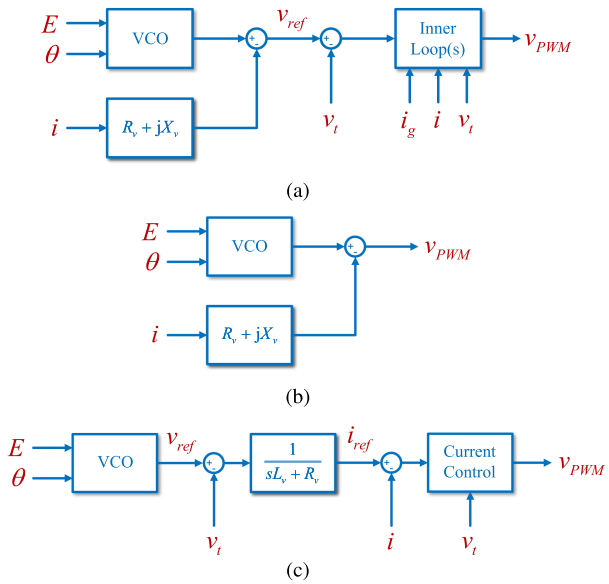

FIGURE 10. Comparisons of different virtual impedance control methods: (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control; (c) virtual admittance. VCO: voltage-controlled oscillator.

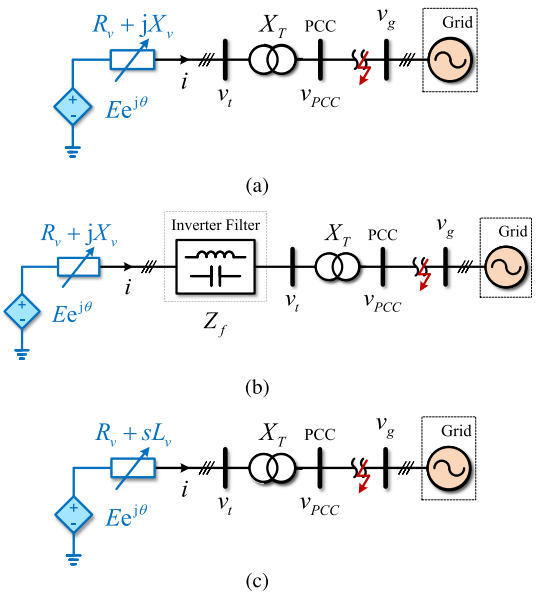

FIGURE 11. Equivalent circuit diagram of different virtual impedance control methods: (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control; (c) virtual admittance.

of the voltage controller, though it ensures transient stability. The phase current magnitude is always kept at 1.2 p.u. since $\|i_{ref}\| > I_M$. Moreover, according to the active current responses in Fig. 8, the GFM inverter with both current limiters needs to absorb active power from the power grid for more than 0.3 s, which is not permitted for certain GFM inverters, e.g., the Type-IV wind turbines. Additionally, the inverter will inject a large amount of reactive current during the fault recovery process, the inverter terminal voltage can be lifted up to 1.4 p.u. as shown in Fig. 9, which can trip the inverter.

IV. VIRTUAL IMPEDANCE

The virtual impedance methods aim to increase the impedance $\|Z_e + jX_T\|$ to limit the phase current magnitude as shown in Fig. 1. Three typical virtual impedance implementation methods are demonstrated in Fig. 10. The corresponding equivalent circuit diagrams of these methods are given in Fig. 11.

A. VIRTUAL IMPEDANCE WITH INNER-LOOP CONTROL

The virtual impedance with inner-loop control is implemented in [18], [30], [31], [54], [55], [56], [57] for current limitation based on the assumption that $v_t = v_{ref}$ can be fast realized by the voltage control loop. An equivalent circuit diagram of this method is demonstrated in Fig. 11(a).

In this method, the virtual impedance is added to v_{ref} when the phase current magnitude I is greater than a certain threshold I_{thres}, i.e.,

$$\begin{cases} R_v = X_v = 0, & I \le I_{thres} \\ \|R_v + jX_v\| > 0, & I > I_{thres} \end{cases} \tag{6}$$

with R_v and X_v being the virtual resistance and reactance, respectively. A typically selection method for R_v and X_v is expressed as follows [18], [31], [54], [55]

$$X_v = \sigma R_v, R_v = \begin{cases} 0, & I \le I_{thres} \\ K_{VI}(I - I_{thres}), & I > I_{thres} \end{cases} \tag{7}$$

where σ is a user-defined X/R ratio for the virtual impedance, K_{VI} is a constant that satisfies

$$\|R_v + jX_v\| = K_{VI}\sqrt{\sigma^2 + 1}(I_M - I_{thres}) \ge \frac{V_{\max}}{I_M} \tag{8}$$

with $V_{\max}$ being the expected maximum magnitude of the voltage difference between $Ee^{j\theta}$ and v_t.

B. VIRTUAL IMPEDANCE WITHOUT INNER-LOOP CONTROL

The virtual impedance without inner-loop control is presented in [32], [58], whose equivalent circuit diagram is demonstrated in Fig. 11(b).

Notice that in this method, the virtual impedance is directly added to the voltage modulation reference v_{PWM} when the phase current magnitude I is greater than I_{thres}.

Different from the previous method, the inverter filter will be in series with the virtual impedance as shown in Fig. 11(b) [24], [59]. Again, R_v and X_v can be selected similarly to (8) [58], satisfying

$$\|R_v + jX_v + Z_f\| \ge \frac{V_{\max}}{I_M}, \quad I = I_M. \tag{9}$$

C. VIRTUAL ADMITTANCE

The virtual admittance control method shown in Fig. 10 is applied in [60], [61] for current limitation. The corresponding equivalent circuit diagram is given in Fig. 11.

Compared with the aforementioned two virtual impedance methods that require a derivative controller to achieve a virtual

inductor L_v [32] or uses an virtual reactor X_v at the nominal frequency, the virtual admittance method can achieve a virtual inductor L_v within the bandwidth of the current control loop.

The virtual admittance method cannot have $R_v = L_v = 0$ in normal operation, whose selection may not follow (8) directly. Alternatively, the virtual admittance can be selected as [60], [61]

$$\begin{aligned} R_v &= \max\{R_{vn}, Z_v/\sqrt{\sigma^2+1}\} \\ L_v &= \max\{L_{vn}, \sigma R_v/\omega_n\} \end{aligned} \tag{10}$$

where $Z_v = \|E\mathrm{e}^{\mathrm{j}\theta} - v_t\|/I_M$, R_{vn} and L_{vn} are the virtual admittance parameters in normal operation, ω_n is the nominal angular frequency. In [16], the virtual admittance parameters are suggested to be chosen as $R_{vn} = 0.1$ p.u. and $L_{vn} = 0.3$ p.u.

D. PERFORMANCE COMPARISONS OF VIRTUAL IMPEDANCE CONTROL METHODS

The virtual impedance method that directly modifies the voltage modulation reference and the virtual admittance method with a fast-tracking current control loop can achieve good current limitation performance when severe disturbances occur [23]. In comparison, the virtual impedance method with inner-loop control achieves current limitation based on the hypothesis that the voltage reference v_{ref} can be fast tracked by the voltage control loop. Since the bandwidth of the voltage control loop is relatively low [62], temporary overcurrent may be observed [63]. To deal with this issue, hybrid current-limiting methods that combine the virtual impedance with the priority-based current limiter [63] and the current magnitude limiter [64] are presented.

To achieve effective current magnitude limitation with the three virtual impedance methods, the control parameters R_v and X_v (L_v) are highly dependent on the magnitude of the voltage difference between $E\mathrm{e}^{\mathrm{j}\theta}$ and v_t, which introduces a tradeoff between current limitation and stability [18], [20], [21], [22]. For the parameter selection method expressed by (8), current limitation can be achieved if the condition $V_{\max} \geq \|E\mathrm{e}^{\mathrm{j}\theta} - v_t\|$ holds. On one hand, when using a small $V_{\max}$, the phase current magnitude I cannot be ensured to be within I_M when $\|E\mathrm{e}^{\mathrm{j}\theta} - v_t\|$ is larger than $V_{\max}$. On the other hand, when using a large $V_{\max}$, according to (8), large R_v and X_v will be applied, which can induce instability issues. The instability problem also exists in the parameter selection method in (10), which requires large R_v and L_v when $\|E\mathrm{e}^{\mathrm{j}\theta} - v_t\|$ increases.

As shown in Fig. 11, the inverter under disturbances behaves as a voltage source behind adaptive impedance. The output current vector angle will be determined by the voltage difference ($E\mathrm{e}^{\mathrm{j}\theta} - v_t$) and the X/R ratio of the virtual impedance if only the virtual impedance methods are used. To meet the fault current contribution requirement, a proper design of the X/R ratio is thus needed. An alternative solution that can relax this parameter selection requirement is to combine the virtual impedance methods with the power reference adjustment method in (5) [23]. However, the voltage source behavior of the inverter can be lost.

Besides, from Figs. 2 and 10, it is noticed that these virtual impedance methods will not introduce windup problems to the inner-loop current and voltage controllers, whose fault recovery capability is thus better than that of the current limiters [65], [66]. However, anti-windup control designs are still required for the outer-loop voltage magnitude controller to ensure the fault recovery capability of the GFM inverter.

TABLE 2. Virtual Impedance Parameters

I_{thres}	σ (X/R ratio)	K_{VI}
1 p.u.	5.0	0.8172
1 p.u.	0.2	4.0858

E. CASE STUDY

Simulation tests of the virtual impedance with inner-loop control [65] and without inner-loop control [20] are conducted. Again, the system and control parameters in Appendix are used. The virtual impedance parameters calculated according to (8) with $V_{\max} = 1$ p.u. are listed in Table 2. Two disturbances including a 0.8 p.u. grid voltage drop and a -60° grid voltage phase jump are simulated.

1) GRID VOLTAGE DROPS TO 0.2 P.U. FOR 100 MS

The results of these two virtual impedance methods with an X/R ratio of 5 are depicted in Figs. 12–14. As shown in Fig. 12, a temporary overcurrent with a peak value of 1.5 p.u. for 3 ms occurs upon the grid voltage drop. When the disturbance is cleared, a temporary overcurrent with a peak value of 1.4 p.u. occurs again. These overcurrent phenomena are mainly induced by the transient dc component in phase currents [23]. Moreover, during the grid voltage drop, the phase current magnitude is less than 1.2 p.u. since $\|E\mathrm{e}^{\mathrm{j}\theta} - v_t\| < V_{\max}$ holds. The GFM inverter with these two virtual impedance methods cannot fully utilize its overcurrent capability. The active and reactive current trajectories are given in Fig. 13. By virtue of the maintained internal voltage source behavior, the inverter can supply 1 p.u. reactive current within about 6 ms after the grid voltage drops with an appropriate selected X/R ratio. However, both virtual impedance methods require more than 2 s to exit the current-limiting mode. Finally, the terminal voltage profiles are given in Fig. 14, one can notice that a slight overvoltage with a peak value of 1.06 p.u. occurs. Afterward, the terminal voltage can be kept with in 1 p.u.

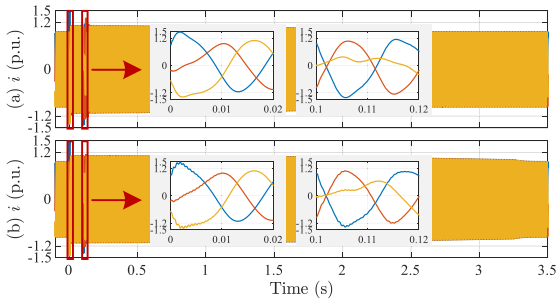

FIGURE 12. Inverter phase current when the grid voltage drops to 0.2 p.u. from 0 s to 0.1 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

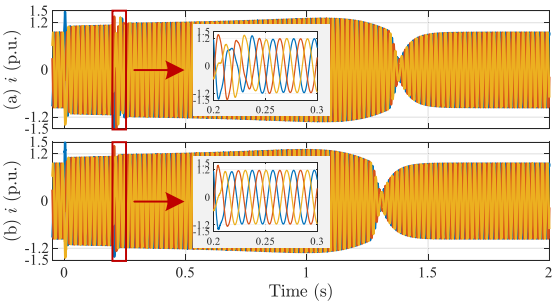

FIGURE 15. Inverter phase current when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

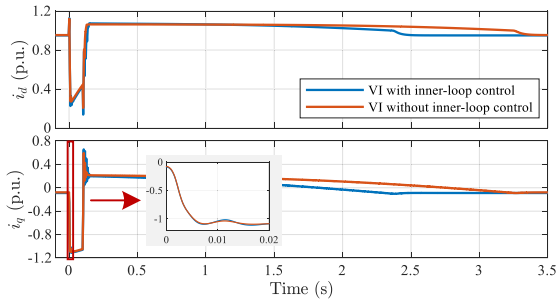

FIGURE 13. Fault current contribution with the virtual impedance when the grid voltage drops to 0.2 p.u. from 0 s to 0.1 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$).

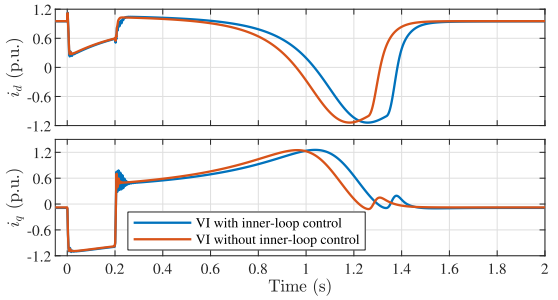

FIGURE 16. Fault current contribution with the virtual impedance when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$).

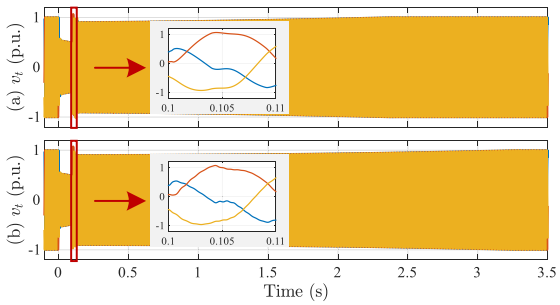

FIGURE 14. Inverter terminal voltage when the grid voltage drops to 0.2 p.u. from 0 s to 0.1 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

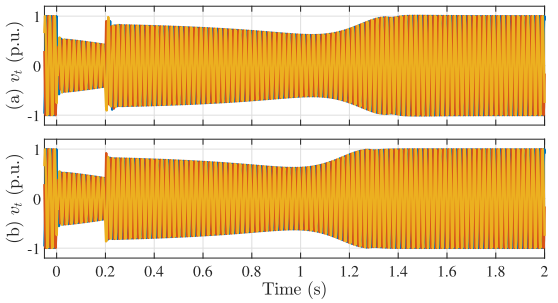

FIGURE 17. Inverter terminal voltage when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

2) GRID VOLTAGE DROPS TO 0.2 P.U. FOR 200 MS

The results with an X/R ratio of 5 are depicted in Figs. 15–17. As demonstrated in Fig. 15, a temporary overcurrent with a peak value of 1.5 p.u. occurs when the grid voltage drops and the disturbance is cleared. During the fault recovery process, the current magnitude limitation is compromised again since the required condition for the virtual impedance methods, i.e., $\|Ee^{j\theta} - v_t\| \leq V_{\max}$, is violated. The corresponding active and reactive current trajectories are depicted in Fig. 16. One can notice that the inverter needs about 1.2 s to recover from the disturbance and has to withstand negative active power from the power grid for more than 0.3 s. The terminal voltage trajectories are given in Fig. 17. It can be seen that the inverter terminal voltage can be well maintained within 1 p.u. during the low-voltage ride-though process.

Next, the results with a decreased X/R ratio to 0.2 are given in Figs. 18–20. One can notice that the virtual impedance with inner-loop control becomes unstable when grid voltage drops. Comparing Fig. 15(b) with Fig. 18(b), one can notice that the temporary overcurrent upon the grid voltage drops decreases to 1.3 p.u. due to the increased virtual resistance to damp the dc component in phase currents. However, temporary overcurrent still occurs during the fault recovery process since $\|Ee^{j\theta} - v_t\| > V_{\max}$. In Fig. 19, the active and reactive

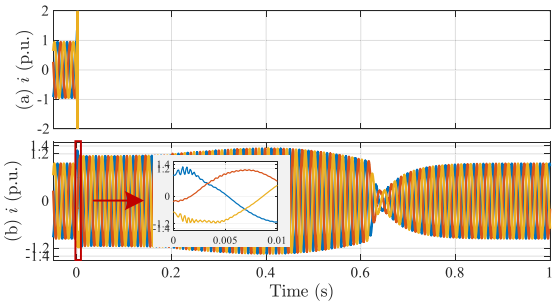

FIGURE 18. Inverter phase current when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 0.2 ($\sigma = 0.2$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

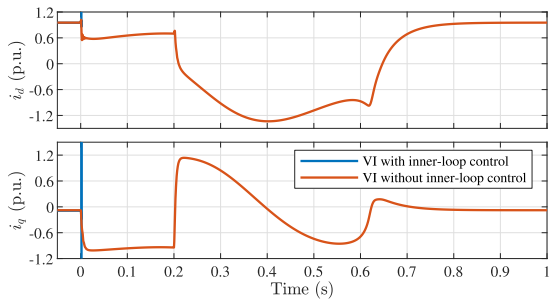

FIGURE 19. Fault current contribution with the virtual impedance when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 0.2 ($\sigma = 0.2$).

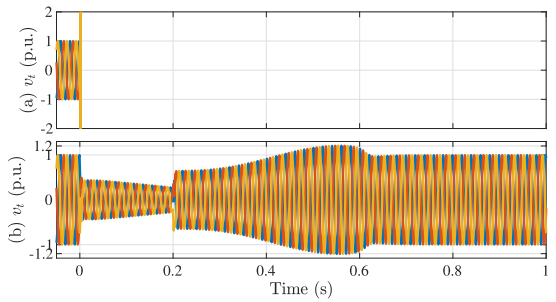

FIGURE 20. Inverter terminal voltage when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s. The virtual impedance X/R ratio is 0.2 ($\sigma = 0.2$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

current trajectories of the two virtual impedance methods are given. During the voltage drop disturbance, one can notice the inverter can again deliver reactive current to the power grid quickly with the help of the internal voltage source behavior. However, its peak value is reduced due to the decreased X/R ratio. Moreover, the inverter needs about 0.5 s to restore its normal operation. From Fig. 20, one can notice that a transient overvoltage of 1.2 p.u. happens due to the undesired reactive current contribution when the voltage drop is cleared.

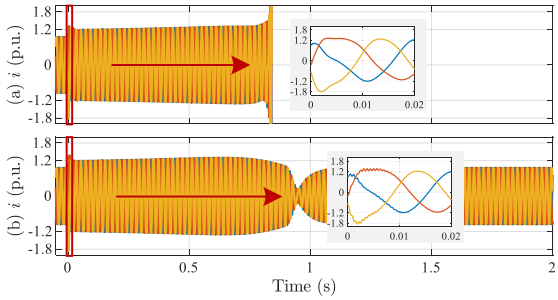

FIGURE 21. Inverter phase current when the grid voltage phase angle jumps by $-60°$ at 0 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

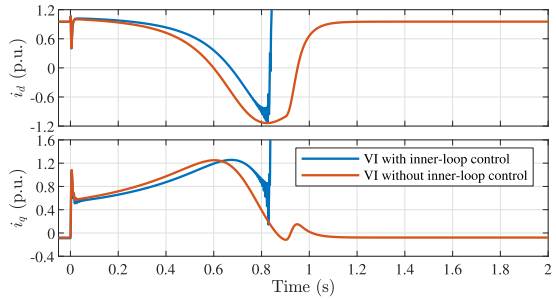

FIGURE 22. Fault current contribution with the virtual impedance when the grid voltage phase angle jumps by $-60°$ at 0 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$).

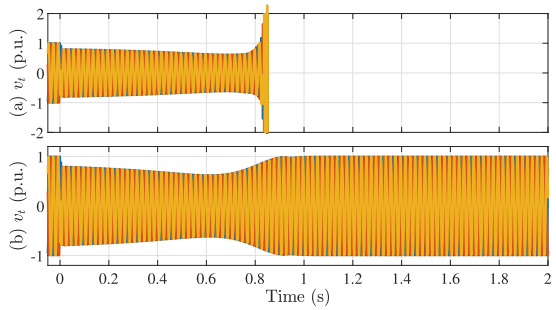

FIGURE 23. Inverter terminal voltage when the grid voltage phase angle jumps by $-60°$ at 0 s. The virtual impedance X/R ratio is 5 ($\sigma = 5$): (a) virtual impedance with inner-loop control; (b) virtual impedance without inner-loop control.

3) GRID VOLTAGE PHASE ANGLE JUMPS BY $-60°$

The results when a large grid voltage phase angle jump occurs are shown in Figs. 21–23. The X/R ratio for the virtual impedance is selected as 5. Again, the virtual impedance with inner-loop control becomes unstable during the disturbance ride-through process. As demonstrated in Fig. 21, one can notice that a large transient overcurrent with its peak value of 1.8 p.u. happens upon the phase angle jumps. Besides, since $\|Ee^{j\theta} - v_t\| \leq V_{\max}$ is violated again, the current limitation objective is jeopardized. As shown in Fig. 22, the GFM inverter requires a period of about 1 s to recover from the large

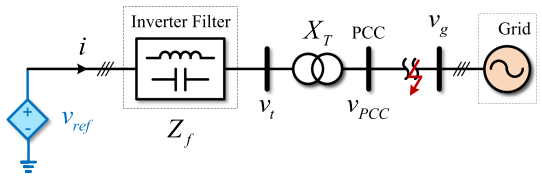

FIGURE 24. Equivalent circuit diagram of voltage limiters with v_{ref} being a saturated voltage reference.

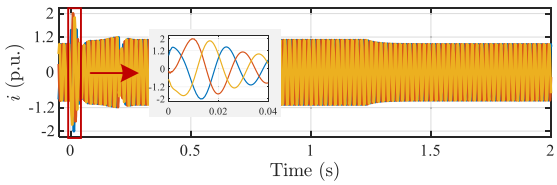

FIGURE 25. Inverter phase current with the voltage limiter when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s.

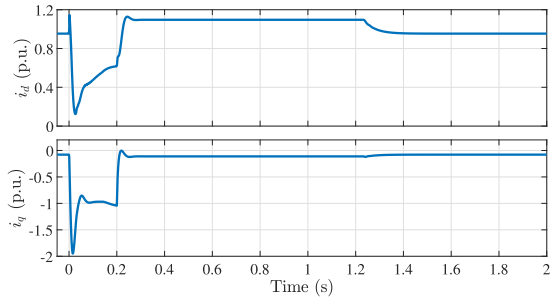

FIGURE 26. Fault current contribution with the voltage limiter when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s.

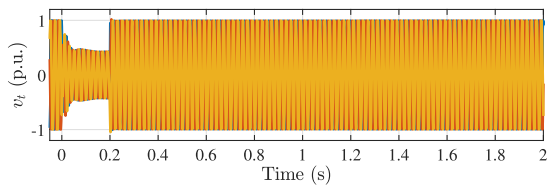

FIGURE 27. Inverter terminal voltage with the voltage limiter when the grid voltage drops to 0.2 p.u. from 0 s to 0.2 s.

phase jump, while the terminal voltage can be maintained with in 1 p.u. as illustrated in Fig. 23.

V. VOLTAGE LIMITER

Voltage limiters aim to directly reduce the voltage difference $\|v_{PWM} - v_t\|$ to be smaller than $\|Z_f\|I_M$ [33], [34], [67], [68], which modifies the voltage reference generated by the outer-loop control to realize current magnitude limitation as shown in Fig. 2. This method is a suggested solution in [7] since it does not require adaptive virtual impedance that can destabilize the system under certain conditions [20]. For the voltage limiters, the inner-control loop is commonly transparent, i.e., $v_{PWM} = v_{ref}$. Subsequently, an equivalent circuit diagram of this current-limiting method can be expressed as in Fig. 24.

The implementation of the voltage limiter is usually achieved by regulating E and θ generated by the outer-loop control, expressed as [33], [34]

$$\|v_{ref}\| = \begin{cases} V_t + E_{\lim}, & E > V_t + E_{\lim} \\ E, & V_t - E_{\lim} \le E \le V_t + E_{\lim} \\ V_t - E_{\lim}, & E < V_t - E_{\lim} \end{cases}, \quad (11)$$

and

$$\arg(v_{ref}) = \begin{cases} \theta_t + \delta_{\lim}, & \theta > \theta_t + \delta_{\lim} \\ \theta, & \theta_t - \delta_{\lim} \le \theta \le \theta_t + \delta_{\lim} \\ \theta_t - \delta_{\lim}, & \theta < \theta_t - \delta_{\lim} \end{cases} \quad (12)$$

where θ_t is the phase angle of v_t, $E_{\lim}$ and $\delta_{\lim}$ are maximum allowed magnitude difference and angle difference, respectively, which are selected to ensure that $\|v_{ref} - v_t\| \le \|Z_f\|I_M$. Notice that this type of voltage limiter can be implemented without the magnitude and angle information of i as the other current-limiting methods. However, it requires extra information of the terminal voltage v_t, such as its phase angle θ_t [33] and magnitude V_t [34].

In [67], [68], a voltage limiter is directly designed in the *abc*-frame where the voltage limits are calculated based on each phase current. This type of voltage limiter is simple in implementation, yet introduces non-sinusoidal phase currents like the instantaneous current limiter.

Besides, to ensure the fault recovery capability, appropriate anti-windup designs for outer-loop controllers are required due to the saturation of the control signals E and θ. When both E and θ are saturated as in (11)–(12), the voltage reference v_{ref} has to follow the change of its terminal voltage v_t. The output current will become $i = [(V_t \pm E_{\lim})e^{j(\theta_t \pm \delta_{\lim})} - V_t e^{j\theta_t}]/Z_f$. Appropriate design of control parameters $E_{\lim}$ and $\delta_{\lim}$ is needed to meet the fault current contribution requirement.

A. CASE STUDY

Simulation tests of the voltage limiter in (11) and (12) are performed. The system and control parameters in Appendix are used. The parameters for the voltage limiter are $\delta_{\lim} = 0.05$ rad/s and $V_{\lim} = 0.033$ p.u. Two disturbances including a 0.8 p.u. grid voltage drop and a -60° grid voltage phase jump are simulated.

1) GRID VOLTAGE DROPS TO 0.2 P.U. FOR 200 MS

The corresponding results with the voltage limiter when grid voltage drops are shown in Fig. 25–27. From Fig. 25, one can notice that a temporary overcurrent with a peak value of 2 p.u. for 20 ms occurs due to the lack of active/passive damping. Afterward, the phase current magnitude can be well maintained within 1.2 p.u. From Fig. 26, one can notice that with the help of the partially maintained voltage source behavior, the inverter can supply reactive current required by grid code quickly upon the voltage drop. However, the inverter needs more than 1 s to restore its normal operation. The inverter terminal voltage during the low-voltage ride-through process

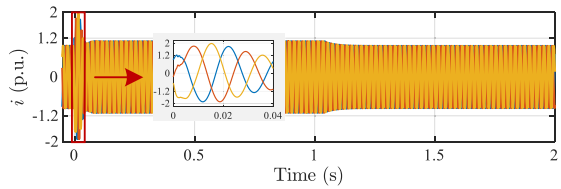

FIGURE 28. Inverter phase current with the voltage limiter when the grid voltage phase angle jumps by −60° at 0 s.

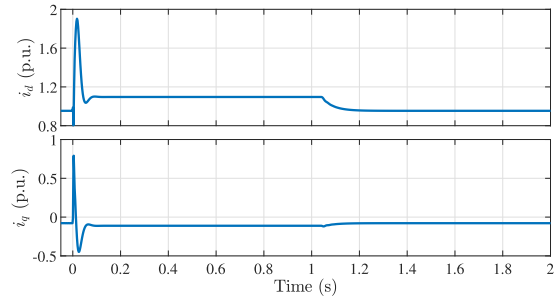

FIGURE 29. Fault current contribution with the voltage limiter when the grid voltage phase angle jumps by −60° at 0 s.

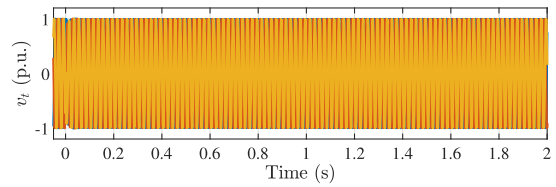

FIGURE 30. Inverter terminal voltage with the voltage limiter when the grid voltage phase angle jumps by −60° at 0 s.

can be well maintained within its allowed operating range as shown in Fig. 27.

2) GRID VOLTAGE PHASE ANGLE JUMPS BY −60°

The performance of the voltage limiter when the grid voltage phase angle jumps by −60° is depicted in Figs. 28–30. Again, from Fig. 28, due to the lack of damping, a large temporary overcurrent of 2 p.u. happens upon the disturbance inception. Further, as shown in Fig. 29, the inverter maintains its current-limiting mode for more than 1 s after the phase jump. Finally, again, the inverter terminal voltage during the disturbance ride-through process can be well maintained within 1 p.u. as shown in Fig. 30.

For comparison, the simulation results of all case studies are summarized in Table 3.

VI. OPEN ISSUES

A. TRANSIENT STABILITY ASSESSMENT

System stability is an essential requirement for both GFM inverter protection and successful disturbance ride-through.

Given certain disturbances, numerical methods are widely applied to testify the stability of a single GFM inverter with current limiters [27], [28], [45], power limiters [69], [70], virtual impedance/admittance [31], [61], and hybrid methods [16], [48]. Furthermore, the stability of multiple GFM inverters with different current-limiting methods are illustrated by the numerical methods in [29], [33], [36], [37], [38], [39], [56], [57], [58], [71], [72], [73].

Although all details of the inverter nonlinear dynamics can be included in the numerical methods for stability assessment, significant computational resources will be required for the stability analysis of a power grid with high penetration of GFM inverters. Moreover, the numerical simulations fail to shed analytical insights into the impacts of control loops.

Besides the numerical method, nonlinear system theory is also used to analyze the stability of GFM inverters, such as bifurcation theory [74], Lyapunov theory [75], phase plane analysis [23], [42], [76], [77], [78], [79], etc. The advantage of these theoretical methods is that they can guide the selection of control parameters [42]. However, these results are hard to extend to the transient stability assessment of multiple GFM inverters under overcurrent conditions.

For a power grid with multiple GFM inverters, due to its complex dynamic model, transient stability is hard to be assessed either theoretically or numerically. One possible way is to develop simplified models for transient stability assessment. In general, a GFM inverter with limited output current can be modeled as a synchronized current source with fixed or state-dependent phase current magnitude or a synchronized voltage source with a nonlinear output impedance. However, the nonlinear impedance in these models introduces time-varying parameters into the electrical network, which may make the conventional transient stability assessment methods based on fixed network model invalid. How to assess the transient stability of multiple GFM inverters with time-varying electrical network parameters is still a challenging issue.

B. VOLTAGE SOURCE BEHAVIOR UNDER OVERCURRENT CONDITIONS

With current-limiting controls, the GFM inverter cannot maintain its normal voltage source behavior under overcurrent conditions. Fortunately, although the GFM inverter's phase current magnitude is limited, its vector angle can still be adjusted freely.

The first method is to precisely regulate the output current vector angle to make the inverter behave as a PLL-synchronized current source [15], [45], [80] or a power-synchronized current source [29], [81]. Such a method can easily achieve the current magnitude limitation and fault current contribution [14] objectives by setting the active and reactive current references according to grid codes under disturbances [16]. However, this method may require extra mode-switching mechanism to restore normal operation when disturbances are cleared since the GFM inverter loses its voltage source behavior during the severe disturbances.

Notice that the voltage source behavior of a GFM inverter is more demanded than the precise control of the output current vector angle. In other words, during severe disturbances, the output current vector angle can be indirectly adjusted through

TABLE 3. Summary of Case Studies Under the System and Control Parameters in Appendix

Method	Voltage drop	Phase jump	Stable	i_q contribution	Recoverable	Temporary overcurrent	Transient overvoltage
Current magnitude limiter	0.2 p.u., 200 ms	/	✓	✓	✓	None	1.2 p.u.
Current magnitude limiter	/	−60°	✓	/	✓	1.3 p.u., 1 ms	1.3 p.u.
Priority-based limiter ($\phi = 0$)	0.2 p.u., 200 ms	/	✓	✓	✓	None	1.2 p.u.
Priority-based limiter ($\phi = 0$)	/	−60°	✓	/	✗	None	1.4 p.u.
VI w/ inner-loop control ($\sigma = 5$)	0.2 p.u., 100 ms	/	✓	✓	✓	1.5 p.u., 3 ms	1.06 p.u.
VI w/ inner-loop control ($\sigma = 5$)	0.2 p.u., 200 ms	/	✓	✓	✓	1.5 p.u., 20 ms	None
VI w/ inner-loop control ($\sigma = 0.2$)	0.2 p.u., 200 ms	/	✗	/	/	/	/
VI w/ inner-loop control ($\sigma = 5$)	/	−60°	✗	/	/	/	/
VI w/o inner-loop control ($\sigma = 5$)	0.2 p.u., 100 ms	/	✓	✓	✓	1.5 p.u., 3 ms	1.06 p.u.
VI w/o inner-loop control ($\sigma = 5$)	0.2 p.u., 200 ms	/	✓	✓	✓	1.5 p.u., 3 ms	None
VI w/o inner-loop control ($\sigma = 0.2$)	0.2 p.u., 200 ms	/	✓	✗	✓	1.3 p.u., 2 ms	1.2 p.u.
VI w/o inner-loop control ($\sigma = 5$)	/	−60°	✓	/	✓	1.8 p.u., 5 ms	None
Voltage limiter	0.2 p.u., 200 ms	/	✓	✓	✓	2 p.u., 20 ms	None
Voltage limiter	/	−60°	✓	/	✓	2 p.u., 25 ms	None

the regulation of an internal voltage source and the equivalent output impedance such as the virtual impedance methods and voltage limiters. Such kinds of methods can improve not only the fault recovery capability of the inverter but also the speed of the output current response. A recently implemented grid code [7] requires the GFM inverters to begin injecting reactive current to the power system in less than 5 ms when the PCC voltage drops below 0.9 p.u. In such a small timescale, it seems to be a better choice to keep the voltage source behavior of GFM inverters to some extent during disturbances with a natural current response than to directly control the output current vector angle of the GFM inverter [11]. However, how to generate the magnitude and phase angle for the voltage source during severe disturbances, which satisfy the current magnitude limitation and fault current contribution requirements with ensured stability, is still an open issue.

C. WINDUP OF VOLTAGE CONTROLLERS

A successful disturbance ride-through process requires that GFM inverters should be able to restore their normal operation from the current-limiting mode when disturbances are cleared [13], [52]. All control loops should be able to resume their status in normal operation automatically.

One main challenge in the fault recovery process is caused by the windup of voltage controllers including the voltage vector controller and the voltage magnitude controller. When disturbances occur, the inverter terminal voltage has to drop to reduce the inverter phase current magnitude [11]. Therefore, these voltage controllers will suffer from the windup issues.

To solve the fault recovery issue induced by voltage controller windup, appropriate anti-windup methods should be designed for GFM inverters. In addition to the commonly used methods, such as back-calculation, clamping, etc., novel anti-windup algorithms for different current-limiting controls may be developed to help GFM inverters recover from the undesired current saturation. For example, in [51], the integrator of the voltage vector controller is set to zero when the current magnitude limiter is triggered to improve the fault recovery capability of the GFM inverter. In [76], [82], the outer-loop controllers are re-designed for priority-based current limiters to avoid the windup of the voltage vector controller. However, the application of these methods are limited to specified inner-loop and outer-loop control structures and system parameters. Once the control structure or system parameter changes, such as adding or removing feedforward terms or changing the grid impedance, those methods may lose their effectiveness. The anti-windup methods for voltage controllers that guarantees the inverter fault recovery capability is still missing in the literature.

VII. CONCLUSION

This paper presents an overview of the existing current-limiting control methods for grid-forming (GFM) inverters under severe symmetrical disturbances, including current limiters, virtual impedance, and voltage limiters. The performance and challenges of these methods in satisfying the current magnitude limitation, fault current contribution, and fault recovery objectives during the disturbance ride-through process are discussed and demonstrated by comparative simulations under grid voltage drops and phase jumps.

Among these methods, the current limiters can meet the fault current contribution requirement by adjusting current or power references but may fail to recover from severe disturbances. In comparison, the virtual impedance methods and

TABLE 4. System Parameters

Quantity	Value
Nominal power	2500 VA (1 p.u.)
Grid phase-to-ground voltage	155.56 V (1 p.u.)
Grid angular frequency	100π rad/s (1 p.u.)
Grid inductance	0.2 p.u.
Transformer inductance	0.1 p.u.
Inverter filter inductance	0.03 p.u.
Inverter filter capacitance	0.07 p.u.
Sampling frequency	10 kHz

TABLE 5. Control Parameters

Quantity	Value
Active power reference P_{ref}	0.95 p.u.
Reactive power reference Q_{ref}	0 p.u.
Voltage reference V_{ref}	1 p.u.
Active power control P gain	0.02 p.u.
Reactive power control P & I gains	0.1 p.u., 15 p.u.
Low-pass filter bandwidth in power control	0.4 p.u.
Voltage vector control P & I gains	1 p.u., 5 p.u.
Vector current control P & I gains	1 p.u., 10 p.u.
Maximum allowed current magnitude I_M	1.2 p.u.

voltage limiters can allow for automatic fault recovery. But their control parameters should be appropriately selected to supply the grid code required fault current. Moreover, temporary overcurrent and transient overvoltage are observed in the simulation results, which need to be suppressed for GFM inverters. Finally, open issues including transient stability assessment, voltage source behavior under overcurrent conditions, and windup of voltage controllers, are shared.

APPENDIX

The system and control parameters utilized in the case studies are listed in Table 4 and Table 5, respectively.

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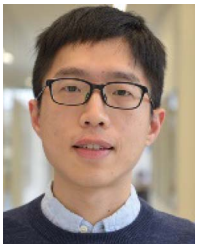
BO FAN (Member, IEEE) received the B.S. degree in automation and the Ph.D. degree in control science and engineering from Zhejiang University, Hangzhou, China, in 2014 and 2019, respectively. From 2018 to 2019, he was a Visiting Pre-doctoral Fellow with Lehigh University, Bethlehem, PA, USA. Since 2020, he has been with the Department of Energy, Aalborg University, Aalborg, Denmark, where he is currently a Postdoctoral Researcher. His research interests include power system stability, power electronics, smart grid, distributed control, and nonlinear systems. Dr. Fan was the recipient of the Best Reviewer Award of IEEE TRANSACTIONS ON SMART GRID in 2019, Outstanding Reviewer Awards of IEEE TRANSACTIONS ON POWER SYSTEMS in 2019 and 2021, Chinese Association of Automation Excellent Doctoral Dissertation Award in 2020, and Marie Skłodowska-Curie Individual Fellowship in 2021.

TENG LIU (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012 and 2019, respectively. Since 2020, he has been a Postdoctoral Researcher with the Department of Energy, Aalborg University, Aalborg, Denmark. His research interests include modeling, control, and stability analysis of grid-connected converters. Dr. Liu was the recipient of the MPCE Excellent Reviewer Award in 2020 and Best Paper Award for IEEE Workshop on Computers in Power Electronics (COMPEL) in 2021.

FANGZHOU ZHAO received the B.S. degree in electrical engineering and automation from the University of Electronic Science and Technology of China, Chengdu, China, in 2014, and the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2019. Since 2020, he has been with the Department of Energy, Aalborg University, Aalborg, Denmark, where he is currently a Postdoctoral Researcher. His research interests include modeling and control of grid-following/grid-forming converters, modular multilevel converters, and grid emulation systems.



HENG WU (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2012 and 2015, respectively, and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2020. From 2015 to 2017, he was an Electrical Engineer with NR Electric Co., Ltd, Nanjing. Since 2017, he has been with the Department of Energy, Aalborg University, where he became a Postdoctoral Researcher in 2020 and an Assistant Professor in 2022. He was a Guest Researcher with Ørsted Wind Power, Fredericia, Denmark, in 2018 and Bundeswehr University Munich, Neubiberg, Germany, in 2019. His research interests include modeling and stability analysis of power-electronic-based power systems. Dr. Wu is the Co-Chair of IEEE Task Force on Frequency-Domain Modeling and Dynamic Analysis of HVDC and FACTS, a Technical Committee Member of European Academy of Wind Energy, Member of GB Grid Forming Best Practice Expert Group formed by National Grid ESO, Warwick, U.K., Member of CIGRE Working Group B4.85 and B4/C4.93, and Steering Committee Member of CIGRE Next Generation Network, Denmark. He was identified as the World Ranking Top 2% Scientist by Stanford University in 2019. He was the recipient of the 2019 Outstanding Reviewer Award of the IEEE TRANSACTIONS ON POWER ELECTRONICS and 2021 Star Reviewer Award of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

XIONGFEI WANG (Fellow, IEEE) received the B.S. degree in electrical engineering from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2008, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013. From 2009 to 2022, he was with Aalborg University, where he became an Assistant Professor in 2014, Associate Professor in 2016, and a Professor and Leader of the Electronic Power Grid (eGRID) Research Group in 2018. Since 2022, he has been a Professor with the Division of Electric Power and Energy Systems, KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include modeling and control of power electronic converters and systems, stability and power quality of power-electronics-dominated power systems, and high-power converters. Dr. Wang is currently the Co-Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS and an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the recipient of the 10 IEEE Prize Paper Awards, 2016 AAU Talent for Future Research Leaders, 2018 Richard M. Bass Outstanding Young Power Electronics Engineer Award, 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, 2020 JESTPE Star Associate Editor Award, and 2022 Isao Takahashi Power Electronics Award. He was elected as an IEEE Fellow for his contributions to power-electronic-based power systems in 2022.