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Design of Low Inductance SiC-MOS/Si-IGBT Hybrid Module for PV Inverters

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ABSTRACT In this paper, design of a low parasitic inductance T-type SiC-MOS/Si-IGBT hybrid module for PV inverters is studied. Current commutation loops and self- and mutual inductances model of the hybrid module are analyzed. Then stacked substrates structures with vertical power commutation loop to reduce parasitic inductance are identified and compared. Finally, a hybrid module with stacked bond wire substrates structure is built and test results are provided to verify the design.

INDEX TERMS Hybrid module, stacked bond wire substrates, parasitic inductance, inverter.

I. INTRODUCTION

Hybrid switch with the combination of Si IGBT device and smaller rating SiC MOSFET device is attractive since it can achieve high performance with lower cost for PV inverters [1], [2], [3], [4], [5]. A PV inverter with the hybrid switch is endowed with characteristics of SiC MOSFET and can operate at higher switching frequency than that of Si IGBT. At the same time, the inverter with the hybrid switch has lower cost than that using only SiC MOSFETs. However, design of hybrid switch is challenging because SiC MOSFET part of the hybrid switch is sensitive to parasitic inductance due to its high dv/dt and di/dt. It requires that the inverter with the hybrid switch has low parasitic inductance. Otherwise, it will cause large switching ringing in the circuit. The inverter designed by the hybrid switch with TO-247 discrete devices has large loop parasitic inductance. The total parasitic inductance of the power loop of T-Type inverter with TO-247 discrete hybrid devices may exceed 40 nH [5]. One solution to reduce parasitic inductance is integrating all dies in one power module. However, packaging both SiC MOSFET and Si IGBT dies into a hybrid module becomes complex due to larger number of dies in the module. There are many studies about package of hybrid module. Single hybrid switch module [6], [7], [8], half bridge hybrid switch module [9], [10] and three phase half bridge hybrid switch module [11] are made with dies, which reduces power loop inductance to about 8.6 nH [9] and 12.38 nH [10].

Stacked packaging can reduce power module's parasitic inductance by changing power loop from lateral structure to vertical structure. It adopts different structures to reduce the parasitic inductance. GaN die is soldered on 4 layer or 6 layer PCB structure in a synchronous buck converter with power loop inductance around 0.4 nH [12], 0.1 nH [13] and 0.2 nH [14]. For SiC half bridge module, dies are soldered on the lower layer by using "4 layer PCB (upper layer) + Cu/Al_2O_3 or AlN/Cu DBC (lower layer)" structure with power loop inductance 3.6 nH [15] and 3.38 nH [16]. Further, to overcome the current limitation of PCB, dies are soldered on the lower layer by using "DBC/Solder/DBC" stacked structure with power loop inductance 6 nH [17] and 1.8 nH [18]. Similarly, "DBC/Solder/DBC/Solder/DBC" stacked structure are used with power loop inductance 11 nH [19]. Dies can also be soldered on the up layer by using Cu/Si_3N_4/Cu/Si_3N_4/Cu AMB structure with power loop inductance 5 nH [20], [21] and 1.15 nH [22].

Predecessors have discussed busbar design of the T-type inverter with 12.7 nH lowest parasitic inductance [23] and 21.8 nH lowest parasitic inductance [24]. The paper [25] studies the module design of a 1200 V/100 A T-type module with 19.9 nH lowest parasitic inductance. Power semiconductor device manufacturers such as Infineon and Semikron have made efforts to customize the design of a T-type module with parasitic inductance 14 nH [26], 25 nH [27], 29 nH [28] and 31 nH [29]. However, how to design low parasitic inductance

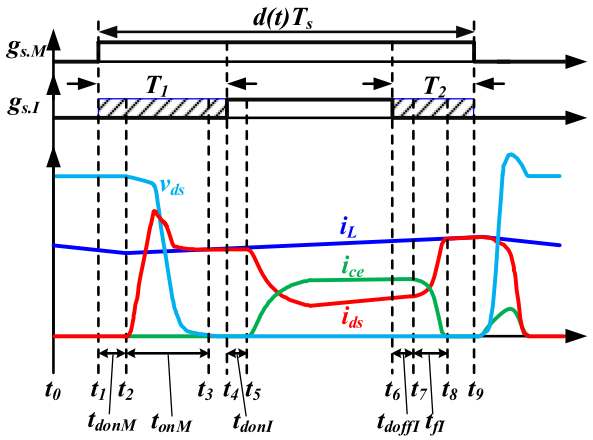

FIGURE 1. Gate drive mode PWM1 and corresponding switching waveforms.

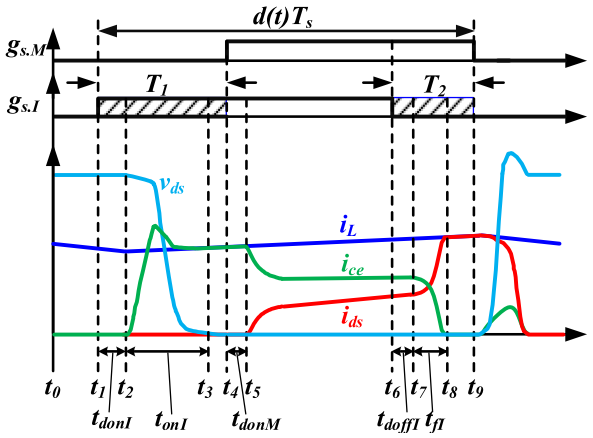

FIGURE 2. Gate drive mode PWM6 and corresponding switching waveforms.

T-type hybrid module with hybrid switch still needs to be explored.

In this paper, the current commutation loops (CCLs) and self- and mutual inductances model of the T-type hybrid module are investigated in Section II. Different stacked substrates structures are compared in Section III. Then different metalized ceramic substrate technologies and various ceramic materials for stacked substrates are reviewed in Section III. Two possible power loop layout designs for T-type hybrid module with low parasitic inductance are compared in Section IV. Finally, a hybrid module prototype with stacked bond wire substrates structure using Si_3N_4 AMB substrates is made and test results are provided to verify the design in Section V. Section VI concludes the paper.

II. COMMUTATION LOOPS AND PARASITIC INDUCTANCES MODEL OF INVERTERS WITH HYBRID MODULE

A. GATE DRIVE MODE FOR HYBRID SWITCH

Since the hybrid switch has two PWM drive signals, this increases the degree of freedom for the PWM gate drive mode for hybrid switch. According to the polarity of the delay time, the gate drive mode can be divided into several patterns, such as PWM1 shown in Fig. 1, PWM6 shown in Fig. 2 and so on [2].

Take PWM1 as an example, at t_1, the turn-on drive signal of SiC MOSFET is applied. After the turn-on delay time t_{donM} of SiC MOSFET, SiC MOSFET is turned on at t_2. After the turn-on time t_{onM} of SiC MOSFET, SiC MOSFET is fully turned on at t_3. At t_4, the turn-on drive signal of Si IGBT is applied. After the turn-on delay time t_{donI} of Si IGBT, Si IGBT is turned on under ZVS-on condition at t_5. During t_5 to t_6, SiC MOSFET and Si IGBT commutate and share the total current. At t_6, the turn-off drive signal of Si IGBT is applied. After the turn-off delay time t_{doffI}, Si IGBT is turned off under ZVS-off condition at t_7 and the current of Si IGBT decreases to 0 at t_8. The large amount of stored charge in Si IGBT decreases as a result of the minority carrier recombination after t_7. At t_9, the turn-off drive signal of SiC MOSFET is applied and SiC MOSFET is turned off under hard switch condition. The current due to the remaining stored charge in Si IGBT after t_9 and the current which charges the parasitic capacitor of Si IGBT will cause the current spike in Si IGBT. The larger the T_2, the less the stored charge in Si IGBT and the lower the turn-off loss of Si IGBT. The influence of T_1 and T_2 on loss and system efficiency under different PWM drive modes is analyzed [2], [3], [4], [6], [7], [9].

Different drive modes will affect the current conducting paths during current commutation. For example, in Fig. 2, SiC MOSFET and Si IGBT will commutate with the horizontal bridge arm at the same time when

$$T_1 < t_{donI} + t_{onI} - t_{donM} \tag{1}$$

where t_{donI} is the turn-on delay time of Si IGBT and t_{onI} is the turn-on time of Si IGBT. While

$$T_1 \geq t_{donI} + t_{onI} - t_{donM} \tag{2}$$

only Si IGBT will commutate with the horizontal bridge arm. in Fig. 2.

B. TYPICAL COMMUTATION LOOPS AND PARASITIC INDUCTANCES MODEL OF INVERTERS WITH HYBRID MODULE

The circuit of a single phase inverter with T-type SiC-MOS/Si-IGBT hybrid module is shown in Fig. 3. Each arm of the vertical leg is made by paralleling an Si IGBT with SiC MOSFET. The horizontal arm is built by serially connecting two Si IGBTs with reverse direction. The IGBT's anti-parallel diode is selected with either Si diode or SiC diode. In the figure the vertical devices such as S_{1I}, S_{1M}, S_{4I} and S_{4M} are 1200 V rating devices while the horizontal devices use 650 V rating devices. In the figure i_0 is output current and u_g is grid voltage.

PV inverters are required to output reactive power during grid faults. It typically needs to operate from −0.8 to 0.8 power factor (PF). Fig. 4 shows the waveform of u_g and i_0 with PF = 0.8. In the figure, the utility cycle is divided into

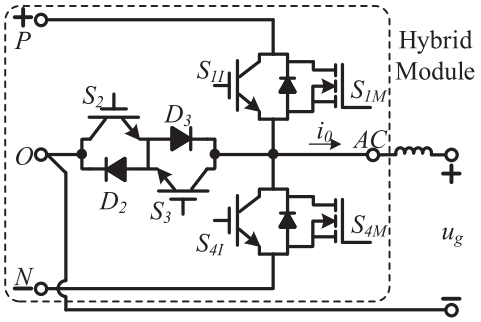

FIGURE 3. A single-phase inverter with T-type SiC-MOS/Si-IGBT hybrid module.

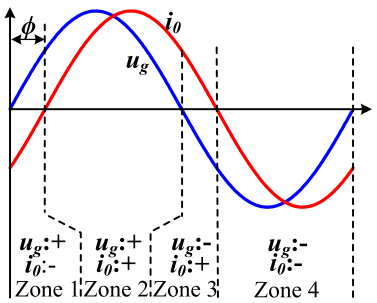

FIGURE 4. The waveform of u_g, i_0 with PF = 0.8.

four zones: Zone 1, Zone 2, Zone 3 and Zone 4 according to the polarities of u_g and i_0.

Current flowing paths in the inverter circuit change in different zones as shown in Fig. 5. Fig. 5 also describes the self- and mutual inductances model of the hybrid module. If $i = j$, L_{ij} corresponds to the self-partial inductance. If $i \neq j$, L_{ij} corresponds to the mutual-partial inductance. The polarity of the mutual inductance depends on the relative orientation of the current between two path segments [30]. Current Commutation Loop (CCL) is defined as the current conducting paths that do not overlap before and after current commutation. The AC terminal path segment is not in the CCLs, so its parasitic inductance is not analyzed in Fig. 5.

At Zone 2, both the grid voltage and grid current are positive. Either upper arm of the vertical leg or the horizontal arm conducts as shown in Fig. 5(a) and (b). For the horizontal arm, only S_2 and D_3 can conduct because the grid current i_0 is positive. For the upper arm of the vertical leg, the grid current can flow through either Si IGBT S_{1I} or SiC MOSFET S_{1M}. Generally, there are two conducting paths for vertical arms. With PWM control, the grid current commutates between the upper arm and the horizontal arm. Due to the parasitic inductance in the CCL in these two arms, voltage or current rings occur during the current commutation. Two CCLs in Zone 2 are represented with red dashed line in Fig. 5(a) and (b). Loop1 has SiC MOSFET device. Loop2 only has Si IGBTs. According to the reference direction of the CCL in the figure,

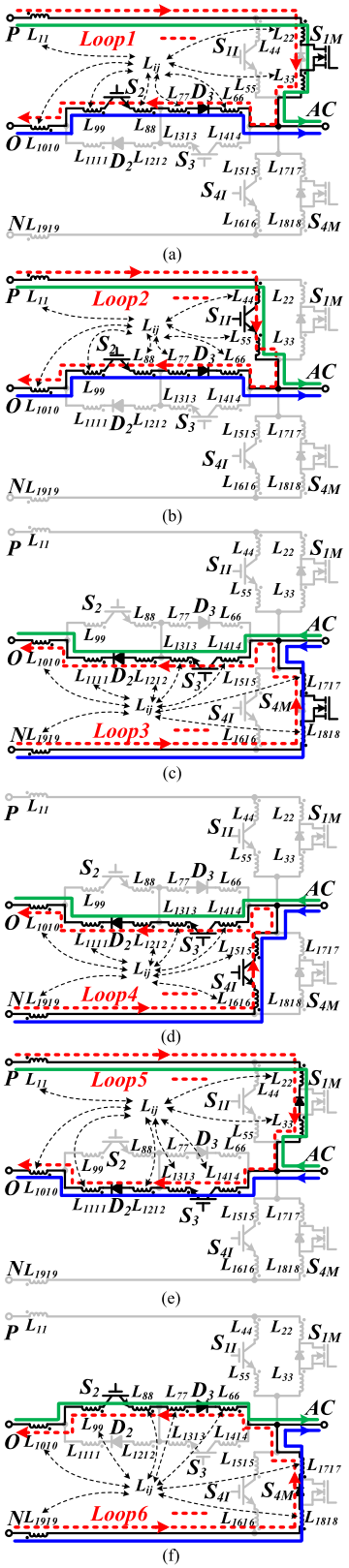

FIGURE 5. Current conducting paths, typical CCLs and self- and mutual inductances model of the hybrid module. (a) Loop1 of Zone 2. (b) Loop2 of Zone 2. (c) Loop3 of Zone 4. (d) Loop4 of Zone 4. (e) Loop5 of Zone 1. (f) Loop6 of Zone 3.

the parasitic inductance of Loop1 can be expressed as

$$L_1 = \sum_{i=1;i\neq4,5}^{10} \sum_{j=1;j\neq4,5}^{10} L_{ij} \tag{3}$$

Similarly, the parasitic inductance of Loop2 can be shown as

$$L_2 = \sum_{i=1;i\neq2,3}^{10} \sum_{j=1;j\neq2,3}^{10} L_{ij} \tag{4}$$

At Zone 4, both the grid voltage and grid current are negative. Similar to Zone 2, there are two CCLs as shown in Fig. 5(c) and (d). Loop3 has SiC MOSFET device while Loop4 has only Si IGBTs. According to the reference direction of the CCL in the figure, the parasitic inductance of Loop3 can be expressed as

$$L_3 = \sum_{i=10;i\neq15,16}^{19} \sum_{j=10;j\neq15,16}^{19} L_{ij} \tag{5}$$

Similarly, the parasitic inductance of Loop4 can be shown as

$$L_4 = \sum_{i=10;i\neq17,18}^{19} \sum_{j=10;j\neq17,18}^{19} L_{ij} \tag{6}$$

At Zone 1, the grid voltage is positive while the grid current is negative. With PWM control, the grid current commutates between the upper arm and the horizontal arm. For the horizontal arm, only S_3 and D_2 can conduct because the grid current i_0 is negative. For the same reason, for the upper arm of the vertical leg, the grid current can flow only through the body diode in dead time. There are only one CCL, Loop5, as shown in Fig. 5(e). Similarly there are only one CCL, Loop6 for Zone 3 as shown in Fig. 5(f). Both Loop5 and Loop6 commutate between Si IGBT and SiC body diode. According to the reference direction of the CCL in the figure, the parasitic inductance of Loop5 can be expressed as

$$L_5 = \sum_{i=1;i\neq4,\ldots9}^{14} \sum_{j=1;j\neq4,\ldots9}^{14} L_{ij} \tag{7}$$

Similarly, the parasitic inductance of Loop6 can be shown as

$$L_6 = \sum_{i=6;i\neq11,\ldots16}^{19} \sum_{j=6;j\neq11,\ldots16}^{19} L_{ij} \tag{8}$$

SiC MOSFET and Si IGBT will commutate with the horizontal bridge arm at the same time in some special cases for example when T_1 satisfies (1) in Fig. 2 for Zone 2 and Zone 4. The parasitic inductance in these special cases is smaller than Loop1 or Loop2 or Loop3 or Loop4. These special cases are not considered as typical CCLs.

From (3)–(8), it can be concluded that reducing the self-inductance, making the mutual inductance negative and increasing the absolute value of the mutual inductance as much as possible can reduce the loop inductance. In other words, the smaller the geometry size of the CCL, the smaller the parasitic inductance. Totally there are 6 typical CCLs for the inverter. Due to lower speed of Si IGBT compared with SiC MOSFET, CCLs with SiC MOSFET switching is critical, which is more sensitive to parasitic inductance. It means Loop1 and Loop3 are more sensitive to parasitic inductance than other four loops. Therefore, Geometry size of Loop1 and Loop3 are required to be minimized as small as possible.

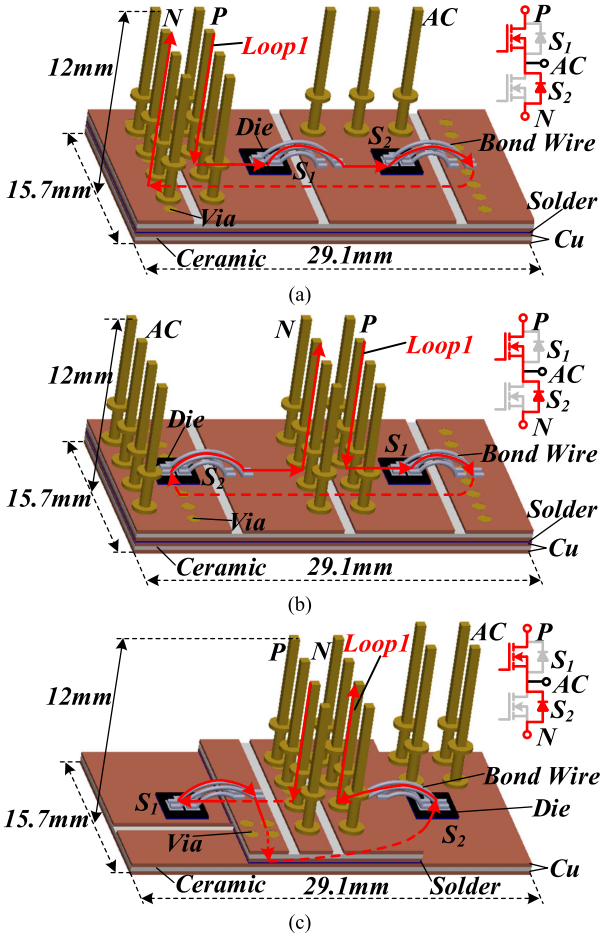

FIGURE 6. Illustration of common half bridge stacked conductive vias substrates structure. Chip on the upper substrate:(a) Structure 1 and (b) Structure 2. Chip on the lower substrate: (c) Structure 3.

III. STACKED SUBSTRATES STRUCTURE FOR HYBRID MODULE

To reduce CCLs, the hybrid module package is studied.

A. STACKED SUBSTRATES STRUCTURE WITH CONDUCTIVE VIAS

The stacked substrate structure is used to reduce CCLs. Traditionally, conductive via is used to connect a upper substrate with a lower substrate for a half bridge module as shown in Fig. 6 [18], [20]. In Fig. 6(a), (b), the semiconductor dies are soldered on the upper substrate. The stacked

TABLE 1. Parasitic Inductance and Steady Self-Thermal Resistance Comparison of Structure 1, 2 and 3

Structure	1	2	3
Self-inductance/nH	11.23	10.86	10.15
Mutual inductance/nH	-5.9	-5.57	-4.7
Total inductance/nH	5.33	5.29	5.45
R_{thjcS1} of S_1(K/W)	0.708	0.716	0.531
R_{thjcS2} of S_2(K/W)	0.699	0.655	0.525

TABLE 2. Parasitic Inductance and Steady Self-Thermal Resistance Comparison of Structure 4, 5 and 6

Structure	4	5	6
Self-inductance/nH (Loop1/Loop3)	9.85/9.43	9.87/9.28	8.35/8.98
Mutual inductance/nH (Loop1/Loop3)	-5.1/-4.87	-5.28/-4.81	-3.05/-4.05
Total inductance/nH	4.75/4.56	4.59/4.47	5.3/4.93
$R_{thjcS1M}$ of S_{1M}(K/W)	0.675	0.705	0.526
$R_{thjcS1I}$ of S_{1I}(K/W)	0.126	0.138	0.076
R_{thjcS2} of S_2(K/W)	0.331	0.342	0.226
R_{thjcD2} of D_2(K/W)	0.634	0.62	0.463
R_{thjcS3} of S_3(K/W)	0.356	0.353	0.226
R_{thjcD3} of D_3(K/W)	0.607	0.636	0.463
$R_{thjcS4M}$ of S_{4M}(K/W)	0.715	0.709	0.525
$R_{thjcS4I}$ of S_{4I}(K/W)	0.138	0.138	0.076

structure can be Cu/ Ceramic /Cu/Solder/Ceramic/Cu or Cu/ Ceramic/Cu/Ceramic/Cu. However, this structure has higher thermal resistance because the dies are located relatively far away from the heatsink. The thermal characteristics can be improved if the dies are soldered on the lower substrate shown in Fig. 6(c).

To evaluate the parasitic inductances of different structures, the solution results at 5MHz is selected in the Q3D simulation due to the reason that the values of parasitic inductances become stable beyond 1 MHz [31]. In addition, 5MHz is a suitable value for the lab's KEYSIGHT Impedance Analyzer E4990A (20Hz∼10MHz) which can be compared with experimental testing result.

Table 1 shows the simulated parasitic inductances for Loop1 of Structure 1, 2 and 3. Also the simulation results of the steady self-thermal resistance by COMSOL software from junction to case(the lowest copper edge in the figure) of different structures are shown in Table 1. Both the upper and lower substrates are Si_3N_4 AMB substrates with Cu/Si_3N_4/Cu 0.3 mm/0.32 mm/0.3 mm in the simulation. The thickness of the solder layer is 0.1mm. The following simulation conditions are the same. The simulation results show that the compromise of Structure 3 compared with Structure 1 and 2 is that CCL and the parasitic inductance become larger while with smaller thermal resistance.

Stacked substrates structures with conductive vias for Loop1 and Loop3 of hybrid module are shown in Fig. 7. Table 2 shows the simulated parasitic inductances for Loop1 and Loop3 of Structure 4, Structure 5 and Structure 6. Also the simulation results of the steady self-thermal resistance are shown in Table 2. The simulation results show that the

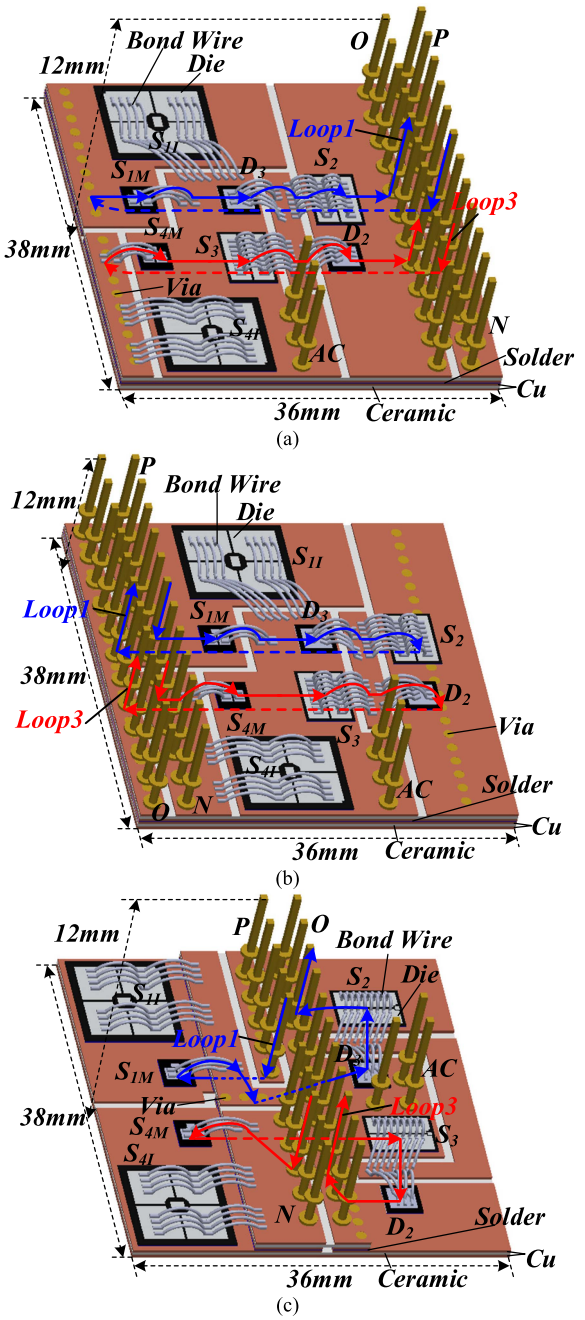

FIGURE 7. Illustration of Loop1 and Loop3 of hybrid module for stacked conductive vias substrates structure. Chip on the upper substrate:(a) Structure 4 and (b) Structure 5. Chip on the lower substrate: (c) Structure 6.

compromise of Structure 6 compared with Structure 4 and Structure 5 is that CCL and the parasitic inductance become larger while with smaller thermal resistance.

For the stacked substrates structure with conductive vias, the production of conductive vias is critical. There are three metalized ceramic substrate technologies: direct bonded copper (DBC), active metal brazed (AMB) and direct plated copper (DPC). Their comparison is listed in Table 3. DBC and AMB can be used in higher current application while

TABLE 3. Metalized Ceramic Substrate Technologies [32]

	DBC	AMB	DPC
Copper Thickness(mm)	<0.6	<0.8	<0.254
Via Feasibility	Very difficult	Can be made	easy
Cost	Low	Low	Medium
Power	High	High	low

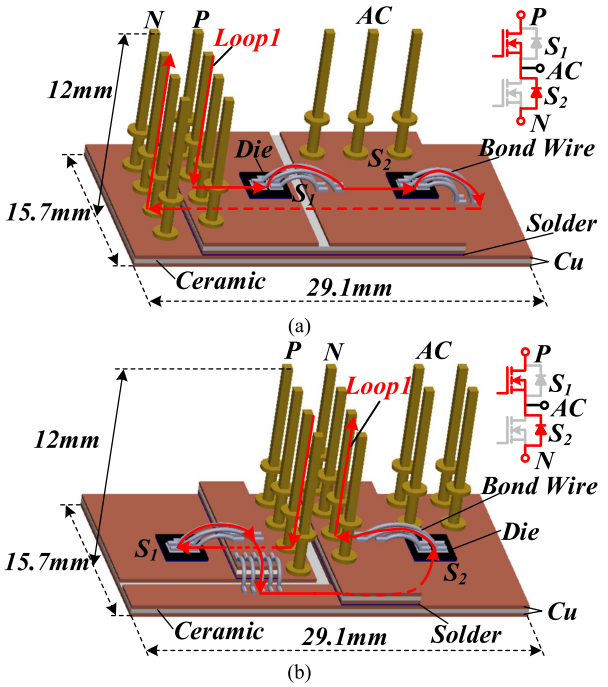

FIGURE 8. Illustration of the half bridge stacked bond wire substrates structure. Chip on the upper substrate: (a) Structure 7. Chip on the lower substrate: (b) Structure 8.

regular DPC is used in lower current application such as LED. Actually it is difficult to make conductive vias for DBC. For AMB, few companies can make conductive vias. It is easy to make conductive vias for DPC. However, currently DPC is not suitable for high power applications research.

B. STACKED SUBSTRATES STRUCTURE WITH BOND WIRE

Because stacked conductive vias of DBC or AMB substrates are not easy to make, bond wire is used to replace the conductive vias. The bond wire structure is easier to make and also is less costly. The stacked substrates structure connects the upper substrate with the lower substrate by bond wires for a half bridge module shown in Fig. 8. Table 4 shows the simulated parasitic inductances for Loop1 of Structure 7 and Structure 8. Also the simulation results of the steady self-thermal resistance of two structures are shown in Table 4. The compromise of Structure 8 compared with Structure 7 is that CCL and the parasitic inductance become larger while with smaller thermal resistance.

Stacked bond wire substrates structures for Loop1 and Loop3 of hybrid module are shown in Fig. 9. Table 5 shows

TABLE 4. Parasitic Inductance and Steady Self-Thermal Resistance Comparison of Structure 7 and 8

Structure	7	8
Self-inductance/nH	11.93	11.56
Mutual inductance/nH	-6.8	-5.24
Total inductance/nH	5.13	6.32
R_{thjcS1} of S_1(K/W)	0.707	0.525
R_{thjcS2} of S_2(K/W)	0.724	0.525

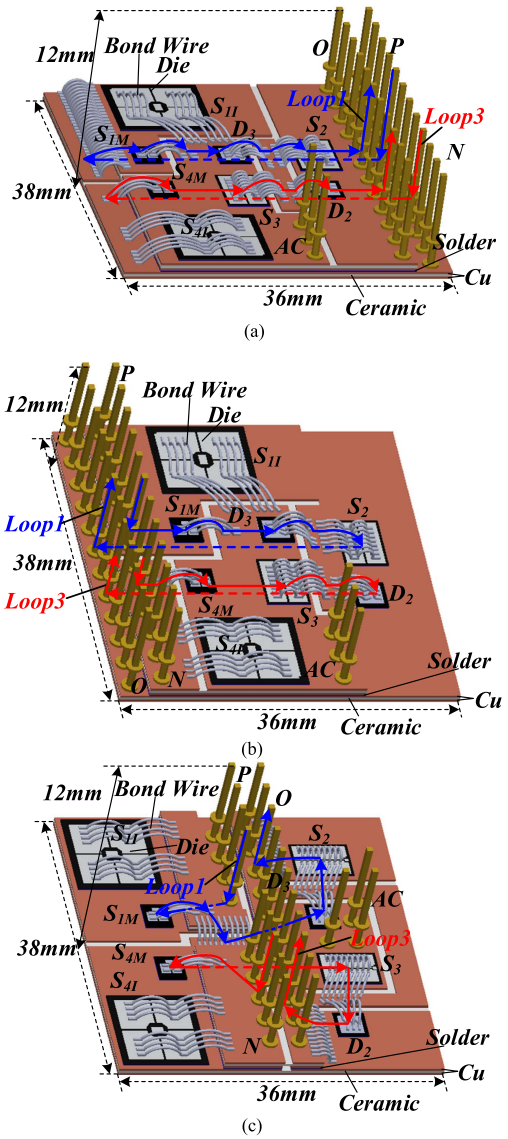

FIGURE 9. Illustration of Loop1 and Loop3 of hybrid module for stacked bond wire substrates structure. Chip on the upper substrate: (a) Structure 9. Chip on the up and lower substrate: (b) Structure 10. Chip on the lower substrate: (c) Structure 11.

the simulated parasitic inductances for Loop1 and Loop3 of Structure 9, Structure 10 and Structure 11. Also the simulation results of the steady self-thermal resistance are shown in Table 5. The compromise of Structure 11 compared with

TABLE 5. Parasitic Inductance and Steady Self-Thermal Resistance Comparison of Structure 9, 10 and 11

Structure	9	10	11
Self-inductance/nH (Loop1/Loop3)	10.34/10.12	9.89/9.4	9.11/8.98
Mutual inductance/nH (Loop1/Loop3)	-5.4/-5.35	-5.4/-4.99	-3.36/-4
Total inductance/nH	4.94/4.77	4.49/4.41	5.75/4.98
$R_{thjcS1M}$ of S_{1M}(K/W)	0.714	0.705	0.526
$R_{thjcS1I}$ of S_{1I}(K/W)	0.138	0.138	0.076
R_{thjcS2} of S_2(K/W)	0.355	0.225	0.226
R_{thjcD2} of D_2(K/W)	0.634	0.458	0.463
R_{thjcS3} of S_3(K/W)	0.357	0.353	0.226
R_{thjcD3} of D_3(K/W)	0.64	0.636	0.462
$R_{thjcS4M}$ of S_{4M}(K/W)	0.705	0.709	0.526
$R_{thjcS4I}$ of S_{4I}(K/W)	0.138	0.138	0.076

TABLE 6. Ceramic Materials [32]

Ceramic Materials	Thermal conductivity (W/m·K)	CTE (ppm/℃)	Flexural Strength (MPa)
Al_2O_3	24-33	6.0-7.2	317-345
AlN	150-180	4.6	360
Si_3N_4	70-90	2.5-3.0	820-932

CTE: Coefficient of Thermal Expansion.

Structure 9 and Structure 10 is that CCL and the parasitic inductance become larger while with smaller thermal resistance.

C. CERAMIC MATERIALS SELECTION

The ceramic material selection is important to power module performance. The most discussed ceramic materials for the insulation layer are Al_2O_3, AlN and Si_3N_4, whose characteristics are compared in Table 6. There are both SiC chip and Si chip in hybrid module. CTE of SiC is 3-4.6 ppm/˚C and CTE of Si is 2.8 ppm/˚C. AlN and Si_3N_4 can be chosen by considering their closer CTE to both the SiC and Si chips compared with Al_2O_3. Besides, AlN and Si_3N_4 also have higher thermal conductivity. With regards to the flexural strength, Si_3N_4 is the best. In short, AlN and Si_3N_4 can be selected for the hybrid module design while their cost is more expensive than Al_2O_3.

IV. DESIGN OF LOW INDUCTANCE HYBRID MODULE

Fig. 10 shows the circuit diagram of the hybrid module. The hybrid module is designed to realize kelvin source connection and kelvin drain connection. The inductances of 6 loops from Loop1 to Loop 6 are defined as L_1, L_2, L_3, L_3, L_4, L_5 and L_6.

Structure 10 and Structure 11 in Fig. 9 are designed in detail in Figs. 11 and 12 respectively. The simulation results for parasitic inductance of Layout 1 and Layout 2 with terminals length 12 mm away from the lowest copper edge are listed in Table 7. Fig. 13 also describes the self- and mutual inductances. The parasitic inductances introduced by the copper terminals are 1.65 nH, 1.44 nH, 2.19 nH and 2.02 nH respectively which can be further optimally reduced by integrating snubber capacitors into module or terminal laminated busbar

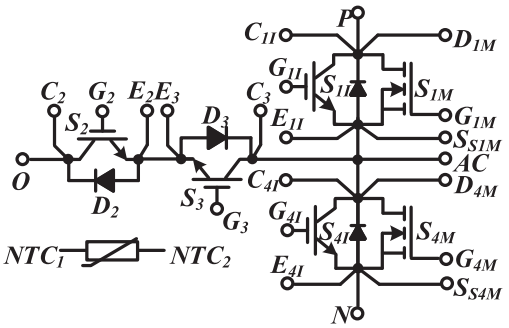

FIGURE 10. Circuit diagram of the hybrid module.

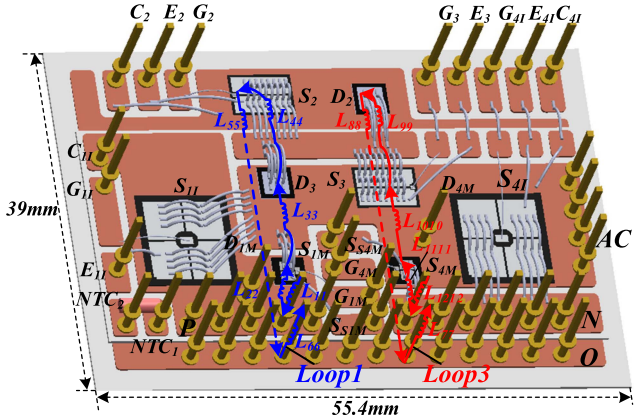

FIGURE 11. Layout 1: Stacked substrates structure with bond wire by soldering most dies on the upper substrate.

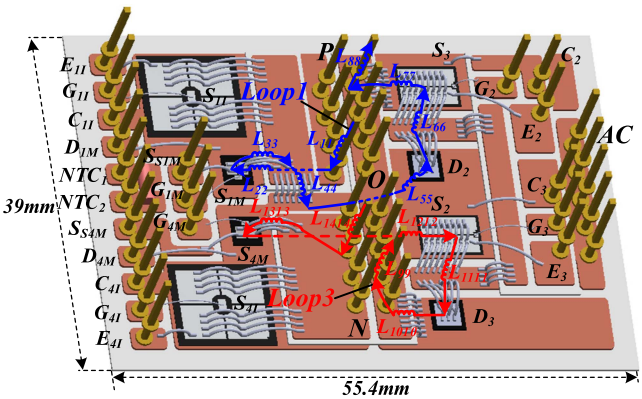

FIGURE 12. Layout 2: Stacked substrates structure with bond wire by soldering dies on the lower substrate.

TABLE 7. Parasitic Inductance Comparison of Layout 1 and Layout 2

	Self-inductance/nH	Mutual inductance/nH	Total inductance/nH
L_1(Layout1/2)	10.93/10.54	-5.91/-3.98	5.02/6.56
L_2(Layout1/2)	9.28/11.51	-4.61/-4.8	4.67/6.71
L_3(Layout1/2)	10.27/10.88	-5.41/-4.97	4.86/5.91
L_4(Layout1/2)	8.84/10.2	-4.43/-4.85	4.41/5.35
L_5(Layout1/2)	11.85/10.63	-6.39/-3.57	5.46/7.06
L_6(Layout1/2)	12.17/11.08	-6.99/-4.63	5.18/6.45

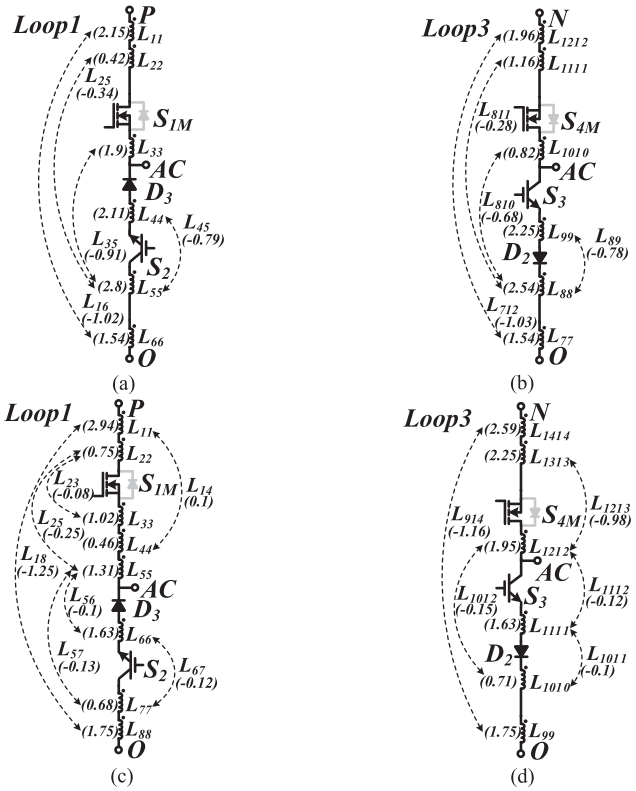

FIGURE 13. Self- and mutual inductances. (a) (b): Layout 1. (c) (d): Layout 2.

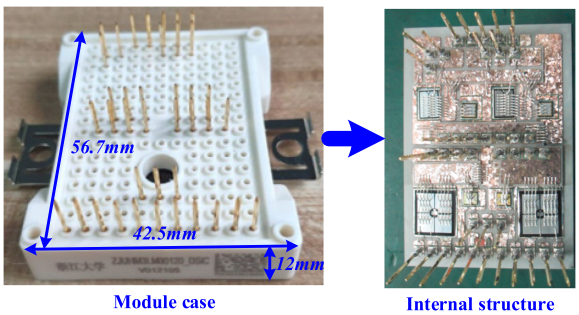

FIGURE 14. The case and internal structure of the hybrid module with SiC SBD.

structure. Generally, the parasitic inductance in Layout 1 is smaller than that of Layout 2 because of smaller CCL.

The steady thermal resistance matrix R_{th} (K/W) including self-thermal resistance and mutual thermal resistance of the module can be calculated with (9) where $T_{j,S1M}$, $T_{j,S1I}$, $T_{j,S2}$, $T_{j,D2}$, $T_{j,T3}$, $T_{j,D3}$, $T_{j,S4M}$, $T_{j,S4I}$ are the junction temperatures, P_{S1M}, P_{S1I}, P_{S2}, P_{D2}, P_{S3}, P_{D3}, P_{S4M}, P_{S4I} are the power losses of the chips and T_C is the case temperature(the lowest copper edge in the figure). The simulation results of the steady thermal resistance matrix by COMSOL software of Layout 1 and Layout 2 are shown as (10) and (11). Obviously, Layout 2 has lower thermal resistance.

$$\begin{pmatrix} T_{jS1M} & T_{jS1I} & T_{jS2} & T_{jD2} & T_{jS3} & T_{jD3} & T_{jS4M} & T_{jS4I} \end{pmatrix}^T = R_{th} \cdot \begin{pmatrix} P_{S1M} & P_{S1I} & P_{S2} & P_{D2} & P_{S3} & P_{D3} & P_{S4M} & P_{S4I} \end{pmatrix}^T + T_C \quad (9)$$

$$R_{th1} = \begin{pmatrix} 718 & 3.5 & 0 & 0 & 0 & 1.2 & 0.2 & 0 \\ 19 & 136 & 0 & 0 & 0 & 9.7 & 0 & 0 \\ 0 & 0 & 226 & 0 & 0 & 1.3 & 0 & 0 \\ 0 & 0 & 0 & 461 & 0.5 & 0 & 0 & 0 \\ 0.2 & 0 & 0 & 0.6 & 352 & 3.1 & 5.2 & 5.2 \\ 1.5 & 1.9 & 0.3 & 0 & 1.5 & 635 & 0 & 0 \\ 0.2 & 0 & 0 & 0 & 2.7 & 0 & 722 & 3 \\ 0 & 0 & 0 & 0 & 12.9 & 0 & 14.5 & 136 \end{pmatrix} \times 10^{-3} \quad (10)$$

$$R_{th2} = \begin{pmatrix} 525 & 1.1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 8.8 & 75.6 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 227 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 466 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 227 & 0.9 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.4 & 466 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 525 & 1.1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 8.9 & 75.6 \end{pmatrix} \times 10^{-3} \quad (11)$$

Moreover, the smaller ceramic substrate area used in Layout 2 means lower cost. Finally, Layout 2 is chosen with tradeoff among parasitic inductance, thermal resistance and cost.

V. EXPERIMENTAL RESULTS

A hybrid module with the Layout 2 in Fig. 12 is built as shown in Fig. 14. The vertical arms is formed by paralleling 1200 V/27 A SiC MOSFET with 1200 V/100 A Si IGBT. The horizontal switches consist of 650 V/75 A Si IGBT and 650 V/68.5 A SiC SBD. In another version of a hybrid module 650 V/75 A Si diode is used to replace the SiC SBD. The power bond wire is 12 mil and the driving bond wire is 5 mil. Both the upper and lower substrate are Si_3N_4 AMB substrates with Cu/Si_3N_4/Cu 0.3 mm/0.32 mm/0.3 mm.

A. STATIC CHARACTERISTIC TEST

The conduction characteristics are measured using Tektronix 371 A High Power Curve Tracer. The junction temperature for the device under test is 125 °C. The measured conduction characteristics of S_{1M} and S_{1I} are shown in Figs. 15 and 16.

B. MODULE PARASITIC INDUCTANCE MEASUREMENT

A hybrid module without bare dies is made to measure the parasitic inductance of the hybrid module as shown in Fig. 17. The 6 CCLs in part II can be obtained respectively by cutting the corresponding bond wires. To measure parasitic inductance, an additional PCB and copper sheet are used to connect the tested module shown in Fig. 18. The corresponding 3D graphic is presented in Fig. 19. The parasitic inductances are measured using KEYSIGHT Impedance Analyzer E4990A (20 Hz∼10 MHz). It is noted that the height of the copper

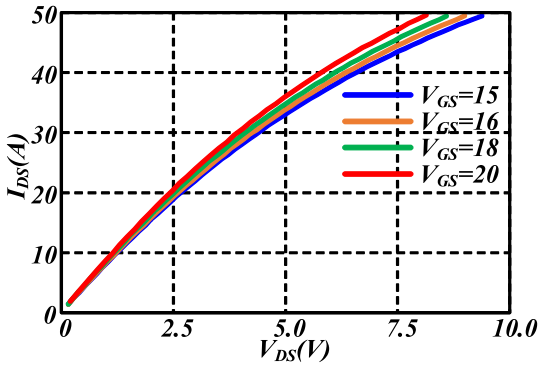

FIGURE 15. Conduction characteristic of S_{1M} between D_{1M} to S_{S1M} @ 125 °C.

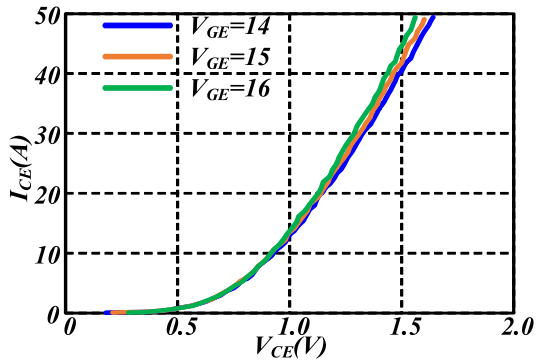

FIGURE 16. Conduction characteristic of S_{1I} between C_{1I} to E_{1I} @ 125 °C.

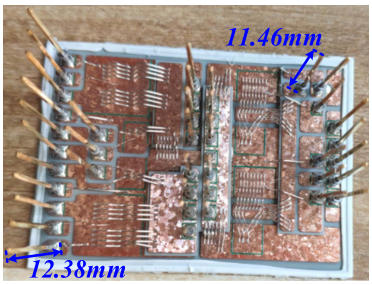

FIGURE 17. The internal structure of the parasitic inductance test SiC SBD hybrid module without bare dies.

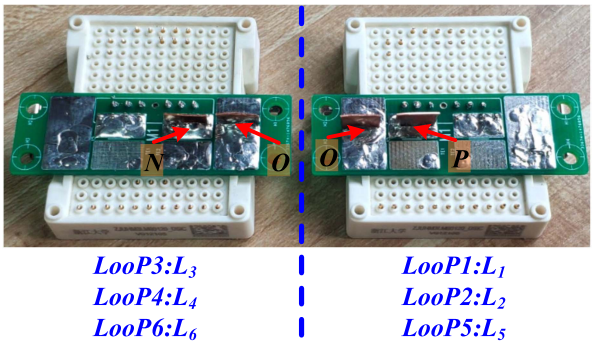

FIGURE 18. The parasitic inductance test circuit.

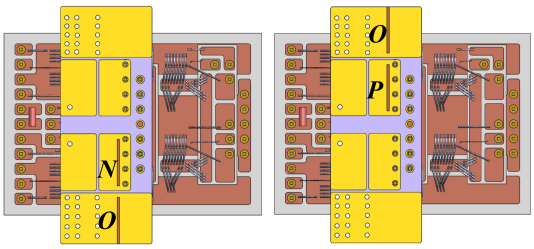

FIGURE 19. The 3D graphic of the parasitic inductance test circuit.

TABLE 8. Switching Loop Inductances (nH)

	L_1	L_2	L_3	L_4	L_5	L_6
Module Simulation	8.71	8.76	8.15	7.49	9.54	8.72
Test Circuit Simulation	10.61	10.7	10.15	9.56	11.61	10.87
Measurement	8.99	9.14	8.49	7.47	10.47	9.38
Measurement + L_{short}	9.91	10.06	9.41	8.39	11.39	10.3

terminal on the upper layer is 11.46 mm and the height of the copper terminal on the lower layer is 12.38 mm under test and Q3D simulation.

The simulation results of parasitic inductance for the hybrid module and test circuit using ANSYS Q3D Extractor at 5 MHz excitation are listed in Table 8. The test circuit measurement results for all the 6 CCLs are also shown in Table 8. The measured results are about 1.1∼2.1 nH smaller than the test circuit simulation results. Before testing, a copper sheet is used for short circuit calibration. The parasitic inductance simulation results for the short circuit calibration copper sheet L_{short} at 5 MHz excitation is 0.92 nH. The test circuit measured results plus L_{short} are also summarized in Table 8. The regulated measured results are still 0.2∼1.2 nH smaller than the test circuit simulation results. The extracted parasitic inductances are verified by the measurement.

C. DOUBLE PULSE TEST

A double pulse test platform is shown in Fig. 20. The double pulse test circuit is represented in Fig. 21. According to the analysis of measuring the current of wide bandgap devices in the literature [33], the coaxial shunt and Pearson current transformer are suitable for current measurement of wide bandgap devices. The total switching current of SiC MOSFET and Si IGBT in the experiment is measured by a magnetic current transformer and a Pearson 2877 shown in Fig. 20. However, inserting a current transformer will significantly increase the parasitic inductance of the commutation loop [34]. The height of the copper terminal on the upper layer is 12.16 mm and the height of the copper terminal on the lower layer is 13.08 mm. According to the simulation results, the parasitic inductance L_3 at 5 MHz (including snubber capacitor inductance) is about 30 nH. With the addition of the current transformer, the parasitic inductance increases about 20 nH.

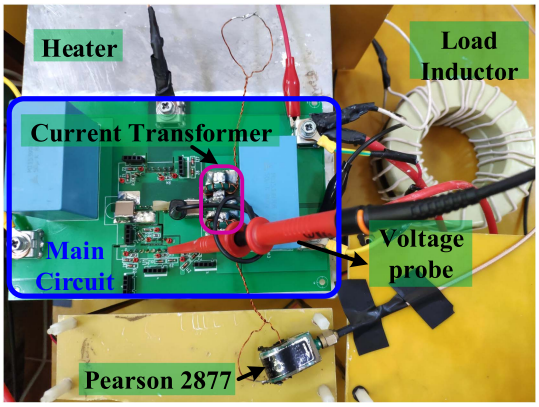

FIGURE 20. The double pulse test platform.

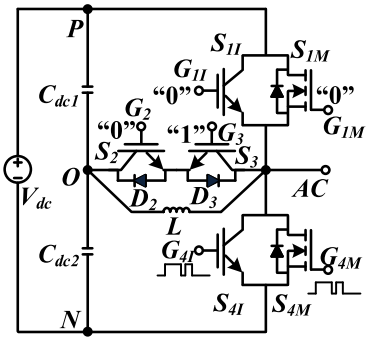

FIGURE 21. The double pulse test circuit topology.

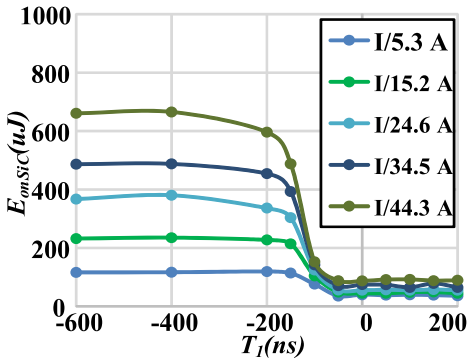

FIGURE 22. Measured turn on switching loss vs T_1 of the hybrid module with SiC SBD@125 °C.

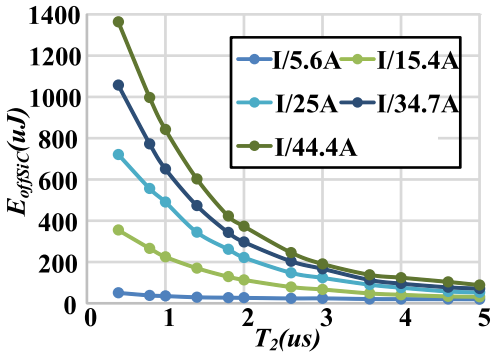

FIGURE 23. Measured turn off switching loss vs T_2 of the hybrid module with SiC SBD @125 °C.

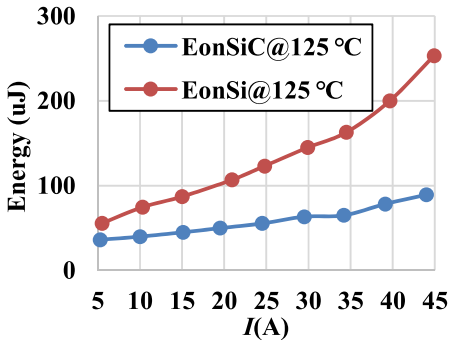

FIGURE 24. Comparison of measured switching loss of the hybrid module with SiC SBD and Si diode under PWM1 gate drive mode (T_1 200 ns, T_2 1 us).

The voltage measurement uses a high voltage passive high bandwidth 300 MHz probe.

As shown in Figs. 22, 23, and 24, the switching loss of the hybrid module with SiC SBD and Si diode is measured respectively under 600V bus voltage, junction temperature 125 °C and current from 5A to 45A. E_{onSiC} and E_{offSiC} respectively represent the total turn on and turn off loss of the hybrid module with SiC SBD. E_{onSi} and E_{offSi} respectively represent the total turn on and turn off loss of the hybrid module with Si diode. Fig. 22 shows the relationship between turn on loss and the time delay T_1 of hybrid module with SiC SBD. "$T_1 \geq 0$" represents PWM1 and "$T_1 < 0$" represents PWM6. The turn on loss is close to that only SiC MOSFET is turned on when

$$T_1 \geq -(t_{donI} - t_{donM} - t_{onM}) \tag{12}$$

The turn on loss is close to that only Si IGBT is turned on when

$$T_1 \leq -(t_{donI} + t_{onI} - t_{donM}) \tag{13}$$

Between them the turn on loss decrease as T_1 increases. Fig. 23 shows the relationship between turn off loss and the time delay T_2. The turn off loss decrease as T_2 increases. Compared with hybrid module with Si diode, the turn-on loss of the hybrid module with SiC SBD is greatly reduced due to the better reverse recovery characteristics of SiC SBD shown in Fig. 24.

D. GRID CONNECTED EXPERIMENT

A single phase grid inverter prototype as shown in Fig. 25 is built to verify the design of the hybrid module. The hybrid module with SiC SBD is used in the inverter. The DC bus snubber capacitor is placed nearby the output terminal of the hybrid module to reduce CCL loop inductance. The simulation results of the parasitic inductance of the inverter including the snubber capacitor at 5 MHz excitation are listed

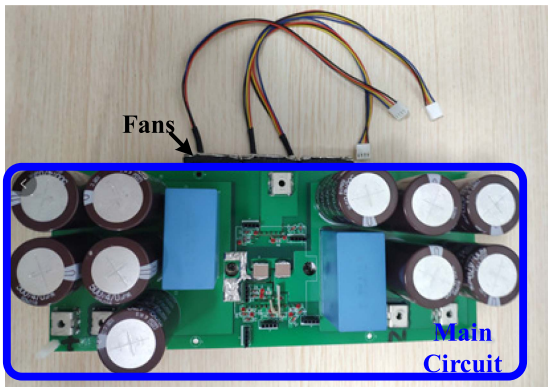

FIGURE 25. A single phase 3LT² SiC-MOS/Si-IGBT grid inverter platform.

TABLE 9. Switching Loop Inductances of the Inverter (nH)

	L_1	L_2	L_3	L_4	L_5	L_6
+L_C	9.97	10.01	9.4	8.74	10.75	9.93

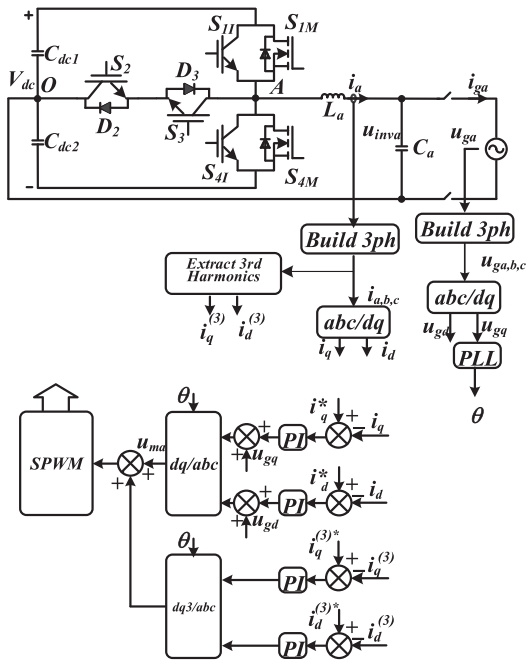

FIGURE 26. The control diagram of the grid inverter.

in Table 9, which are less than 11nH. The control block diagram of the grid inverter is shown in Fig. 26. The modulation method adopts pseudo DQ SPWM. Compared with traditional SPWM, pseudo DQ SPWM control has less static error. In order to suppress the third harmonic in the grid current, the third current harmonic loop is added to the control. The inverter parameters are shown in Table 10.

Fig. 27 and 28 respectively show the grid inverter startup waveform and steady state waveform at rated load. Fig. 29 shows the measured efficiency of the inverter under PWM1 gate drive mode (T_1 0 ns and T_2 1 us) and PWM6 gate drive mode (T_1 200 ns and T_2 1 us). The grid inverter efficiency can reach 98.2% with 50 kHz switching frequency at rated load.

TABLE 10. Parameters of the Inverter

Parameters	Symbol	Value
Switching frequency	f_s	50kHz
Filter inductor	L_a	321μH@0A
Filter capacitor	C_a	4.7μF
DC link voltage	V_{dc}	700V
Grid voltage (RMS)	u_{ga}	232V
Fundamental frequency	f_g	50Hz
Rated power	P	6.7kW

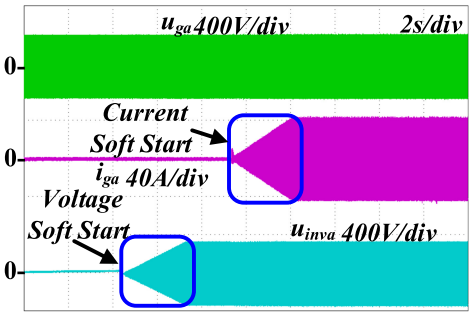

FIGURE 27. The grid inverter startup waveform and steady state waveform at rated load.

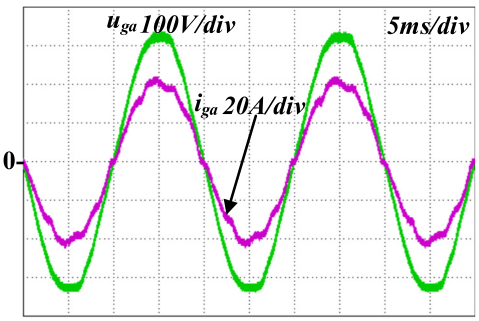

FIGURE 28. The grid inverter steady state waveform at rated load.

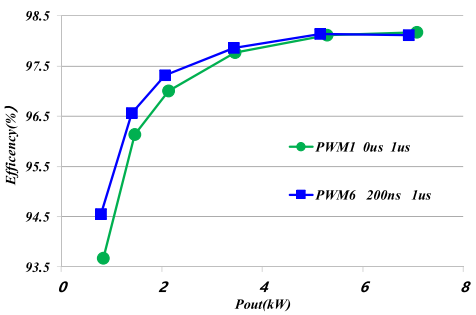

FIGURE 29. Measured grid inverter efficiency at 50 kHz switching frequency.

VI. CONCLUSION

In this paper, a low parasitic inductance three-level T-type SiC-MOS/Si-IGBT module for PV inverter is designed. After analysis of the CCLs of the hybrid module, Loop1 and Loop3 are critical among 6 CCLs. Self- and mutual inductances model of the hybrid module are analyzed. Different stacked substrates structures are compared. Different metalized ceramic substrate technologies and various ceramic materials for stacked substrates are reviewed. Then the stacked substrate structure with the bond wire is chosen among other designs. A hybrid module prototype by using Si_3N_4 AMB substrates with Cu/Si_3N_4/Cu 0.3 mm/0.32 mm/0.3 mm is made. The static characteristics, the parasitic inductances and switching loss are measured. Finally, an inverter prototype with the hybrid module is built. The design of the module is verified by the experiment.

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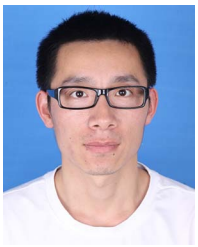

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