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High Frequency Passivity Properties of Grid-Connected Admittance With Double-Sampling Asymmetric Dual-Edge Modulator

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ABSTRACT Small-signal stability and dynamic interactions among power electronic converters (PECs) and electrical grids are widely analyzed using the impedance-based approach. To reduce such interactions, a desirable feature of PECs is that their admittance exhibits dissipative behavior. Due to control delays, the PEC admittance usually exhibits non-dissipative zones around and above the crossover frequency of the inner control loop, possibly reducing the stability margins of the contemporary electrical grids. This paper proposes the double-sampling asymmetric dual-edge digital pulse-width modulator (ADE-DPWM) as an effective way to improve the passivity properties of the PEC admittance. Even in the digital implementation, the ADE-DPWM features zero delay and almost unity magnitude up to half of the switching frequency. Moreover, this paper examines the influence of ADE-DPWM on the PEC admittance even at higher frequencies, where destabilization of poorly damped grid resonances may be influenced by sampling and pulse-width modulation sidebands. Due to an operating point dependent ADE-DPWM small-signal model, the high-frequency passivity properties highly depend on the steady-state operating point. The analytical predictions are shown to be in excellent agreement with the experimental admittance measurements up to twice the switching frequency for all tested steady-state operating points.

INDEX TERMS Admittance, asymmetric dual-edge digital pulse-width modulator (ADE-DPWM), passivity properties, power-electronic converters (PECs), sidebands.

I. INTRODUCTION

Power electronic converters (PECs) are the enabling technology for the exploitation of renewable sources, the management of energy storage, as well as the realization of concepts of electric mobility, long-distance high voltage dc (HVDC) transmission, dc distribution, and microgrids [1], [2]. As a consequence and driven by the demand to achieve carbon neutrality, there is a growing penetration of PECs in transmission and distribution grids [1].

The stability of such heterogeneous power grids is one of the main challenges of today's research [3], [4]. Due to interactions between various PECs, harmonic instability may arise in the form of resonances or abnormal harmonics in a wide frequency range [5]. This compromises normal system operation not only in low voltage distribution networks such as dc nanogrids and microgrids [6], [7], but also in medium or high voltage systems such as railways, HVDC systems, offshore wind farms [8], [9], [10].

To avoid harmonic instability issues [5], the PEC control loops should be designed to ensure stable operation for all possible operating conditions [3], [4], [6]. Passivity-based control (PBC) has been used to achieve this [11], [12], [13], [14], [15]. Taking inspiration from the stability approach based on impedance [4], PBCs assume designing the PEC controller structure such that its admittance exhibits dissipative behavior [11], [12], [13], [14], [15]. Provided that the grid to which the PEC is connected is passive, a sufficient condition for system stability is the passivity of the PEC [11], [12]. Thus, PBC can be considered an effective tool to shape PEC admittance to guarantee the stability of the system that consists of numerous PECs [13], [16]. Since, due to delays, digitally controlled PEC cannot be passive, i.e., dissipative at all frequencies, it is usually required to eliminate non-dissipative zones in the limited frequency range [13], [17], [18].

This paper focuses on analyzing the PEC admittance at frequencies around and above the crossover frequency of an inner control loop, where harmonic instability is mainly caused by sampling, computation, and modulation delays [5], [13]. Two approaches can be used to address the impact of such delays on PEC admittance. The first assumes compensating for delays by providing additional damping to the system [11], [19], [20], [21], [22], [23], [24]. Therefore, passive or active damping (AD) strategies can be used. Since passive damping introduces additional losses into the system [22], [23], AD is usually the preferable solution [11], [19], [20], [21], [24]. Various AD strategies have been proposed to compensate for the delays mentioned above [11], [19], [20], [21]. These can be implemented using a single- or multi-loop controller structure [11], [19], [20], [21]. Single-loop methods rely on additional phase-lead filters, such as derivative action [19], [20]. Although these methods are simple to implement, they only offer improvements at medium frequencies. Instead, multi-loop methods rely on additional feedforward and feedback actions [11], [21]. The downsides of these methods are the increased complexity introduced in the structure of the control system, practical implementation issues, and the fact that passivity properties deteriorate near the Nyquist frequency [25]. An alternative approach is to reduce the control delays [15]. Multi-sampling has recently been proposed as an effective way to reduce computation and modulation delays of systems that employ digital pulse-width modulators (DPWMs), resulting in an inherently dissipative admittance [26]. However, with a multi-sampled approach, some nonlinear properties might appear [26]. Thus, it is worth investigating alternative approaches for the delay reduction. The novel delay reduction-based method to improve the passivity properties of digitally controlled PEC is proposed in [27]. Instead of using state-of-the-art trailing-triangle edge (TTE) carrier-based DPWM [28], the recently proposed asymmetric dual-edge DPWM (ADE-DPWM) is considered [29], [30]. Since in its double-sampling implementation the ADE-DPWM features zero delay and almost unity magnitude up to half of the switching frequency, dissipative behavior of the PEC admittance is improved.

In addition to delays, destabilization of poorly damped grid resonances at high frequencies may also be influenced by sampling and PWM sidebands [5], [13], [14], [21]. Extending the analysis in [27], this paper examines the passivity properties of PECs with ADE-DPWM above half of the switching frequency. To predict system performance at these frequencies, a multiple-frequency model that takes into account sidebands is essential [31]. The admittance model from [31] is also shown to be applicable to accurately predict the high-frequency passivity properties of the PECs with double-sampling ADE-DPWM. Furthermore, it is shown that, as in the case of the TTE-DPWM [31], high-frequency passivity properties of the PEC admittance with ADE-DPWM depend on the steady-state operating point (SSOP). The experimental admittance measurements, performed on a single-phase current-controlled full-bridge converter up to twice the switching frequency, are in excellent agreement with the analytical predictions for all tested SSOPs.

The paper is organized as follows. In Section II, the working principle of the ADE-DPWM is explained. The influence of ADE-DPWM on PEC admittance is analyzed in Section III, where the core principles of the considered multiple-frequency modeling approach are outlined. Experimental admittance measurements are provided in Section IV. Conclusions and a summary are given in Section V.

II. ASYMMETRIC DUAL-EDGE DIGITAL PULSE-WIDTH MODULATOR

A naturally sampled PWM (NS-PWM) based on the asymmetric dual-edge carrier is introduced in [32]. An application based on a similar carrier comes from [33]. In [34] a hysteretic modulator based on the current ripple synthesis is proposed. These three works are similar in terms of the strategy used and the final improvement of dynamic performance. The first digital PWM architecture based on the asymmetric dual-edge carrier is presented in [29]. The latter features the basic operation, the synchronization correction strategy, and an intuitive graphical-based approach for the small-signal analysis. An accurate dynamic model and its experimental validation are presented in [30].

Fig. 1(a) exemplifies the steady-state (gray lines) and the transient operation (black and purple lines) of the double-sampling ADE-DPWM. In this example, the sampling rate is $f_{\mathrm{smpl}} = 2f_s$, where f_s is the steady-state switching frequency, while the samples are acquired at half of T_{on} and T_{off} respectively. Since, during transients, the ADE-DPWM operates at a variable switching frequency, a synchronism correction is required to keep the sampling instants at the proper position, i.e., to ensure center-pulse sampling. A suitable synchronization strategy can be obtained by modulating the upper and lower thresholds, as proposed in [29].

The basic operation of the double-sampling ADE-DPWM can be summarized as follows. Information about the acquired

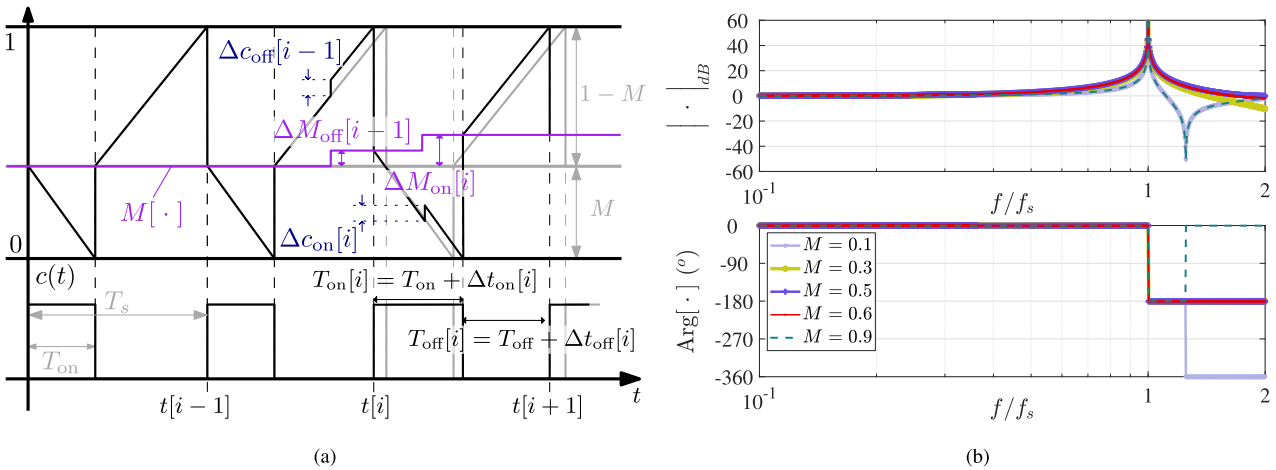

FIGURE 1. Double-sampling asymmetric dual-edge DPWM: (a) Steady-state (gray lines) and transient (black and purple lines) operation and (b) Bode plots of $G_{\text{ADE-DPWM}}(s)$ for different operating points, i.e., $M = 0.1, 0.3, 0.5, 0.6, 0.9$.

samples is written directly on the carrier, i.e., $\Delta c_{\text{off}}[i] = \Delta M_{\text{off}}[i]$ and $\Delta c_{\text{on}}[i] = \Delta M_{\text{on}}[i]$. In doing so, $T_{\text{on}}[i]$ and $T_{\text{off}}[i]$, defined as in Fig. 1(a), can be modulated separately. For example, assume that the modulating signal is increasing, as in Fig. 1(a). Being able to modulate T_{on} and T_{s} separately, the ADE-DPWM can increase the duty-cycle, i.e., $D[i] \triangleq T_{\text{on}}[i]/T_{\text{s}}[i]$, while anticipating the rising-edge of $c(t)$, free from the constraint of a constant switching period. From the analysis disclosed in [30] and using Fig. 1(a) as a reference, it yields

$$\begin{aligned} T_{\text{on}}[i] &= T_{\text{on}} + \Delta t_{\text{on}}[i] = T_{\text{s}}\left(M + \Delta M_{\text{on}}[i]\right) \\ T_{\text{off}}[i] &= T_{\text{off}} + \Delta t_{\text{off}}[i] = T_{\text{s}}\left(1 - M - \Delta M_{\text{off}}[i]\right) \end{aligned} \quad (1)$$

while the resulting i-th modulating period is given by

$$T_{\text{s}}[i] = T_{\text{s}}\left(1 + \Delta M_{\text{on}}[i] - \Delta M_{\text{off}}[i]\right). \quad (2)$$

Expressions (1) and (2) completely describe the time-domain operation of the double-sampling ADE-DPWM exemplified in Fig. 1(a). Equation (1) highlights that the duration of on- and off-phases can be modulated separately. The result, as highlighted by (2), is that the transient switching period is different from the steady-state period.

From the more general small-signal model developed in [30], the (1) and (2) allow to derive the following transfer function

$$G_{\text{ADE-DPWM}}(s) = \frac{e^{s\frac{MT_s}{2}}\left(1 - e^{-sMT_s}\right)}{1 - e^{sT_s}}\left(1 - e^{s\frac{T_s}{2}}\right) + e^{-s\frac{MT_s}{2}} \quad (3)$$

where M is the considered SSOP and s is the complex variable of the Laplace transform.

Fig. 1(b) shows the Bode diagram of (3). Up to half of the switching frequency, the magnitude of $G_{\text{ADE-DPWM}}(s)$ is close to unity, and the phase of $G_{\text{ADE-DPWM}}(s)$ is close to zero, regardless of the SSOP. This result is consistent with the graphical analysis developed in [29]. The double-sampling ADE-DPWM does not introduce any phase delay up to the switching frequency, which is instead commonly observed in conventional DPWM modulators based on TTE carriers. However, the magnitude response of the small-signal model (3) considerably deviates from unity above half of the switching frequency, as shown in Fig. 1(b). At higher frequencies, the influence of SSOP becomes evident both in magnitude and phase. Therefore, the impact of the double-sampling ADE-DPWM on the PEC admittance has to be studied not only up to half of the switching frequency, but also above. This is analyzed in the following section.

III. IMPACT OF ADE-DPWM ON THE PEC ADMITTANCE

A. SYSTEM OVERVIEW

A digitally current-controlled single-phase two-level PEC with an inductive filter is used as a case study, as shown in the block diagram of Fig. 2(a). However, the proposed analysis applies to different PECs and different output filters. The steady-state switching period is $T_s = 1/f_s$, while the control period is $T_{smpl} = 1/f_{smpl} = T_s/2$, i.e., double-sampling is used. The sampling instants are latched with the center of the applied voltage pulses to properly acquire the average current values [35]. The difference between the reference and the sampled current, i.e., $e = i_r - i_{smpl}$, is the input of the current controller G_c. The controller output update is delayed by one sampling period due to a finite execution time. By scaling the controller output to the range [0,1], the digital modulating signal m_s is obtained. This signal is used as an input to the DPWM. Throughout this paper, two DPWM architectures are considered. The first one is the proposed double-sampling ADE-DPWM. The second, used as the benchmark, is the state-of-the-art double-sampling TTE-DPWM. DPWM performs the transition from digital to the continuous time-domain by processing m_s, generating the switching signal x used to control power switches. The difference between the PEC output voltage v_o and the voltage at the point of common coupling (PCC), v_{pcc}, is applied to the

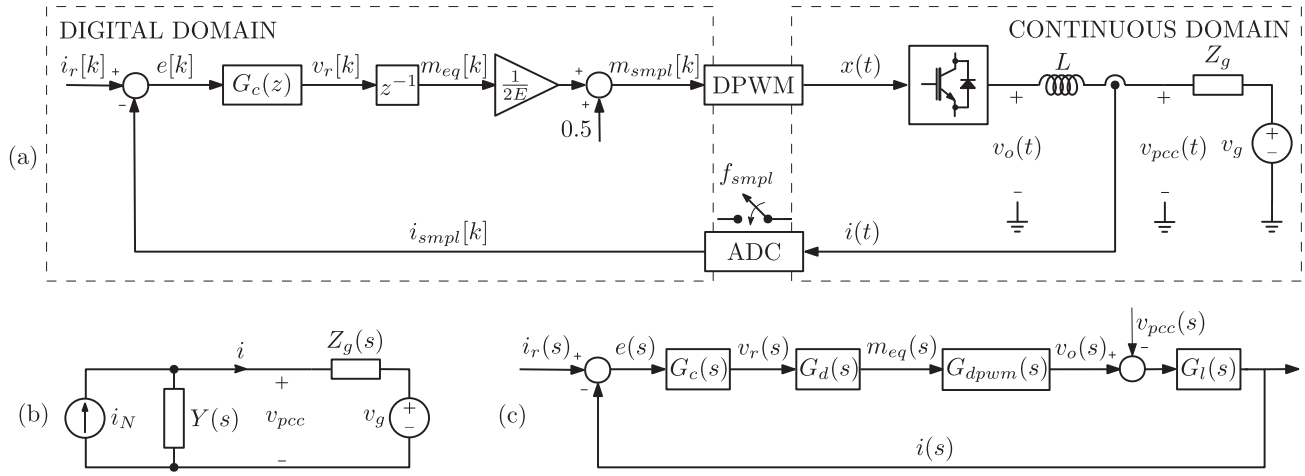

FIGURE 2. Single-phase DPWM grid-following PEC: (a) system block diagram; (b) Norton equivalent circuit used for impedance-based stability analysis; (c) single-frequency small-signal representation of the current loop.

inductive output filter G_l

$$G_l(s) = \frac{i(s)}{v_o(s) - v_{pcc}(s)} = \frac{1}{sL} \tag{4}$$

where L is the filter inductance.

B. IMPEDANCE-BASED STABILITY

For current-controlled systems, the impedance-based stability approach assumes that the PEC is represented by its Norton equivalent circuit, which consists of the current source i_N in parallel with the admittance Y, as shown in Fig. 2(b) [4]. The elements of the Norton equivalent circuit can be found from a small-signal representation of the system, such as in Fig. 2(c). The current source and admittance are defined by

$$i_N(s) = W_{cl}(s) i_r(s), \tag{5}$$

where $W_{cl}(s) = \frac{i(s)}{i_r(s)}\Big|_{v_{pcc}=0}$, and

$$Y(s) = -\frac{i(s)}{v_{pcc}(s)}\Big|_{i_r(s)=0}. \tag{6}$$

Assuming that $W_{cl}(s)$ is stable, the stability of the PEC connected to the grid with the impedance $Z_g(s)$ depends on the product $Y(s)Z_g(s)$, referred to as the minor-loop gain [18]. The system stability can be examined by applying the Nyquist stability criterion to the minor-loop gain [3].

C. PASSIVITY CRITERION

A single-input single-output linear system is considered passive if the real part of its frequency response is non-negative for all frequencies, i.e., its phase is within the range $[-\pi/2, \pi/2]$. In the case that both $Y(s)$ and $Z_g(s)$ are passive, the minor-loop gain always satisfies the Nyquist stability criterion, as its phase is limited in the range $[-\pi, \pi]$. Based on this, the passivity criterion implies that, if the grid impedance Z_g is passive, a sufficient condition for system stability is that PEC admittance Y is also passive. Since, due to delays, Y cannot be passive, i.e., dissipative at all frequencies, the goal of the PBC is to shape Y to be dissipative in a frequency range as wide as possible [13].

D. SINGLE-FREQUENCY SMALL-SIGNAL ADMITTANCE MODEL

Fig. 2(c) illustrates a single-frequency small-signal continuous time-domain representation of the current control loop. In this figure, $G_c(s)$ is the controller transfer function, $G_d(s)$ is s-domain representation of the one-step computation delay

$$G_d(s) = \frac{m_{eq}(s)}{v_r(s)} = e^{-sT_{smpl}}, \tag{7}$$

and $G_{\text{DPWM}}(s) = \frac{v_o(s)}{m_{eq}(s)}$ is the small-signal model of the DPWM. In case of ADE-DPWM, small-signal DPWM model from (3) shall be used. In case of TTE-DPWM, small-signal DPWM model from [28], [36] shall be used

$$G_{\text{TTE-DPWM}}(s) = \frac{1}{2}\left(e^{-sMT_{smpl}} + e^{-s(1-M)T_{smpl}}\right). \tag{8}$$

Based on (6) and using a small-signal representation given in Fig. 2(c), the PEC admittance is determined by

$$Y(s) = \frac{G_l(s)}{1 + H(s)} \tag{9}$$

where $H(s)$ is the loop gain of the system, given by

$$H(s) = \frac{i(s)}{e(s)} = G_c(s) G_d(s) G_{\text{DPWM}}(s) G_l(s). \tag{10}$$

E. SIDEBANDS IN THE SYSTEMS EMPLOYING DPWM

In addition to the desired frequency component, PWM also creates sideband harmonics. These are symmetric around the switching frequency multiples [37]. The PWM sidebands also create additional loops, which have a considerable impact on system performance, near and above the switching frequency [37]. In digital systems, due to the sampling process, there is a second type of sidebands [13]. In addition to the

original frequency component, the sampled signal contains an infinite number of aliases, appearing as sidebands to the sampling frequency multiples [13]. These sidebands create additional loops in the control system, which have a non-negligible impact on system performance near and above the Nyquist frequency [13].

Thus, to accurately model system behavior at high frequencies, a multiple-frequency small-signal model is required. Developing such a model is a challenging task, due to an infinite number of additional loops from the two different origins being present and also mutually coupled [31]. However, as reported in [31], there are cases where modeling can be simplified. Namely, it is shown in [31], that when center-pulse sampling is employed in the systems with TTE-DPWM, PWM sidebands that create additional loops are cancelled out and therefore not introduced in the feedback. This significantly simplifies accurate high-frequency modeling since only sampling sidebands need to be considered. In this paper, it is revealed that the same property is observed in center-pulse sampled PECs with ADE-DPWM.

F. MULTIPLE-FREQUENCY SMALL-SIGNAL ADMITTANCE MODEL

Mathematical procedures similar to those in [31] can be used to verify that cancelation of additional loops induced by the PWM sidebands also holds for the center-pulse-sampled PECs with ADE-DPWM. Thus, depending on the adopted DPWM (TTE- or ADE-DPWM), an accurate multiple-frequency small-signal admittance model of the PEC of Fig. 2 is obtained by incorporating the DPWM model from (8) or (3) in [31]

$$Y_m(s) = \frac{G_l(s)}{1 + \frac{H(s)}{1+H_{sb}(s)-H(s)}} \tag{11}$$

where

$$H_{sb}(s) = \sum_{h=-\infty}^{\infty} H(s - jh2\pi f_{smpl}). \tag{12}$$

The admittance model (11) is verified using a great number of consistent simulated and experimental admittance measurements. The results are presented in the next section.

With the goal of illustrating the differences between single- and multiple-frequency small-signal models, the admittances predicted by (9) and (11) are compared in Figs. 3 and 4 for the PECs with ADE- and TTE-DPWM, respectively. Steady-state operation around $M = 0.85$ is considered. The system parameters provided in Table 1 are used to obtain the plots in Figs. 3 and 4. As an application example, the PI current controller is used

$$G_c(s) = k_p + \frac{k_i}{s}. \tag{13}$$

As seen in Fig. 3, if ADE-DPWM is used, non-negligible differences between (9) and (11) are present starting from approximately $0.5f_s$. The same conclusion holds also for

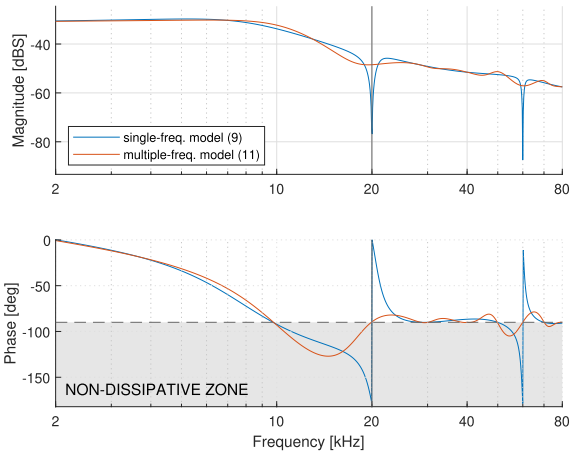

FIGURE 3. Comparison between single- (9) and multiple-frequency small-signal admittance model (11) of the PEC modulated via double-sampling ADE-DPWM at $M = 0.85$. The gray vertical line marks the switching frequency.

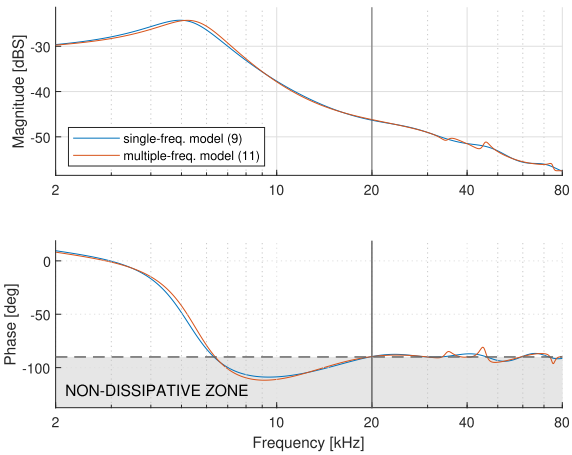

FIGURE 4. Comparison between single- (9) and multiple-frequency small-signal admittance model (11) of the PEC modulated via double-sampling TTE-DPWM at $M = 0.85$. The gray vertical line marks the switching frequency.

TABLE 1. PEC and Control Loop Parameters

PEC	label	value	unit
Nominal dc link voltage	E	200	V
Filter inductance	L	1.5	mH
Switching frequency	f_s	20	kHz
Dead-time	t_{dt}	0.8	μs
Control loop	**label**	**value**	**unit**
Sampling frequency	f_{smpl}	40	kHz
Crossover frequency	f_c	4	kHz
Proportional gain	k_p	38	Ω
Integral gain	k_i	95	kΩ/s

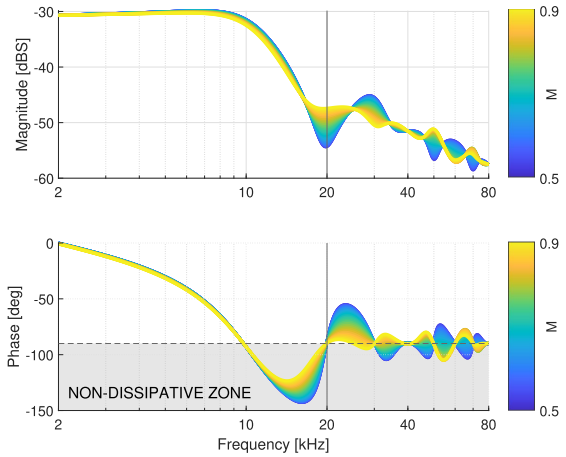

FIGURE 5. Small-signal multiple-frequency admittance model (11) of the PEC modulated via double-sampling ADE-DPWM for different SSOPs, shown in gradient from blue to yellow. The gray vertical line marks the switching frequency.

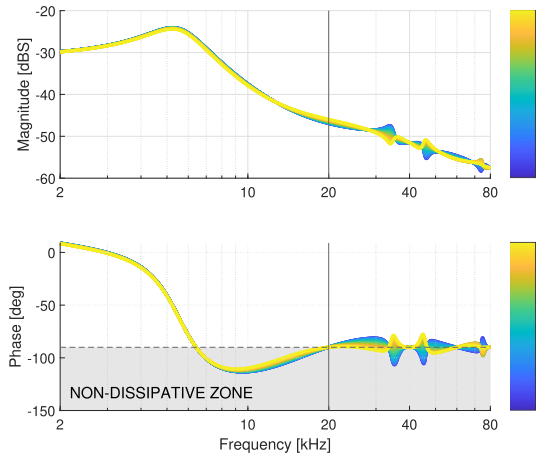

FIGURE 6. Small-signal multiple-frequency admittance model (11) of the PEC modulated via double-sampling TTE-DPWM for different SSOPs, shown in gradient from blue to yellow. The gray vertical line marks the switching frequency.

other SSOPs, but the results are not included for the presentation conciseness. Therefore, to accurately predict the small-signal properties of PECs with double-sampling ADE-DPWM, at frequencies higher than $0.5f_s$, the use of the multiple-frequency admittance model (11) is essential. For lower frequency analyses (9) and (11) can be used indistinguishably, since they yield almost the same admittance frequency response. It is interesting to note that, according to Fig. 4 and analyses in [31], for the PECs with double-sampling TTE-DPWM, the frequency up to which (9) and (11) can be used indistinguishably is approximately $1.6f_s$, which is considerably higher than in ADE-DPWM case.

G. INFLUENCE OF OPERATING POINT ON ADMITTANCE MEASUREMENTS

As shown in [31], SSOP significantly impacts the high-frequency admittance passivity properties of the PECs that use TTE-DPWM. Thus, it is also interesting to examine the influence of the SSOP on the admittance of the PECs that use ADE-DPWM. For these purposes, the admittance predicted by (11) in the case ADE-DPWM is used, is plotted in Fig. 5 for 30 different SSOPs from the range [0.5,0.9]. The similar plot is provided in Fig. 6 for the case when TTE-DPWM is used, with the goal of benchmarking. Note that only results for the SSOPs between 0.5 and 0.9 are shown due to the symmetry of the DPWM models around $M = 0.5$, as seen from (3) and (8). The system parameters provided in Table 1 are used to obtain the plots in Figs. 5 and 6.

The results in Figs. 5 and 6 are plotted for the frequency range [2,80] kHz i.e., up to four times the switching frequency. It is worth noting that the Nyquist frequency is equal to the switching frequency, since double-sampling is considered. According to the presented results, up to approximately half of the switching frequency, ADE-DPWM outperforms TTE-DPWM in terms of ensuring dissipative behaviour of the PEC admittance regardless of the SSOP. However, at higher frequencies, the dependence of the admittance on the SSOP gets pronounced and the non-dissipative zones may appear even with ADE-DPWM.

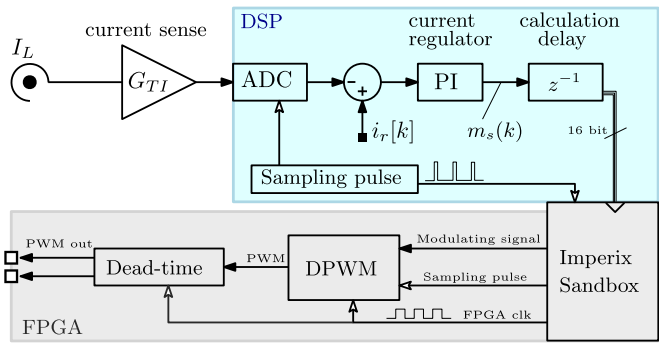

FIGURE 7. Block diagram of the implemented control system.

IV. EXPERIMENTAL VALIDATION

In this section, experimentally measured admittances of the previously discussed PEC modulated by double-sampling ADE-DPWM and TTE-DPWM are provided. The goal is to experimentally verify the analytically shown passivity properties. For this purpose, a single-phase current-controlled full-bridge laboratory prototype shown in Fig. 8 is used, with the hardware and control loop parameters from Table 1. The control system is implemented on Imperix B-Box Rapid Control Prototyping (RCP) platform, using both DSP and FPGA available on the board. The bipolar DPWM is coded through VHDL and implemented on FPGA, whereas the current controller is implemented on DSP. The block diagram of the implemented control system is shown in Fig. 7.

The schematic of the inverter and perturbation circuit used to perform admittance measurements is given in Fig. 9. The perturbation circuit contains the perturbation and the bias branch. A power operational amplifier MP118, from APEX,

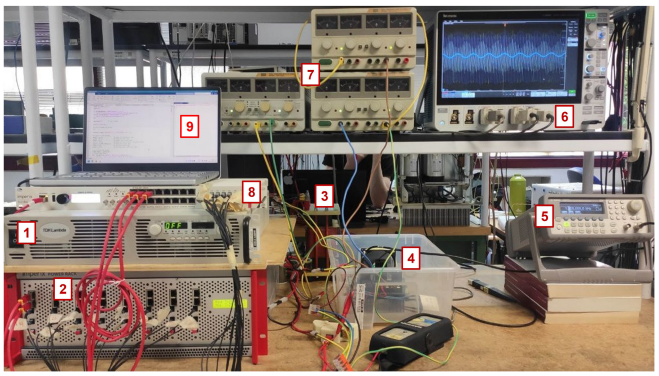

FIGURE 8. Laboratory prototype used for experimental admittance measurements: 1) Input power supply, 2) PEC, 3) output filter, 4) perturbation circuit, 5) signal generator, 6) oscilloscope, 7) supplies for linear-amplifier, 8) controller 9) PC.

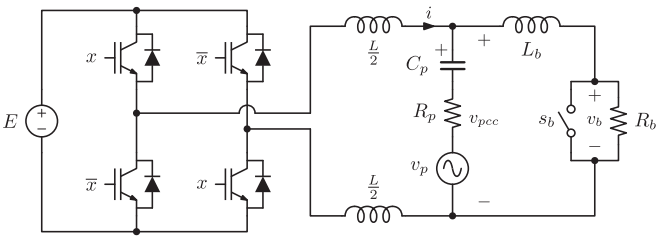

FIGURE 9. Schematic of the inverter and perturbation circuit used for experimental admittance measurements.

is used as a perturbation source, v_p. To ensure precise measurements in the presence of switching ripple and noise, the magnitude of the injected sinusoidal voltage perturbation is calculated for each perturbation frequency to obtain at least 100 mA magnitude of the perturbation current flowing through the PEC. At higher perturbation frequencies, the required magnitude of the voltage perturbation calculated in this way is in the range of several tens of volts. Despite such a high voltage perturbation magnitude, the perturbation component of the modulating signal remains within 2% of the full-range. This is due to the fact that the system responds to the current perturbation, which is in the range of 100 mA. Thus, the small-signal assumptions remain verified.

The perturbation source is connected in series with a capacitor $C_p = 10\ \mu$F and a resistor $R_p = 1\ \Omega$ that is used to smooth any transients. The capacitor is used to block dc currents, as well as to ensure that switching ripple harmonics of i remain the same as if PEC was connected to an ideal grid. The bias branch features an inductance $L_b = 2.4$ mH, used to suppress perturbation currents, and a resistor R_b, which can be bypassed by the switch s_b. The bias branch has two roles. First of all, it allows dc current to circulate. This is important since, for all admittance measurements, a certain dc reference is imposed to avoid zero crossings of the current, which introduce nonlinear damping due to the dead-time [38]. Note that the dc component of i does not impact admittance measurements in the considered frequency range. The second role of the

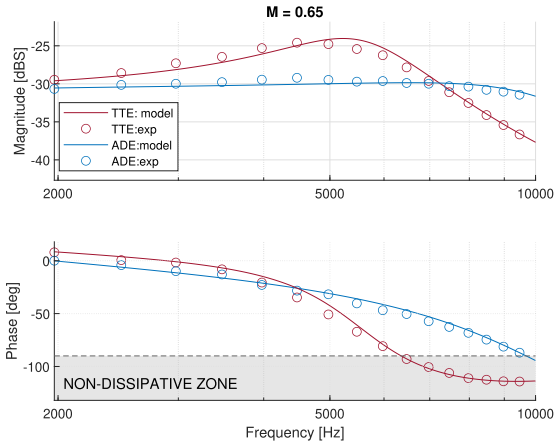

FIGURE 10. Comparison between experimental and modeled admittance frequency response of the PEC modulated via double-sampling ADE-DPWM and TTE-DPWM. Steady-state operation around $M = 0.65$ is considered and the results are given up to half of the switching frequency.

bias branch is to ensure operation around the desired SSOP. That is, when the switch s_b is open, the dc component of i provides a voltage drop across R_b. This results in a dc voltage component of v_{pcc}, referred to as the bias voltage v_b. The bias voltage defines the SSOP as $M = \frac{1}{2}(\frac{v_b}{E} + 1)$.

In order to obtain experimental admittance frequency response, acquisition and post-processing is performed in the following way. The inductor current i and the PCC voltage v_{pcc} are measured via Tektronix 5 series oscilloscope with the data length of 40 ms. Fast Fouries Transform of i and v_{pcc}, is performed in MATLAB to obtain spectral components of i and v_{pcc} at the perturbation frequency. These components are then used to calculate the admittance at the perturbation frequency.

Two sets of experimental admittance measurements are performed, for both considered DPWM architectures, i.e., ADE- and TTE-DPWM. The first set of admittance measurements aims to experimentally verify the improved passivity properties achieved with ADE-DPWM up to half of the switching frequency. For these tests, perturbation is injected at 16 different frequencies, one at a time, starting from 2 kHz and up to 10 kHz. According to Figs. 5 and 6, in this frequency range the admittance is independent of the SSOP. Therefore, the results in Fig. 10 are shown for an arbitrarily SSOP $M = 0.65$. Nevertheless, in order to verify the consistency of the results, the experimental admittance measurements are performed for several other SSOPs. Fig. 10 emphasizes that the PEC admittance is dissipative up to half of the switching frequency using ADE-DPWM modulator, while with TTE-DPWM, the non-dissipative zone starts around $\frac{f_{smpl}}{6} = 6.7$ kHz. This zone is not present in the system using the proposed architecture. This illustrates the benefits of the proposed ADE-DPWM in rendering the PEC admittance dissipative up to half of the switching frequency. Furthermore, according to the presented results, an excellent match is achieved between the admittance theoretically predicted by (11) and the experimental admittance measurements.

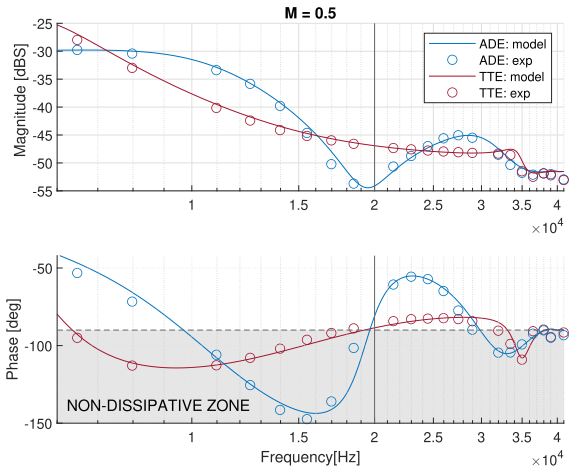

FIGURE 11. Comparison between experimental and modeled admittance frequency response of the PEC modulated via double-sampling ADE-DPWM and TTE-DPWM. Steady-state operation around $M = 0.5$ is considered. The gray vertical line marks the switching frequency.

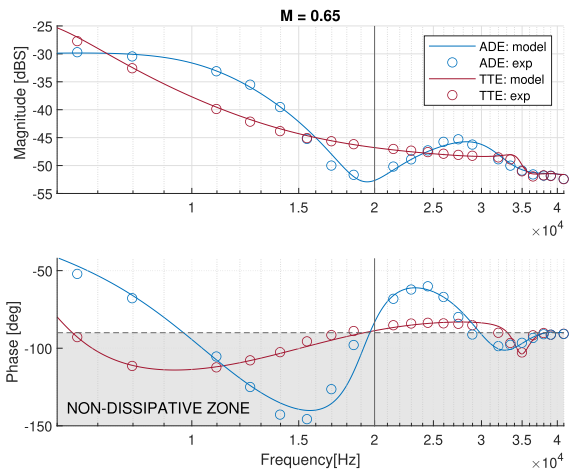

FIGURE 12. Comparison between experimental and modeled admittance frequency response of the PEC modulated via double-sampling ADE-DPWM and TTE-DPWM. Steady-state operation around $M = 0.65$ is considered. The gray vertical line marks the switching frequency.

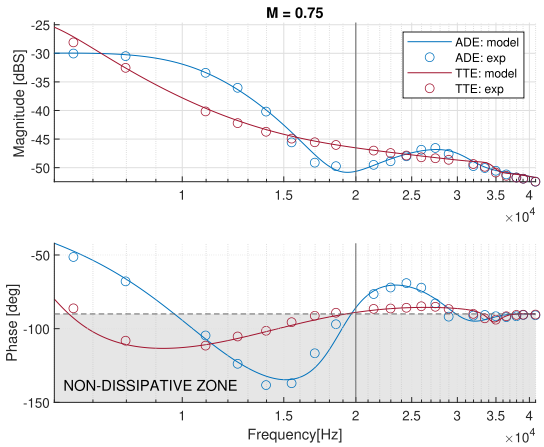

FIGURE 13. Comparison between experimental and modeled admittance frequency response of the PEC modulated via double-sampling ADE-DPWM and TTE-DPWM. Steady-state operation around $M = 0.75$ is considered. The gray vertical line marks the switching frequency.

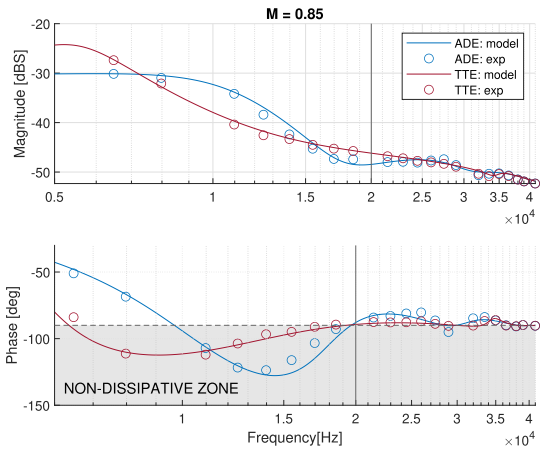

FIGURE 14. Comparison between experimental and modeled admittance frequency response of the PEC modulated via double-sampling ADE-DPWM and TTE-DPWM. Steady-state operation around $M = 0.85$ is considered. The gray vertical line marks the switching frequency.

The second set of experimental tests is used to verify the high-frequency passivity properties of the PEC with ADE-DPWM. For these tests, the perturbation is injected at 21 frequencies, starting from 6 kHz and up to 41 kHz. Perturbations above 41 kHz resulted in the required perturbation voltage magnitude being greater than 60 V, which represents the upper limit due to hardware limitations of the prototype. The limiting factor is the voltage source used to supply the linear amplifier, having the maximum output voltage of 60 V. Therefore, experimental admittance measurements are given up to 41 kHz, which is just above twice the switching frequency. The measurements are performed for several SSOPs and the results are compared to the multiple-frequency model (11) in Figs. 11–14. An excellent match between the proposed model and experimental admittance measurements is achieved for all tested SSOPs and for both DPWM architectures. This attests to the high accuracy and robustness of the modeling approach proposed in [31], while verifying the validity of using the latter for center-pulse sampled PECs with ADE-DPWM.

V. CONCLUSION

This paper investigates the high-frequency passivity properties of the PEC admittance when a double-sampling ADE-DPWM is used. Up to half of the switching frequency, ADE-DPWM exhibits a frequency response that is close to unity, resulting in the reduced modulation delay with respect to the conventional TTE-DPWM. The proposed ADE-DPWM approach outperforms the state-of-the-art modulation method by ensuring dissipative behaviour up to half of the switching frequency. However, at higher frequencies, regardless of whether ADE- or TTE-DPWM is used, the passivity properties strongly depend on the SSOP. The multiple-frequency admittance model from [31] is shown to be applicable also

for accurately predicting high-frequency passivity properties of the PECs with double-sampling ADE-DPWM. The experimental admittance measurements, performed on a single-phase current-controlled full-bridge converter up to twice the switching frequency, are in excellent agreement with the modeled admittance for all tested SSOPs.

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