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Spectral Steady-State Analysis of Inverters With Temperature-Dependent Losses Using Harmonic Balance

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ABSTRACT Accurate calculation of semiconductor losses and temperature is the foundation of any design methodology for a power electronic converter. Computation accuracy and speed play a vital role if a large set of parameters needs to be considered. Averaged loss models often neglect the temperature dependence of transistors, leading to fast, but inaccurate results. In contrast, iterative methods and simulation tools, which can include temperature dependence, take significantly longer to compute, but yield more precise results. This paper presents a best of both worlds approach, by using the harmonic balance method to obtain the steady-state solution for any inverter topology including temperature dependent conduction and switching losses. The proposed method solves for the discrete Fourier series of the device temperature, by expressing the temperature dependence and operating parameters in the frequency domain. The set of equations for each coefficient is solved by a single matrix inversion, resulting in very fast computation for steady-state temperature cycles. The steady-state operation of over one thousand possible inverter designs is calculated within less than one minute, matching iterative simulation in device temperature, conduction and switching losses, at a fraction of the computation time. In addition, the method shows good agreement with temperature measurements of a three-phase silicon-carbide inverter.

INDEX TERMS Harmonic analysis, power converter, losses, power system simulation.

I. INTRODUCTION

Optimization of power electronic converters often aims at multiple goals, such as efficiency, power density, lifetime of components or cost [1], [2]. This procedure often starts with a large number of potential operating parameters and components, in order to meet the desired specifications. For each set of parameters, the losses and performance of the converter components are either calculated based on averaged states or iterated in time for more precise results [3] [4]. Usually, averaged models are much faster than iterative ones, but iterative solutions can include non-linear effects often neglected in averaged models [5]. Depending on the severity of the non-linearity, iterative simulation might be the only commonly available option towards correct results.

In case of power electronic devices, such as silicon or silicon-carbide (SiC) MOSFETs, accurate calculation of the total device losses is severely impeded by the temperature dependence of both conduction and switching losses [6], [7]. The temperature dependent losses can either be obtained through device characterization [8], or analytic modelling [9]. Given the half-bridge inverter in Fig. 1, each transistor experiences a temperature swing because of varying load conditions during each ac cycle. Because the device losses depend on temperature, an algebraic loop is formed: As the device heats up, the losses increase, which in turn further increases the temperature [4]. The convergence of this loop depends on the output frequency of the inverter as well as the thermal interface of the device. Given proper thermal design, the

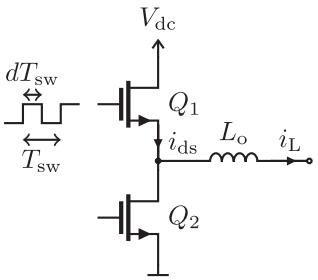

FIGURE 1. Pulse-width modulated half-bridge.

device will reach a periodic steady-state within the allowed operating parameters, after a certain number of cycles. Once in steady-state, the device temperature alternates between a constant minimum and maximum. In this steady-state, the average device losses determine the operating efficiency of the inverter. Furthermore, the temperature swing experienced by the transistor is relevant for lifetime estimation, as thermal expansion of the device, and subsequent bond-wire lift-off or solder-cracks are dominant failure mechanisms in power converters [10]. With non-linearity affecting efficiency and lifetime, precise models and tools are crucial for correct optimization.

One state-of-the-art tool for simulating non-linear thermal behaviour is PLECS [11] [12]. Starting from a given initial condition, it solves the differential equations for all system-states step by step. To do this, PLECS describes the circuit as a set of state-space matrices denoting the change in electric quantities of all passive components, for all possible switching states of semiconductors. To reduce the matrix size and accelerate computation, PLECS can decouple parts of circuits where possible. More detailed information is given in [13]. While PLECS is faster than traditional time-based simulation, a search through a vast solution space still takes a significant amount of time, as several thermal cycles need to be simulated per parameter set until a steady state can be determined.

This paper presents a closed-form solution for the periodic junction-temperature and losses of devices in a power electronic converter including temperature dependence. The method is based on harmonic balance, which thus far, has been applied in power electronics for calculation of distortion caused by non-linear loads [14]. However, the methodology can be adapted to include the non-linearity of losses in calculation of the device temperature. The solution is obtained through a single matrix inversion, making the proposed method orders of magnitude faster than any time-based iterative calculation. To include second-order temperature dependencies, the method can be applied twice to further increase the accuracy. The derivation of the proposed method is covered step-by-step in Section II. Afterwards, a potential use case is demonstrated in Section III. Here, the operating point of a three-phase grid-inverter is calculated for over 1000 possible parameter combinations. The results of the proposed method are compared to simulation done in PLECS, both in accuracy as well as computation speed. In Section IV, the proposed method is compared to measurements on a three-phase SiC inverter. Finally, Section V concludes the paper.

II. TEMPERATURE CALCULATION USING HARMONIC BALANCE

Harmonic balance has been used in circuit simulation to deal with non-linear components in otherwise linear networks [15]. The underlying assumption for harmonic balance is that a given input frequency only produces responses that can be expressed as integer multiples of itself. This allows to express all waveforms in the circuit as discrete Fourier series, and solve the response of each coefficient to the given input frequency. Because harmonic balance works in the frequency domain, differential equations from the time domain transform into algebraic operations. The resulting set of equations can be solved using standard solving methods.

A. POWER TRANSISTOR IN THE FREQUENCY DOMAIN

The basis for the presented method is the equation for the junction temperature of a device $T_j(t)$, given varying conduction losses $P_c(t)$ and switching energies $E_{on}(t)$, $E_{off}(t)$ over time. The device is cooled by a thermal network with a given thermal impulse response $z_{th}(t)$, connected to the ambient temperature T_0. The device's junction temperature is given by

$$T_j(t) = T_0(t) + z_{th}(t) * (P_c(t) + f_{sw}\,[E_{on}(t) + E_{off}(t)]), \quad (1)$$

where '$*$' represents a convolution between the thermal impulse response $z_{th}(t)$ and the losses in the transistor. Transformed to the frequency domain, the convolution becomes a multiplication of the thermal impedance $Z_{th}(j\omega)$ and the loss spectrum, leading to the temperature spectrum

$$T_j(j\omega) = T_0(j\omega) + Z_{th}(j\omega)\ (P_c(j\omega) + f_{sw}E_{sw}(j\omega))\,. \quad (2)$$

The goal is to obtain the discrete Fourier series of the device temperature

$$T_j(t) = \sum_{k=-N}^{N} T_j[k]\, e^{jk\omega_0 t}, \quad T_j[k] = T_j(j\omega_0\, k), \quad (3)$$

where each component corresponds to the temperature spectrum at discrete frequencies $\omega_0\, k$. The underlying assumption is that any sinusoidal current will only cause harmonics at integer multiples of its own frequency. This assumption allows to express each Fourier coefficient of the temperature as a linear combination of the dissipated power and thermal impedance. Only a finite set of N coefficients needs to be considered, as the devices thermal network acts as a low pass and higher frequency coefficients will inevitably tend towards zero. The procedure will produce a system of linear equations for this finite set of coefficients, involving the thermal network, conduction losses and switching losses of the device. By modelling each of these in the frequency domain, including their temperature dependence, a solution for the device temperature can be obtained.

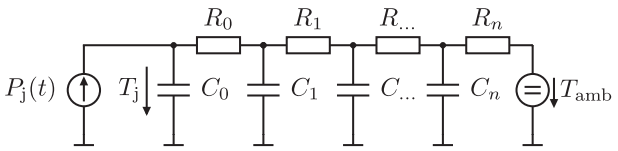

FIGURE 2. Cauer network used to model the thermal path from the device junction to ambient.

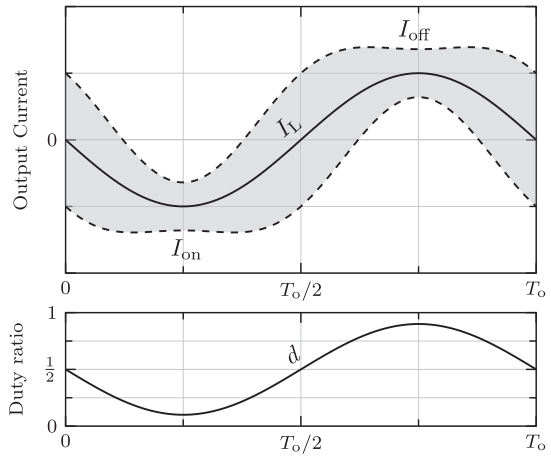

FIGURE 3. Inductor current during a fundamental cycle. The current ripple is centred around the load current I_L and stays between an envelope of I_Δ, dictated by the supply voltage, output inductance, switching frequency and duty ratio.

B. VECTOR NOTATION OF DISCRETE FOURIER SERIES

To solve the set of linear equations, the discrete Fourier coefficients of each series are written as a vector

$$\vec{T_j} = \begin{pmatrix} \dots & T_j[-1] & T_j[0] & T_j[1] & \dots \end{pmatrix}^T, \tag{4}$$

such that the center element corresponds to the average component at zero frequency. Components to the right correspond to positive k and components to the left to negative k. The same representation can be used for other quantities of the inverter, such as the thermal impedance $\vec{Z_{th}}$ or the device losses $\vec{P_c}$ and $\vec{E_{sw}}$.

Using this vector notation, and by writing the thermal impedance as a diagonal matrix of the discrete coefficients $\boldsymbol{Z}_{th} = \mathrm{diag}(\vec{Z_{th}})$, the discrete form of (2) can be written as

$$\vec{T_j} = \vec{T_0} + \boldsymbol{Z}_{th}\left[\vec{P_c}(T_j) + f_{sw}\vec{E_{sw}}(T_j)\right]. \tag{5}$$

C. THERMAL NETWORK

Each transistor has a thermal path from junction to ambient, which determines the thermal response to the power dissipated in the junction. A Cauer network can be used to model this path, as depicted in Fig. 2. Each of the consecutive RC elements can model individual layers within the device or external layers, such as the electric insulation from the device to the heatsink or the heatsink's resistance to ambient temperature. As described in [16], the transfer function of this network can be expressed as

$$Z_{th}(j\omega) = \frac{1}{j\omega C_0 + \frac{1}{R_0 + \frac{1}{j\omega C_1 + \frac{1}{R_1 + \dots}}}}. \tag{6}$$

D. CONDUCTION LOSSES

The basis calculation of the conduction losses is a two-dimensional lookup table $V_{ds}(i_{ds}, T_j)$, which returns the device forward voltage for a given temperature and load current. The table is used to obtain the losses for ambient temperature through direct evaluation, and to model a temperature dependent component through fitting of an arbitrary curve. For simplicity of the loss calculation, the device temperature is assumed to be constant within one switching cycle, which is reasonable given that typical switching frequencies are significantly above the thermal networks cut-off frequency. To begin, the device current is expressed as the sum of the modulated output current I_L and the superimposed current ripple, as depicted in Fig. 3. The load current can be of arbitrary shape, controlled by the modulating the duty ratio $d(t)$ of the half-bridge. This duty ratio is expressed as

$$d(t) = \frac{T_{on}(t)}{T_{sw}}, \tag{7}$$

where $T_{on}(t)$ is the timespan during which the device is conducting current and T_{sw} is the switching period. The amplitude of the current ripple can now be written as

$$I_\Delta(t) = \frac{T_{sw}}{2L_o}\, d(t)\,(V_{dc} - v_o(t)). \tag{8}$$

Within one switching cycle, as depicted in Fig. 4, the device current at turn-on and turn-off can be expressed as $I_{on} = I_L - I_\Delta$ and $I_{off} = I_L + I_\Delta$. At first, the conduction losses at ambient temperature are obtained from the device's look-up table by integrating the voltage current product. The current i_{ds} is known from the operating parameters of the inverter, and the voltage is obtained by evaluating the look-up table $V_{ds}(i_{ds}, T_0)$ at ambient temperature T_0, as shown in Fig. 3(a). The integral is found using Simpson's rule, which gives an exact solution for polynomials provided single values at the beginning, center and end of the conduction interval. The calculation is done in two individual sections, to account for a potential zero crossing of the current, as indicated in Fig. 4, marked in blue and yellow. Either one becomes zero if both turn-on and turn-off current are above or below zero. The total losses at ambient are given in (9) at the bottom of this page.

$$P_{c,0}(t) = \begin{cases} \frac{I_{on}(t)}{6}[V_{ds}(I_{on}(t), T_0) + 2V_{ds}(\frac{I_{on}(t)}{2}, T_0)] + \frac{I_{off}(t)}{6}[2V_{ds}(\frac{I_{off}(t)}{2}, T_0) + V_{ds}(I_{off}(t), T_0)], I_{on} < 0 < I_{off} \\ \frac{1}{6}[I_{on}V_{ds}(I_{on}, T_0) + 4I_L V_{ds}(I_L, T_0) + I_{off}V_{ds}(I_{off}, T_0)], I_{on} < I_{off} < 0 \quad or \quad 0 > I_{on} > I_{off} \end{cases} \tag{9}$$

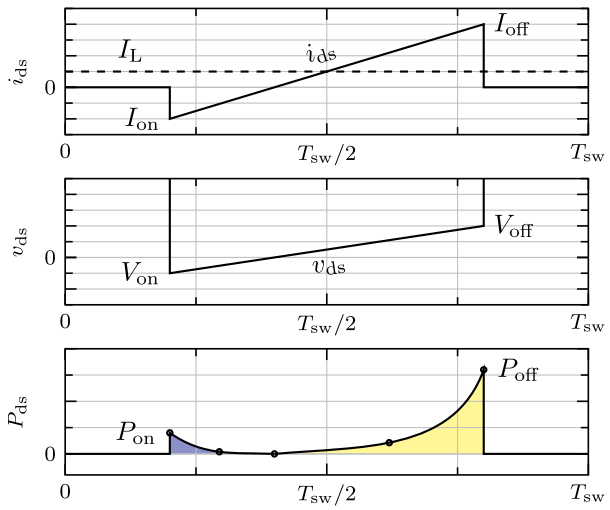

FIGURE 4. Conduction interval of the high-side switch. During the on-state, both device current and voltage increase. The conduction losses are obtained through multiplication of the two quantities. By splitting the conduction losses at the zero crossing, the average loss can be calculated from the mid and end points of the polynomial using Simpson's integration rule.

To now include the temperature dependence, the lookup table is fitted to a second-order temperature-dependent polynomial, with arbitrary functions $f_n(i_{ds})$ for the known device current, such that

$$V_{ds}(i_{ds}, T_j) = V_{ds}(i_{ds}, T_0) + f_1(i_{ds})\,\Delta T_j + f_2(i_{ds})\,\Delta T_j^2, \quad (10)$$

where $\Delta T_j = T_j - T_0$. Analogue to (9), the linear and quadratic dependencies can be formulated as $P_{c,1}$ and $P_{c,2}$, proportional to the linear or square of the temperature. The conduction losses can then be expressed as

$$P_c(t) = P_{c,0}(t) + P_{c,1}(t)\,\Delta T_j(t) + P_{c,2}(t)\,\Delta T_j(t)^2. \quad (11)$$

From this expression in the time domain, the spectrum of the conduction losses can be obtained through a Fourier transform, yielding

$$P_c(j\omega) = P_{c,0}(j\omega) + [P_{c,1}(j\omega) + P_{c,2}(j\omega) * \Delta T_j(j\omega)] * \Delta T_j(j\omega). \quad (12)$$

Using the vector notation described in subsection II-B, the coefficients of the conduction loss spectrum can be formulated as

$$\vec{P_c} = \vec{P_{c,0}} + \boldsymbol{P_{c,T}}\,\vec{\Delta T_j}, \quad (13)$$

where $\boldsymbol{P_{c,T}}$ is a Toeplitz matrix[1] built from

$$P_{c,T}(j\omega) = P_{c,1}(j\omega) + P_{c,2}(j\omega) * \Delta T_j(j\omega). \quad (14)$$

Multiplication of a vector with a Toeplitz matrix carries out the convolution of two discrete Fourier series. $\boldsymbol{P_{c,T}}$ still contains the unknown junction temperature resulting from the second-order terms. This issue is addressed by assuming $\vec{T_j} = \vec{T_0}$ for the initial calculation of $\boldsymbol{P_{c,T}}$ and $\vec{T_j}$, and a subsequent second iteration with the resulting $\vec{T_j}$. Further iteration is possible to improve the results, but little benefit is found for more than two iterations.

E. SWITCHING LOSSES

The switching losses are the sum of the switching energy dissipated in the device each switching cycle at turn-on and turn-off. Again, due to the low pass behaviour of thermal network, the nearly impulse-like switching energy can be averaged over one cycle, yielding

$$P_{sw}(t) = f_{sw}\,(E_{on}(t) + E_{off}(t)). \quad (15)$$

For brevity, this section only covers the derivation of the turn-on losses $E_{on}(t)$. The turn-off losses $E_{on}(t)$ are obtained using the same methodology and the resulting model is included.

The turn-on losses depend on the device current at the beginning of the conduction interval, previously established as I_{on}. Depending on the direction of this current, the device will either experience a hard-switched commutation, dissipating a significant amount of energy, or a soft commutation with little to no energy loss.

PLECS deals with this behaviour through a look-up table $E_{on}(I_{on}, T_j)$ and interpolation between the discrete values. The PLECS loss model for a MOSFET is depicted in Fig. 5(b). For the calculation with harmonic balance, similar as with the conduction losses, the turn-on losses are formulated as an ambient component $E_{on,0} = E_{on}(I_{on}, T_0)$, obtained directly through the loss table, and a part with linear temperature dependence $E_{on,T} = f_{on}(I_{on})\Delta T_j$. The arbitrary function $f_{on}(I_{on})$ is chosen, such that

$$E_{on}(I_{on}, T_j) = E_{on}(I_{on}, T_0) + B_{on}(I_{on})\,f_{on}(I_{on})\,\Delta T_j. \quad (16)$$

As most loss models have zero losses for soft-commutation, the fit $f_{on}(I_{on})$ only needs to be correct for positive turn-on currents. To eliminate the wrong values when f_{on} is evaluated at negative turn-on currents, the resulting energy is multiplied with a boolean function

$$B_{on}(I_{on}) = \begin{cases} 1, & \text{for } I_{on} \geq 0 \\ 0, & \text{otherwise} \end{cases}, \quad (17)$$

blanking any values when the inverter is operating in soft-commutation.

The turn-on losses over time can then be expressed as

$$E_{on}(t) = E_{on,0}(t) + E_{on,T}(t)\,\Delta T_j(t), \quad (18)$$

which can be transformed into the frequency domain as

$$E_{on}(j\omega) = E_{on,0}(j\omega) + E_{on,T}(j\omega) * \Delta T_j(j\omega). \quad (19)$$

Same as with the conduction losses, the vector form of the turn-on loss spectrum is obtained by construction of a Toeplitz matrix $\boldsymbol{E_{on,T}}$ from the temperature dependent spectrum $E_{on,T}(j\omega)$, resulting in

$$\vec{E_{on}} = \vec{E_{on,0}} + \boldsymbol{E_{on,T}}\,\vec{\Delta T_j}. \quad (20)$$

[1] A Toeplitz matrix $\boldsymbol{A}$ is constructed from a vector $\vec{a}$ by $A_{i,j} = a_{i-j}$.

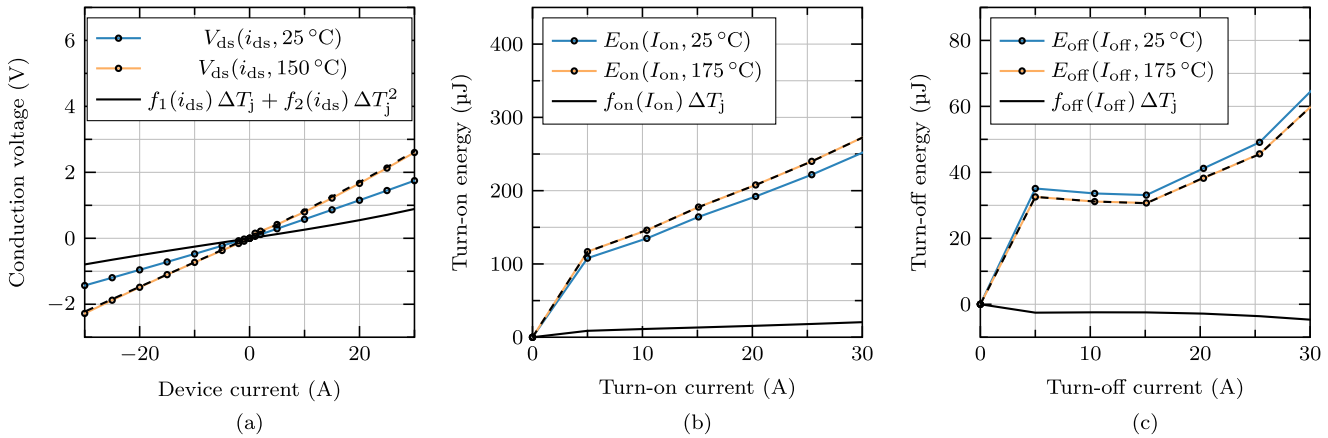

FIGURE 5. Device-loss look-up-table from the device manufacturer (blue, yellow) and fitted loss-model(black) for (a) conduction voltage, (b) turn-on energy and (c) turn-off energy at 700 V. The fitting functions are evaluated at a ΔT_j of 125 °C for the conduction voltage and 150 °C for the turn-on and turn-off energies. When added to the table values of 25 °C, they match the look-up tables at 150 °C and 175 °C respectively (dashed lines). The switching loss fits are only valid for positive device currents. For correct calculation of the switching losses over the fundamental period, the polynomial is multiplied with a boolean function which is zero at times of negative device current, to eliminate the invalid fitting functions.

The same steps can be followed to obtain the expression

$$\vec{E_{\text{off}}} = \vec{E_{\text{off},0}} + \boldsymbol{E_{\text{off},T}}\,\Delta\vec{T_j}, \tag{21}$$

for the turn-off losses, using the turn-off current I_{off}, its corresponding look-up table and boolean function B_{off}. With all loss components modelled in vector format, the initial equation for the junction temperature is solved.

F. SOLVING FOR THE JUNCTION TEMPERATURE

Using the vector notation, (2) can be rewritten using the conduction losses (13), turn-on (20) and turn-off losses (21), resulting in

$$\vec{T_j} = \vec{T_0} + \boldsymbol{Z_{\text{th}}}\left[\vec{P_{c,0}} + \boldsymbol{P_{c,T}}\,\Delta\vec{T_j} + f_{\text{sw}}\left(\vec{E_{\text{on},0}} + \boldsymbol{E_{\text{on},T}}\,\Delta\vec{T_j} + \vec{E_{\text{off},0}} + \boldsymbol{E_{\text{off},T}}\,\Delta\vec{T_j}\right)\right]. \tag{22}$$

The terms proportional to $\Delta\vec{T_j}$ can be collected and T_0 subtracted to obtain

$$\Delta\vec{T_j} = \vec{T_j} - \vec{T_0} = \boldsymbol{Z_{\text{th}}}\left(\vec{P_{c,0}} + f_{\text{sw}}(\vec{E_{\text{on},0}} + \vec{E_{\text{off},0}})\right) + \boldsymbol{Z_{\text{th}}}\left(\boldsymbol{P_{c,T}} + f_{\text{sw}}(\boldsymbol{E_{\text{on},T}} + \boldsymbol{E_{\text{off},T}})\right)\,\Delta\vec{T_j}. \tag{23}$$

Subsequent subtraction and inversion of these terms yield

$$\Delta\vec{T_j} = \left[\boldsymbol{I} - \boldsymbol{Z_{\text{th}}}\left(\boldsymbol{P_{c,T}} + f_{\text{sw}}(\boldsymbol{E_{\text{on},T}} + \boldsymbol{E_{\text{off},T}})\right)\right]^{-1} \boldsymbol{Z_{\text{th}}}\left(\vec{P_{c,0}} + f_{\text{sw}}(\vec{E_{\text{on},0}} + \vec{E_{\text{off},0}})\right), \tag{24}$$

the solution for the increase in junction temperature.

Fig. 6 shows the obtained temperature and losses for the high-side switch of the inverter specified in Table 1 and the fitting functions for the transistor are shown in Table 2. The results from harmonic balance are compared against a reference simulation in PLECS. Both files for simulation and

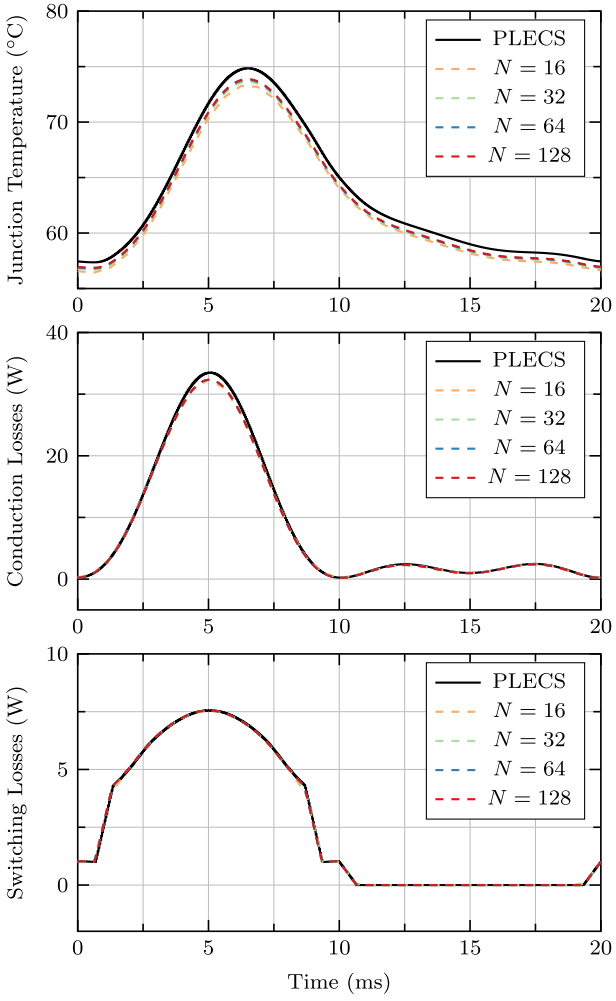

FIGURE 6. Results obtained with harmonic balance (dashed lines) compared to simulation in PLECS (solid line). N denotes the number of harmonics used for harmonic balance, where the first harmonic corresponds to the fundamental of the output current.

TABLE 1. Inverter Parameters

Parameter	Symbol	Value
Switching frequency	f_{sw}	30 kHz
Output frequency	f_{o}	50 Hz
Supply voltage	V_{dc}	700 V
Grid voltage	V_{grid}	230 Vrms
Transistors	Q_1, Q_2	C3M0065100K
Output current	I_{o}	16 Arms
Output inductor	L_{o}	600 µH
Ambient temperature	T_0	40 °C
External thermal interface	$R_{\mathrm{th}}, C_{\mathrm{th}}$	$1\ \frac{\mathrm{K}}{\mathrm{W}}$, $0.05\ \frac{\mathrm{J}}{\mathrm{K}}$

TABLE 2. Polynomial Fits for the Losses of a SiC Transistor (C3M0065100 K)

$$f_1(i_{\mathrm{ds}}) = 26.82\ \tfrac{\mu\mathrm{J}}{\mathrm{A}}\, i_{\mathrm{ds}} 319.45\ \tfrac{\mathrm{nJ}}{\mathrm{A}^2}\, i_{\mathrm{ds}}^2 + 23.23\ \tfrac{\mathrm{nJ}}{\mathrm{A}^3}\, i_{\mathrm{ds}}^3$$
$$f_2(i_{\mathrm{ds}}) = 1.41\ \tfrac{\mu\mathrm{J}}{\mathrm{A}}\, i_{\mathrm{ds}} + 0.96\ \tfrac{\mathrm{pJ}}{\mathrm{A}^4}\, i_{\mathrm{ds}}^4$$
$$f_{\mathrm{on}}(I_{\mathrm{on}}) = 37.4\ \tfrac{\mathrm{nJ}}{\sqrt{\mathrm{A}}}\, I_{\mathrm{on}}^{0.5} - 5.77\ \tfrac{\mathrm{nJ}}{\mathrm{A}}\, I_{\mathrm{on}} + 0.15\ \tfrac{\mathrm{nJ}}{\mathrm{A}^2}\, I_{\mathrm{on}}^2 - 1.15\ \tfrac{\mathrm{pJ}}{\mathrm{A}^3}\, I_{\mathrm{on}}^3$$
$$f_{\mathrm{off}}(I_{\mathrm{off}}) = -17\ \tfrac{\mu\mathrm{J}}{\sqrt{\mathrm{A}}}\, I_{\mathrm{off}}^{0.5} + 4.7\ \tfrac{\mu\mathrm{J}}{\mathrm{A}}\, I_{\mathrm{off}} - 0.1\ \tfrac{\mathrm{nJ}}{\mathrm{A}^2}\, I_{\mathrm{off}}^2 + 0.42\ \tfrac{\mathrm{pJ}}{\mathrm{A}^3}\, I_{\mathrm{off}}^3$$

calculation are uploaded in conjunction with this paper [18]. The PLECS simulation requires an active PLECS standalone license, the harmonic balance method is implemented in python3, which is open source. The semiconductor loss models are available at the manufacturer's website.

Already a very low number of harmonics $N = 16$ yields good accuracy in power losses and temperature. For a higher number of harmonics the calculated temperature approaches the shape of the simulated reference, but at a slight offset. The difference in average temperature can be explained by the slightly lower peak conduction losses. Still, the rest of the curve matches well with simulation results. The switching losses also show very good agreement, with a slight improvement at larger N for the discontinuous sections, where the device enters soft-commutation. To show how the proposed method can be used for fast evaluation and design of inverters, the next section will explore a multitude of operating points for a three-phase inverter, again using PLECS as reference, for both accuracy as well as computation time.

III. DESIGN SPACE EXPLORATION OF A THREE-PHASE SPWM GRID INVERTER

To demonstrate the speed and accuracy of the proposed method, a three-phase grid-inverter, as depicted in Fig. 7, is analysed by search through a vast design space. This space, given in Table 3, spans different load currents, switching frequencies, as well as different filter sizes, yielding a total of 1014 possible combinations. As an application example, the load current is stepped through the profile of the European Efficiency for solar inverters, given by

$$\eta_{\mathrm{euro}} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{15\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.20\eta_{100\%}, \quad (25)$$

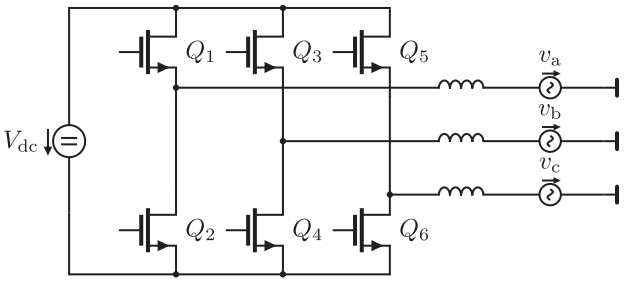

FIGURE 7. Bi-directional three-phase grid-inverter.

TABLE 3. Design Space and Runtime of Simulation

Parameter	Symbol	Value	Steps
Line frequency	f_{g}	50 Hz	-
Line voltage	$v_{\mathrm{a,b,c}}$	230 VAC	-
Ambient temperature	T_{amb}	40 °C	-
Supply voltage	V_{dc}	700 V	-
Switching frequency	f_{sw}	10 kHz to 70 kHz	13
Line current	$I_{\mathrm{o,rms}}$	0.8 A/1.6 A/3.2 A 4.8 A/8 A/16 A	6
Output Inductor	L_{o}	400 µH to 1000 µH	13
Transistors	$Q_{1\ldots6}$	C3M0065100K	-
Total number of simulations		1014	
Runtime PLECS		18 min 23 s	
Runtime Harm. Balance (N = 32)		0 min 11 s	
Runtime Harm. Balance (N = 64)		0 min 25 s	
Runtime Harm. Balance (N = 128)		1 min 10 s	

where η_{xx} is the inverter efficiency at the indicated percentage of maximum load current. For simplicity, the inductive component is treated as lossless, but its impact on the semiconductor losses is considered.

The results obtained through harmonic balance are compared to simulations done in with the PLECS, serving as reference for state-of-the-art steady-state-solvers. Both the harmonic balance method and PLECS use the same look-up table for the device losses, available from the device manufacturer. Thus any discrepancy can be entirely addressed to the proposed method.

For now, both simulation and calculation do not include dead-time, which can become a noticeable contributor to losses at higher switching frequencies [19]. Next to additional losses, dead-time leads to distortion in the output voltage of the inverter [20], which would result in different current ripple and modulation of the device, hindering a direct comparison between calculation and simulation.

A. SIMULATION AND CALCULATION SETUP

Within PLECS, the steady-state analysis tool is used to obtain the device temperature and losses of a single grid cycle. For a fair comparison, both PLECS and the harmonic balance method are run on the same machine (Intel Core i5-7500), as single threaded applications. In a practical scenario, paralleled

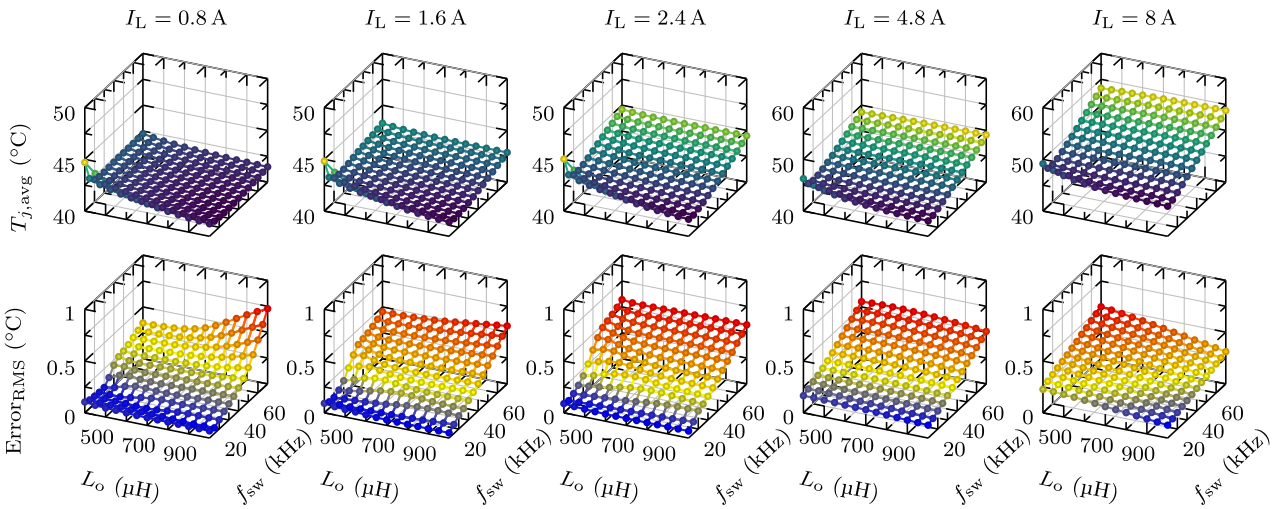

FIGURE 8. Calculation results over one grid cycle in a three phase grid-tied inverter, obtained using harmonic balance (N=128). The load current ranges from 0.8 A to 8 A. Each upper plot displays the average device temperature over one grid cycle, the lower plots show the rms error over the entire period between the calculated waveform and simulation in PLECS.

computing can be used to significantly reduce the absolute computation time of both methods. To evaluate each method's computation time, and not the machine's disk speed, both methods are run without saving of the time domain waveforms, as this significantly affects the time spent by each method. Moreover, the time PLECS takes is extremely dependent on tolerances and other settings. Thus, PLECS is kept at the default parameters preset after installation. The analysis settings and scripts are included within the attached model files.

B. RESULTS

The runtime of each program is listed in Table 3, with PLECS taking 18 min 23 s to analyze all 1014 possible circuit variations. In contrast, harmonic balance run at $N = 32$ harmonics finishes after 11 s. For slightly higher accuracy, the number of harmonics can be increased to $N = 128$, which leads to a computation time of 1 min 10 s, still considerably faster than PLECS.

The calculation results are shown in Fig. 8. The upper set of plots show the average junction temperature for load currents from 0.8 A to 8 A over one fundamental cycle obtained with harmonic balance. To quantify how close the calculation is to simulation, the plots below show the rms error in temperature, calculated by

$$\text{Error}_{\text{RMS}} = \sqrt{\frac{1}{T_0}\int_0^{T_0} (T_{\text{j,PLECS}}(t) - T_{\text{j,Harm.Balance}})^2 dt}. \tag{26}$$

For all operating points, the error stays well below 1 °C. Fig. 9 shows the temperature, conduction and switching losses at a load current of 16 A and their respective rms error to PLECS. Again, the error stays below 1 °C and 1 W respectively. At low inductance and low switching frequency, the high current ripple leads to increased conduction losses. Increasing the switching frequency reduces the conduction losses at first, at a cost of increased switching losses. By further increasing the switching frequency, the feedback effect mentioned in section I sets in: The conduction losses begin to rise, as the increased switching losses heat the device, resulting in higher on-state resistance, and thus larger conduction losses.

TABLE 4. Setup Parameters

Parameter	Symbol	Value
Switching frequency	f_{sw}	10 kHz
Output frequency	f_{o}	50 Hz
Supply voltage	V_{dc}	400 V
Output inductor	L_{o}	5 mH
Dead-time	T_{d}	1 µs
Rms output current	$I_{\text{o,rms}}$	5 A to 10 A
Load cycle frequency	f_{pulse}	0.1 Hz
Load resistance	R_{load}	10 Ω
Ambient Temperature	T_0	25 °C
Heatsink thermal resistance	$R_{\text{th,ca}}$	1.1 $\frac{\text{K}}{\text{W}}$
Heatsink thermal capacitance	$C_{\text{th,ca}}$	7.7 $\frac{\text{J}}{\text{K}}$

For real-world verification, the following section will compare the proposed harmonic balance method to a three-phase inverter, where the junction-temperature of each device can obtained through a high-resolution measurement of the drain-source voltage during conduction.

IV. EXPERIMENTAL RESULTS

The harmonic-balance method is further validated by experiment with a 400 V three-phase SiC inverter, depicted in Fig. 10. The setup parameters are listed in Table 4. The temperature of the transistors is obtained by measurement of the drain-source voltage during conduction. The detailed setup is described in [21]. The measurement is limited by a

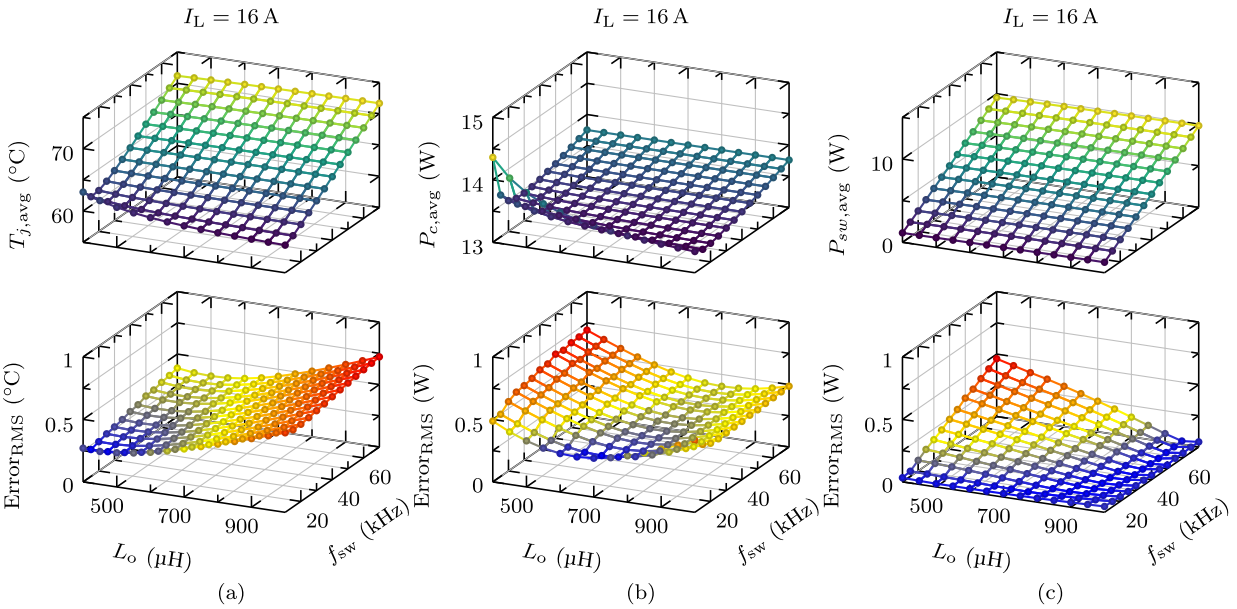

FIGURE 9. Calculation results over one grid cycle in a three phase grid-tied inverter, obtained using harmonic balance (N=128), at a load current of 16 A. The upper plots depict the average quantity over one grid cycle and the lower plots the respective rms error to PLECS for (a) junction-temperature, (b) conduction losses, and (c) switching losses.

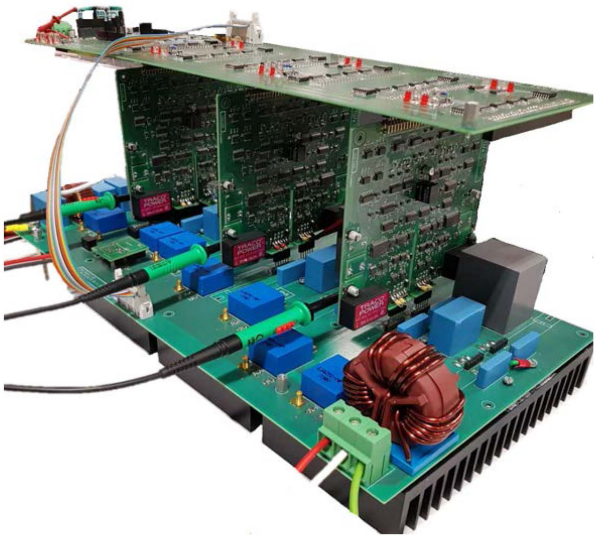

FIGURE 10. Experimental setup for measuring junction temperature swing. Three-phase inverter with clamping circuits to measure the drain-source voltage during conduction.

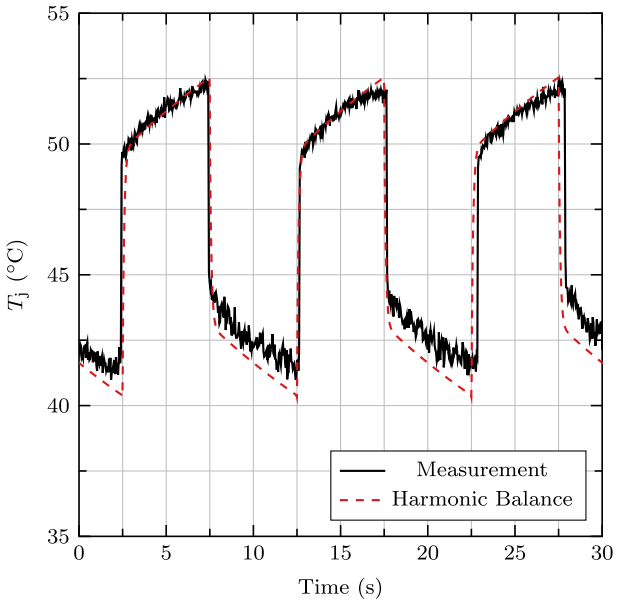

FIGURE 11. Measured temperature cycle compared to calculation using harmonic balance. The calculation result has an offset and amplitude error of about 0.5 °C. Due to imprecise timing of the load pulse generated by the microcontroller, the pulse duration slightly deviates from the programmed 5 s interval. As a result, the early pulses slightly overshoot the calculated response, as the device has less time to cool down. The delayed pulses, on the other hand, undershoot the calculated response, as the device is given slightly more time to cool down.

clamp circuit to obtain sufficient resolution. In combination with a measurement of the load current, the device temperature is obtained through a look-up table. To cycle the device temperature, the inverter supplies a 50 Hz sinusoidal load current with varying amplitude to a 10 Ω resistive load. The amplitude is stepped from 5 A to 10 A in 5 s intervals. The resulting temperature cycle is depicted in Fig. 11, alongside the calculation using harmonic balance. Due to the vast difference in load cycle and output frequency, the matrices become immense and calculation for one cycle takes several seconds. The matrices now contain frequency components up to several 100 Hz at a step size of 100 mHz, which significantly slows down the matrix inversion. Still, the calculation shows good agreement with the measured device temperature. The mismatch between measurement and

calculation is within of 2 °C. Next to possible discrepancies between device and the manufacturer's loss model, the neglect of dead-time losses does affect the calculation result.

V. CONCLUSION

The calculation of device temperature using harmonic balance offers a fast, precise alternative to iterative steady-state solvers, which includes temperature dependence and saturation effects. The results match simulations obtained with commercial state-of-the-art steady-state solvers. Furthermore, good agreement is shown between calculation and measurement results of a 400 V three-phase SiC inverter. The steady state is calculated given a temperature dependent look-up table for the device losses available from the manufacturer, as well as the device current and duty ratio. For well known topologies, these operating parameters are easily written analytically. Otherwise, harmonic balance could serve as an addition to steady-state solvers, producing a solution after the device operating parameters are obtained through a first simulation cycle.

Several aspects of the presented method can be improved for more accurate results and universal application. As previously addressed, dead-time was omitted to simplify the analytic description of the inverter's output voltage and to limit potential error sources. For future work, dead-time losses need to be added as a term proportional to the switching frequency, including load current and temperature dependence. Furthermore, the conduction losses are calculated assuming a triangular output current, as is the case for PWM inverters or buck/boost converters. To extend application of the harmonic-balance calculation method to other topologies, different load current shapes have to be modelled, such as sinusoidal waveforms for resonant converters, or trapezoidal waveforms for active-bridge converters.

In combination with analytic loss models such as [9], it could enable fast, fully analytic evaluation of a power stage solely from the transistor datasheet. Next to thermal design of the inverter, the obtained temperature cycles can serve as input for life-time estimations [22]. State-of-the-art calculation methods for inductor and capacitor losses could be added to optimize the complete system [23], [24]. Beyond design of inverters, a possible application of harmonic balance could be over-temperature protection. Given that harmonic balance only requires standard matrix functions, it could be implemented on capable DSPs used to control the inverter. As the calculation produces the inverter's steady-state response, the controller could predict over-temperature of the transistors, before their thermal network reaches the undesired operating point and limit the load current to prevent this.

Harmonic balance performs best at small timescales, such as 50 Hz to 60 Hz grid cycles, up to several seconds for step responses of the thermal network, due to the required matrix inversion. For longer periods, such as drive cycles for electric vehicle inverters, the system matrix becomes extremely large, as it would contain frequency components in the kHz range for the load current, down to components in the mHz range for the driving profile. As the computation time for matrix inversion grows exponentially with size, iterative methods would become the faster option. Further research is necessary to see if simplified, reduced timescale models would provide sufficient accuracy.

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