A Modified Forward PFC Converter for LED Lighting Applications

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ABSTRACT A modified forward power factor correction (PFC) converter for light-emitting-diode (LED) lighting applications is proposed in this paper. The proposed circuit topology is an integration of a forward converter and a flyback converter with a multi-windings transformer. The flyback converter is operated as an auxiliary voltage source (AVS) connected in series with the rectified ac grid voltage to achieve low harmonic current distortion and high power factor. The magnetizing inductance energy is recycled to charge the capacitor in the AVS. The commonly used constant on-time control and primary side regulation can be easily adopted to control the proposed LED driver. The operation principle of the proposed converter is presented followed by the mathematical derivation of the parameter design. An 80 W prototype converter was built and tested to verify the performance of the proposed PFC converter. Experimental results show that the proposed PFC converter can comply with the IEC 61000-3-2 standard with high efficiency, low current harmonics, and a nearly unity power factor under universal input voltage range.

INDEX TERMS AC-DC power converter, power factor correction, total harmonics distortion.

I. INTRODUCTION

The light-emitting-diode (LED) characterized by compact size, high efficiency, and long-life cycle, is now to be the most popular lighting source. With the increased popularity of LEDs in the lighting market, the electrical performance of their drivers has to be certified by US Department of Energy, Energy Star, California Energy Commission, IEC standards, and so on. To comply with these standards, the key features of LED lighting drivers are high conversion efficiency, high power factor (PF), and low total harmonic distortion (THD). The IEC 61000-3-2 Class C aims to set limits to the harmonic currents to maintain the quality of the ac mains [1], [2], [3], [4], [5], [6], [7], [8]. Therefore, the demanding specifications of the LED driver have challenged electronic engineers to come up with efficient and cost-effective solutions to the circuit design.

The most commonly used power factor correction (PFC) circuit is the boost-type circuit topology. It can achieve the feature of continuous input current, high PF and low THD within the universal input voltage range. However, the high output voltage of boost-type PFC circuit has to be stepped down by an additional converter, which reduces the power efficiency for the LED application.

To meet the requirement of low out voltage with high efficiency, the buck-type PFC circuit has become an alternative solution. Nevertheless, the buck-type PFC has inherent drawbacks of poor PF and high THD, due to the dead zone of the discontinuous input current while the input voltage is lower than the output voltage [9], [10], [11], [12], [13]. To overcome this disadvantage, different non-isolated buck-type PFC converters via circuit integration have been proposed to eliminate the dead zone to achieve high PF and low THD [14], [15]. Unfortunately, these integrated converters have relatively low efficiency due to the additional component counts by comparing to the conventional single-stage buck-type PFC converters. Also, they require relatively complex control methods to achieve the demanded functions. On the

other hand, a conventional buck converter cascaded by a voltage source, coupling from the buck inductor, to ensure the input current continuity to achieve high PF and low THD has been proposed for LED lighting applications [16], [17], [18], [19]. However, both boost-type and buck-type converters cannot meet the galvanic isolation safety standards.

The most popular circuit topology adopted for the PFC application with galvanic isolation is the flyback converter. Unfortunately, the high voltage spike caused by the leakage inductance of the transformer and the large output voltage ripple are the major drawbacks of LED applications. Usually, the flyback PFC is adopted for the low power LED lighting applications.

On the other hand, the buck-derived forward converter does not have the voltage spike caused by the leakage inductance and has a relatively smaller output voltage ripple so it is good for the LED application. However, it still suffers from the dead zone of input current which leads to low PF and high THD features. Furthermore, an extra reset winding and a diode are required to prevent transformer saturation.

To synthesize the merits of the flyback and the forward converters, many integrated flyback-forward converters have been proposed to improve the power factor and power efficiency [20], [21], [22], [23]. Among those integrated converters, the flyback converter is integrated into the forward converter to maintain the continuity of the input current in the dead zone and reset the magnetizing inductor. However, sophisticated control schemes need to be developed and complicated auxiliary circuits are required which are not suitable for those cost-effective LED applications.

Therefore, a modified forward PFC converter is proposed in this paper to meet the requirements of galvanic isolation, high PF, low THD, and high efficiency for LED lighting applications. In the proposed modified forward PFC converter, a novel auxiliary voltage source (AVS) is inserted in series with the rectified ac input source to sustain the continuity of input current during the low voltage interval. The AVS in the proposed modified forward PFC converter is realized by the original reset winding, blocking diode, and input capacitor so no extra component is required. The proposed modified forward PFC converter can be applied to different applications including LED lighting with the merits of small size, low cost, high PF, low THD, and high efficiency.

II. CIRCUIT CONFIGURATION
The circuit configuration of the conventional forward PFC converter is shown in Fig. 1. By controlling the switch Q, the input current can be regulated to be sinusoidal and in phase with the input voltage. The auxiliary winding, N_a, is essential to release the residual magnetizing flux energy to the input terminal to prevent transformer saturation. To maintain the continuity of the input current when the rectified input voltage, v_i, is lower than the reflected output voltage, the AVS is adopted, as shown in Fig. 2, to improve the power factor of the forward PFC converter. When v_i is lower than the reflected output voltage, the AVS provides a sufficient voltage source
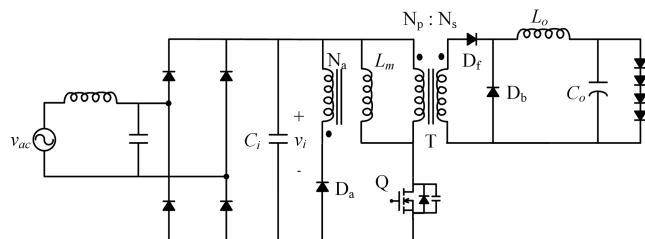

FIGURE 1. The conventional forward converter for power factor correction.
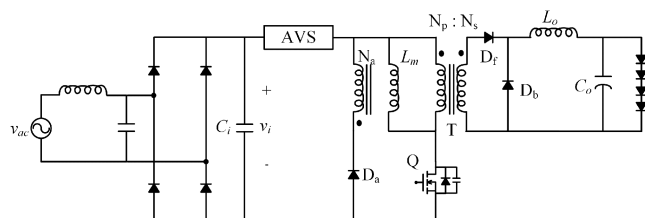

FIGURE 2. The forward converter with AVS for power factor improvement.
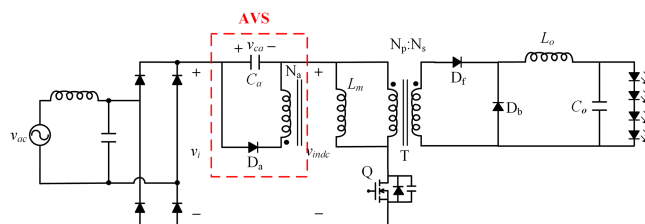

FIGURE 3. The proposed modified forward PFC converter.

for the forward converter to continuously deliver the power to the load. Therefore, the dead zone of the input current can be mitigated or eliminated the PF and THD can be improved significantly. However, additional circuitries and components are required to realize the AVS.

The proposed modified forward PFC converter with a novel AVS is illustrated in Fig. 3. To realize the AVS, the rest winding N_a is adopted to deliver the stored energy in the transformer via the reset diode D_a to the series capacitor C_a to build up the required voltage. The original input capacitor C_i is adopted to fulfill the energy storage capacitor C_a inside the AVS. Eventually, the power factor and THD of the modified forward converter can be improved dramatically with the same component counts using the same control scheme by comparing to the conventional forward converter. Also, the power density will not be affected by the proposed AVS since no additional components are required.

III. CIRCUIT OPERATION
The primary-side regulation (PSR) is adopted as the control scheme of the proposed converter. With fewer components and simplified feedback circuits, the PSR is the most popular control method to regulate the output current for LED lighting applications [24], [25], [26], [27]. The proposed modified forward PFC converter with PSR control is illustrated in Fig. 4. The zero current detection (ZCD) method using an
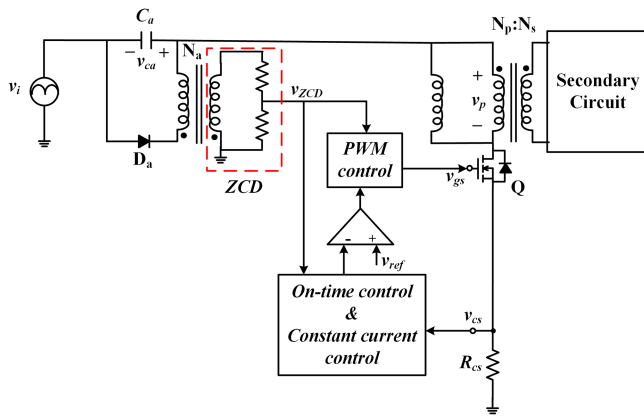
FIGURE 4. The proposed modified forward PFC converter with PSR control.

FIGURE 5. Operation stages. (a) Stage I. (b) Stage II. (c) Stage III.

auxiliary winding is adopted to fulfill the critical conduction mode (CrM) operation. When the auxiliary winding current drops to zero, the change of the auxiliary winding voltage will generate the V$_{\text{oturn-on}}$ signal for the switch Q. The reference voltage, v_{ref}, determines the on-time duration of the constant on-time control. Also, the LED constant current control is achieved by detecting the peak values of the primary-side current. It is worth mentioning that the dimming function can be accomplished by changing v_{ref} to adjust the constant on-time duration to regulate the peak values of the primary-side current. Eventually, different levels of constant output currents can be achieved to fulfill the dimming feature of LED lighting applications.

The circuit operation of the modified forward PFC converter can be categorized into three operation stages according to the status of the power switch Q and the output inductor L_o. The auxiliary winding N$_a$ of the AVS is designed for the CrM operation, which is a condition to achieve remanence resetting. The output inductor, L_o, can operate at the discontinuous conduction mode (DCM) or the continuous conduction mode (CCM) depending on the load conditions.

The equivalent circuits for different operation stages, showing key component currents, are illustrated in Fig. 5, while theoretical voltage and current waveforms of key components are depicted in Fig. 6. The transformer turns ratios among different windings are defined as:

$$n_f = \frac{N_S}{N_p}. \tag{1}$$

$$n_{af} = \frac{N_a}{N_p}. \tag{2}$$

The description of different operation stages will be introduced in the following. It should be mentioned that before entering *Stage I*, the magnetic energy stored in transformer T is fully released to the AVS because of the designed CrM operation of the auxiliary winding N$_a$.
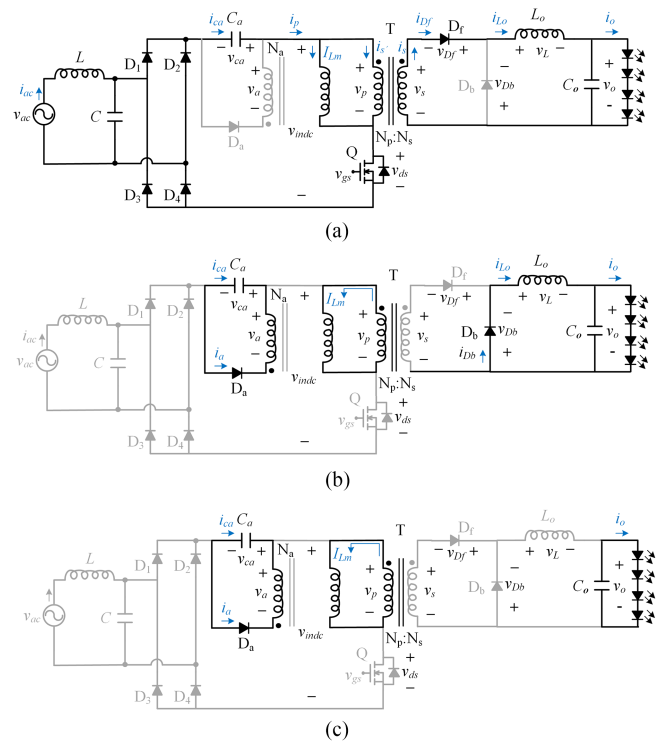
A. STAGE I: T$_0$ < T < T$_1$

Stage I begins when Q is turned on, as shown in Fig. 5(a). In this stage, the diode D$_f$ is forward-biased to deliver the power from the primary side to the secondary side. The primary winding voltage, v_p, on T is the sum of the series-connected input voltage v_{ac} and AVS capacitor voltage v_{ca}. The secondary side voltage of T, v_s, is $(v_i + v_{ca})n_f$, which is designed to be larger than the output voltage v_o to ensure the input current continuity for achieving high PF. As shown in Fig. 6(a) and (b), the increasing current i_P during *Stage I* is composed of the magnetizing current, i_{Lm}, and the reflected secondary current, i_s'. Meanwhile, the capacitor C_a is discharged by i_P, and the output inductor current i_{Lo} is increasing linearly because of the positive inductor voltage v_L. *Stage I* ends when Q is turned off.

B. STAGE II: T$_1$ < T < T$_2$

As Q is turned off at the beginning of *Stage II*, the diodes D$_a$ and D$_b$ are forward-biased. N$_a$ and D$_a$ provide a path to reset the remanence of T while charging the AVS capacitor C_a. The energy stored inside the output inductor L_o is released to the load via the freewheeling diode D$_b$. As shown in Fig. 6(b), both i_{Lm}, i_{Lo}, and i_a are decreasing linearly by assuming the switching frequency, f_s, is much higher than the line frequency and the capacitor ripple voltages are neglected.

This stage ends when the decreasing reset winding current i_a reaches zero. Then, the power switch Q will be turned on again and the operation stage goes back to *Stage I*. However,
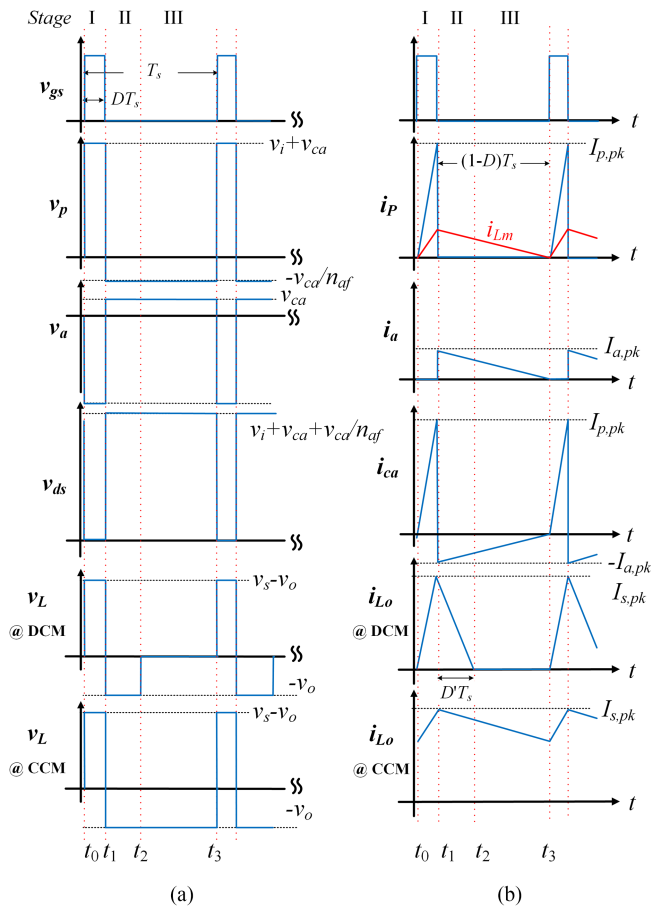
FIGURE 6. Theoretical waveforms on the key components. (a)The voltage waveforms. (b) The current waveforms.

FIGURE 7. The waveforms of the input ac voltage v_{ac}, ac current i_{ac}, and the rectified input voltage v_{indc} during the positive half cycle of the ac mains.

FIGURE 8. Magnified waveforms of i_P, i_{ac}, and v_{indc} within the *Area*1 of Fig. 7.

if the decreasing output inductor current i_{Lo} is still higher than zero at the end of *Stage II*, then the L_o is operated at CCM. Otherwise, the L_o is operated at DCM and the operation will enter *Stage III*.

C. STAGE III: T$_2$ < T < T$_3$

In *Stage III*, the decreasing i_a continues to charge C_a of the AVS. Since the output inductor current, i_{Lo}, has been dropped to zero and the L$_o$ is operated at DCM, both D$_f$ and D$_b$ are turned off. The output LEDs are supplied by the output capacitor C_o only. Once i_a declines to zero, which indicates the remanence has been reset completely, the switch Q will be turned on again, and the operation goes back to *stage I*.

IV. ANALYSIS AND DESIGN CRITERIA

To simplify the mathematical equation derivation of the critical parameter design, the following assumptions are made. (1) the AVS capacitor C_a and the output capacitor C_o are large enough so that v_{ca} and v_o are constant in a line period; (2) the integrated transformer T has negligible leakage inductance and has the turns ratios of n_f and n_{af}.

Fig. 7 illustrates waveforms of the input ac voltage v_{ac}, ac current i_{ac}, and the rectified input voltage v_{indc} during the
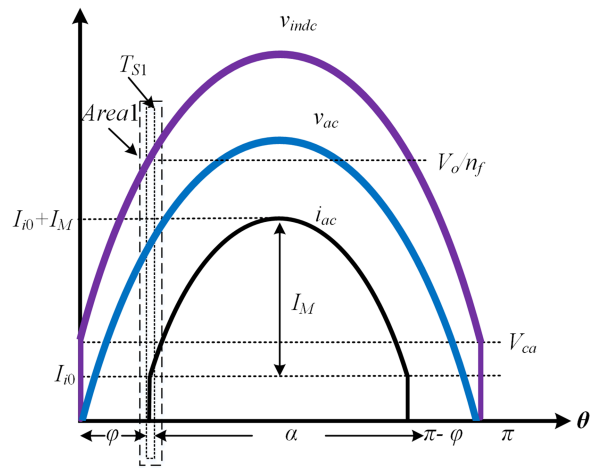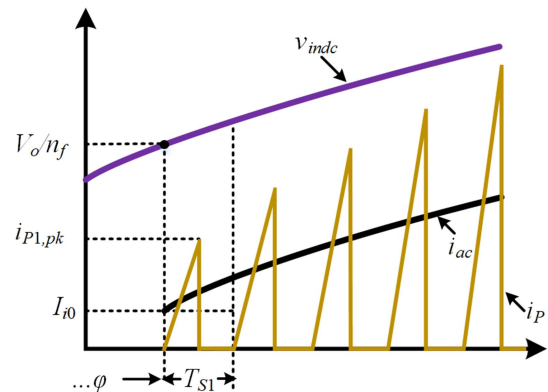
positive half cycle of the ac mains. Because v_{indc} is the summation of the rectified input ac voltage and the AVS voltage, the waveform of the v_{indc} is the same as the input voltage v_{ac} with a dc offset v_{ca}. When v_{indc} reaches the value of the reflected output voltage, v_o/n_f, from the secondary side, the input current i_{ac} starts to conduct at the starting angle φ with an initial value of I_{i0}. The i_{ac} has an amplitude of I_M, which is related to the output power, and its peak value becomes $I_{i0} + I_M$. The i_{ac} drops to zero when the value of v_{indc} is less than v_o/n_f at the moment of $(\pi - \varphi)$ due to the symmetry of the sinusoidal function. The conduction angle α is defined as the time between φ and $(\pi - \varphi)$.

The initial current I_{i0} shown in Fig. 7 is the averaged value of primary winding current i_P during the first switching period, T_{S1}, right after the starting angle φ. Key waveforms of i_P, i_{ac}, and v_{indc} within *Area*1 of Fig. 7 are magnified and shown in Fig. 8. The primary winding current i_P increases linearly when switch Q is turned on. It reaches the peak value $i_{P1,pk}$ right before Q is turned off. The pulsating i_P is filtered and

averaged by the commonly used input LC filter to achieve a smooth input current i_{ac}.

A. THD EVALUATION

The proposed modified forward PFC converter with the AVS can mitigate the dead zone of the input current to improve the current THD and comply with international standards, such as the EN/IEC 61000-3-2 Class C or the ANSI C82.77.

The formula of input current THD can be expressed in (3), where $I_{ac,rms}$ is the root-mean-square (rms) values of i_{ac} and $I_{ac1,rms}$ is the rms value of the fundamental component of i_{ac}.

$$\text{THD} = \sqrt{\left(\frac{I_{ac,rms}}{I_{ac1,rms}}\right)^2 - 1} \tag{3}$$

As shown in Fig. 7, i_{ac} is a sinusoidal waveform with the amplitude I_M because of the PFC control function. Due to the feature of the inserted AVS, the conduction angle φ and the initial current I_{i0} should be included. Therefore, the input current can be expressed as:

$$i_{ac} = I_M (\sin\theta - \sin\varphi) + I_{i0}. \tag{4}$$

From (4), the rms value of i_{ac} can be expressed:

$$I_{ac,rms} = \sqrt{\frac{1}{\pi} \int_{\varphi}^{\pi-\varphi} [I_M (\sin\theta - \sin\varphi) + I_{i0}]^2 d\theta}. \tag{5}$$

By solving the integral equation in (5), $I_{ac,rms}$ can be rewritten as:

$$I_{ac,rms} = \sqrt{\frac{\frac{\alpha}{\pi}\left[\frac{1}{2}I_M^2 + (I_M\sin\varphi - I_{i0})^2\right]}{-\frac{I_M}{\pi}\cos\varphi\,(3I_M\sin\varphi + 4I_{i0})}}. \tag{6}$$

To calculate the input current THD expressed in (3), the amplitude of the fundamental component of i_{ac} needs to be derived, too. By following the mathematical derivation presented in the appendix section of this paper, the rms value of the fundamental component of input current can be obtained:

$$I_{ac1,rms} = \frac{I_M}{\sqrt{2}\pi}(\alpha + \sin2\varphi) + \frac{4}{\sqrt{2}\pi}\cos\varphi\,(I_{i0} - I_M\sin\varphi). \tag{7}$$

Although the input current THD can be calculated by using (3), (6), and (7), parameters φ, α, I_M, and I_{i0}, need to be determined first.

B. PARAMETER DERIVATION

As shown in Fig. 7, the starting angle φ occurs at the moment when the v_{indc}, which is the sum of v_{ac} and V_{ca}, equals to the reflected output voltage, V_o/n_f, and can be obtained as:

$$\varphi = \sin^{-1}\left[\frac{\left(\frac{V_o}{n_f}\right) - V_{ca}}{V_{ac}}\right]. \tag{8}$$

Because of the symmetrical circuit operation during the half ac mains cycle shown in Fig. 7, the conduction angle α can be expressed:

$$\alpha = \pi - 2\varphi. \tag{9}$$

The amplitude of input current I_M is related to the input power P_i, which can be calculated by (10) during the input current conduction period from φ to $(\pi-\varphi)$.

$$P_i = \frac{1}{\pi} \int_{\varphi}^{\pi-\varphi} v_{ac} \times i_{ac} d\theta. \tag{10}$$

By assuming a sinusoidal input voltage and plugging (4) into (10), the input power P_i can be expressed as:

$$P_i = \frac{1}{\pi} \int_{\varphi}^{\pi-\varphi} V_{ac}\sin\theta\,(I_M\sin\theta - I_M\sin\varphi + I_{i0})\,d\theta \tag{11}$$

By solving (11), the following mathematical equation for P_i can be obtained:

$$P_i = \frac{V_{ac}I_M}{2\pi}[\alpha + \sin2\varphi - 4\sin\varphi\cos\varphi] + \frac{2V_{ac}}{\pi}I_{i0}\cos\varphi. \tag{12}$$

Eventually, from (12) the I_M can be expressed as:

$$I_M = \frac{2\pi\frac{P_i}{v_{ac}} - 4I_{i0}\cos\varphi}{\alpha + \sin2\varphi - 4\sin\varphi\cos\varphi}. \tag{13}$$

As illustrated in Fig. 8, the value of I_{i0} is equal to the average current of i_P in the first switching period, T_{S1}, after the starting angle φ. In the first switching period, the secondary side voltage v_s is slightly higher than or almost equal to the output voltage v_o. Therefore, the output inductor voltage v_L is nearly zero which leads to a negligible inductor current i_L. Eventually, the secondary side current can be neglected, and the primary side current i_{P1} is equal to the magnetizing current. Therefore, the following equation can be obtained:

$$I_{i0} = i_{P1,avg} = \frac{1}{T_{s1}}\left(\frac{i_{P1,pk}DT_{s1}}{2}\right) = \frac{D^2V_o}{2f_sL_mn_f}. \tag{14}$$

In the derivation of (14), $i_{P1,pk}$ is substituted by (15) because of the CrM operation.

$$i_{P1,pk} = \frac{(V_i + v_{ca})DT_{S1}}{L_m} = \frac{V_oDT_{s1}}{L_mn_f}. \tag{15}$$

It should be noticed that the parameters, n_f and L_m, in (14) are designed according to the circuit specifications.

The proposed AVS utilizes the residual flux energy to charge the capacitor C_a using the fashion of flyback CrM operation. Therefore, the turns ratio n_{af} of the auxiliary winding has constraints related to the maximum duty ratio, D_{max}, and the transformer's primary side voltage V_o/n_f due to the current of N_a must decrease to zero at the end of the switching cycle. It should be mentioned that the D_{max} of constant on-time control occurs at the very first switching cycle after the starting angle φ because of the shortest turn-off time. Also, during the D_{max} switching cycle, the primary side voltage of transformer T equals V_o/n_f when the switch is on or v_{Ca}/n_{af} when the switch is off and v_i is close to zero. Eventually, the following equation

can be obtained:

$$n_{af} = \frac{V_{ca}}{V_o/n_f} \times \frac{1 - D_{max}}{D_{max}} \leq 1. \tag{16}$$

On the other hand, the minimum turns ratio $n_{af,\min}$ of the transformer can be expressed as:

$$n_{af,\min} = \frac{V_{Ca}}{V_o/n_{f,\min}} \times \frac{1 - D_{\max}}{D_{\max}} \tag{17}$$

On the other hand, to achieve higher efficiency for low power applications, the output inductor L_o is designed to operate in DCM. Because the output inductor current must return to zero for the DCM operation, the value of L_o should be constrained by the maximum duty D_{max} of the constant on-time control strategy, which is accompanied by a minimum reflected input voltage from the primary side of the transformer. The maximum turns ratio $n_{f,max}$ of the transformer can be determined as shown in (18) by using the voltage-second balance theorem of the operation condition under the minimum primary side voltage and the maximum duty ratio D_{max} of the constant on-time control.

$$\left(V_{ac,min}\sin\varphi + V_{ca}\right)n_{f,max}D_{max} = V_o \tag{18}$$

where $V_{ac,min}$ is the amplitude of the minimum rms value of the input ac voltage. Therefore, the maximum turns ratio $n_{f,\max}$ of the transformer can be determined as:

$$n_{f,max} = \frac{V_o}{\left(V_{ac,min}\sin\varphi + V_{ca}\right)D_{max}} \tag{19}$$

On the contrary, the minimum turns ratio $n_{f,\min}$ of the transformer can be determined by the demanded starting angle φ. As shown in Fig. 7, the value of v_{indc} must be larger than V_o/n_f for the proposed AVS to participate the circuit operation after the starting angle φ. From (8), the minimum turns ratio $n_{f,\min}$ of the transformer can be derived as:

$$n_{f,min} = \frac{V_o}{\left(V_{ac,min} + V_{ca}\right)} \tag{20}$$

From (16) and (19), the following equation for $D_{\max}$ can be derived:

$$D_{max} \geq \frac{-V_{ca} + \sqrt{V_{ca}^2 + 4V_{ca}\left(V_{ac,min} + V_{Ca}\right)}}{2\left(V_{ac,min} + V_{ca}\right)}. \tag{21}$$

The magnetizing inductance L_m of the transformer is designed according to the averaged secondary current of the AVS. From Fig. 5, the average value of the transformer's magnetizing inductance current i_{Lm} can be derived as:

$$I_{Lm,avg} = \frac{(v_{ac} + v_{ca})D^2}{2L_m f_s}. \tag{22}$$

According to the design criteria shown in (16), (19), and (20), it is understandable the design of the transformer turns ratio n_f and n_{af} are related to the circuit specifications and the AVS voltage V_{ca}. Theoretically, the V_{ca} voltage will be automatically regulated based on energy flow of the output power and discharged magnetizing inductance. Also, the transformer

TABLE 1. Specifications of the Prototype LED Driver

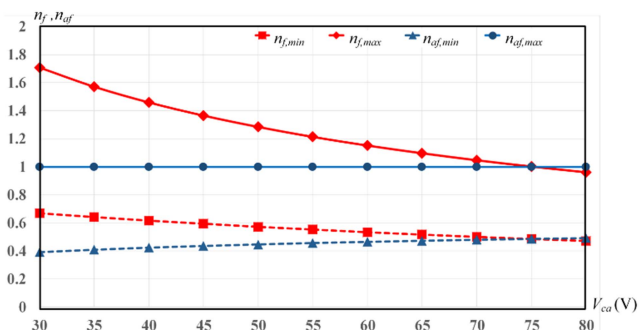|	
Universal input voltage, v_{ac}	90 ~ 264 V_{ac}
Rated Power, P_O	80 W
Output voltage, V_o	80 V
Rated output current, I_o	1 A

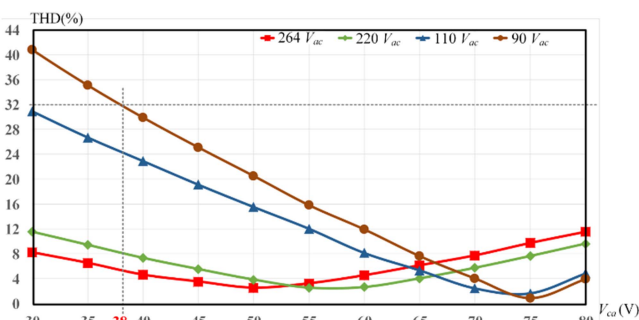**FIGURE 9.** Relationship between the turn ratio limitations and the V_{ca}.

FIGURE 10. Relationship between THD and V_{ca} with different input voltages.

turns ratio will affect the V_{ca} voltage level which will affect the THD current eventually. To verify the performance of the proposed circuit topology and the design criteria, a prototype LED driver with the specifications shown in Table 1 was built and tested. According to the derived equations from (16), (19), and (20), Fig. 9 illustrates the design limitations of n_f and n_{af} for different V_{ca} under the specification shown in Table 1.

Consequently, based on the derived (5), (6), (13), and (14), the input current THD of the proposed modified PFC converter can be determined. For the prototype converter with the specifications shown in Table 1, the calculated input current THDs versus different AVS capacitor voltages V_{ca} under various input voltages are shown in Fig. 10. For the prototype LED driver to comply with the THD limitation in ANSI C82.77 standard, which is less than 32%, V_{ca} would be set higher than 38 V. As the V_{ca} increases, the input current THD

TABLE 2. Specifications and Key Parameters of the Proposed LED Driver

Universal input voltage, V_{ac}	$90 \sim 264\ V_{ac}$
Line frequency, f_{ac}	60 Hz
Output voltage, V_o	80 V
Rated output current, I_o	1 A
Average voltage of AVS, V_{ca}	65 V
Magnetic inductance of T, L_m	750 µH
Primary winding turns, N_p	25
Secondary winding turns, N_s	19
Auxiliary winding turns, N_a	15
Output inductor, L_o	75 µH
transformer turns ratios, n_f	0.76
transformer turns ratios, n_{af}	0.6
AVS capacitance	2.2 µF x 3
Output capacitance	330 µF x 2
Power switch, Q	AOT42S60L
Diodes, D_f and D_b	DPG20C300PN-ND
Diode, D_a	MUR860

can be reduced by following the design of the output inductor and the transformer presented in this paper.

V. EXPERIMENTAL VERIFICATION

A prototype LED driver with the specifications shown in Table 2 was designed and tested with the universal ac voltage range, 90 V_{ac} to 264 V_{ac}, and 60 Hz line frequency. The voltage and current ratings of the LED lamp are 80 V and 1 A, respectively. The simple primary side regulation (PSR) is adopted for circuit simplicity. The LED driver is controlled by the analog IC RT7306 which adopts the constant on-time CrM control to achieve the PFC and constant output current feature. The RT7306 is a variable switching frequency control IC due to the CrM operation and the switching frequency range from 20 kHz to 117 kHz. The LED driver is operated at the boundary conduction mode to achieve high power efficiency.

Based on the curves shown in Fig. 10, the AVS voltage is designed as 65 V to minimize the THD for universal input voltages. From (21) with $V_{ca} = 65$ V and $V_{ac,min} = 90\sqrt{2}$ V, the value of $D_{max} = 0.47$ can be obtained. From Fig. 9 at $V_{ca} = 65$ V, the ranges of turn ratios of the transformer are:

$$0.52 < n_f < 1.10. \quad (23)$$

$$0.47 < n_{af} < 1.00. \quad (24)$$

According to those numbers of winding turns shown in Table 2, the transformer turns ratios n_f and n_{af} are 0.76 and 0.6, respectively, which meet the constrains shown in (23) and (24).

The input current i_{ac}, output voltage v_o and AVS voltage V_{ca} under 110 V_{ac} and 220 V_{ac} input voltages are shown in Fig. 11. The sinusoidal input currents i_{ac} illustrate the demanded PFC function for the universal input voltage range while the output voltage is well-regulated at 80 V. Also, it is found that the stored magnetizing inductance energy increases slightly as the
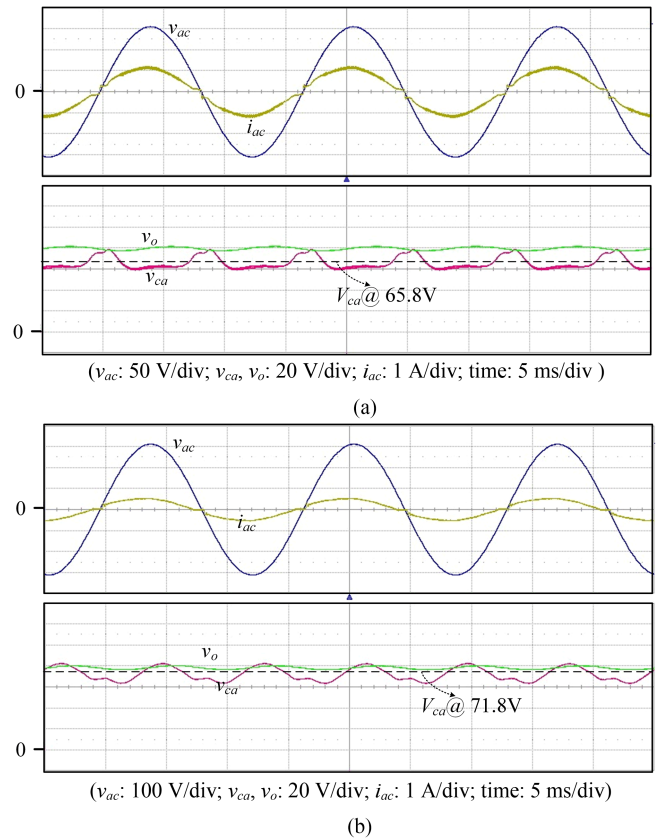

(v_{ac}: 50 V/div; v_{ca}, v_o: 20 V/div; i_{ac}: 1 A/div; time: 5 ms/div)

(a)

(v_{ac}: 100 V/div; v_{ca}, v_o: 20 V/div; i_{ac}: 1 A/div; time: 5 ms/div)

(b)

FIGURE 11. Key waveforms of input voltage v_{ac}, input current i_{ac}, output voltage v_o, and AVS voltage V_{ca} under different ac line voltage conditions. (a) 110 V_{ac} (b) 220 V_{ac}.
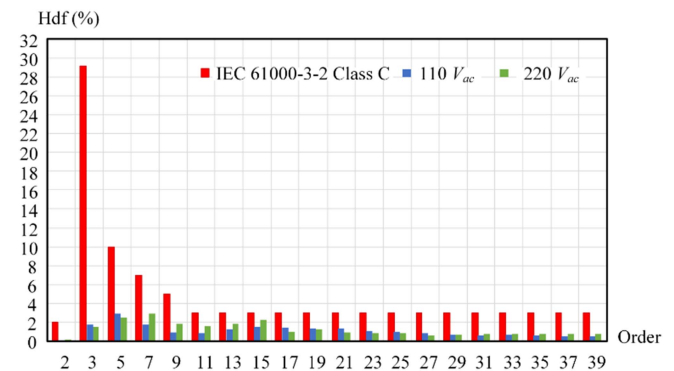

FIGURE 12. The IEC61000-3-2 class C standard and measured input current harmonics under different ac line voltage conditions.

input voltage increases, so the averaged AVS voltage V_{ca} is 65.8 V at low line voltage 110 V_{ac} while it is 71.8 V at high line voltage 220 V_{ac}. The measured input current harmonics under different input voltage conditions are shown in Fig. 12.

The standard of IEC61000-3-2 class C is also listed in Fig. 12 to verify the compliance of input current harmonics. The measured values of THD are 5.84% and 6.77% for line voltages 110 Vac and 220 Vac, respectively. On the other hand,
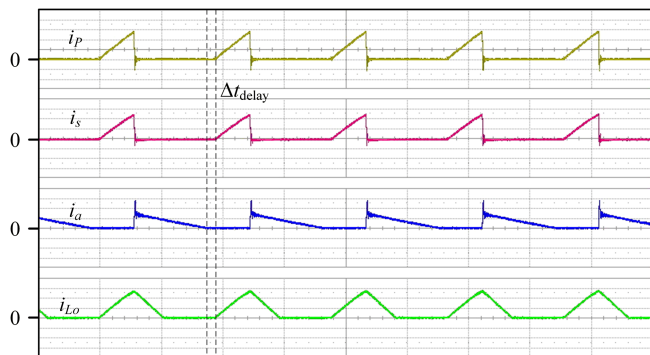
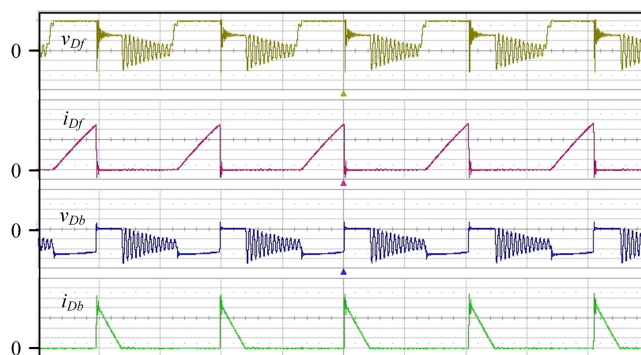**FIGURE 13.** Key current waveforms of transformer T and output inductor L_b.

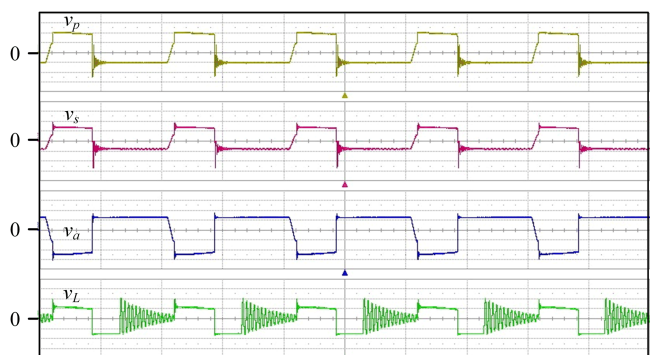**FIGURE 15.** The voltage and current waveforms of D_f and D_b.

FIGURE 14. Key voltage waveforms of transformer T and output inductor L_b.
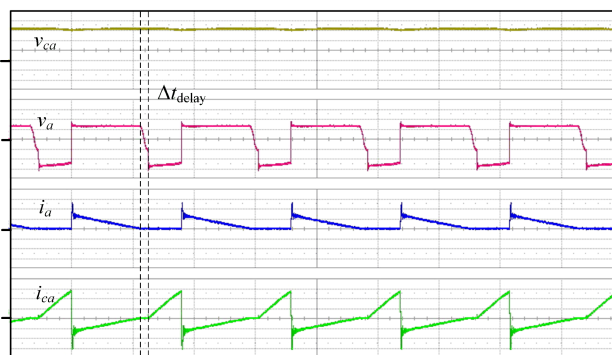

FIGURE 16. The voltage and current waveforms of the AVS.

the measured power conversion efficiencies are 91.38% and 92.31% under input voltages 110 V_{ac} and 220 V_{ac}, respectively.

Fig. 13 shows the steady-state switching current waveforms. When the power switch Q is turned on, transformer currents, i_P, and i_s, and output inductor current i_{Lo} increase linearly. When Q is turned off, i_{Lo} decreases linearly to zero before the next switching begins, so the expected DCM operation of the output inductor is achieved. The stored energy in the magnetic inductance will be transferred to the AVS via the auxiliary winding with charging current i_a. Due to the boundary conduction mode operation, the next cycle begins when i_a reaches zero plus an inherent time delay Δt_{delay} caused by the control IC.

The corresponding voltage waveforms of the transformer and output inductor are shown in Fig. 14. Due to the on or off status of the power switch Q, the polarity of those voltage waveforms will change accordingly. It should be mentioned that as the i_{Lo} decreases to zero, a resonance path is formed by the transformer's leakage inductance and the parasitic capacitance of D_f and D_b. The measured resonant frequency is 1.57 MHz. The voltage and the current waveforms of D_f and D_b are shown in Fig. 15.

Fig. 16 shows the measured voltage and current waveforms of the AVS. When the switch Q is turned on, the AVS
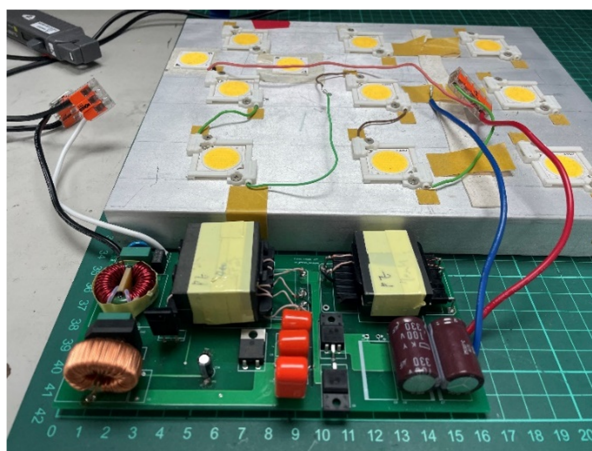

FIGURE 17. The prototype modified forward PFC converter and LED modules.

capacitor current i_{ca} is positive and equal to the transformer current for energy delivery. The auxiliary winding voltage v_a is negative to block the diode D_a. Once the switch is turned off, the auxiliary winding starts to charge the AVS capacitor so i_a is equal to negative i_{ca}. Although the AVS capacitor voltage V_{ca} remains a constant value with negligible switching ripple, it should be mentioned that the AVS capacitor has an inevitable double-line frequency voltage ripple due to the ac input current magnitude variation. The picture of prototype

modified forward PFC converter and LED modules is shown in Fig. 17.

VI. CONCLUSION

A modified forward PFC converter for LED lighting applications is proposed in this paper. The proposed circuit topology employs an AVS which can eliminate the dead zone of the ac input current to achieve a low current THD and a high power factor. The operation principle of the proposed LED driver is presented followed by the mathematical derivation of the parameter design. The commonly used constant on-time control and primary side regulation control can be easily adopted to control the proposed converter. An 80 W prototype LED driver is built and tested under the universal input voltage range. The experimental waveforms verify the performance of the proposed modified forward PFC converter. The measured power factor is 0.99 and input current THD is 5.84% when input voltage is 110 V_{ac}. For 220 V_{ac} input ac voltage, the measured power factor is 0.97 and input current THD is 6.77%. The measured efficiency of the prototype without component optimization is over 91 % for universal input voltage operation.

APPENDIX

A. THE DERIVATION OF $I_{AC,RMS}$

(A.1)–(A.2) shown at the bottom of this page.

B. THE DERIVATION OF $I_{AC,RMS\,1}$

Based on the Fourier Series theorem, the periodic ac line current can be expressed as:

$$i_{ac} = i_{dc} + \sum_{n=1}^{\infty} (a_n cos n\theta + b_n sin\, n\theta)$$

where

$$a_n = \frac{2}{\pi} \int_{\varphi}^{\pi-\varphi} i_{ac} \cos n\theta d\theta \text{ and } b_n = \frac{2}{\pi} \int_{\varphi}^{\pi-\varphi} i_{ac} sin\, n\theta d\theta$$

Since i_{ac} is odd-function symmetry and has no dc component, coefficients a_n and i_{dc} are zero. Eventually, the rms value of the fundamental component (n = 1) of input ac line current can be expressed as:

$$\begin{aligned}
I_{ac,rms1} &= \frac{2}{\sqrt{2}\pi} \int_{\varphi}^{\pi-\varphi} i_{ac} \sin\theta d\theta \\
&= \frac{2}{\sqrt{2}\pi} \left[\int_{\varphi}^{\pi-\varphi} [I_M (\sin\theta - \sin\varphi) + I_{i0}]\, \sin\theta d\theta \right] \\
&= \frac{2}{\sqrt{2}\pi} \left[I_M \int_{\varphi}^{\pi-\varphi} \sin^2\theta d\theta - I_M \sin\varphi \int_{\varphi}^{\pi-\varphi} \sin\theta d\theta) \right. \\
&\quad \left. + I_{i0} \int_{\varphi}^{\pi-\varphi} \sin\theta d\theta \right] \\
&= \frac{2}{\sqrt{2}\pi} \left[I_M \left(\frac{\pi}{2} - \varphi + \frac{-\sin(2\pi - 2\varphi) + \sin(2\varphi)}{4} \right) \right.
\end{aligned}$$

$$I_{ac,rms} = \sqrt{\frac{1}{\pi} \int_{\varphi}^{\pi-\varphi} [I_M (sin\theta - sin\varphi) + I_{i0}]^2 d\theta} \tag{A.1}$$

$$\begin{aligned}
&= \sqrt{\frac{1}{\pi} \int_{\varphi}^{\pi-\varphi} [I_M^2 (\sin\theta - \sin\varphi)^2 + 2I_M I_{i0} (\sin\theta - \sin\varphi) + I_{i0}^2] d\theta} \\
&= \sqrt{\frac{1}{\pi} \left[I_M^2 \int_{\varphi}^{\pi-\varphi} [\sin^2\theta - 2\sin\theta\sin\varphi + \sin^2\varphi] d\theta + 2I_M I_{i0} \int_{\varphi}^{\pi-\varphi} [(\sin\theta - \sin\varphi)] d\theta + I_{i0}^2 \int_{\varphi}^{\pi-\varphi} d\theta \right]} \\
&= \sqrt{\frac{1}{\pi} \left\{ I_M^2 \left[\left(\frac{\pi}{2} - \varphi + \frac{-\sin(2\pi-2\varphi)+\sin(2\varphi)}{4} \right) - 2 (\sin\varphi (-\cos(\pi-\varphi) + \cos\varphi)) + (\pi - 2\varphi)\sin^2\varphi \right] \right.} \\
&\quad \overline{+2I_M I_{i0} [(-\cos(\pi-\varphi) + \cos\varphi) - \sin\varphi(\pi-2\varphi)] + I_{i0}^2 (\pi - 2\varphi)\}} \\
&= \sqrt{\frac{1}{\pi} [I_M^2 [\frac{1}{2}(\pi-2\varphi) + \frac{1}{2}\sin(2\varphi) - 4\sin\varphi\cos\varphi + (\pi-2\varphi)\sin^2\varphi] + 4I_M I_{i0}\cos\varphi - 2I_M I_{i0}\sin\varphi(\pi-2\varphi) + I_{i0}^2(\pi-2\varphi)]} \\
&= \sqrt{\frac{1}{\pi} [\frac{1}{2}I_M^2(\pi-2\varphi) + I_M^2(\pi-2\varphi)\sin^2\varphi - 2I_M I_{i0}\sin\varphi(\pi-2\varphi) + I_{i0}^2(\pi-2\varphi) + \frac{1}{2}I_M^2\sin(2\varphi) - 4I_M^2\sin\varphi\cos\varphi + 4I_M I_{i0}\cos\varphi]} \\
&= \sqrt{\frac{1}{\pi} [(\pi-2\varphi)[\frac{1}{2}I_M^2 + I_M^2\sin^2\varphi - 2I_M I_{i0}\sin\varphi + I_{i0}^2] + \frac{1}{2}I_M^2\sin(2\varphi) - 4I_M^2\sin\varphi\cos\varphi + 4I_M I_{i0}\cos\varphi]} \\
&= \sqrt{\frac{1}{\pi} [(\pi-2\varphi)[\frac{1}{2}I_M^2 + (I_M\sin\varphi - I_{i0})^2] + \frac{1}{2}I_M^2[\sin(2\varphi) - 8\sin\varphi\cos\varphi] + 4I_M I_{i0}\cos\varphi]} \\
&= \sqrt{\frac{1}{\pi} [(\pi-2\varphi)[\frac{1}{2}I_M^2 + (I_M\sin\varphi - I_{i0})^2] + \frac{1}{2}I_M^2[2\sin\varphi\cos\varphi - 8\sin\varphi\cos\varphi] + 4I_M I_{i0}\cos\varphi]} \\
&= \sqrt{\frac{1}{\pi} [(\pi-2\varphi)[\frac{1}{2}I_M^2 + (I_M\sin\varphi - I_{i0})^2] - I_M\cos\varphi(3I_M\sin\varphi + 4I_{i0})]} \\
&= \sqrt{\frac{\alpha}{\pi}[\frac{1}{2}I_M^2 + (I_M\sin\varphi - I_{i0})^2] - \frac{I_M}{\pi}\cos\varphi(3I_M\sin\varphi + 4I_{i0})}
\end{aligned}$$

$$\tag{A.2}$$

$$- (I_M \sin \varphi - I_{i0}) (2\cos\varphi) \Bigg]$$

$$= \frac{2}{\sqrt{2}\pi} \left[I_M \left(\frac{1}{2} (\pi - 2\varphi) + \frac{1}{2}\sin(2\varphi) \right) \right.$$

$$\left. - (I_M \sin \varphi - I_{i0}) (2\cos\varphi) \right]$$

$$= \frac{1}{\sqrt{2}\pi} I_M (\alpha + \sin2\varphi) - \frac{4}{\sqrt{2}\pi}\cos\varphi (I_M \sin \varphi - I_{i0})$$

$$= \frac{I_M}{\sqrt{2}\pi} (\alpha + \sin2\varphi) + \frac{4}{\sqrt{2}\pi}\cos\varphi (I_{i0} - I_M \sin \varphi) \tag{A.3}$$

C. THE DERIVATION OF P_I

$$P_i = \frac{1}{\pi} \int_\varphi^{\pi-\varphi} V_{ac} \sin\theta (I_M \sin\theta - I_M \sin\varphi + I_{i0}) d\theta \tag{A.4}$$

$$= \frac{1}{\pi} \int_\varphi^{\pi-\varphi} (V_{ac} \sin\theta I_M \sin\theta) d\theta$$

$$- \frac{1}{\pi} \int_\varphi^{\pi-\varphi} (V_{ac} \sin\theta I_M \sin\varphi) d\theta$$

$$+ \frac{1}{\pi} \int_\varphi^{\pi-\varphi} (V_{ac} \sin\theta I_{i0}) d\theta$$

$$= \frac{V_{ac}I_M}{\pi} \int_\varphi^{\pi-\varphi} \sin^2\theta d\theta - \frac{V_{ac}I_M}{\pi} \sin\varphi \int_\varphi^{\pi-\varphi} \sin\theta d\theta$$

$$+ \frac{V_{ac}I_{i0}}{\pi} \int_\varphi^{\pi-\varphi} \sin\theta d\theta$$

$$= \frac{V_{ac}I_M}{\pi} \left[\frac{\pi}{2} - \varphi + \frac{-\sin(2\pi - 2\varphi) + \sin 2\varphi}{4} \right]$$

$$- \left[\frac{V_{ac}I_M}{\pi} \sin\varphi (-\cos(\pi - \varphi) + \cos\varphi) \right]$$

$$+ \frac{V_{ac}I_{i0}}{\pi} (-\cos(\pi - \varphi) + \cos\varphi)$$

$$= \frac{V_{ac}I_M}{2\pi} [\pi - 2\varphi + \sin 2\varphi] - \left[\frac{V_{ac}I_M}{\pi} \sin\varphi (2\cos\varphi) \right]$$

$$+ \frac{V_{ac}I_{i0}}{\pi} (2\cos\varphi)$$

$$= \frac{V_{ac}I_M}{2\pi} [\alpha + \sin 2\varphi] - \frac{2V_{ac}I_M}{\pi} \sin\varphi \cos\varphi + \frac{2}{\pi} V_{ac}I_{i0} \cos\varphi$$

$$= \frac{V_{ac}I_M}{2\pi} [\alpha + \sin 2\varphi - 4sin\varphi cos\varphi] + \frac{2}{\pi} V_{ac}I_{i0} \cos\varphi \tag{A.5}$$

D. THE DERIVATION OF D_{MAX}

From (16)~(18) with starting angle $\varphi = 90$ and $n_f = n_{f,max}$, the following mathematical equation can be obtained:

$$\frac{V_{ca}}{(V_{ac,min} + V_{ca}) D_{max}} \times \frac{1 - D_{max}}{D_{max}} \le 1$$

$$\Rightarrow V_{ca} (1 - D_{max}) \le (V_{ac,min} + V_{ca}) \times D_m ax^2$$

$$\Rightarrow (V_{ac,min} + V_{ca}) \times D_{max}^2 + V_{ca}D_{max} - V_{ca} \ge 0$$

$$D_{max} = \frac{-V_{ca} + \sqrt{V_{ca}^2 + 4V_{ca} (V_{ac,min} + V_{ca})}}{2 (V_{ac,min} + V_{ca})} \tag{A.6}$$

REFERENCES

[1] L. Araújo, E. Agostini, and C. B. Nascimento, "Single-stage converter based on the Boost-PFC rectifier employing a current-source charge-pump for power LEDs applications," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10571–10583, Mar. 2021.

[2] H. Li, S. Li, and W. Xiao, "Single-phase LED driver with reduced power processing and power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4540–4548, Apr. 2021.

[3] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "Analysis and design of a charge-pump-based resonant AC–DC converter with inherent PFC capability," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 3, pp. 2067–2081, Sep. 2020.

[4] I. Castro, A. Vazquez, M. Arias, D. G. Lamar, M. M. Hernando, and J. Sebastian, "A review on flicker-free AC–DC LED drivers for single-phase and three-phase AC power grids," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10035–10057, Oct. 2019.

[5] H. Wu, S. Wong, and C. K. Tse, "A more efficient PFC single-coupled-inductor multiple-output electrolytic capacitor-less LED driver with energy-flow-path optimization," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9052–9066, Sep. 2019.

[6] Z. P. D. Fonseca, C. B. Nascimento, and A. A. Badin, "Single-stage PFC charge-pump bridgeless converters for LED driver applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12750–12761, Dec. 2022.

[7] A. M. Ammar, F. M. Spliid, Y. Nour, and A. Knott, "A 1-MHz resonant LED driver with charge-pump-based power factor correction," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 5, pp. 5838–5850, Oct. 2021.

[8] *Electromagnetic Compatibility (EMC) - Part 3-2: Limits for Harmonic Current Emissions*, IEC 61000-3-2: 2018, Jan. 2018.

[9] X. Liu, Y. Wang, M. He, Q. Zhou, and X. Meng, "Buck-type single-switch integrated PFC converter with low total harmonic distortion," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6859–6870, Aug. 2021.

[10] Z. Chen, J. Xu, X. Liu, P. Davari, and H. Wang, "High power factor bridgeless integrated buck-type PFC converter with wide output voltage range," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12577–12590, Oct. 2022.

[11] F. Sahlabadi, M. R. Yazdani, J. Faiz, and E. Adib, "Resonant bridgeless buck PFC converter with reduced components and dead angle elimination," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9515–9523, Aug. 2022.

[12] N. Molavi, M. Maghsoudi, and H. Farzanehfard, "Quasi-resonant bridgeless PFC converter with low input current THD," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7965–7972, Jul. 2021.

[13] T. Liu, X. Liu, M. He, S. Zhou, X. Meng, and Q. Zhou, "Flicker-free resonant LED driver with high power factor and passive current balancing," *IEEE Access*, vol. 9, pp. 6008–6017, 2021.

[14] Z. Chen, B. Liu, Y. Yang, P. Davari, and H. Wang, "Bridgeless PFC topology simplification and design for performance benchmarking," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5398–5414, May 2021.

[15] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A family of single-phase hybrid step-down PFC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5271–5281, Jul. 2017.

[16] Y. T. Huang, C. H. Li, and Y. M. Chen, "A modified asymmetrical half-bridge flyback converter for step-down AC–DC applications," *IEEE Trans. Power Electron.,* vol. 35, no. 5, pp. 4613–4621, May 2020.

[17] G. Z. Abdelmessih, J. M. Alonso, and W. T. Tsai, "Analysis and experimentation on a new high power factor off-line LED driver based on interleaved integrated buck flyback converter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4359–4369, Jul./Aug. 2019.

[18] C. R. Lee, W. T. Tsai, and H. S. Chung, "A buck-type power-factor-correction circuit," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 2013, pp. 586–590.

[19] W. T. Tsai, C. R. Lee, P. Y. Chen, and C. T. Pan, "Active buck power factor correction device," U.S. Patent US 9048750 B2, Jun. 2015.

[20] H. Dong, X. Xie, L. Jiang, Z. Jin, and X. Zhao, "An electrolytic capacitor-less high power factor LED driver based on a 'One-and-a-Half stage' forward-flyback topology," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1572–1584, Feb. 2018.

[21] X. Xie, J. Li, K. Peng, C. Zhao, and Q. Lu, "Study on the single-stage forward-flyback PFC converter with QR control," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 430–442, Jan. 2016.

[22] J. H. Lee, J. H. Park, and J. H. Jeon, "Series-connected forward–flyback converter for high step-up power conversion," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3629–3641, Dec. 2011.

[23] H. E. Tacca, "Power factor correction using merged flyback-forward converters," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 585–594, Jul. 2000.

[24] H. Dong, X. Xie, F. Mao, L. Zhang, and Y. He, "A novel primary-side regulation control scheme for CCM and DCM LLC LED driver based on 'Magnetizing current cancellation method," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12223–12237, Nov. 2020.

[25] Y. Chen, C. Chang, and P. Yang, "A novel primary-side controlled universal-input AC–DC LED driver based on a source-driving control scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4327–4335, Aug. 2015.

[26] H. H. Chou, Y. S. Hwang, and J. J. Chen, "An adaptive output current estimation circuit for a primary-side controlled LED driver," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4811–4819, Oct. 2013.

[27] J. Zhang, H. Zeng, and T. Jiang, "A primary-side control scheme for high-power-factor LED driver with TRIAC dimming capability," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4619–4629, Nov. 2012.

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