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Improving Power Density of a Three-Level ANPC Structure Using the Electro-Thermal Model of Inverter and a Modified SPWM Technique

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ABSTRACT Multilevel inverter structures have become an interesting substitute for the well-known two-level inverters in a variety of applications due to their exceptional characteristics when compared to conventional inverters. One major issue regarding multilevel structures is the unequal junction temperature of the switches which deteriorates the power density and increase the cost of the inverter by reducing the maximum achievable output power with a given thermal model and cooling system. Hence, on account of the aggressive goals of power density and cost in a majority of power electronic applications, this article proposes a new technique for reducing the maximum junction temperature of switches in a three-level active neutral-point clamped (ANPC) inverter based on a junction temperature estimation method and a modified SPWM control scheme. This technique can ensure up to a 12% rise in the power density value when compared to basic SPWM techniques with no loss distribution algorithm. Moreover, the suggested approach can be used as a protection stage in the inverter which protects the inverter in transient loads, while allowing for reaching the maximum power capability of the inverter. Finally, the simulations of the proposed technique are validated with experimental results of a 400 V, 20 kW three-level ANPC inverter, controlled by the conventional and proposed techniques.

INDEX TERMS Electric vehicles, junction temperature, multilevel structures, power density, sinusoidal pulse width modulation (SPWM), three-level ANPC inverter.

I. INTRODUCTION

Multilevel inverters (MLIs) have been offered as an interesting replacement for their well-known two-level counterparts in many industrial applications. Their outstanding advantages over the two-level structure are lower voltage and current THD, lower voltage stress over the switches, lower $\frac{dv}{dt}$, and fault-tolerance capability [1]. These exceptional benefits help using faster low-voltage switches in applications with a high voltage DC-link. For instance, as the battery voltage of electric vehicles is getting closer to 1 kV, multilevel structures enable lower-voltage GaN or SiC devices to be used in the inverter structure while ensuring a low $\frac{dv}{dt}$ and high reliability.

Various applications of three-phase inverters have a variety of requirements. However, high power density and low cost are essential to most applications, such as traction inverters [2], [3] in which the power density has become an important criterion where the goal for electric vehicle inverters in 2025 has been set to 100 $\frac{kW}{L}$ which is 87% higher than the former goal for 2020 [4]. Therefore, efforts have been made in both electrical and mechanical design stages of power electronic inverters in many applications.

One major limiting factor for having power-dense power electronic converters is the unequal maximum junction temperature among the power switches. This unequal junction

temperature is a result of first, different energy loss in each switch, and second, unequal case temperatures and unsymmetrical thermal models. This issue needs even more attention in case of multilevel inverters, where the number of switches has increased compared to the conventional structures. In case of a three-level neutral point clamped (NPC) inverter, the number of semiconductor devices has increased from 6 to 18. An NPC inverter suffers from a lack of flexibility in distributing the power loss in the switches. This drawback leads to some switches being the limiting factor for increasing the power rating of the inverter while the other switches are not utilized with their maximum capability [5].

The three-level Active NPC (ANPC) structure, which is the focus of this article, has managed to solve the aforementioned power loss sharing issue by employing two different modulation techniques, called modulation patterns I and II [6], [7]. In pattern I, most of the switching loss is dissipated in the outer switches of each leg. On the other hand, in pattern II modulation scheme, the switching losses are moved to the inner switches. However, employing patterns I or II for the whole period will not address the issue of unbalanced loss since the majority of switching loss is transferred to either outer or inner switches and there is no active balancing algorithm. Therefore, there are some research studies on the methods for employing the best combination of the two patterns, as well as modifying the inverter structure.

In [8] and [9], hybrid ANPC structures are investigated and compared to each other in terms of power loss sharing. In a hybrid structure, inner or outer IGBTs are replaced with SiC MOSFETs with low turn-on/turn-off losses. The proper modulation pattern is then utilized to ensure that the switching loss occurs in the low-loss SiC devices. Although the hybrid structures have proven to increase the power density and decrease the junction temperature gap in certain operating conditions, there is no temperature balancing algorithm which aggravates the temperature gap when the operating condition of the inverter varies.

Another modulating strategy, called double-frequency (DF) modulation, is investigated in [6]. With the DF modulation method, switching events happen evenly among the inner and outer switches. Hence, switching loss is equally distributed. However, the conduction loss is higher in inner switches than in outer switches which turns the inner switches to the inverter's hotspot. There is no temperature balancing algorithm to control the distribution of the instantaneous energy loss in the semiconductors. Also, this method does not consider the inverter's electro-thermal model and unbalance in the case temperatures of the switching devices.

A loss balancing algorithm is proposed in [10], named an adaptive loss distribution (ALD). In this method, the conduction losses of the inner and outer switches are derived based on the operating conditions of the inverter, mainly the power factor and modulation index. Based on the gap between the switches' conduction losses, a switching loss distribution ratio is derived which controls the modulation modes. Although this method proves to be more efficient in temperature balancing, its drawback is that the thermal models of the switch and inverter are not employed for temperature estimation. Without utilizing the online temperature estimation, although the losses can be distributed evenly over a period of time, the gap between instantaneous junction temperatures in transient conditions can not be reduced effectively. Another drawback of the proposed modulation method is that the difference in the case temperatures of the switches in an actual inverter leg is not taken into account.

A more advanced junction temperature balancing is proposed in [11] and [12], where the switch foster thermal model is employed for online junction temperature estimation. The idea in [11] is to optimize the distribution of the power loss in each switching cycle by using the calculated instantaneous power loss and the foster equivalent network. Although this method is more effective than the previously discussed approaches, its main drawback is the extremely large computations required during each switching period which makes it impractical to go to high switching frequencies, especially when high-level foster networks are employed. The experimental tests in [11] are performed at the low switching frequency of 1 kHz. Also, the variations in the case temperatures of switches in an actual high-power setup are not considered.

Some studies in the literature have proposed model-predictive control (MPC) for the three-level ANPC where junction temperature balancing is added as an additional objective term to the cost function [13], [14]. One major drawback of using this control method for junction temperature balancing is the large computation burden when the temperature estimation is going to happen at each switching cycle.

In this article, an adaptive SPWM technique is proposed for minimizing the hotspot temperature in a three-level ANPC structure. After presenting a loss model for this topology, a thermal model will be presented for the inverter. The electro-thermal model includes two parts. First, the heatsink's model is extracted with some experimental tests, and second, a second-order foster equivalent thermal network is used to estimate the device's junction temperature. The junction temperature estimation is performed in the intervals of T_{th}, to ensure a limited gap between the junction temperatures of the devices. Using this method, the power density of the three-level inverter can be improved considerably without adding any complexity to the inverter hardware. Moreover, an investigation of the sensitivity of the proposed method on the thermal parameters is performed. The presented method is then verified using a 400 V, 20 kW three-level ANPC inverter.

The structure of the article is as follows: The three-level ANPC inverter structure as well as the electro-thermal model is introduced in Section II. The proposed control technique is presented in Section III, where the thermal interval, T_{th}, is calculated first, and then the case and junction temperature estimation method is explained. A sensitivity analysis is performed in Section IV, where the sensitivity of the proposed control technique is evaluated with regard to the uncertainties in thermal parameters. The simulation results which compare the proposed technique to the previous methods are presented in Section V. These results are validated in Section VI with a

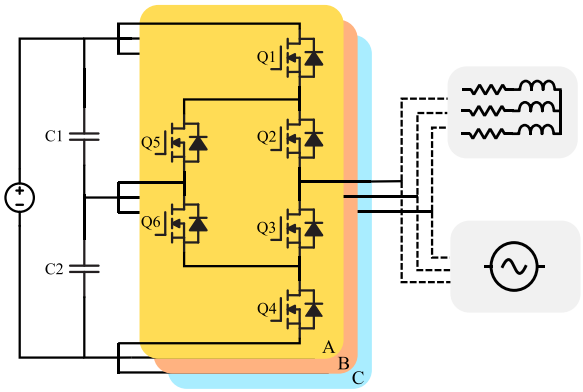

FIGURE 1. The structure of a three-phase, three-level ANPC.

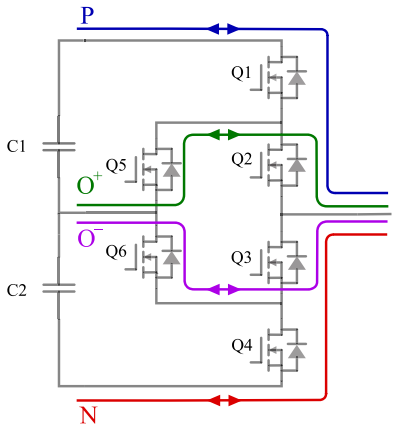

FIGURE 2. Different operating modes in one leg of ANPC inverter.

400 V, 20 kW experimental setup in different load conditions. Finally, the conclusion is presented in Section VII.

II. INVERTER STRUCTURE AND ELECTRO-THERMAL MODEL

The structure of a three-phase, three-level ANPC inverter is shown in Fig. 1. Two clamping diodes in each leg of an NPC inverter are replaced with active switches in a three-level ANPC structure. This replacement gives the converter the flexibility to choose the switching state "O" in each leg between two options, "O^+" and "O^-" as shown in Fig. 2. Utilizing either of the options for the transitions to/from "O" state does not affect the output voltage and current waveforms since the output is only responding to the state of the legs, not the transitions. However, selecting the proper "O" state can alter the energy dissipation in the switches of each leg. In this section, first, the effect of each switching state "O" on loss distribution is investigated. Then, a loss model for three-level ANPC is derived which is used in the following sections for junction temperature estimation. Additionally, the thermal model of the inverter is investigated.

A. POWER LOSS DISTRIBUTION

In a single leg of a three-level ANPC inverter, which is shown in Fig. 2, "O^+" switching state is realized through Q_2 and Q_5 switches. On the other hand, "O^-" switching state can be achieved through Q_3 and Q_6 switches. In this article, the term "Pattern I" is used when the outer switches (Q_1 and Q_4 in leg A) are used for switching to/from "O" state. On the other hand, the term "Pattern II" refers to inner switching (Q_2 and Q_3 in leg A). Hence, considering a transition from state "P" to state "O" in leg A with pattern II, Q_2 must turn off and Q_3 must turn on with the appropriate deadtime. Then, the current path is redirected from Q_1 and Q_2 to Q_3 and Q_6. A reverse process can be used for transition from state "O" to state "P". In transitions between states "P" and "O," the switching energies is dissipated in Q_1 and Q_5 if pattern I is utilized and in Q_2 and Q_3 if pattern II is employed. The same analysis can be performed for transitions from state "N" to state "O".

As discussed briefly in the introduction, this feature in a three-level ANPC structure results in extra flexibility in loss distribution. To have a smart junction temperature minimization, the loss distribution must be in accordance with the junction temperatures of the switches. Therefore, the electro-thermal model of the inverter is essential for an effective minimization of junction temperatures. Utilizing the converter's thermal model avoids adding complexity and cost to the hardware since it does not require the addition of any temperature sensors to measure the case temperatures.

B. LOSS MODEL

Derivation of a loss model is essential for estimating the loss values of the MOSFETs in each operating condition. A precise loss model gives accurate loss values while increasing the required calculations in the controller which makes it impractical. Therefore, a trade-off between higher computational burden and higher inaccuracy is inevitable.

1) CONDUCTION LOSS

The conduction loss in a power MOSFET can be calculated with the well-known resistive loss equation, (1).

$$P_{con,Q_x} = R_{on,Q_x} \times \left(I^2_{rms,Q_x}\right) \tag{1}$$

The main elements in determining the conduction loss of MOSFETs are the on-resistance, $R_{ds,on}$, and RMS current, I_{rms}. Variations of the resistance versus junction temperature can be approximated by a quadratic equation as (2). The appropriate coefficients, ρ_1, ρ_2, and ρ_3, can be extracted using MATLAB curve fitting tool and the $R_{ds,on}$ graph in the MOSFET datasheet.

$$R_{on,pu}(T) = \rho_1 T^2 + \rho_2 T + \rho_3 \tag{2}$$

To calculate the RMS current of the MOSFET, two approaches can be taken based on the output fundamental frequency of the inverter, f_o. If the time period of the output waveform, $\frac{1}{f_o}$, is larger than the thermal time constant of the junction temperature, the RMS current in each fundamental period can be used as a constant current value for junction

TABLE 1. Conduction Energy Losses, E_{con}, in a Period of T_L in Leg a Switches

Conduction Loss for $0 < D_a < 1$		
Switch	Pattern I	Pattern II
Q1	$D_a * R_{ds,1} * I^2 * T_L$	$D_a * R_{ds,1} * I^2 * T_L$
Q2	$R_{ds,2} * I^2 * T_L$	$D_a * R_{ds,2} * I^2 * T_L$
Q3	0	$(1 - D_a) * R_{ds,3} * I^2 * T_L$
Q4	0	0
Q5	$(1 - D_a) * R_{ds,5} * I^2 * T_L$	0
Q6	0	$(1 - D_a) * R_{ds,6} * I^2 * T_L$

temperature estimation. This approach is most useful in estimating the temperature in different locations on the heatsink which have a large thermal time constant. Equation (3) is used to derive the RMS current in one fundamental period for each switch in leg A.

$$I_{rms,Q_x} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{Qx}^2 \, \mathrm{d}\omega t} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} D_x(t)\, i_a^2 \, \mathrm{d}\omega t} \tag{3}$$

where $D_x(t)$ can be derived based on the conduction periods of the switch Q_x. As an example, for Q_1, (4) can be written:

$$D_1(t) = \begin{cases} M\sin(\omega t), & \sin(\omega t) \geq 0 \\ 0, & \sin(\omega t) < 0 \end{cases}, \; M = \frac{\sqrt{2}V_{rms}}{V_{ds}/2} \tag{4}$$

Using (3) for all the switches in leg A, the RMS currents can be derived as (5):

$$\begin{aligned} I_{rms,Q_{1,4}} &= I_{rms}\sqrt{\frac{M}{\pi}}\sqrt{1 + \frac{1}{3}\cos 2\phi} \\ I_{rms,Q_{2,3}} &= \frac{I_{rms}}{\sqrt{2}} \\ I_{rms,Q_{5,6}} &= \frac{I_{rms}}{\sqrt{\pi}}\sqrt{\frac{\pi}{2} - \frac{M}{3}(3 + \cos(2\phi))} \end{aligned} \tag{5}$$

It has to be noted that while the switching patterns change the instantaneous energy loss distribution, the RMS current over a period remains similar. Therefore, (5) is valid for both patterns.

Although simple, this approach cannot model the fast temperature changes of the junction temperatures. Therefore, a second approach is taken to calculate the power loss in time periods smaller than the time constant of junction temperatures. In the second approach, the conduction energy loss in a period of T_L is calculated based on the measured phase current at each point as summarized for one case in Table 1 where $D_a = M\sin(\omega t)$.

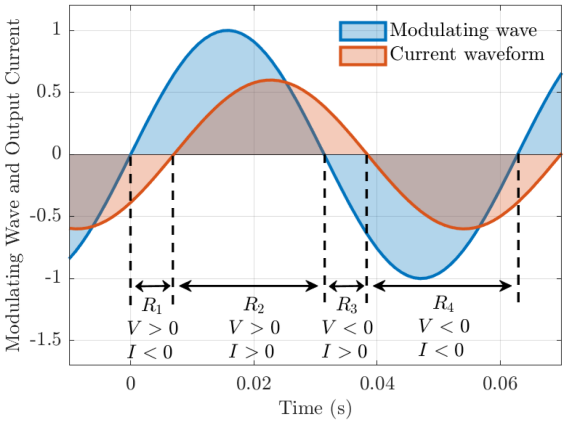

FIGURE 3. Modulating wave and current waveform in one output fundamental period.

2) SWITCHING LOSS

Based on the signs of the modulating and current waveforms shown in Fig. 3, each fundamental period can be divided into four regions. The energy losses per each $P \rightarrow O \rightarrow P$ or $N \rightarrow O \rightarrow N$ transition can be found in Table 2 for each of the four regions. Some minor loss components, such as the MOSFET internal gate resistance loss, are ignored.

The turn on and turn off switching energies, E_{on} and E_{off}, as well as reverse recovery energy, E_{rr}, are functions of voltage, current, and temperature. The dependence of switching energies on current and temperature can be approximated by cubic and quadratic equations, respectively. The corresponding coefficients can be extracted using the curve-fitting tools. Also, the MOSFET's output capacitor energy loss, E_{oss}, is a function of the voltage on the switch before the turn-off moment. By knowing the adjusted values of turn-on and turn-off energies, Table 2 lists the power loss value for each of the switches in leg A.

3) TOTAL LOSSES

Table 3 summarizes the total amount of power loss in each semiconductor in leg A based on the operating region and used patterns in which $E_{tot} = E_{on} + E_{off} + E_{oss}$.

C. THERMAL MODEL

Derivation of a thermal model for the three-level inverter is divided into two steps according to the thermal time constants. In modeling the temperature difference from MOSFET's case to junction, the case temperature is assumed to be constant since it has a much larger time constant. On the other hand, the heatsink model is derived separately to estimate the case temperatures for all MOSFETs.

1) JUNCTION TO HEATSINK THERMAL MODEL

Traditionally, two types of equivalent thermal networks have been used to model semiconductor devices. Foster and cauer networks, shown in Figs. 4 and 5, can be used to estimate the junction temperature when the case temperature and power

TABLE 2. Switching Energy Loss, E_{sw}, in a Single Transition for Switches in Leg a

	R_2 , $(P \rightarrow O \rightarrow P)$		R_4 , $(N \rightarrow O \rightarrow N)$	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	$E_{on}+E_{off}+E_{oss}$	0	0	0
Q2	0	$E_{on}+E_{off}+E_{oss}$	0	E_{rr}
Q3	0	E_{rr}	0	$E_{on}+E_{off}+E_{oss}$
Q4	0	0	$E_{on}+E_{off}+E_{oss}$	0
Q5	E_{rr}	0	0	0
Q6	0	0	E_{rr}	0
	R_1 , $(P \rightarrow O \rightarrow P)$		R_3 , $(N \rightarrow O \rightarrow N)$	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	E_{rr}	0	0	0
Q2	0	E_{rr}	0	$E_{on}+E_{off}+E_{oss}$
Q3	0	$E_{on}+E_{off}+E_{oss}$	0	E_{rr}
Q4	0	0	E_{rr}	0
Q5	$E_{on}+E_{off}+E_{oss}$	0	0	0
Q6	0	0	$E_{on}+E_{off}+E_{oss}$	0

TABLE 3. Total Losses in Leg a Switches

Total power Loss for switches in leg A				
	R_2		R_4	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	$DR_{ds,1}I^2+f_{sw}(E_{tot})$	$DR_{ds,1}I^2$	0	0
Q2	$R_{ds,2}I^2$	$DR_{ds,2}I^2+f_{sw}(E_{tot})$	0	$(1-\|D\|)R_{ds,2}I^2+f_{sw}(E_{rr})$
Q3	0	$(1-D)R_{ds,3}I^2+f_{sw}(E_{rr})$	$R_{ds,3}I^2$	$\|D\|R_{ds,3}I^2+f_{sw}(E_{tot})$
Q4	0	0	$\|D\|R_{ds,4}I^2+f_{sw}(E_{tot})$	$\|D\|R_{ds,4}I^2$
Q5	$(1-D)R_{ds,5}I^2+f_{sw}(E_{rr})$	0	0	$(1-\|D\|)R_{ds,5}I^2$
Q6	0	$(1-D)R_{ds,6}I^2$	$(1-\|D\|)R_{ds,6}I^2+f_{sw}(E_{rr})$	0
	R_1		R_3	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	$DR_{ds,1}I^2+f_{sw}(E_{rr})$	$DR_{ds,1}I^2$	0	0
Q2	$R_{ds,2}I^2$	$DR_{ds,2}I^2+f_{sw}(E_{rr})$	0	$(1-\|D\|)R_{ds,2}I^2+f_{sw}(E_{tot})$
Q3	0	$(1-D)R_{ds,3}I^2+f_{sw}(E_{tot})$	$R_{ds,3}I^2$	$\|D\|R_{ds,3}I^2+f_{sw}(E_{rr})$
Q4	0	0	$\|D\|R_{ds,4}I^2+f_{sw}(E_{rr})$	$\|D\|R_{ds,4}I^2$
Q5	$(1-D)R_{ds,5}I^2+f_{sw}(E_{tot})$	0	0	$(1-\|D\|)R_{ds,5}I^2$
Q6	0	$(1-D)R_{ds,6}I^2$	$(1-\|D\|)R_{ds,6}I^2+f_{sw}(E_{tot})$	0

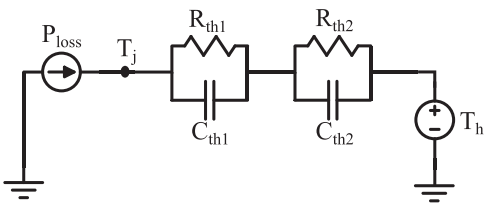

FIGURE 4. Second-order foster thermal equivalent network.

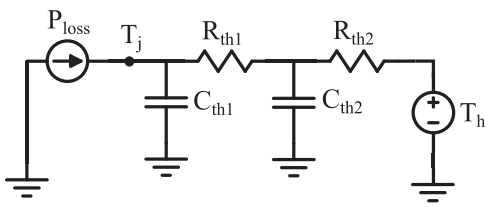

FIGURE 5. Second-order cauer thermal equivalent network.

loss values are known. While the equivalent voltage of each node in the cauer network indicates the actual temperature of a MOSFET layer, the *RC* blocks in the foster network do not have physical meaning and can only be used for junction temperature estimation [15]. Foster network is chosen in this article due to its more simple calculations. Assuming a first-order foster network with a single *RC* block, the junction to case temperature, ΔT_{jc} after a period of T_{th} with power loss P is estimated as (6) [13]:

$$\Delta T_{jc}^{(t_0+T_{th})} = R_{th} * \left(1 - e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) * P + \left(e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) * \Delta T_{jc}^{(t_0)} \tag{6}$$

Then, by adding T_c to ΔT_{jc}, junction temperature, T_j, can be obtained.

Although the first-order foster network gives an estimate of the junction temperature of the semiconductor, it can not

accurately model the fast dynamic behavior of the junction temperature. Hence, a more accurate thermal network which consists of two or three *RC* blocks can model the fast dynamics as well as the steady-state situation. For a second-order foster network shown in Fig. 4, (7) can be used in two steps for calculating the junction temperature of the switch.

$$\begin{aligned}\Delta T_{jm}^{(t_0+T_{th})} &= R_{th1} * \left(1 - e^{\left(\frac{-T_{th}}{R_{th1}C_{th1}}\right)}\right) * P \\ &\quad + \left(e^{\left(\frac{-T_{th}}{R_{th1}C_{th1}}\right)}\right) * \Delta T_{jm}^{(t_0)} \\ \Delta T_{mc}^{(t_0+T_{th})} &= R_{th2} * \left(1 - e^{\left(\frac{-T_{th}}{R_{th2}C_{th2}}\right)}\right) * P \\ &\quad + \left(e^{\left(\frac{-T_{th}}{R_{th2}C_{th2}}\right)}\right) * \Delta T_{mc}^{(t_0)} \end{aligned} \tag{7}$$

2) HEATSINK THERMAL MODEL

Based on [16], a foster-based equivalent thermal model can be extracted for a heatsink using a foster equivalent network for modeling the temperature rise at each location due to the heat applied at other locations. By applying constant heat into each section separately, and measuring the temperature in all sections, the thermal impedance Z_{ij} is defined as the thermal impedance at location i on the heatsink, caused by the heat dissipated at location j as written in (8):

$$Z_{ij} = \frac{\Delta T_{H_iC}(t)}{P_j} \tag{8}$$

Consequently, an impedance matrix can be formed for a heatsink divided into n locations as shown in (9). Based on [17], the temperatures at each heatsink position can be calculated at each time instant using (10):

$$Z = \begin{bmatrix} Z_{11} & \dots & Z_{1n} \\ \vdots & \ddots & \vdots \\ Z_{n1} & \dots & Z_{nn} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} T_{HS1}(t) \\ \vdots \\ T_{HS9}(t) \end{bmatrix} = \int_0^t \begin{bmatrix} \dot{Z}_{11}(t-\tau) & \dots & \dot{Z}_{1n}(t-\tau) \\ \vdots & \ddots & \\ \dot{Z}_{n1}(t-\tau) & & \dot{Z}_{nn}(t-\tau) \end{bmatrix} \times \begin{bmatrix} P_1(\tau) \\ \vdots \\ P_n(\tau) \end{bmatrix} d\tau + T_C \tag{10}$$

III. PROPOSED CONTROL METHOD

The main objective of the proposed control algorithm is to minimize the maximum junction temperatures of the switches in each leg. To achieve this goal, the junction temperatures of the switches in each leg will be calculated for each pattern based on the power loss calculated using the loss model introduced in the previous section. The pattern which results in a lower maximum junction temperature will be selected for switching transitions in the respective leg. Although the ideal case is to do the temperature calculation before each transition, this will result in an extremely large computational burden on the microprocessor which makes it impossible to employ in high switching frequencies. Instead, a thermal interval will be determined in this article, so that thermal calculations can be performed at a lower frequency that is independent of the switching frequency. On the other hand, if the thermal interval is too large, the control system can not effectively reduce the maximum junction temperature. Hence, using the MOSFET equivalent thermal network, the maximum allowed thermal interval is calculated to limit the junction temperature fluctuations. Then the optimum pattern will be selected using the electro-thermal model.

A. THERMAL INTERVAL DERIVATION

The first step is to determine the time step for thermal calculations, T_{th}. This interval is selected in a way to ensure that the junction temperature change in one T_{th} does not exceed a predefined limit, $\delta T_{j,lim}$:

$$\Delta T_{jc}^{(t_0+T_{th})} \leq \Delta T_{jc}^{(t_0)} + \delta T_{j,lim} \tag{11}$$

By replacing (11) into (6), (12) can be calculated:

$$\begin{aligned}\Delta T_{jc}^{(t_0)} + \delta T_{j,lim} \geq R_{th} * \left(1 - e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) * P \\ + \left(e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) * \Delta T_{jc}^{(t_0)}\end{aligned} \tag{12}$$

Equation (12) can be rewritten after some simplifications as (13):

$$\left(1 - e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) * \left[R_{th} * P - \Delta T_{jc}^{(t_0)}\right] < \delta T_{j,lim} \tag{13}$$

Since the maximum power loss in each switch is known and the minimum $\Delta T_{jc}^{(t_0)}$ is equal to zero, the only variable that can be controlled to limit the left-hand side of (13) is T_{th}. Hence, the proper value for T_{th} is extracted.

The calculations can be done for the two-step foster network as well. The final simplified derived equation is shown in 14:

$$\begin{aligned}&\left(1 - e^{\left(\frac{-T_{th}}{R_{th1}C_{th1}}\right)}\right) * \left[R_{th1} * P - \Delta T_{jm}^{(t_0)}\right] \\ &\quad + \left(1 - e^{\left(\frac{-T_{th}}{R_{th2}C_{th2}}\right)}\right) * \left[R_{th2} * P - \Delta T_{mc}^{(t_0)}\right] < \delta T_{j,lim}\end{aligned} \tag{14}$$

Equivalently, by knowing all the worst case values in (14), T_{th} is the only parameter that determines the maximum junction temperature change in a single thermal step.

B. JUNCTION TEMPERATURE ESTIMATION AND MODE CONTROL

By knowing the value of T_{th} and the power loss value for each MOSFET, the junction temperature of all switches in each leg can be estimated at steps of T_{th} for each of the two patterns. For this purpose, (6) and (7) can be used for

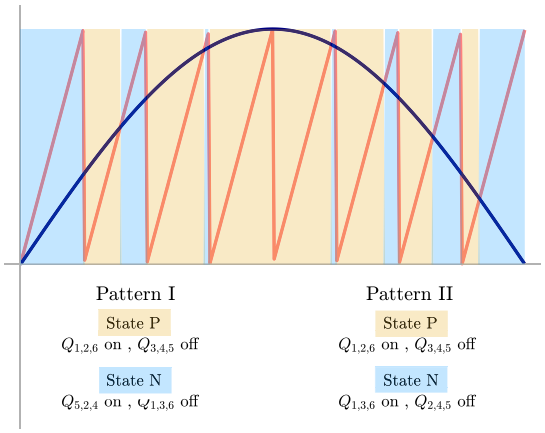

FIGURE 6. Realization of states P and O using SPWM modulation with patterns I and II.

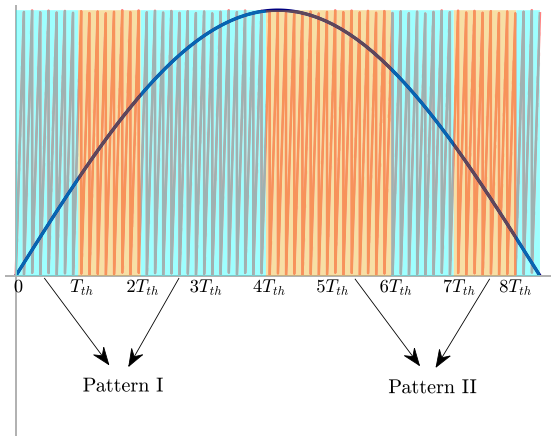

FIGURE 7. An example of switching between patterns I and II at periods of T_{th}.

first-order and second-order foster networks, respectively. In junction temperature estimation, the case temperature, T_c, is considered constant. However, T_c for all switches is estimated according to (10).

For each leg, the pattern which leads to a lower maximum junction temperature will be selected and applied to the switches in the corresponding inverter leg. The method for applying the patterns in a three-level ANPC inverter with simple SPWM modulation is depicted in Fig. 6. Using the proposed method in this article, Fig. 7 illustrates an example of the modulation technique in which the utilized pattern is changing based on the junction temperature estimation at steps of T_{th}. A flowchart of the proposed method is depicted in Fig. 8 where H_j and H_c are the time periods for updating the temperature changes in the junction and case temperatures. These time periods can be calculated based on the thermal parameter values of and the first or second-order foster network equations.

In a comparison of efficiency among the presented modulation schemes, it should be noted that the variations in

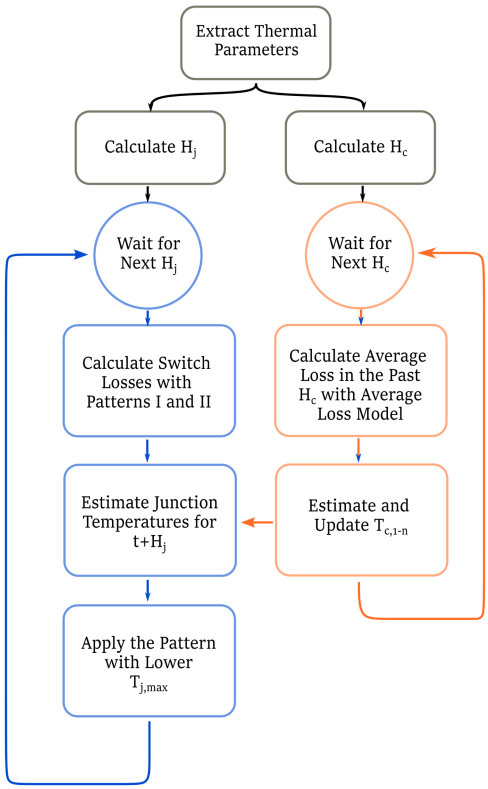

FIGURE 8. A flowchart of the proposed control method.

the total energy loss among the presented methods are minimal. This can be resulted from Table 3, in which the sum of loss over a period in all the switches is equal with both patterns. However, as an aftereffect of lowering the difference among the junction temperature of the switches in a leg, and due to the non-linear relationship between the temperature and loss-related parameters of a MOSFET, the total power loss slightly varies in different patterns. These variations are not further studied in this article due to their negligible values.

IV. SENSITIVITY ANALYSIS

While the derived equations for calculating ΔT across a single block of the foster network are accurate and no approximation is made in their derivation, the inaccuracy of loss and thermal parameters can lead to an inexact temperature estimation. This inaccuracy in the thermal parameters results from a variety of sources. First, according to the datasheets of many industrial MOSFETs, the R_{th} values can vary by up to 30% in two similar devices. The second source of uncertainty is the external factors. For example, the thermal pads which are usually placed between the MOSFET tab and the heatsink can increase the total R_{th} by an uncertain value that directly depends on the pressure on the pad.

To investigate the sensitivity of the temperature calculation to the uncertainty in thermal parameters, this section presents a sensitivity analysis and determines the sensitivity to different parameters in different situations.

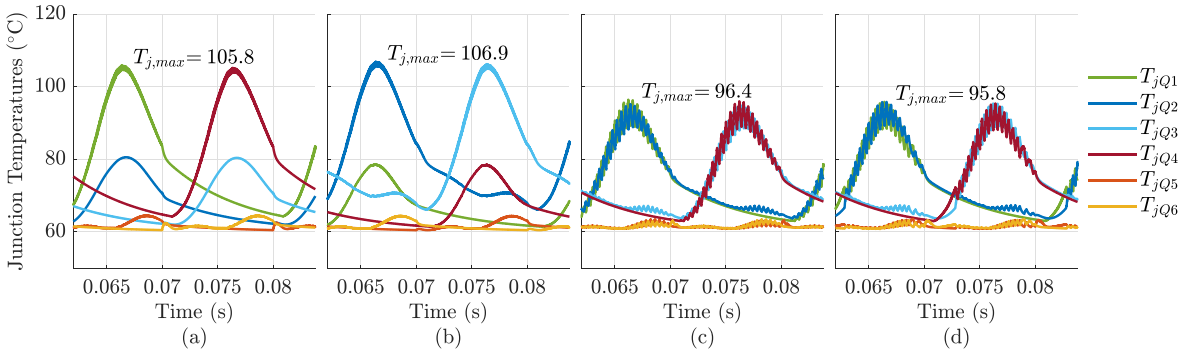

FIGURE 9. Junction temperatures of the switches with equal case temperatures in one leg of the inverter, using (a) pattern I, (b) pattern II, (c) equal power loss distribution, and (d) proposed equal junction temperature technique.

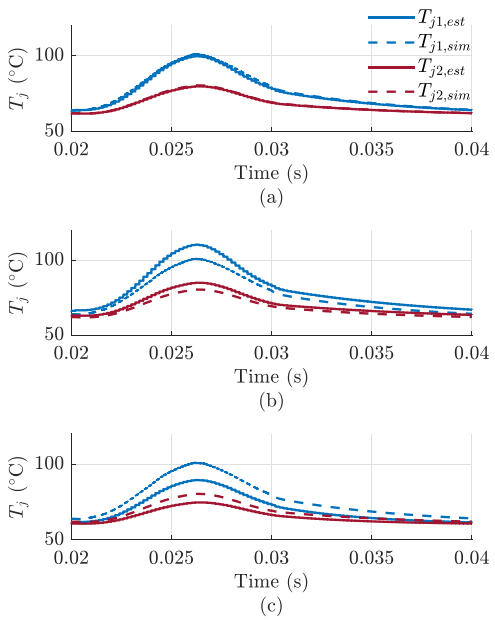

FIGURE 10. Comparison of the simulated and estimated switch temperatures for Q1 and Q2 with pattern I switching and output current of 40 A; (a) equal R_{th} in estimation and simulation, (b) R_{th} in estimation 30% higher than R_{th} in simulation, and (c) R_{th} in estimation 30% lower than R_{th} in simulation.

In order to determine the sensitivity of (6) to the thermal variables, partial derivatives of (6) to R_{th} and C_{th} are calculated as shown in (15) and (16).

$$\frac{\partial\left(\Delta T_{jc}^{(t_0+T_{th})}\right)}{\partial R_{th}} = P\left[\left(1-e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) + R_{th}\left(\frac{T_{th}}{R_{th}^2C_{th}}e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right)\right] + \Delta T_{jc}^{(t_0)}\left(\frac{T_{th}}{R_{th}^2C_{th}} * e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) \quad (15)$$

$$\frac{\partial\left(\Delta T_{jc}^{(t_0+T_{th})}\right)}{\partial C_{th}} = R_{th}P\left(\frac{T_{th}}{R_{th}C_{th}^2}e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) + \Delta T_{jc}^{(t_0)}\left(\frac{T_{th}}{R_{th}C_{th}^2} * e^{\left(\frac{-T_{th}}{R_{th}C_{th}}\right)}\right) \quad (16)$$

By replacing R_{th} and C_{th} in the equations with their values for a semiconductor device, the sensitivity values can be extracted and compared. By plugging in the $R_{th} = 0.35$ and $C_{th} = 0.0036$, which are the values of a first-order foster network, corresponding to an SiC MOSFET with TO-247 package (UJ4C075018K4S), the sensitivity values for 50 W power loss is as follows:

$$\frac{\partial\left(\Delta T_{jc}^{(t_0+T_{th})}\right)}{\partial R_{th}} = 56 \qquad \frac{\partial\left(\Delta T_{jc}^{(t_0+T_{th})}\right)}{\partial C_{th}} = 1578 \quad (17)$$

A direct outcome of calculating the sensitivity values is that a small variation in the thermal parameters can result in a large deviation in the accuracy of the formula. These small variations could happen due to manufacturing tolerances, thermal pad R_{th}, etc. In order to examine the sensitivity of the temperature estimation method to the changes in thermal resistivity with simulations, the estimated temperature is examined in three cases as shown in Fig. 10. Mismatches of up to 9 degrees can be seen between the estimated and simulated temperatures of the switches. Hence, in the experimental section of this article, instead of relying on the datasheet values, the accurate thermal parameters of the semiconductors are first extracted using some high current pulse tests on the MOSFETs.

V. SIMULATION RESULTS

The proposed control method for reducing the hotspot temperature in a three-level ANPC inverter is simulated using a Simulink/PLECS co-simulation. The main specifications of the simulated inverter is listed in Table 4. Loss-related parameters, as well as the extracted thermal network components for a second-order foster network, are presented in Table 5. In this section, the results obtained from the proposed hotspot temperature minimization method is compared to the results

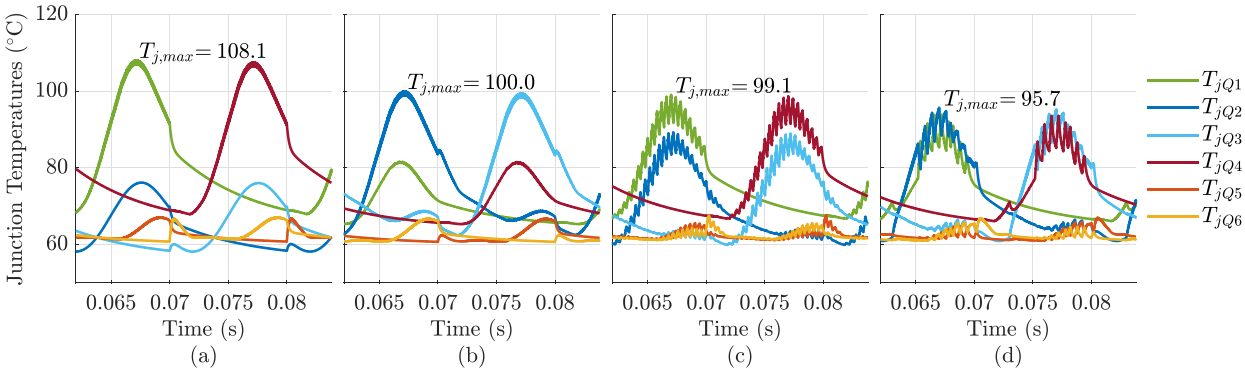

FIGURE 11. Junction temperatures of the switches with unequal case temperatures in one leg of the inverter, using (a) pattern I, (b) pattern II, (c) equal power loss distribution, and (d) proposed equal junction temperature technique.

TABLE 4. Inverter Specifications for Simulations and Experimental Setup

Parameter	Value
Rated Input Voltage	400 V
Rated Output RMS Current	40 A
Selected Switch	UJ4C075018K4S
Switching Frequency	50 kHz

TABLE 5. Selected MOSFET Characteristics

Parameter	Value
Rated R_{on} at 25C (mΩ)	18
E_{on} and E_{off} at 400V, 50A (μJ)	453, 304
2nd-order Foster R_{th1}, C_{th1}	0.255, 0.027
2nd-order Foster R_{th2}, C_{th2}	0.135, 0.0014

of pattern I, pattern II, and equal loss distribution control methods. The dynamic response of the junction temperature controller to sudden changes in load is presented, as well as its operation under a constant three-phase load.

A. CONSTANT LOAD, EQUAL CASE TEMPERATURES

In this subsection, the simulations have been performed for an RL load with a power factor of 0.86 as can be seen in Fig. 9. The modulation index, M, is set to 1 and the case temperatures for all the switches are considered to be equal to 60 °C. The control circuit is simulated in Simulink, while the power stage is simulated in PLECS. The junction temperatures of the switches are achieved based on the switching and conduction losses and thermal characteristics of the MOSFETs.

Fig. 9 shows the junction temperatures of the six MOSFETs in one leg of the converter for each of the four control methods. Pattern I, pattern II, equal loss distribution control, and the proposed equal junction temperature control techniques are used and compared to each other. The maximum junction temperature in the switches of each leg is specified in each case.

TABLE 6 Summary of Comparison Between the Four Control Methods

	Equal T_c		Unequal T_c	
Control method	Max T_j	$P_{density}$	Max T_j	$P_{density}$
Pattern I	105.8	100%	108.1	100%
Pattern II	106.9	98.2%	100.0	107.7%
Equal loss	96.4	109.4%	99.1	108.8%
Proposed method	95.8	110%	95.7	113.2%

B. CONSTANT LOAD, UNEQUAL CASE TEMPERATURES

In the previous case, both the equal loss distribution method and the proposed technique proved to result in the lowest maximum junction temperature compared to other techniques. However, in many experimental setups, the case temperatures of the MOSFETs may not be totally equal. Therefore, in the simulations in this section, the inner switches are considered to be closer to the coolant input which results in lower case temperature (This assumption is based on the designed cooling system for the experimental setup and will be discussed in more detail in Section VI). Fig. 11 shows the junction temperatures of all the switches in one leg of the inverter. The case temperature of the outer switches, clamping switches, and inner switches are set to 63 °C, 60 °C, and 57 °C, respectively.

A direct consequence of the reduction of maximum junction temperature is increasing the maximum output power of the inverter and hence, improving the power density. Using the results of the mentioned simulations, Table 6 summarizes the maximum junction temperatures in each case, as well as the increase in the maximum output power that can be achieved in each case compared to pattern I.

It can be seen that in the case of equal case temperature, both equal loss and the proposed technique result in an almost 10% increase in the power density of the inverter. However, since the case temperatures of switches are not similar in actual power converters, the proposed minimum junction temperature method can be the most effective control method in

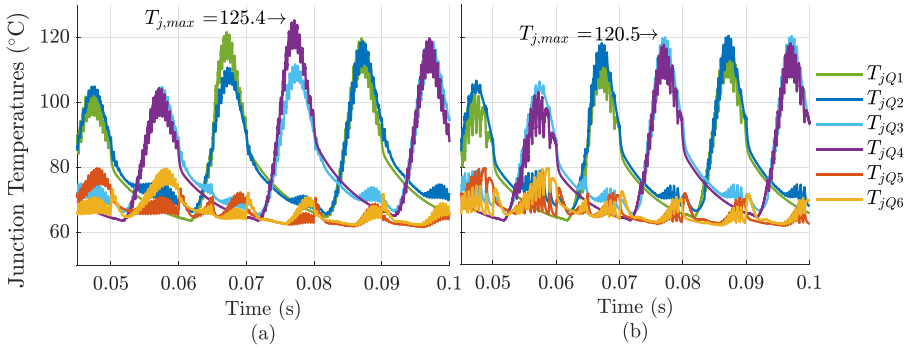

FIGURE 12. Dynamic response of the junction temperatures of the switches under two control methods; (a) equal loss balancing control, and (b) proposed equal junction temperature technique.

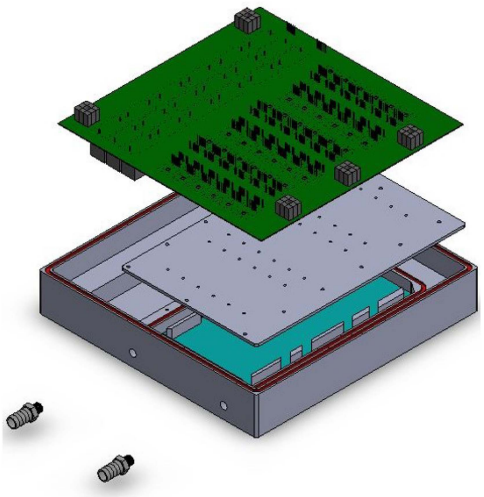

FIGURE 13. Exploded view of the power PCB, fin base and enclosure.

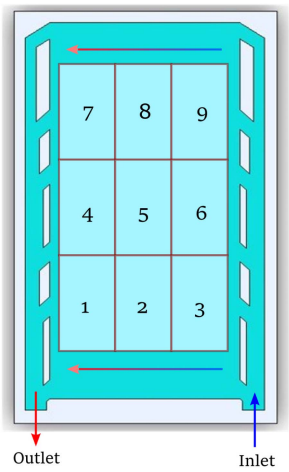

FIGURE 14. Fin base of the cooling block, divided into 9 locations.

terms of power density improvement by up to a 13% increase in the power density.

C. DYNAMIC RESPONSE

To evaluate the dynamic response of the proposed technique and compare it to the equal loss balancing method, a dynamic scenario has been employed and simulated in which the value of M is changed at $t = 0.065\,s$ from 0.5 to 1. The results of equal loss balancing control, and the proposed minimum junction temperature technique in this dynamic situation is depicted in Fig. 12. It can be seen that in the case of the equal loss balancing control, there is a considerable gap in the temperatures of the switches for one period before the new ratio is calculated. However, with the proposed technique, the balance between the temperatures of the hot switches is kept in the transition instances at the cost of a larger computational burden.

VI. EXPERIMENTAL RESULTS

A. EXPERIMENT SETUP

The three-level ANPC experimental setup has been implemented based on the specifications given in Table 4, and the main switches are UJ4C075018K4S, with the characteristics listed in Table 5. TMS320f28379 d dual-core microcontroller is used in the experimental setup and both cores as well as the two control law accelerators (CLA) are used to increase the computation capacity of the microcontroller. The inverter's top view is shown in Fig. 15 where the control and gate driver board are shown. By removing the gate driver board, the power PCB is placed underneath the gate driver board, mounted on the heatsink as shown in Fig. 13. All the switches and DC-link capacitors are mounted on the heatsink from the bottom of the power board. An RL load is selected as the load where a three-phase inductor bank using 2.5 mH inductors and a three-phase resistor bank utilizing 2.5 Ω resistors are employed.

A heater is submerged into the cooling tank which is used to set the initial coolant temperatures of the MOSFETs to the desired initial value. Fig. 14 shows the mounting plate for the MOSFETs. In the cooling design of the inverter, the inner MOSFETs are mounted at locations 3, 6, and 9, closer to the coolant input where the temperature is lowest, and outer MOSFETs are placed at locations 1, 4, and 7, closer to the coolant output where the temperature is the highest. K-type thermocouples are attached to the heatsink right underneath each MOSFET through the vented screws used for attaching

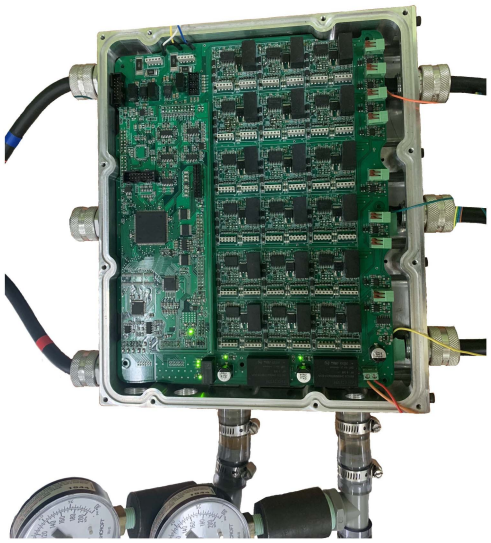

FIGURE 15. Top view of the inverter; Control and gate driver board.

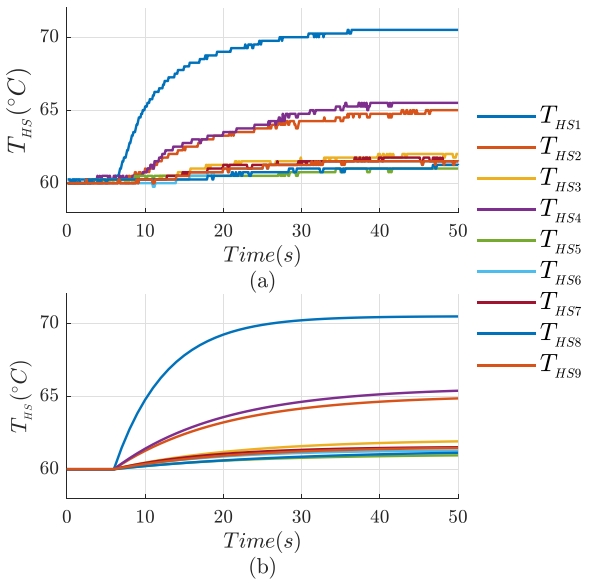

FIGURE 16. The temperature change in heatsink sections when the heat is applied to section HS1. (a) Experimentally extracted temperatures and (b) curve-fitted first-order foster network.

the MOSFETs to the heatsink. These thermocouples are used in extracting the inverter's thermal characteristics.

For the reduction of computational burden on the microprocessor, the junction temperature estimation is performed only for the two hottest switches in each leg at every T_{th}.

B. THERMAL PARAMETERS' EXTRACTION

In order to apply the proposed hotspot minimization algorithm to the experimental setup, the actual thermal parameters of the system need to be extracted. Although a more accurate thermal model can be extracted using intensive mechanical simulations and tests, the goal here is to obtain a less accurate but simple model that can be evaluated in real time by the available microcontrollers on the market. Hence, based on [16] and by conducting some experimental tests, a thermal model is extracted to be used in the next steps of the experiments.

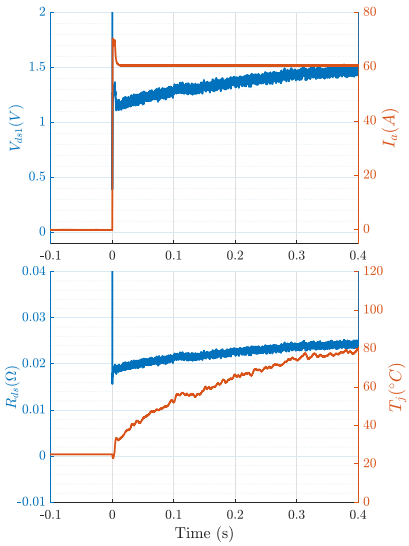

FIGURE 17. High-current pulse tests an V_{on} measurement for extracting thermal characteristics.

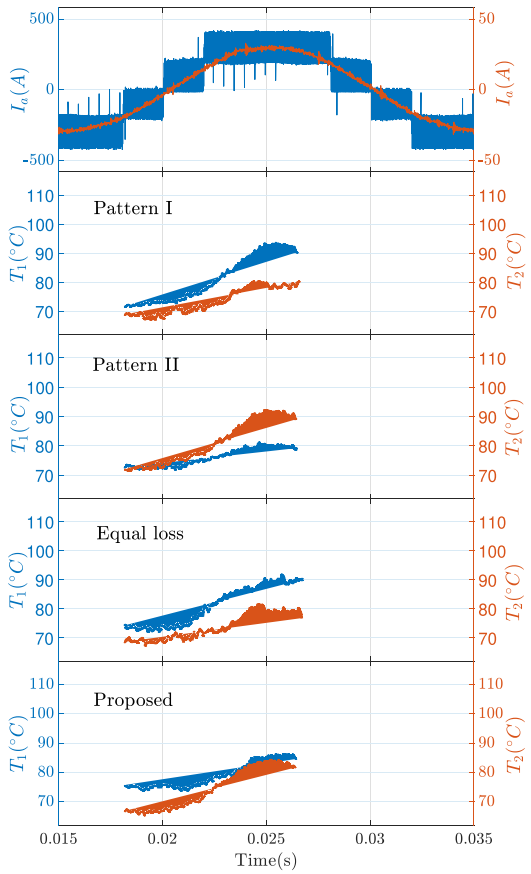

FIGURE 18. Experimental results and a comparison of junction temperatures in two switches in leg A using the conventional and proposed control techniques.

1) HEATSINK PARAMETERS

To measure the heatsink temperature right underneath each MOSFET, thin K-type thermocouples have been placed inside the vented screws used for mounting the MOSFETs on the plate. The thermocouple amplifier circuitry along with the serial communication with the microcontroller allows for online temperature measurements in steps of $0.25\,^{\circ}C$. The coolant temperature is first set to $60\,^{\circ}C$ and then, to apply the heat at each position on the plate, a controlled short circuit with limited current is created using the MOSFETs at desired locations. The resulting conduction losses of the MOSFET determine the loss value. At coolant inlet temperature of $60\,^{\circ}C$, a maximum of 120 W can be dissipated per MOSFET based on the MOSFET and source capabilities. As an example, the temperature changes in all heatsink sections are plotted in Fig. 16(a) when 40 W power is dissipated in HS1.

Since the thermal model is needed for temperature predictions, each of the thermal impedances between the two points is fitted to the response of a first-order foster network as written in (18). Fig. 16(b) depicts the fitted curves. An impedance matrix can be formed for the heatsink using the extracted thermal parameters as shown in (19) at the bottom of this page.

$$f(t) = PR\left(1 - e^{\left(\frac{-t}{RC}\right)}\right) \tag{18}$$

2) JUNCTION TO HEATSINK PARAMETERS

The MOSFET's junction-to-case thermal model is usually known from the manufacturer datasheet as discussed before. However, the manufacturing uncertainties, silicone pad, and thermal grease present between the tab and the heatsink introduce additional thermal components to the previously investigated model which need to be extracted for a more accurate thermal model.

To extract the thermal parameters, high current tests are performed on the MOSFETs, where an intentional short circuit is made in the leg, and a pulse current of up to 100 A is passed through the switches for very short periods of time as shown in Fig. 17. By measuring the changes in on-resistance, the changes in junction temperatures of switches are extracted versus the amount of dissipated energy in the MOSFETs. Based on the changes in the on-resistance, the junction temperature can be extracted as shown in Fig. 17.

It needs to be mentioned that the thermal characteristics of the switching devices can change with time due to the degradation. This change in the thermal variables may be unequal in each semiconductor device. Since the presented thermal model does not use a temperature or voltage feedback to update itself, the accuracy of the temperature simulation can decrease with time. However, the proposed thermal tests can be performed again to update the thermal model.

C. JUNCTION TEMPERATURES

The experimental tests have been run using all four methods introduced in the simulations section. The junction

$$\begin{bmatrix} R_{ij} \\ C_{ij} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} 0.26 \\ 25 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 281 \end{bmatrix} & \begin{bmatrix} 0.16 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 397 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 372 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 301 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 394 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 347 \end{bmatrix} \\ \begin{bmatrix} 0.13 \\ 110 \end{bmatrix} & \begin{bmatrix} 0.24 \\ 27 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 100 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 263 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 134 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 244 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 410 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 402 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 369 \end{bmatrix} \\ \begin{bmatrix} 0.05 \\ 316 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 140 \end{bmatrix} & \begin{bmatrix} 0.19 \\ 31 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 212 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 297 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 162 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 603 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 659 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 590 \end{bmatrix} \\ \begin{bmatrix} 0.14 \\ 98 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 258 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 266 \end{bmatrix} & \begin{bmatrix} 0.25 \\ 25 \end{bmatrix} & \begin{bmatrix} 0.15 \\ 93 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 309 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 94 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 402 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 375 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 649 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 113 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 245 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 165 \end{bmatrix} & \begin{bmatrix} 0.25 \\ 27 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 97 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 121 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 208 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 393 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 296 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 122 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 517 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 189 \end{bmatrix} & \begin{bmatrix} 0.22 \\ 30 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 346 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 381 \end{bmatrix} & \begin{bmatrix} 0.09 \\ 190 \end{bmatrix} \\ \begin{bmatrix} 0.04 \\ 320 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 349 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 317 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 128 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 480 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 497 \end{bmatrix} & \begin{bmatrix} 0.24 \\ 28 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 131 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 243 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 695 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 309 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 124 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 307 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 142 \end{bmatrix} & \begin{bmatrix} 0.22 \\ 31 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 295 \end{bmatrix} \\ \begin{bmatrix} 0.04 \\ 396 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 355 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 290 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 312 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 409 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 276 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 314 \end{bmatrix} & \begin{bmatrix} 0.21 \\ 32 \end{bmatrix} \end{bmatrix} \tag{19}$$

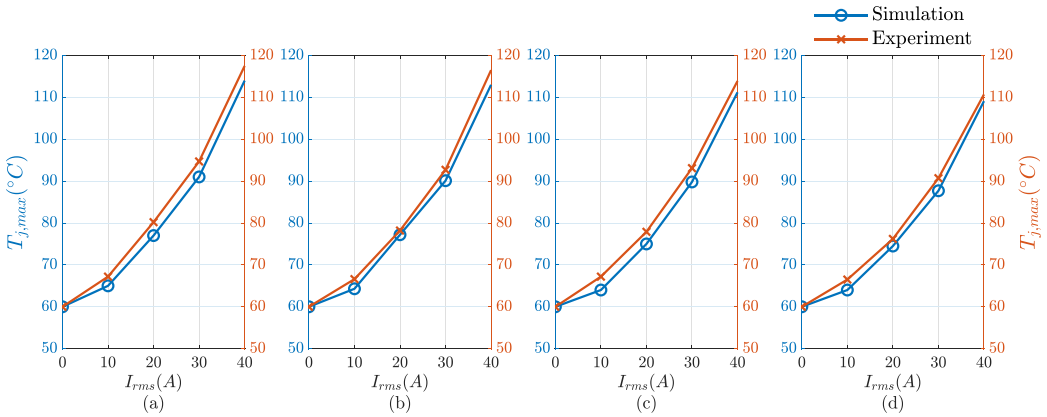

FIGURE 19. Comparison of maximum temperature in switching devices in leg A based on simulation and experimental results for M = 1; (a) Pattern I, (b) Pattern II, (c) equal loss balancing, and (d) proposed method.

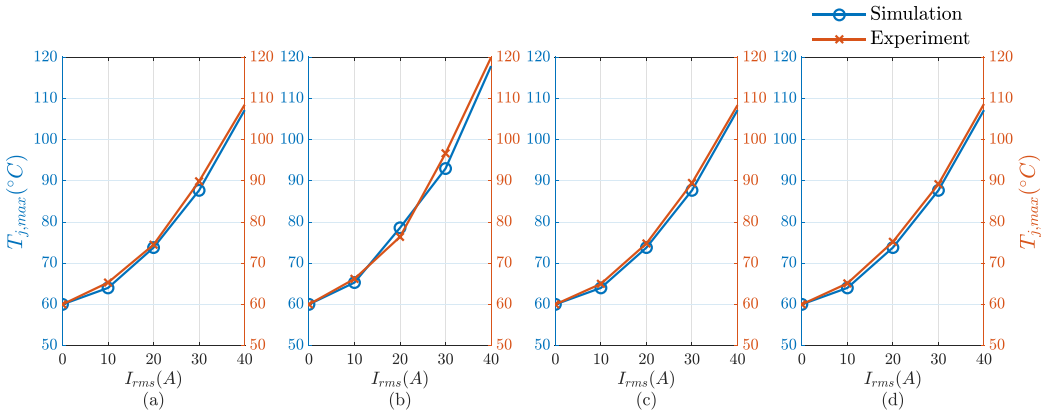

FIGURE 20. Comparison of maximum temperature in switching devices in leg A based on simulation and experimental results for M = 0.5; (a) Pattern I, (b) Pattern II, (c) equal loss balancing, and (d) proposed method.

temperatures of the MOSFETs are monitored by measuring drain to source voltage as well as the output current. The resulting on-resistance can give an estimation of the junction temperature. The final maximum temperature results are extracted from the measured on-resistances for the two hottest switches in one leg of the converter. The results are shown in Fig. 18, where the output current value and frequency are 20 A RMS and 50 Hz, respectively. By using the proposed control method, a reduction of 7.2, 5.3, and 4.5 degrees can be observed when compared to the pattern I, pattern II, and equal loss techniques, respectively. A summary of simulation and experimental results can be seen in Figs. 19 and 20 for M=1 and M=0.5, respectively. Figs. 19 and 20 show the maximum junction temperature in the switching devices of leg A of the inverter, $max(T_{j1}, T_{j2}, T_{j3}, T_{j4}, T_{j5}, T_{j6})$. It must be mentioned that for the comparisons presented in Figs. 19 and 20, the thermal model extracted from the experimental tests is used and the values in the datasheets are no longer utilized.

D. POWER DENSITY IMPROVEMENT

In order to test the increase in the power density using each of the mentioned patterns, 125 °C is set as the limit for junction temperatures in the experimental setup. Then, using the junction temperature prediction method, the output power is gradually increased by increasing the load current. The maximum power that can be achieved using each control method at different frequencies is then recorded and compared. An increase of 12.4%, 10.4%, and 4.1% is observed in the power density of the inverter with the proposed technique when compared to the pattern I, pattern II, and equal loss techniques, respectively.

VII. CONCLUSION

In this article, a new control method for a three-level ANPC inverter is proposed in which the maximum junction temperature of the MOSFETs in the inverter is reduced compared to the previous techniques. After presenting an electro-thermal model for the three-level ANPC inverter, the temperature at different heatsink locations can be estimated using a foster equivalent network. Then, the junction temperatures of the MOSFETs in each leg are estimated and the best pattern is selected in each calculation period to minimize the hotspot temperature and increase the power density.

Using simulations and experimental tests, the proposed technique has proven to increase the power density of the inverter by almost 12% compared to the classical pattern I and

pattern II techniques, and by 4% compared to the equal loss balancing method. In addition to reducing the hotspot temperature in the inverter, this technique can be used as a protection stage in the inverter which can ensure that the semiconductors will not exceed the allowed temperatures, especially in the transient loads.

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