IEEE Open Journal of
Power Electronics

Received 17 August 2022; revised 20 September 2022 and 10 October 2022; accepted 12 October 2022. Date of publication 19 October 2022; date of current version 9 November 2022. The review of this article was arranged by Associate Editor Liangzong He.

Digital Object Identifier 10.1109/OJPEL.2022.3215539

A Bi-Lateral Energy Resonant Conversion (BERC) Technique for Improved Passive Utilization in Hybrid Switched-Capacitor Converters

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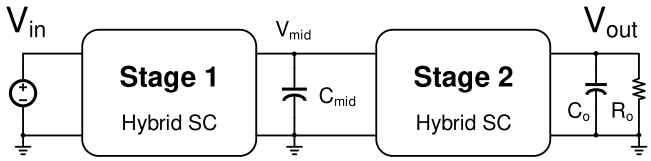
This work was supported by Intel Corporation.

ABSTRACT Hybrid or resonant switched-capacitor (ReSC) based converters are enticing with their high performance in high- and fixed-ratio applications, due to their efficient utilization of both active semiconductors and passive components. In particular, the cascaded or two-stage topologies have shown promising device utilization with least components required for high conversion ratios. This paper presents a novel bi-lateral energy resonant conversion (BERC) technique, that further improves the passive utilization in two-stage topologies by merging voltage- and current-type hybrid SC converters, beneficial in achieving smaller form factor while maintaining high efficiency. The current-type hybrid SC topology, which relocates the output inductor to its input and enables energy process simplification between adjacent cascaded stages, is first introduced in this paper. A 48-to-12 V converter prototype employing the BERC technique is implemented, validated and demonstrated with a very compact size of 0.18 in^3, along with an excellent overall peak efficiency of 98.8% (including all gate driver losses) using a zero voltage switching scheme designed for BERC. The prototype is tested up to 60 A, thus achieving a power density of 3900 W/in^3 with a full-load efficiency more than 98%.

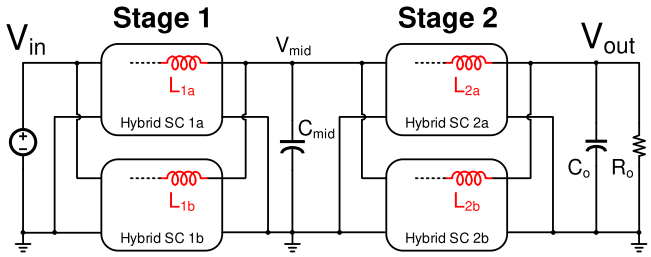
INDEX TERMS Switched-capacitor (SC), hybrid, resonant, interleaving, merged inductor, cascaded.

I. INTRODUCTION

Owing to the high electricity demand by data centers, improving their energy efficiency is critical for the purposes of reduced cost and reduced environmental impact. As a result, the intermediate bus architecture (IBA) adopts a higher backplane voltage, ranging from 40 V to 60 V, to decrease the detrimental conduction loss along the high-current power delivery [1]. While many approaches are working toward direct point-of-load (PoL) conversion [2], [3], [4] in a single stage, it is still challenging when interfacing with current-demanding and fast-changing computing loads. To further meet the stringent power requirements in data center applications, another widely adopted trend is dividing the power conversion into two parts: 1) power and volume-efficient high-voltage conversion and 2) fast-response regulation. The hybrid or resonant switched capacitor (ReSC) converter is well suited for the first part, since this type of converter can significantly reduce the passive size by maximizing the passive energy utilization, without the constraint of maintaining regulation capability. Many prior arts [5], [6], [7], [8], [9], [10], [11], [12], [13], [14] have shown promising performance for the power conversion from 48 V to 12 V intermediate bus through different topologies, which include cascaded [5], [6], [7], [8], Dickson [9], [10], flying capacitor multi-level [11] and transformer-based [12], [13] topologies. Meanwhile, several works have performed theoretical research and comparison [15], [16], [17], [18], [19], [20] between different ReSC topologies. In particular, the cascaded resonant converters [5], [6] have demonstrated the highest efficiency and power density for this



(a) Two-stage hybrid SC approach with middle bypass capacitance.



(b)

(b) Two-phase interleaving for two-stage hybrid SC approach.

FIGURE 1. Bypass capacitance and multiphase interleaving technique for two-stage hybrid SC approach.

application to date, due to their excellent switch and passive utilization.

The cascaded resonant converters or generally the two-stage hybrid SC approaches [21], [22] as shown in Fig. 1(a) comprise two independent stages with middle bypass capacitance, C_{mid}, in between, for stabilizing the middle voltage, V_{mid}. To achieve high performance, stable V_{mid} or larger C_{mid} is required to maintain independent and predictable LC resonant operation within each stage; otherwise, the LC networks would get complicated and less efficient due to the undesired involvement of C_{mid}. Even worse, the capacitance requirement increases with the output current, limiting the converter performance in terms of power density. Therefore, the multiphase interleaving technique as shown in Fig. 1(b) can be applied to reduce the current flowing to the bypass capacitor and increase the equivalent bypass capacitance, which helps maintain low capacitance requirement without compromising the high power density benefits from the two-stage approaches. However, each added phase requires additional resonant inductors, leaving some room for more improvement in passive utilization.

Simplifying the energy conversion process can further improve the passive utilization. At present, hybrid SC converters with a single inductor [15], [18], [19], [20], [23] at the output are derived from voltage-type buck converter by replacing the two complementary switches into SC topologies. The voltage-type hybrid SC converters undergo a *V-I-V* process to transfer energy from one voltage level to another through an inductor current, where *V* means voltage and *I* means current. The flying capacitors from the SC topology in turn reduce the voltage across or the energy processed by the inductor. However, the output inductor can be split and relocated to the converter input through current-type canonical switching cells [24], [25], [26], offering an *I-V-I* conversion process. The transformation from voltage- to current-type converters maintains all original features, with the extra benefit of continuous input and output current. By applying the current-type canonical switching cell, the current-type hybrid SC converters can be synthesized, which enables the relocation of the inductor, beneficial in reducing the existing two-stage conversion sequence of *{V-I-V}{V-I-V}* to *V-I-V* by simplifying the middle sequence of ".. *I-V}{V-I*.." into just ".. *I*..."; in practice, less *I* process suggests smaller required inductor. The combination of both voltage- and current-type hybrid SC converters maintains soft-charging operation in SC topologies and also provides a great opportunity to merge inductors between two adjacent stages. This is called Bi-lateral Energy Resonance Conversion (BERC) — a technique that reduces passive requirement in two-stage approach by having a shared inductor resonating with the flying capacitors in adjacent stages. As compared to traditional resonance within independent stages, the BERC technique can help obtain high power density while maintaining low switch stress and high efficiency.

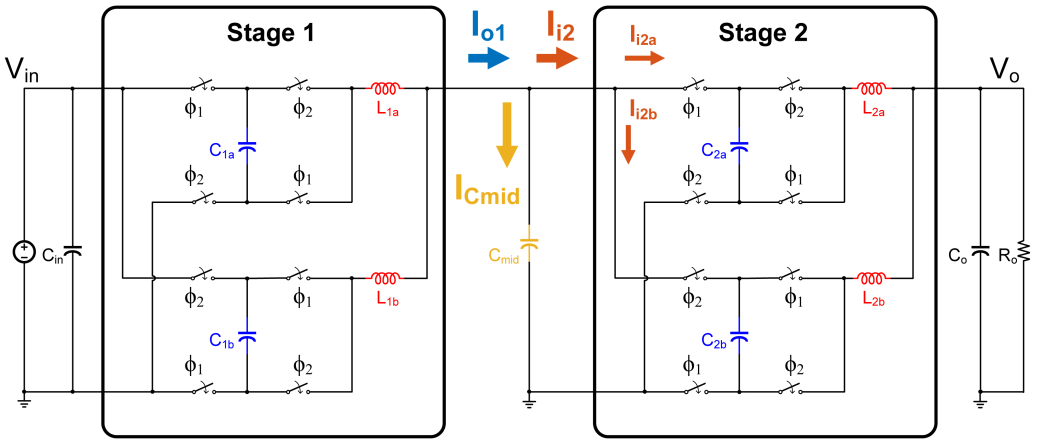
In this work, the BERC concept is implemented and analyzed in a dual-phase interleaved two-stage approach using the 2-to-1 ReSC topology. This work extends the previous conference publication [27], with a more general theoretical and quantitative analysis, on top of the conceptual model in merging the voltage- and current-type hybrid SC converters. More experiments were conducted and the results are included in this paper to demonstrate the performance of the converter. The remainder of this paper is organized as follows. Section II discusses the techniques for passive reduction, including improved effective middle capacitance and reduced inductors. The development of the BERC concept is then unveiled in Section III, along with the detailed circuit operation and design considerations of the resonant capacitors and inductors. After that, a zero voltage switching (ZVS) technique designed for BERC will be illustrated in Section IV. Measurement results for a fabricated hardware prototype will be shown in Section V, followed by a conclusion.

II. PASSIVES REDUCTION

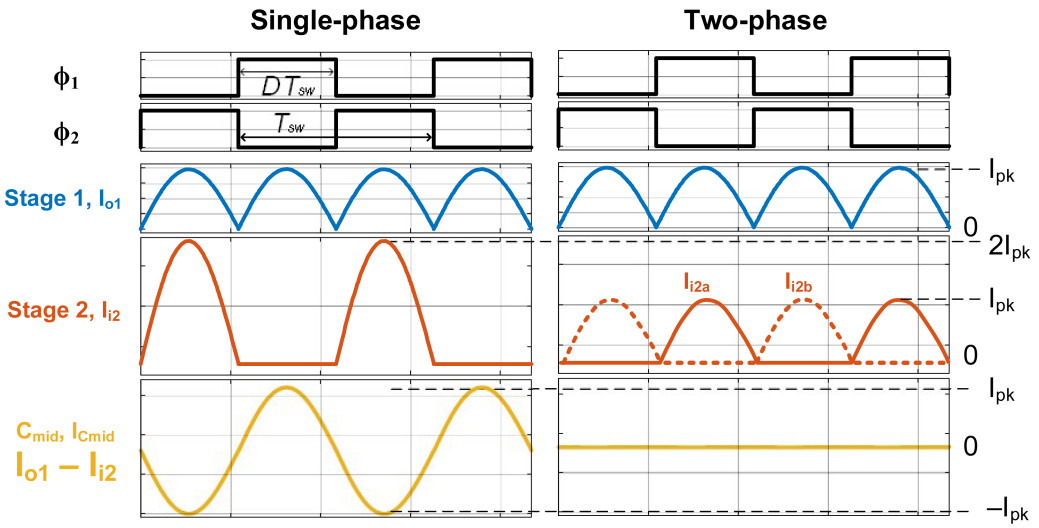
The passive components account for a significant portion of the power converter size, mainly due to redundant design and their limited energy density. For example, bypass capacitors typically have to be large to ensure flying capacitor balancing [28] and high efficiency [29]; also, resonant inductors for soft-charging operation are included in every stage [5]. Reducing the capacitor and inductor requirement can significantly improve the power density. This section discusses two techniques that manipulate the energy flow between passive components to achieve this goal.

A. IMPROVED EQUIVALENT BYPASS CAPACITANCE

A sufficient bypass capacitor, C_{mid}, as shown in Fig. 1, is required between stages to suppress the voltage ripple, ΔV_{mid},



(a) Dual-phase interleaved cascaded ReSC converter



(b) Single- and dual-phase operations

FIGURE 2. **(a) Schematic of a dual-phase interleaved cascaded ReSC converter and (b) the significant difference in middle bypass capacitor current between single and dual-phase operation.**

at V_{mid}, which can be expressed as:

$$\Delta V_{mid} = \frac{1}{C_{mid}} \cdot \left| \int_0^{DT_{sw}} (I_{o1} - I_{i2})\, dt \right|, \tag{1}$$

where D is the duty ratio of an operational phase, T_{sw} is the switching period, and I_{o1} and I_{i2} are the first-stage output current (injected into C_{mid}) and the second-stage input current (withdrawn from C_{mid}), respectively. Low-voltage ripple is required to avoid device breakdown for power converters; in particular, low-voltage ripple also helps decouple the stages and avoids unpredictable resonant operation in practical ReSC implementations. Take a single-phase cascaded ReSC converter (Fig. 2(a) converter with only *phase a:* C_{1a}, L_{1a}, C_{2a} and L_{2a}) as an example, when ϕ_1 is on, the resonant frequency of the first stage correlates with the inductor, L_{1a}, and the equivalent capacitance, C_{eqL1a}, seen by L_{1a}:

$$C_{eqL1a} = C_{stage1} \,/\!/\, (C_{stage2} + C_{mid}), \tag{2}$$

where C_{stage1} and C_{stage2} are the equivalent capacitance of the first and the second stages, respectively when each stage is considered independently. In the case of a single-phase cascaded ReSC converter, $C_{stage1} = C_{1a}$ and $C_{stage2} = C_{2a}$. To ensure simple resonant operation in the first stage, C_{mid} needs to be designed much larger than C_{stage1} and C_{stage2}, so that C_{eqL1a} is simply C_{stage1} and the resonant frequency can be reasonably predicted by

$$f_{res} = \frac{1}{2\pi\sqrt{L_{1a} \cdot C_{stage1}}}. \tag{3}$$

As a result, the first stage can be operated and designed independently, as can the second stage. Meanwhile, the stage decoupling ensures that C_{eqL1a} or C_{eqL2a} is always the same for all operational states (either ϕ_1 is on or ϕ_2 is on), allowing a full and smooth resonant cycle.

The voltage ripple is determined not only by the capacitance but also by the total charge going in (or out of)

the capacitor, according to (1). To reduce ΔV_{mid}, rather than increasing C_{mid} which compromises the power density, another way is to decrease the charge going through the capacitor, which equivalently improves the bypass capacitance. The multi-phase interleaving technique is widely adopted due to its simplicity and effectiveness in enhancing the effective bypass capacitance, and an example of a dual-phase interleaved two-stage cascaded ReSC converter is shown in Fig. 2(a), which has two sets of 2-to-1 ReSC converter within each stage, operating with 180° phase shift between each other. Fig. 2(b) compares the operating current for single- and dual-phase interleaved operations, given the same output current. In the single-phase operation, the large difference between I_{o1} and I_{i2} leads to a high amount of current going into C_{mid}, therefore increasing the capacitance requirement to ensure limited voltage ripple. Contrarily in the dual-phase operation, highly similar behaviors at I_{o1} and I_{i2} significantly reduce the charge injecting into the capacitor, beneficial in higher effective bypass capacitance or largely reduced capacitor size if the same voltage ripple is assumed for both cases. However, the number of inductors is doubled after adding one more phase, leaving some room for passive reduction.

B. MERGED SOFT-CHARGING INDUCTORS

The inductor is an essential element to achieve soft-charging operation and eliminate the charge sharing loss in pure SC converters [15], [30]. Conventionally, each stage is independently operated with sufficiently large bypass capacitance in the middle, and every set of the converters employs one inductor to soft-charge the flying capacitor individually. Fig. 3(a) shows the simplified schematic for a single-phase two-stage approach with the large bypass capacitance modeled as a voltage source and the inductor as a current source; for simplicity, only one of the operational states is shown, i.e. state 1 when the $Q_{1B} - Q_{2A}$ pair is on. With a dual-phase operation, the bypass capacitance requirement is significantly reduced; ideally, the middle branch can be assumed open circuited as shown in Fig. 3(b), without affecting the resonant operation of the two stages since the current going to the middle branch is almost zero when I_{o1} and I_{i2} are matched. To simultaneously fulfill the efficient step-down conversion and the soft-charging operation, the converter only requires: (i). flying capacitors (at least one in each stage to reduce the voltage ratings) for sustaining the voltage difference between the input and output voltage, and (ii). one inductor for soft-charging the flying capacitors. As shown in Fig. 3(c), it is possible to swap the locations of the current source, L_{stage2}, and the flying capacitor, C_{stage2} of the second stage, so that L_{stage2} can be merged with L_{stage1} to reduce the inductor requirement. Since the merged inductor soft-charges flying capacitors on two adjacent stages, this technique is called bi-lateral energy conversion (BERC) and the practical implementation will be unveiled in the next section.

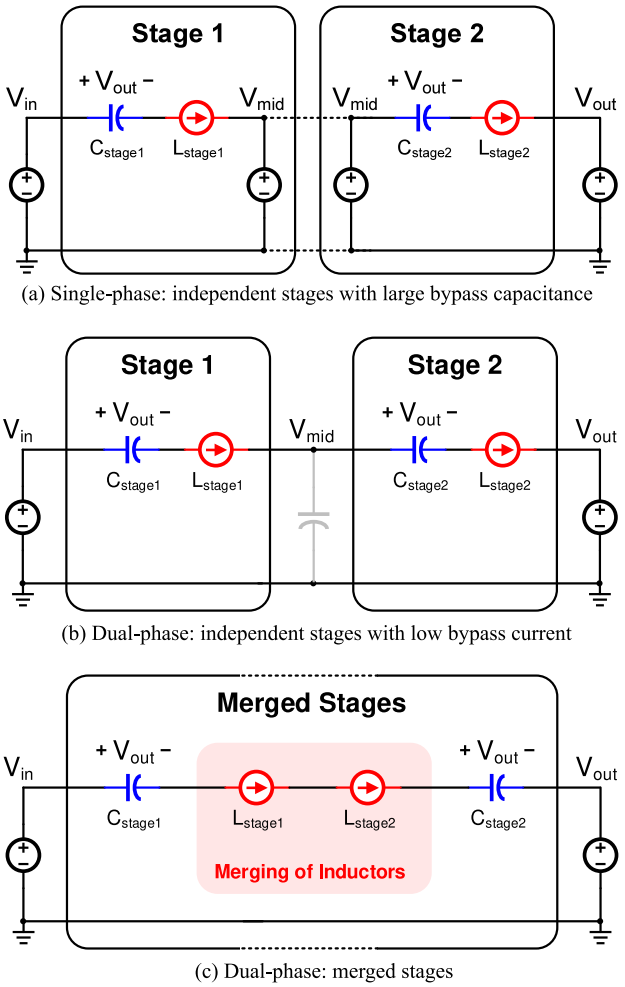


FIGURE 3. Simplified schematics for single- and dual-phase operations with independent and merged stages.

III. BI-LATERAL ENERGY RESONANT CONVERSION (BERC)

The BERC technique requires a step-down hybrid SC converter with inductor at its input, according to the merging process shown in Fig. 3(c). As of now, the commonly seen hybrid SC converters with single output inductor are derived from voltage-type buck converters. In order to relocate the inductor, a new current-type hybrid SC converter is developed through the duality principle in the canonical switching cells. By combining both voltage- and current-type hybrid SC converters, the operating principle of the BERC technique is discussed and validated using 2-to-1 ReSC converters for each stage in this section.

A. CANONICAL SWITCHING CELLS FOR HYBRID SC CONVERTERS

Canonical switching cell is the basic building block for high-frequency switching converters [24], and the way of connecting the cell with external systems leads to the distinctions

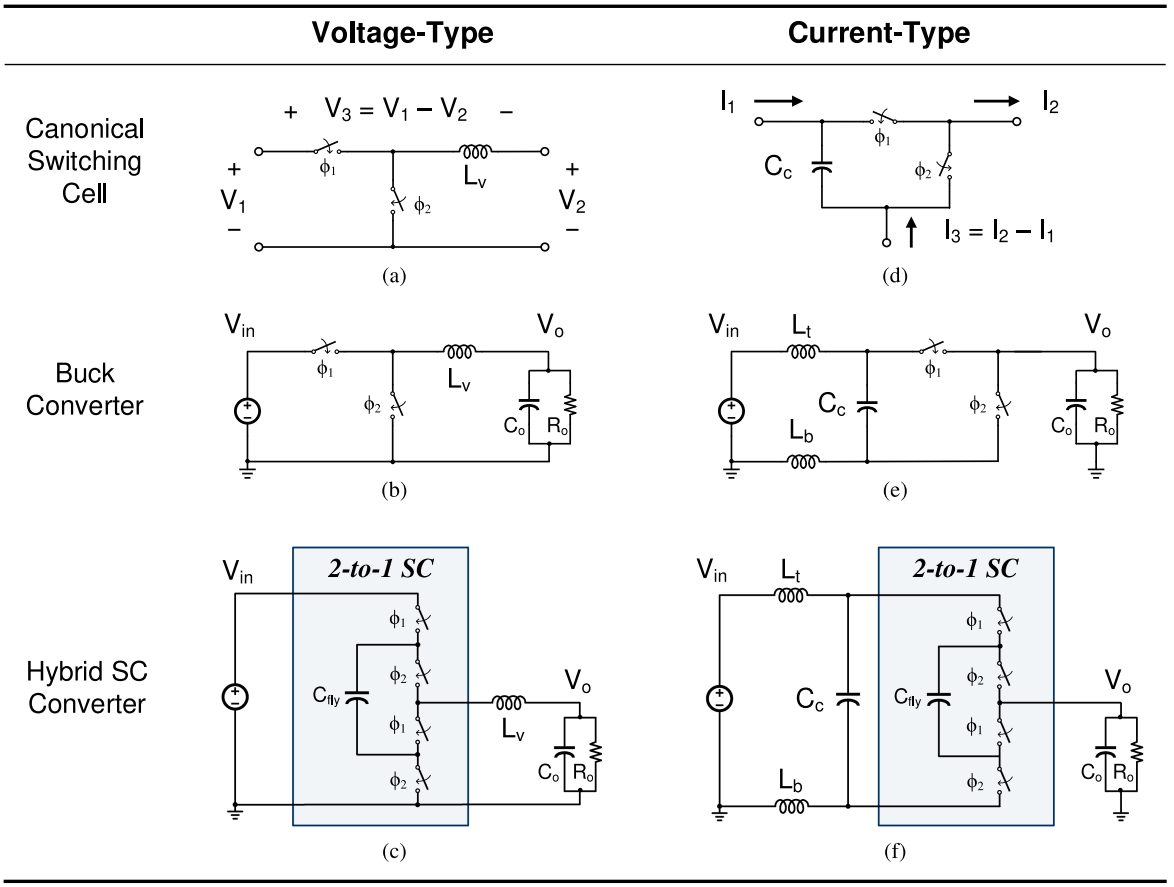


FIGURE 4. Voltage- and current-type hybrid SC converters.

among converters. This section begins with two-switch cell for building up step-down converters, which can then be extended and combined with SC cells for the benefits of switch and capacitor voltage reduction. In this paper, the operation mode of interest is continuous conduction mode (CCM) and forced CCM, and the converter switches around the resonant frequency.

Fig. 4(a) shows the voltage-type canonical switching cell for inductor-based converters, which is a typical three-terminal network composed of two switches and an inductor. By tapping V_1 as the input voltage and V_2 as the output voltage, a buck converter can be synthesized as shown in Fig. 4(b). The buck converter then serves as the basic structure for building up voltage-type hybrid SC converters. Fig. 4(c) shows an example schematic of a 2-to-1 ReSC converter, which is structured by adding an inductor at the output of the 2-to-1 SC converter; or, from other perspective, the two buck switches are replaced by a switch-and-capacitor matrix. As opposed to the energy transfer through an inductor in a voltage-type canonical switching cell and according to the principle of current-voltage duality, a current-type canonical switching cell using a capacitor can help us structure current-type hybrid SC converters.

The current-type canonical switching cell is shown in Fig. 4(d), which is composed of two switches and one transferring capacitor. As compared to Fig. 4(a), the connection in Fig. 4(d) between actives and passives is transformed from T-network to π-network, and the key parameters that characterize the switching cell are replaced by terminal current. The current-type switching cell amplifies current instead of voltage, and it can be used to form current-type power converters. For example, the current-type buck converter as shown in Fig. 4(e) can be formed by choosing I_1 and I_2 as the input and output terminals, respectively; note the output current is higher than the input current for step-down voltage conversions. In practical implementations, voltage sources are usually available and inductors are employed to transform voltage to current, e.g. from V_{in} to I_1 through L_{c1}. Note only two of the three terminals in the current-type canonical switching cell require voltage-to-current transformation since the third terminal current is just the sum of the other two and it naturally features continuous current. In Fig. 4(e), the terminals 1 and 3 are chosen since they carry less current and therefore the conduction loss on the inductors can be reduced. Similar to the voltage-type hybrid SC converter, a new current-type hybrid SC converter as shown in Fig. 4(f)

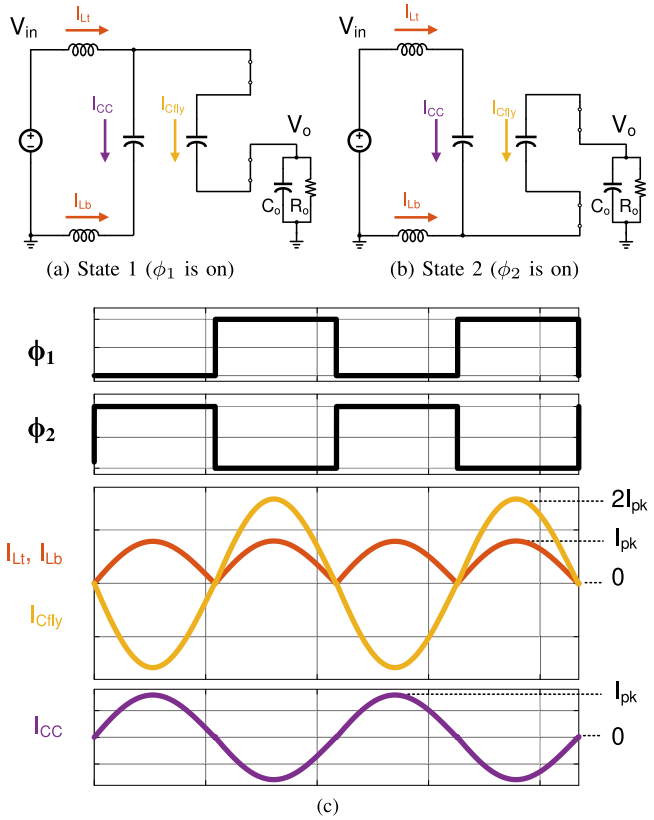


FIGURE 5. Resonant operation of a current-type hybrid SC converter using a 2-to-1 ReSC converter.

can be structured by replacing the two switches with switch-and-capacitor matrix, facilitating the relocation of the current source (inductor) from output to input.

The operational circuit states and waveform of a current-type hybrid SC converter are shown in Fig. 5. As observed from Fig. 5(a) and (b), the two inductors are always in parallel and simultaneously injecting current, I_{Lt} and I_{Lb}, into C_{fly} as well as the output, featuring lower inductor current and continuous input and output current due to the intrinsic interleaving characteristics. As a result, the volume or the available energy [31] of the two inductors, L_t and L_b, is no bigger than that of the single inductor in voltage-type hybrid SC converters:

$$2 \cdot 2L \cdot \left(\frac{I_o}{2}\right)^2 \Big|_{\text{current-type}} = L \cdot I_o^2 \Big|_{\text{voltage-type}}, \qquad (4)$$

given the same resonant frequency, $\frac{1}{2\pi\sqrt{LC_{fly}}}$, for both converters, and both L_t and L_b are $2L$. Fig. 5(c) shows the case of $D = 50\%$ where I_{Lt} and I_{Lb} have the same amplitude. The only downside of current-type hybrid SC converters is the additional transferring capacitance, C_C, which experiences the same current amplitude as L_t and L_b, leading to an unavoidable effect of C_C to the resonant operation as well as high bypass capacitance requirement. To maintain high power density, this issue can simply be addressed by combining the multi-phase interleaved technique.

B. DUAL-PHASE INTERLEAVED 4-TO-1 CONVERTER WITH BERC

Fig. 6(a) shows the BERC technique by placing the voltage-type (front) and current-type (rear) hybrid SC converters side by side, providing an opportunity to merge the inductors in the middle for an example of a 4-to-1 step-down conversion. To further reduce the capacitance requirement on C_C, another set of power converter, with control signals ϕ_1 and ϕ_2 swapped, can be added to form a dual-phase interleaved converter. In this paper, as shown in Fig. 6(b), ϕ_1 is split into Q_{1B} and Q_{2A} while ϕ_2 is split into Q_{2B} and Q_{1A} for the purpose of ZVS scheme, which will be discussed later. Compared to the conventional cascaded resonant converter shown in Fig. 2(a), the new converter with BERC technique displaces the two output inductors, L_{2a} and L_{2b}, in the second stage and implements them by two middle inductors, L_t and L_b. The new location of L_t is now shared between the output of the first stage and the input of the second stage, allowing the absorption of the other two inductors, L_{1a} and L_{1b}, in the conventional first stage. As a result, through BERC technique, less inductors are required and higher power density is possible.

There are mainly two circuit states for operating BERC, with the driving signals ϕ_1 and ϕ_2 working in a complementary fashion. To achieve zero current switching (ZCS), the converter will be switched at resonant frequency, f_{res}, with the $Q_{1B} - Q_{2A}$ pair assigned the same as ϕ_1, and the $Q_{1A} - Q_{2B}$ pair as ϕ_2, i.e. $Q_{1A} = Q_{2B} = \overline{Q_{2A}} = \overline{Q_{1B}}$. Note that a dead-time is added between ϕ_1 and ϕ_2 to prevent shoot-through events. During state 1 or when $Q_{1B} - Q_{2A}$ is toggled high, the equivalent circuit of the BERC is formed as shown in Fig. 7(a); while for state 2, the equivalent circuit is obtained by simply interchanging the locations of C_{1a} and C_{1b} as well as C_{2a} and C_{2b}. The nominal blocking voltage is $V_{in}/2 = 2V_o$ for switches and capacitors in the first stage; and $V_{in}/4 = V_o$ for those in the second stage, except that $2V_o$ is needed for C_C.

In order to understand the resonant frequency, f_{res}, of BERC, an ac equivalent circuit of Fig. 7(a) can be obtained as shown in Fig. 7(b). It is practical to assume that the input and output capacitance, C_{in} and C_o, are much larger than the flying capacitance, C_{1a-2b}, and therefore V_{in} and V_o can be assumed shorted to ac ground with low ac impedance across C_{in} and C_o. Other than that, owing to the bypass capacitor current cancellation by multiphase interleaving technique as highlighted and discussed in Section II-A, the equivalent capacitance at C_C across V_{swt} and V_{swb} can be made sufficiently large such that the ac impedance is dominated by C_{2a} and C_{2b} in stage 2. In order to keep the same resonant frequency for both states 1 and 2, it is designed that $C_{2a} = C_{2b} = C_2$; further, $C_{1a} = C_{1b} = C_1$ is considered for symmetric printed circuit board (PCB) layout. As a result, there are two independent resonant tanks formed by L_t and L_b: (i). $L_t - C_2//2C_1$ and (ii) $L_b - C_2$. For control simplicity, the resonant frequency, f_{res},

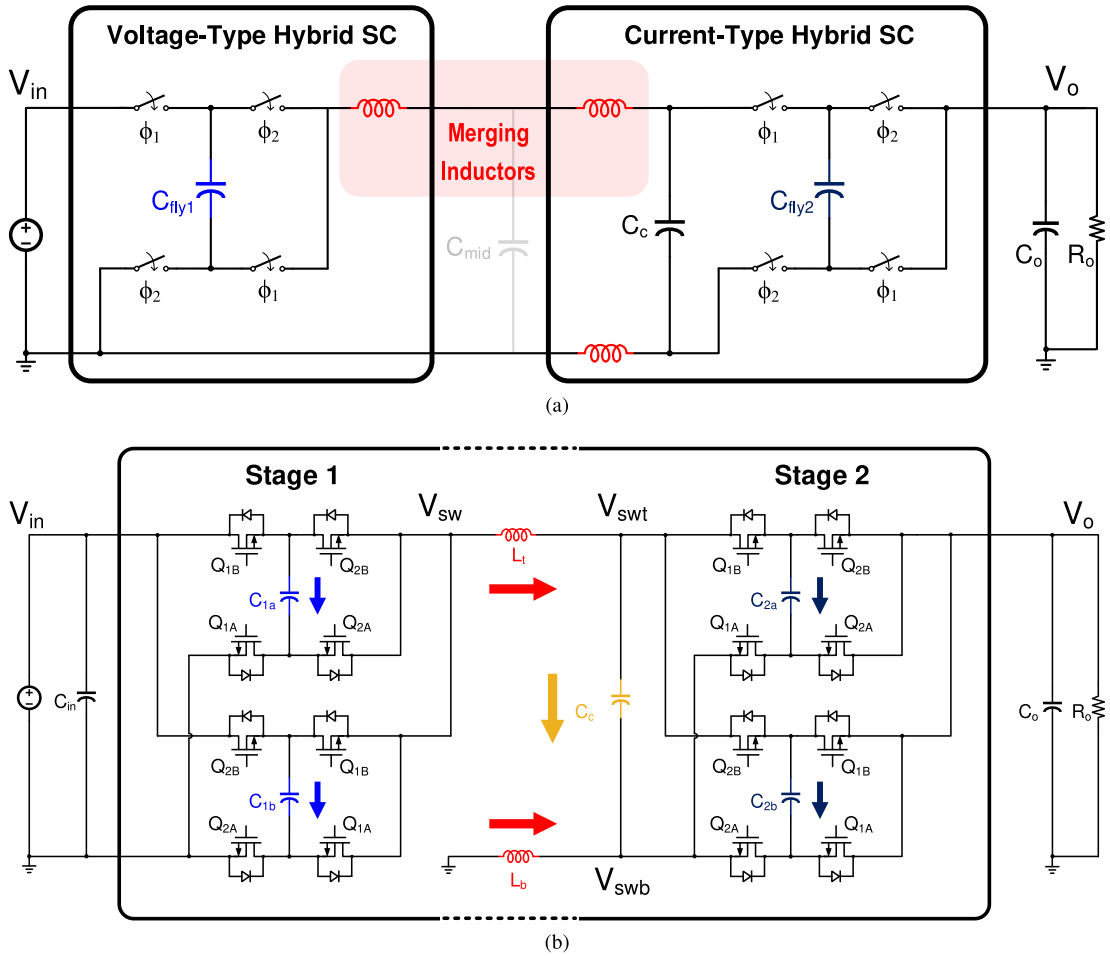


FIGURE 6. (a) Bi-lateral Energy Resonant Conversion (BERC) technique using voltage- and current-type hybrid SC converters and (b) a dual-phase interleaved 4-to-1 converter with BERC.

of both tanks are equalized:

$$f_{res} = \frac{1}{2\pi \cdot L_t \cdot \left(\frac{1}{2C_1} + \frac{1}{C_2}\right)^{-1}} = \frac{1}{2\pi \cdot L_b \cdot C_2}. \quad (5)$$

After some manipulations, (5) becomes

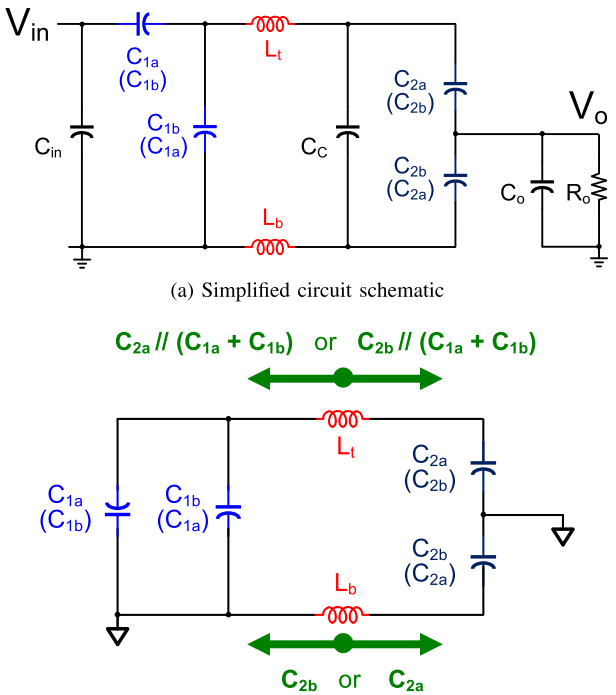
$$\frac{L_t}{L_b} = \frac{2}{\frac{C_2}{C_1} + 2}, \quad (6)$$

which expresses the ratios of LC design for stages 1 and 2. Considering the electrical operating conditions and energy densities of the passive components in different stages, there exist an optimal relationship between C_1, C_2, L_t and L_b in order to achieve the smallest form factor with a reasonable resonant frequency. For example, C_1 sustains higher voltage than that of C_2; therefore, less capacitance density is available for C_1, and smaller capacitance on C_1 and larger inductance on L_t can be expected. In this work, $C_1 = 0.5 \cdot C_2$ and $L_t = 2L_b$, for simplicity and compactness of PCB layout.

The key waveform for BERC operating around its resonant frequency is shown in Fig. 8, following the passives design suggested by (6). It can be observed that $I_{Lt} = I_{Lb} = |I_{C2a}| = |I_{C2b}| = 2|I_{C1a}| = 2|I_{C1b}|$, and all resonant tanks resonate with the same frequency. Equalizing the resonant frequency helps evenly distribute the output current between two inductors and lowering the component current stress. The shared inductor, L_t, bridges between the flying capacitors of both stages, collecting the output current from stage 1 and emitting it to stage 2 through I_{Lt}; meanwhile, L_b is providing a continuous current to the flying capacitor not involved with L_t in a given phase, e.g. C_{2b} in state 1. Also, it can be observed that symmetries between I_{Lt} and I_{Lb} as well as I_{C2a} and I_{C2b} mutually cancel the current processed at the top and the bottom plates of C_C, greatly reducing the capacitance requirement and further justifying the assumption made in Fig. 7(b).

C. PERFORMANCE COMPARISON

Many hybrid switched-capacitor converter topologies have been investigated and compared in prior research [15], [16], [17], [18], [19], [20], and the cascaded resonant converter has been demonstrated, in theory and experiment, to be an excellent candidate for achieving high power density and high



(a) Simplified circuit schematic

(b) ac equivalent circuit

FIGURE 7. Simplified circuit schematic and ac equivalent circuit of a dual-phase interleaved 4-to-1 converter with BERC during state 1 (or state 2).

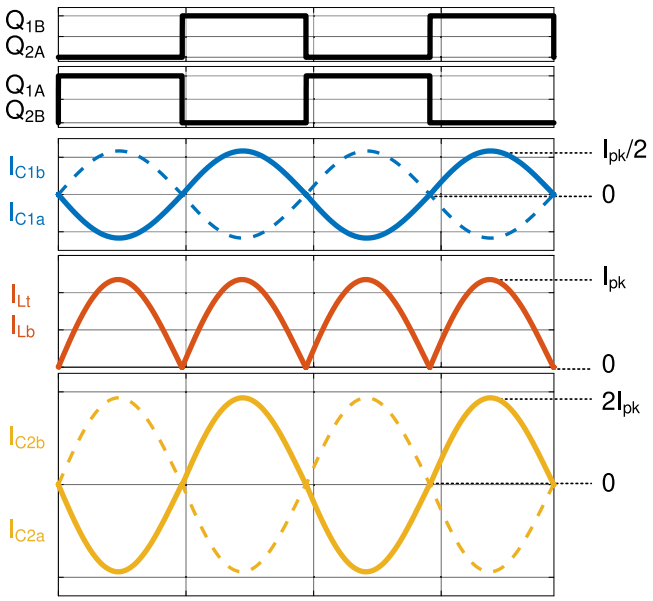


FIGURE 8. Key operational ZCS waveform of a dual-phase interleaved 4-to-1 converter with BERC.

TABLE 1. Key Differences Before and After Applying BERC Technique on Two-Phase Interleaved Cascacded Resonant Converter, Where Each Phase Has Two 2-to-1 ReSCs

	Before BERC	After BERC
Number of inductors	4	2
Avg inductor current	$I_o/4$ for L_{1a} and L_{1b}	$I_o/2$ for L_t
	$I_o/2$ for L_{2a} and L_{2b}	$I_o/2$ for L_b
f_{res} (1st stage)	$\frac{1}{2\pi\sqrt{L_1 C_1}}$	$\frac{1}{2\pi \cdot L_t \cdot \left(\frac{1}{2C_1'}+\frac{1}{C_2'}\right)^{-1}}$
f_{res} (2nd stage)	$\frac{1}{2\pi\sqrt{L_2 C_2}}$	$\frac{1}{2\pi \cdot L_b \cdot C_2'}$

peak efficiency. The BERC technique can be generally applied in different topologies when cascading stages for higher conversion ratios. In this section, the conventional cascaded resonant converter with independent two stages and two-phase interleave operation is used for comparison, and Table 1 lists the converter requirement before and after applying the BERC technique.

A middle capacitor or transferring capacitor is required by both approaches for the energy conversion between two inductor currents, i.e. $--I-V-I--$: the conventional one needs the capacitor to decouple between stages, whereas the BERC technique requires the capacitor in its current-type converter. Ideally, this middle capacitor current is zero given the two-phase interleave operation and 50% duty ratio, and therefore the middle capacitor can be very small when the resonant frequencies in both stages match, i.e. $f_{res1} = f_{res2}$. However, there are many practical factors that lead to unmatched resonant frequencies, such as process variation and stress coefficient (primarily voltage and temperature) on the passive components. The variation in resonant frequencies further creates unmatched inductor current between stages, and the middle capacitor requirement is determined by the current mismatch, i.e. $\Delta I_L \propto C_C$, between stages 1 and 2, which is validated to be small through experiments shown in section V. After applying the BERC technique, the output voltage ripple can be expressed as

$$\Delta V_o = \frac{I_o}{C_o \cdot 2\pi f_{sw}} \left(\sqrt{\pi^2 - 4} - \pi + 2 \arcsin \frac{2}{\pi} \right) \quad (7)$$

during its resonant operation, which is the same as the original converter. Note the output current of the current-based converter at the second stage is continuous, even though the inductor is not directly at the output.

The key benefit of the BERC architecture is the reduction in the number of inductors, which helps improve the power density by reducing passive component sizes, and hence the overall converter size. The BERC also benefits from the same current rating for both inductors, which simplifies the PCB layout and allows further miniaturization. In theory, to understand the volume difference before and after the BERC technique, the total energy processed by the inductors and capacitors can be compared as follows:

$$\begin{cases} \text{Vol}_{\text{before}} = 2\alpha \sum_{i=1,2} \frac{1}{2} L_i I_i^2 + 2\beta \sum_{i=1,2} \frac{1}{2} C_i V_i^2 \\ \text{Vol}_{\text{after}} = \alpha \sum_{i=t,b} \frac{1}{2} L_i I_2^2 + 2\beta \sum_{i=1,2} \frac{1}{2} C_i' V_i^2 \end{cases}, \quad (8)$$

where $I_{1,avg} = I_o/4$, $I_{2,avg} = I_o/2$, $V_1 = 2V_o$, $V_2 = V_o$ and α and β are volumetric factors for inductors and capacitors. For the sake of simplicity, it is assumed that both converters

have the same resonant frequency (ans therefore the same switching loss), $L_b = L_2$ and $C_2' = C_2$. The volume reduced by the BERC technique is

$$\mathrm{Vol}_{\mathrm{reduced}} = \alpha\left(\frac{1}{4}L_1 + \frac{1}{2}L_2 - \frac{1}{2}L_t\right)I_2^2 + \beta\left(C_1 - C_1'\right)V_1^2. \tag{9}$$

From (9), more volume can be reduced when choosing L_t closer to L_b or L_2, since α/β is fairly large [16], i.e. larger than 100. In the case of $C_1 = 0.5C_2$ and $L_t = 2L_b$, it is expected that $\mathrm{Vol}_{\mathrm{reduced}} > 0$ when $L_1 > L_2$ is chosen in the conventional approach. An example of $L_1 = 3.6L_2$ from the prior art [5] gives $\mathrm{Vol}_{\mathrm{reduced}} \approx 0.4\alpha L_2 I_2^2$, showing the possible passives reduction when applying the BERC technique and therefore pushing toward higher power density.

Maintaining high efficiency while increasing power density is challenging, since these two perfomance indices are tied to each other in an inverse relationship given the same converter topology. To understand the converter efficiency, the power loss can be generally broken down into conduction, P_{cond}, switching, P_{sw}, and VI-overlap losses, P_{ov}, [32]

$$P_{loss} = P_{cond}(I_o) + P_{sw}(f_{sw}) + P_{ov}(V_o, I_o, f_{sw}), \tag{10}$$

which are functions of output current, output voltage, and switching frequency. The conduction loss, which dominates the heavy-load region and full-load efficiency consists of switch on-resistance, R_{on}, PCB trace, $R_{\mathrm{PCB,trace}}$, and inductor resistance, R_{ind}:

$$P_{cond} = k \cdot \sum_{i=1,2}\left[I_i^2\left(4R_{on,i} + 2R_{\mathrm{PCB,trace,i}} + \sum R_{ind,i}\right)\right]. \tag{11}$$

In (11), each stage of the cascaded converter has two interleaved phases, and each phase always has two switches turning on and one lumped $R_{\mathrm{PCB,trace}}$. Eq. (11) represents the general conduction loss for cascaded resonant converters: (i) the conventional approach has an inductor for each phase of a stage and $\sum R_{ind,i} = 2R_{ind,i}$; (ii) the BERC technique merges the inductors and $\sum R_{ind,1} = 0$ and $\sum R_{ind,2} = 3R_{ind2}$ for the case of $L_t = 2L_b = 2L_2$. As a result, the power loss difference at the inductor, before and after applying the BERC technique, can be expressed as

$$\begin{aligned}\Delta P_{ind} &= k \cdot \left(2I_1^2 R_{ind1} + 2I_2^2 R_{ind2} - 3I_2^2 R_{ind2}\right) \\ &= k \cdot I_2^2\left(\frac{1}{2}R_{ind1} - R_{ind2}\right).\end{aligned} \tag{12}$$

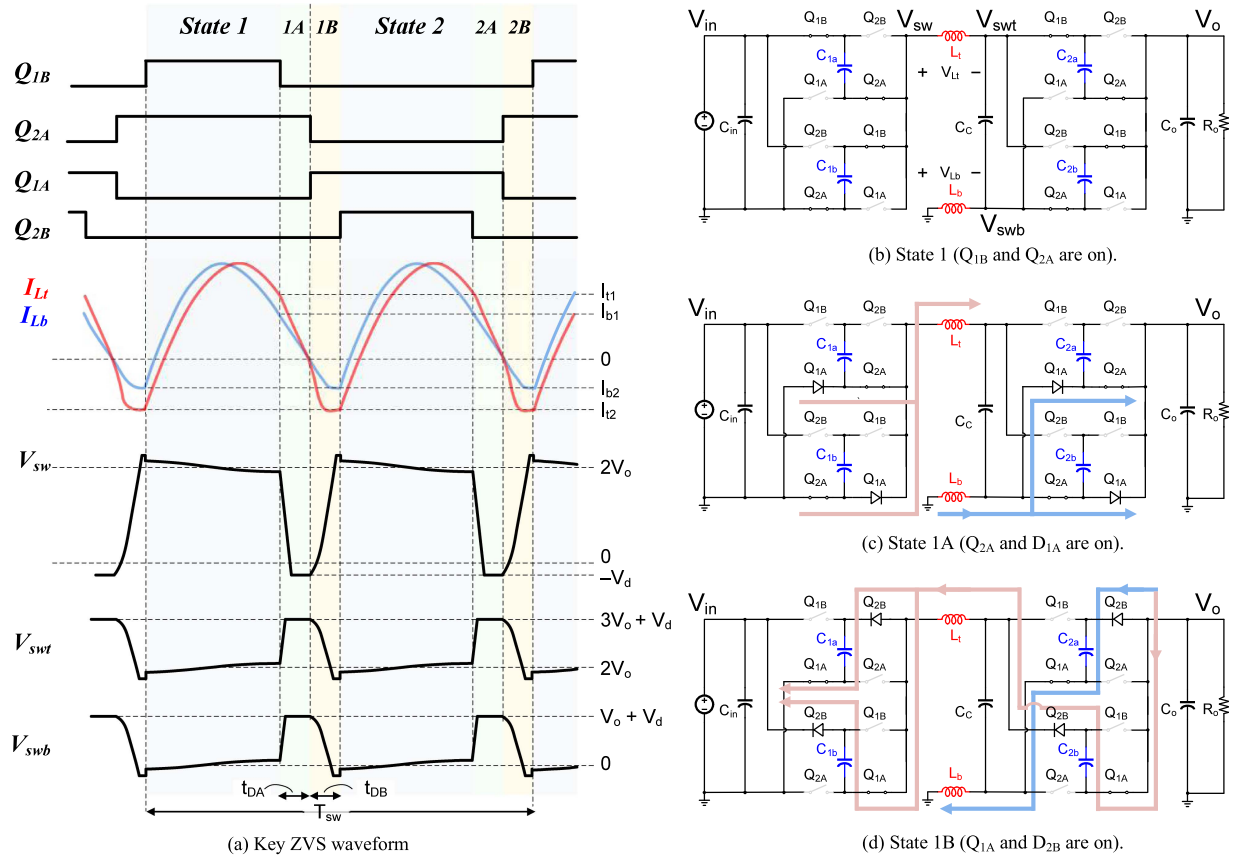
Given the same package size, inductor resistance generally increases with inductance due to more winding required. In the case of [5], the first stage uses XAL6030-181MEL (180 nH, 39 A) with $R_{ind1} = 1.75\ m\Omega$, whereas the second stage uses SLC7530S-500ML (50 nH, 50 A) with $R_{ind2} = 0.123\ m\Omega$. As a result, employing BERC technique reduces the inductor loss by $0.75\ m \cdot kI_2^2$. For the switch conduction loss, the two compared approaches share the same number of switches and switch utilization, and the only difference comes from switch technology nodes. As opposed to the conduction loss, the switching loss determines the light-load efficiency, and it can be expressed as

$$P_{sw} = \left(\sum Q_g V_{gs} + \sum Q_{oss} V_{block}\right) \cdot f_{sw}. \tag{13}$$

where Q_g and Q_{oss} are the total gate charge and output charge, respectively. The power loss of $\sum Q_g V_{gs} f_{sw}$ will be indicated by the gate driver loss in the measurement section and the reduction of $\sum Q_{oss} V_{block}$ will be illustrated in the next section. Switching loss does not change much after the BERC technique, since the same resonant frequency (and therefore the same switching frequency can be chosen) and same number of switches were chosen. Overall, the BERC technique contributes to reduce the inductor size and loss, and therefore pushing toward higher power density and higher efficiency simultaneously.

IV. ZERO VOLTAGE SWITCHING (ZVS) TECHNIQUE

The large-swing inductor current while operating around resonant frequency provides design freedoms in achieving soft-switching operation. While the ZCS switching mechanism developed in the previous section significantly reduces the VI overlap loss during switching transitions, the switching loss, $P_{oss} = C_{oss} V_{block}^2 f_{sw}$, correlated with the transistor output referred capacitance, C_{oss}, remains a large part of power losses; particularly, for light-load, high-voltage and high-switching-frequency conditions. Therefore, there is a strong need to implement ZVS turn-on techniques for further improvement in light-load efficiency. To eliminate the switching losses, the ZVS operation charges and discharges C_{oss} through an inductive current: (i). discharging C_{oss} of turning-on switches – the residual capacitive energy stored across V_{ds} is brought down to zero (practically, a body diode voltage drop, $-V_d$); (ii). charging C_{oss} of turning-off switches – the required blocking voltage is built up before their neighboring switches are about to turn on. These two conditions coexist, serving as important indicators of the ZVS completeness, e.g. a complete ZVS operation should have turned-on body diodes for turning-on switches and nominal blocking voltage ready for turning-off switches before the switch turn-on events. In order to turn on the body diodes, the conducting direction of the body diode and the inductor current should align with each other. For the dual-phase interleaved 4-to-1 converter as shown in Fig. 6(b), all switches can be divided into two groups: (i). pointing toward $V_o - Q_{1A}$ and Q_{2A}; (ii). pointing toward $V_{in} - Q_{1B}$ and Q_{2B}, which means the inductor current needs to be bi-directional in order to achieve ZVS turn-on for all switches. The proposed switching scheme to achieve ZVS operation is shown in Fig. 9(a). Four more auxiliary states are added on top of the original main states 1 and 2, including states 1 A, 1B, 2 A and 2B. The duration for states 1 A and 2 A is defined as t_{DA}, and t_{DB} for states 1B and 2B. Different from the ZCS scheme, the pulse width of Q_{1B} (Q_{2B}) is smaller than that of Q_{2A} (Q_{1A}) in order to form states 2B and 1 A (1B and 2 A), which help create negative and positive inductor current, respectively.



(a) Key ZVS waveform

(b) State 1 (Q_{1B} and Q_{2A} are on).

(c) State 1A (Q_{2A} and D_{1A} are on).

(d) State 1B (Q_{1A} and D_{2B} are on).

FIGURE 9. Zero voltage switching techniques for a dual-phase interleaved 4-to-1 converter with BERC.

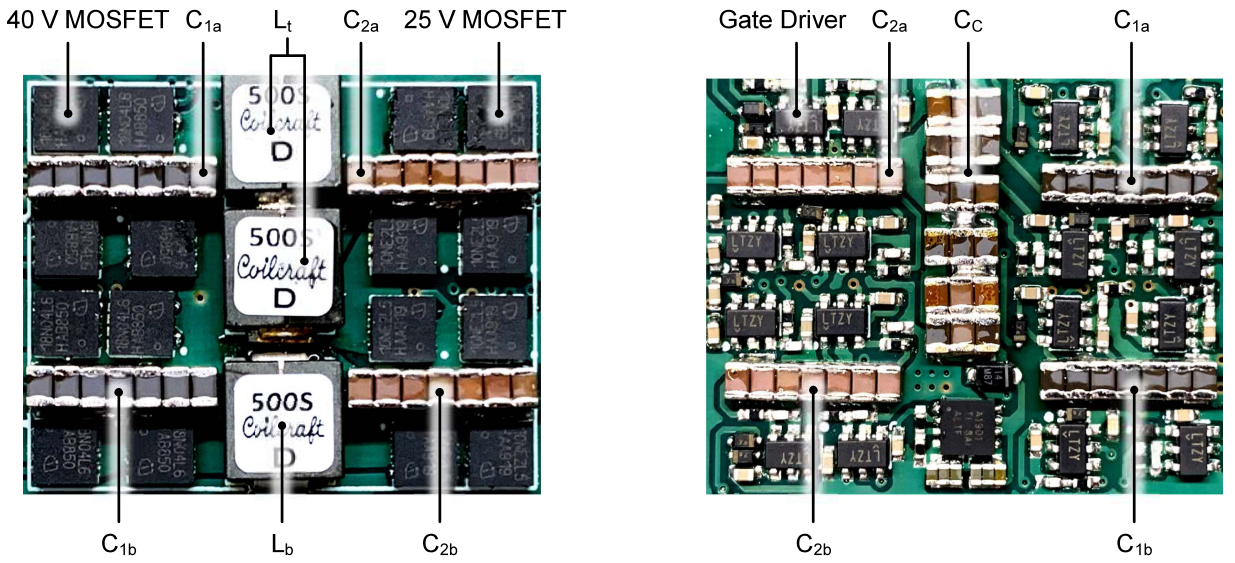
During state 1, the circuit schematic is shown in Fig. 9(b) with Q_{1B} and Q_{2A} turned on. As the converter transitions into state 2, it undergoes states 1 A and 1B to smoothly turn on Q_{1A} and Q_{2B}, respectively. At first, the converter enters state 1 A by turning off Q_{1B} while I_{Lt} and I_{Lb} are still positive, i.e. $I_{1t}, I_{1b} > 0$, which can be achieved by running the converter at a switching frequency moderately higher than the resonant frequency, i.e. $f_{sw} > f_{res}$. As shown in Fig. 9(c), the positive I_{Lt} and I_{Lb} align with the conducting directions of D_{1A} in the first and second stages, pulling the residual charge across Q_{1A} away and meanwhile building the blocking voltage, $2V_o$ (V_o), up across Q_{2B} in the first (second) stage. To achieve full ZVS on all Q_{1A} switches [33],

$$\begin{cases} \frac{1}{2}L_t I_{t1}^2 > \sum Q_{oss1} \cdot (2V_o) \\ \frac{1}{2}L_b I_{b1}^2 > \sum Q_{oss2} \cdot V_o \end{cases}, \tag{14}$$

where Q_{oss1} and Q_{oss2} represent the switch Q_{oss} of the first and second stages, I_{t1} and I_{t2} have to be large enough to discharge Q_{oss} of turning-on switches, Q_{1A}, and charge Q_{oss} of turning-off switches, Q_{1B}. Note that I_{t1} is greater than I_{b1} since L_t needs to take care of more switches and higher parasitic capacitor voltage; the condition of $I_{t1} > I_{b1}$ is naturally achieved when both stages employ the same ZVS switching scheme. The ZVS process is deemed completed when: (i) stage 1, V_{sw} ramps down to $-V_d$; (ii). stage 2, V_{swt} and V_{swb} climb up with an increment of $V_o + V_d$ due to the connection between V_{swb} and V_o through D_{1A}. At this moment, switches controlled by Q_{1A} are ready for ZVS turn on.

State 1 A reverses the inductor current and creates the conditions of $V_{swb} = V_o + V_d > 0$ and $V_{swt} - V_{sw} = 3V_o + 2V_d > 0$, guaranteeing negative inductor current in the upcoming state, i.e. state 1B. On the other side, to prevent D_{1A} from turning back off and undermining the ZVS process, t_{DA} cannot be extended too long and the converter needs to enter state 1B with the pair of $Q_{2A} - Q_{1A}$ toggled before I_{Lt} and I_{Lb} becoming too negative. After entering into state 1B, both negative inductor voltage and negative inductor current enable Q_{oss} removal across all Q_{2B} as shown in Fig. 9(d): stage 2, V_{swb} is targeting $V_o - V_{C2a} - V_d$ and so V_{swt} is being dragged down to $3V_o - V_{C2a} - V_d$; meanwhile stage 1, V_{sw} is increasing toward $2V_o$ with more time as compared to the final values for V_{swt} and V_{swb}. During this process, I_{Lt} and I_{Lb} keep decreasing until the inductor voltage is close to 0, which correspond to relatively constant current, i.e. I_{t2} and I_{b2}. As a result, to achieve full ZVS on all Q_{2B} switches, I_{t2} and I_{b2} are only responsible for the remaining voltage:

$$\begin{cases} \frac{1}{2}L_t I_{t2}^2 > \sum Q_{oss1} \cdot (V_{C1a} + V_{C2a} - 3V_o + 2V_d) \\ \frac{1}{2}L_b I_{b2}^2 > \sum Q_{oss2} \cdot (V_{C2a} - V_o + V_d) \end{cases}, \tag{15}$$



(a) Top view (b) Bottom view

FIGURE 10. Prototype photograph of the dual-phase interleaved 4-to-1 converter with BERC, dimensions: 0.819 in x 1.016 in x 0.217 in (or 2.08 cm x 2.58 cm x 0.55 cm).

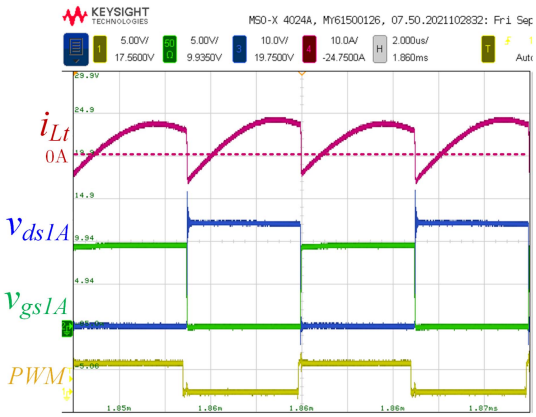
TABLE 2. Main Components for the BERC PCB and Their Specifications

Component	Part Number	Specification
Stage-1 MOSFET Switch	Infineon BSZ018N04LS6	40 V, 40 A, 1.8 $m\Omega_{max}$ @ 10 V_{GS}
Stage-1 Flying Capacitor, C_1	C2012X5R1V226M125AC	35 V, 22 μF x 21 for each
BERC Top Inductor, L_t	Coilcraft SLC7530S-500	50 nH, 50A_{sat}, 0.123 $m\Omega_{nom}$ x 2
BERC Bottom Inductor, L_b	Coilcraft SLC7530S-500	50 nH, 50A_{sat}, 0.123 $m\Omega_{nom}$
Transferring Capacitor, C_C	C2012X5R1V226M125AC	35 V, 22 μF x 18
Stage-2 MOSFET Switch	Infineon BSZ010NE2LS5	25 V, 40 A, 1 $m\Omega_{max}$ @ 10 V_{GS}
Stage-2 Flying Capacitor, C_2	C2012X6S1C226M125AC	16 V, 22 μF x 21 for each
Gate Driver	Analog Devices LTC4440	80 V, 2.4 A pull up, 1.5 Ω pull down
Microcontroller	TI TMS320F28069	32-bit, 90 MHz

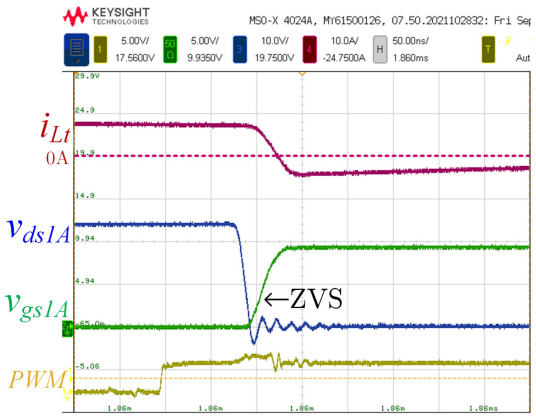
where $V_{C1a} + V_{C2a} \approx 3V_o$ and $V_{C2a} \approx V_o$; therefore, I_{t2} and I_{b2} requirement can be easily met. At the end of state 1B, Q_{2B} is ready for ZVS turn on and the converter is prepared for smooth transition to state 2. Accordingly, the ZVS turn-on process from state 2 to state 1 can be derived, which has similar inductor current flow, both positive and negative, as shown in Fig. 9(c) and (d), except that D_{2A} and D_{1B} are being conducted. Note that I_{Lt} decreases steeper than I_{Lb} during ZVS states due to larger negative voltage across L_t, which in turn helps achieving $I_{t1} > I_{b1}$ and also maintaining similar I_{Lt} and I_{Lb} peak current.

V. MEASUREMENT RESULTS

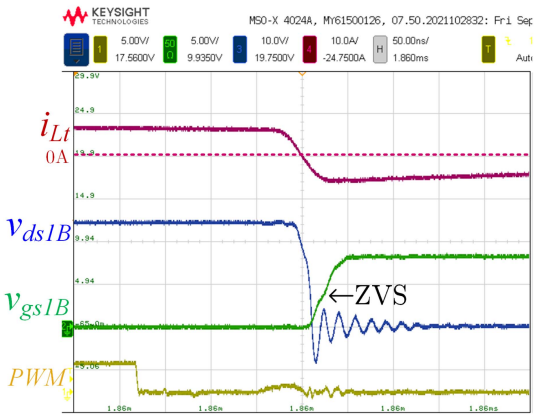
An annotated photograph of the hardware prototype is shown in Fig. 10, with main components highlighted and detailed in Table 2. The fabricated PCB has four layers, with 4-oz copper for the outer layers and 3-oz copper for the inner layers. The thick copper layers significantly reduce the trace resistance and serve as an effective heat sink, raising the converter current rating without hitting the thermal limits. High-current and high-di/dt components and return paths are all laid out closely adjacent to each other on the top layer of the PCB in order to avoid any high-resistance and high-inductance vias, reducing the conduction loss and alleviating unexpected LC resonance. All active and passive components are arranged in the most symmetric and compact way, thanks to the BERC technique. The inductor merging of the BERC technique simplifies the layout by segregating the inductors in the middle of the converter, beneficial in achieving a superior floor plan. Each stage utilizes uniform power MOSFETs, 40 V for the first stage and 25 V for the second stage, providing sufficient headroom for the 48-to-24 V power conversion. All



(a) Q_{1A} of the first stage



(b) Zoomed-in positive-edge Q_{1A} of the first stage



(c) Zoomed in positive-edge Q_{1B} of the first stage

FIGURE 11. Zero voltage switching (ZVS) waveforms.

the switches are gate driven by small-footprint LTC 4440, which supports high-voltage and high-current driving capabilities in order to reduce the switch on resistance as well as the switching VI overlap loss. Together with efficient bootstrap techniques [28] using a few auxiliary capacitors and diodes (very small footprint and low profile), all floating gate drivers are placed on the bottom layer for immediate connections with V_{gs} of the MOSFETs on the top layer. All voltage supplies around the gate drivers are well-decoupled with sufficient

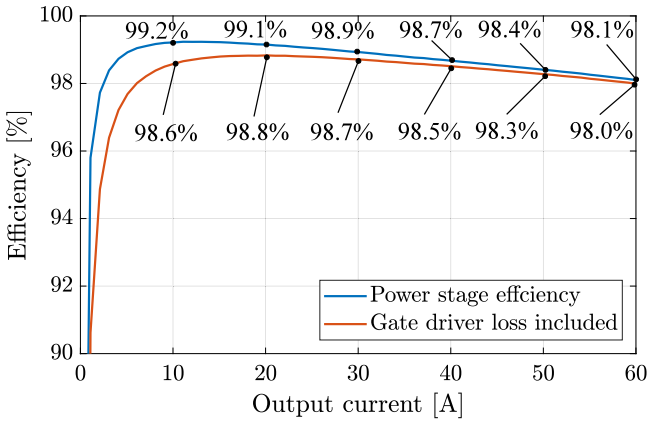


FIGURE 12. Efficiency measurement for 48 V-to-12 V voltage conversion. Efficiency measured using Yogokawa WT3000 for highest possible measurement accuracy.

capacitance to provide stable gate drive signal to the power MOSFETs. Two sets of the command signals, $S_{1A} - S_{1B}$ and $S_{2A} - S_{2B}$, are provided externally by TMS320F28069 to the gate drivers. The whole PCB prototype has everything packed in a small box volume of 0.18 in^3. Sufficient input and output capacitance are added to stabilize the input and output voltage.

The converter's key ZVS waveforms at 100 kHz are shown in Fig. 11, validating the feasibility of ZVS operations by observing the inductor current, i_{Lt}, gate-source voltage, V_{gs}, and drain-source voltage, V_{ds}. The PWM signal at the last row shows the command that generates the gate control signals for $Q_{1A} - Q_{1B}$ and $Q_{2A} - Q_{2B}$ from the microcontroller. Fig. 11(b) shows the zoomed-in waveform of Fig. 11(a) at the positive edge of V_{gs1A}. It can be seen that positive i_{Lt} brings V_{ds1A} down before V_{gs1A} is turning on, which provides evidence of ZVS turn on for Q_{1B}. Fig. 11(c) shows the positive edge of V_{gs1B}, which again shows the ZVS operation on Q_{1B}. As opposed to V_{ds1A}, V_{ds1B} is brought down by negative i_{Lt} since Q_{1B} is now at high side. Other than the ZVS operation, from Fig. 11(a), it is shown that i_{Lt} has relatively constant amplitudes for adjacent half cycles, validating that the resonant frequencies of stages 1 and 2 are similar.

The efficiency plot for 48-to-12 V power conversion is shown in Fig. 12, where the converter is operated at 86 kHz switching frequency (slightly above the resonant frequency in order to achieve low VI overlap loss as well as ZVS operation). The efficiency was measured with a Yokogawa WT3000 precision power analyzer, showing 99.2% power converter efficiency for 12 A output current and 98.8% overall efficiency (including all gate driving losses) for 20 A output current. The highest output current tested is 60 A, facilitating a very high power density of 3900 W/in^3. The temperature monitored at full-load condition is shown in Fig. 13, where the peak temperature is 68 °C with only fan cooling, thanks to the low output impedance of the proposed converter (4 mΩ in total). The output impedance is composed of topology-dependent switch utilization (≈2 mΩ), PCB trace (≈1.2 mΩ), and the

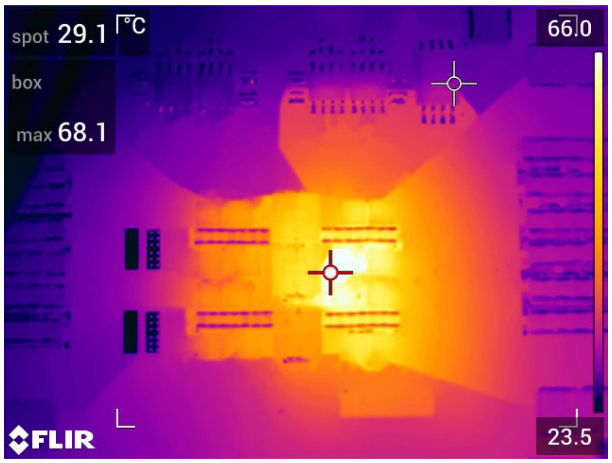


FIGURE 13. Thermal monitor at 60 A output current with fan cooling only.

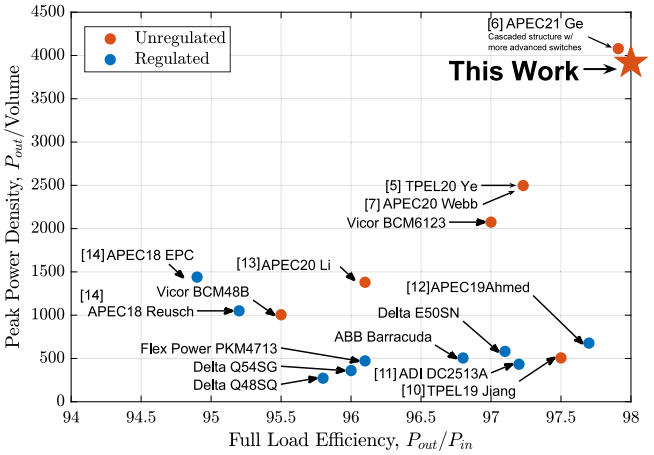


FIGURE 15. Performance comparison for 48 V-to-12 V voltage conversion.

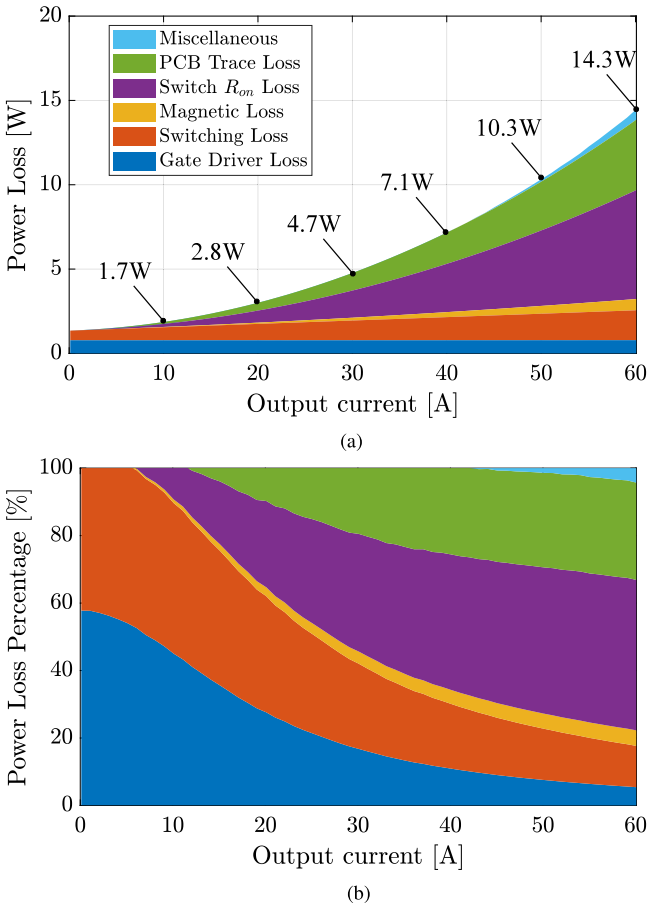


FIGURE 14. Power loss break down for 48 V-to-12 V voltage conversion.

remainder are gate driver loss, switching loss, and magnetic loss.

Fig. 14 further details the power loss breakdown over various load conditions. It can be observed that the power loss can be divided into three regions: (i). light-load condition $I_o \ll 20A$, (ii). peak efficiency $I_o \approx 20A$ and (iii). heavy-load condition $I_o \gg 20\,A$. At very light-load condition or condition (i), the power loss is mainly dominated by the gate driver and switching losses. The gate driver loss is independently monitored through a digital multimeter Keysight 34401 A. The measured gate driver loss is 0.78 W, and its estimated value is 0.74 W per (13) given that the driving voltage or V_{gs} is fixed at 10 V for all 16 switches. From (13), the gate driver loss is a simple function of f_{sw} once the driving voltage and switches are selected, it can also be seen that the gate driver loss at the bottom of Fig. 14(a) is relatively constant since the switching frequency is fixed while varying the load current. On top of the gate driver loss, two more f_{sw}-related power losses, i.e. P_{Coss} and P_{ov}, are combined into the switching loss in Fig. 14(a). As a result of the proposed ZVS scheme elaborated in Section IV, both P_{Coss} and P_{ov} are tied together with the load current. At very light load, P_{Coss} is easier to be identified and measured as 0.57 W, whereas the estimated value is 0.94 W. The distinction comes from the power loss reduction using the effective ZVS scheme in reducing P_{coss}. As load current increases, the switching loss slightly increases due to P_{ov}, which is mainly the function of load current when input-output voltage is fixed. Furthermore, other than the switching loss or the relatively fixed power loss, there is conduction loss in the shape of parabola. Take full-load condition (60 A) as the validation example, the total of the estimated PCB trace loss, switch R_{on} loss and magnetic loss is estimated as 11.2 W, whereas the measured power loss reads 11.8 W. Part of the deviation comes from resistance increases over temperature due to 40^oC temperature difference (as compared to very light-load condition), which is not modeled in the estimation. Between heavy and light load conditions, the optimal efficiency occurs when f_{sw}- and I_o-related power losses are balanced.

This work is also compared with the state-of-the-art 4-to-1 converters as shown in Fig. 15. While there is a tradeoff in simultaneously achieving high power density and high efficiency in regulated works, the unregulated ones are gaining momentum in pushing toward very high performance. In particular, the cascaded or two-stage topologies provide

promising results; this work, employing the BERC technique, achieves high performance with older technology switches (higher R_{dson}).

VI. CONCLUSION

This paper presents a novel inductor merging technique (BERC) in conjunction with multiphase interleaving, greatly improving the passive utilization of hybrid SC converters. It is shown that the developed current-type hybrid SC topologies does not only enable the BERC techniques, but also features an alternative interleaving technique for scaling up the output current. In theory and with a hardware prototype, we have demonstrated that the BERC technique can greatly improve the 48-to-12 V power delivery in data-center applications. The converter prototype enables an extremely high power density of 3900 W/in^3 for 48 V-to-12 V applications, which is 28 % improvement compared to the conventional cascaded resonant converter, and the highest published performance to date for this class of converters. A ZVS technique specifically tailored for BERC improves the light load efficiency and enables a peak power converter efficiency of 99.2%, while maintaining very high efficiency at heavy load condition. While the analysis and experiments were primarily performed for 2-to-1 ReSC, the BERC technique can be extended to general two-stage ReSC converters [21] for higher conversion ratios.

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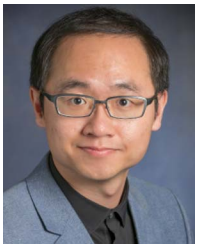

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