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Implementation of Time Division Multiplexing With Commercial Flyback Controller for Multi-Outputs USB Power Delivery Charger

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ABSTRACT Universal serial bus power delivery (USB-PD) chargers are more attractive to consumers with multiple output ports where more devices can be charged simultaneously. Existing multiple-port charger designs take multi-stage approaches, which increases power loss, charger size, and cost. This paper addresses this issue by presenting a time-division multiplexing (TDM) quasi-resonant (QR) flyback converter that eliminates the buck converter stages with simple and commercial analog implementations without the need of microprocessors. The circuit operation and practical design considerations are discussed in detail. An universal AC input, dual-USB-C GaN prototype validates the concept, while demonstrating USB-PD compliant operation, passed conducted EMI, and superior efficiency which passes the most stringent efficiency standards with margin where the benchmark GaN charger fails. Thanks to the elimination of buck stages, the proposed dual-USB-C charger achieves 1.9 W/cm^3 uncased power density, close to that of single-USB-C charger.

INDEX TERMS USB-PD, quasi-resonant flyback, time-division multiplexing, Gallium Nitride (GaN) device.

I. INTRODUCTION

USB power delivery (PD) has unified the charging standard for most consumer electronics devices since 2012 and the latest USB PD version 3.1 standard has extended the output power up to 240 W [1], further broadening its potential to supply gaming laptops, docking stations, 4 K monitors and beyond. A USB-PD charger's output needs to be automatically adjusted to a voltage level according to the device's requirement. For example, mainstream phones can work with 5 V or 9 V charging, laptops usually require 20 V for its higher voltage batteries. USB-PD chargers supporting those applications should provide real-time adjustable output voltages over 5–20 V range. This wide output voltage range, together with the universal input range (90–264 Vac wide) requirement, poses design challenges on the USB-PD chargers. This has been addressed by adopting typologies such as quasi-resonant or active clamp flyback [2] [3], current-source resonant converter [4], cascaded switched-capacitor converter [5], and two-stage architecture [6], as well as advanced controls [7] and [8]. Power density can also be improved by shrinking the double-line-frequency dependent bulk capacitor by using a half-bridge series-stacked buffer [6] or a self-driven thyristor [9].

A charger equipped with multiple USB-PD outputs boosts user convenience by allowing simultaneously charging of multiple devices. As USB-PD charger normally uses USB Type-C connectors at the output, for simplicity, in this paper we designate the charger with multiple USB-PD outputs as multi-USB-C charger. With the rapid adoption of USB-PD for most building plug loads, multi-USB-C chargers can also be integrated as part of the building electrical infrastructure (such as a wall socket) to provide most user benefits and ultimately, reduce the number of chargers to be manufactured and disposed as electronic wastes at end-of-life.

When it comes to topology, most multiple-output USB-PD chargers adopt a two-stage configuration which consists of 1)

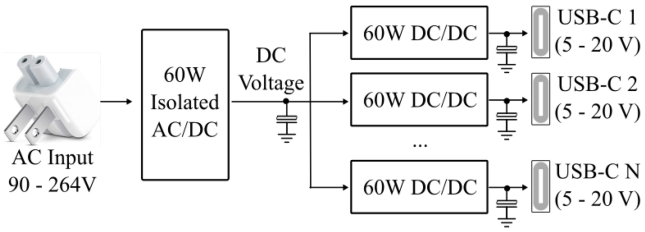

FIGURE 1. Conventional two-stage power architecture for a 60 W multi-USB-C USB-PD chargers. Each DC/DC is fully rated at 60 W to enable "blind plug-in" feature where each output can provide.

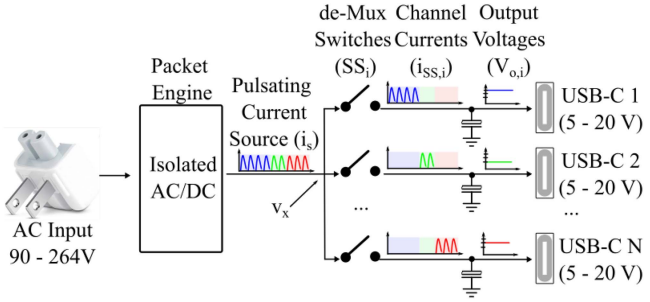

FIGURE 2. Time division multiplexing scheme concept to realize power converter with multiple outputs. The AC/DC converter or the packet engine generates a pulsating current source, which get dispatched by the de-MUX switch to each port at the respective time frame.

an isolated AC-DC front-end stage to interface with universal line input, achieve galvanic isolation, and generate a regulated DC voltage, and 2) multiple non-isolated DC-DC converters to provide independently adjustable outputs in compliance with the USB-PD power requirement. The output of the AC-DC stage is often selected at about 22 V that is slightly higher than USB-PD output range of 5-20 V if buck topology is used at the DC/DC stages. The power architecture for a 60 W charger is shown in Fig. 1. Besides the 60 W isolated AC/DC stage, it is noteworthy that each DC/DC converter is also rated at full 60 W so that each port can provide 60 W in single-port mode, regardless of the port selection at plug-in, designated as the feature of "blind plug-in". Lowering the power ratings of specific DC/DC converters result in different power capability across the USB-C ports, which is not preferred because the dedicated markings to differentiate those output ports confuse consumers, especially when the number of output ports increases. "Blind plug-in" therefore provides the best user experience. The solution in Fig. 1 to achieve "blind plug-in" is intuitive and simple. However, it also lacks of techno-economical scalability at high port numbers since each additional port will need one fully rated DC/DC converter, which increases cost and size.

In order to reduce cost and size, it is possible to combine the two stages by multi-purposing some key components, either active switches or passive components (e.g. magnetics). Active-switch sharing topologies normally take advantage of redundant switching state that can be configured to generate more regulated outputs, such as [10] using the synchronous rectifier as a controlled switch, [11], [12] to using duty cycle and frequency, and [13] using duty-cycle and phase-shift. Compared to active switch sharing, magnetic component sharing scheme benefits system density more since those components are major size contributors in a power converter. One prominent example of this concept is researched broadly as single-inductor-multiple-outputs (SIMO) converter [14], [15]. The energy stored in the inductor can be shared by time frames, and during each designated time frames, energy is transferred to a specific output. In this way, the energy is distributed following a time-division multiplexing (TDM) scheme. Existing TDM-based implementation [15], [16], [17], [18] all use a digital signal processor (DSP) to generate clocked time frames to implement TDM, which increases implementation cost and renders them impractical for low-power USB PD applications. Furthermore, light load management for TDM implementation is rarely discussed in literature, impeding its adoption in practical production which has to meet stringent efficiency standards at various load conditions (10%, 25%, 50%, 75%, and 100% load), such as European Union's CoC Tier 2 and U.S. Depart of Energy Level VI [19].

We proposed in [20] using simple analog circuitry which can conveniently work with commercial quasi-resonant (QR) flyback controllers to achieve multiplexing operation. This paper provides more theoretical analysis and implementation details of the proposed converter. An universal input, dual-port USB-PD charger using GaN power IC was designed, which demonstrated smooth operation through no load to full load at various output voltage combinations, also in compliance with USB-PD protocol requirement. The resultant charger achieves high efficiency, high power density, and low component count, which promises industry adoption. The rest of the paper is organized as follows: Section II and III brief the concept of TDM and QR flyback operation, respectively. Section IV details the implementation of the proposed TDM QR flyback using commercial-available analog controller. Section V provides the experimental results of the built GaN-based Dual-USB-C charger. Section VI concludes the paper.

II. TIME DIVISION MULTIPLEXING CONCEPT FOR MULTI-OUTPUTS CONVERTER

Although TDM scheme has been used for different topology, the fundamental concept stays the same. There will be a packet engine comprised of semiconductor switches and passive components that generate energy packets, a de-multiplexing (de-MUX) switch network to distribute the energy packets to different outputs, a filter network to reconstruct the discrete energy packets back to a DC voltage, and the sensing and control elements to manage the operation of the packet engine and the de-MUX for specific control target, including independent regulation of the output voltages. Fig. 2 shows a high-level illustration of the TDM concept, such as packet engine, de-MUX switches, and output capacitors as filters, implemented under the context of a 60 W multi-USB-C

charger. The sensing & control blocks are intentionally omitted for clarity herein given that they will be discussed in great details at Section IV.

Similar to the two-stage solution, an isolated AC/DC converter is still used to interface with the AC grid including rectifying the AC voltage into a DC voltage by a diode bridge and filtering the electromagnetic interference (EMI) noises originated from switching actions by inserting EMI filters. It also provides galvanic isolation for safety purpose by using a high-frequency transformer. However, the difference is that the isolated AC/DC converter (also serves as a packet engine to generate energy "packets") has a current-source type of output instead of a voltage source. The source pulsating current is de-multiplexed by the switches so each channel only receives the source current at its designated time frame and stays at zero current at the rest of the time. Each channel current charges the respective output capacitor to maintain a DC output voltage at that USB-C port. Note that there is no capacitor needed at the output of the isolated AC/DC converter thanks to its current source nature. By contrast, the two-stage solution needs a capacitor between the two stages or maintain a stable DC voltage bus.

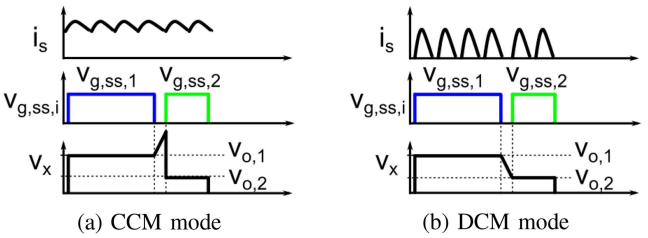

FIGURE 3. Illustrative waveforms of the de-MUX operation when the current source (i_s) is in CCM or DCM modes.

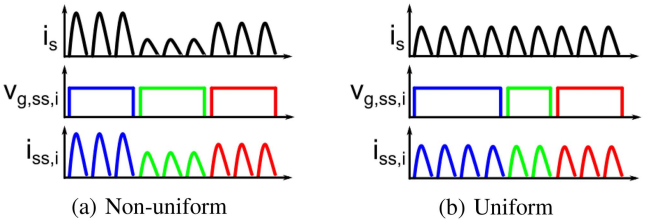

FIGURE 4. De-MUX schemes for a triple-output case showing packet engine output current i_s, de-MUX control signal $v_{g,ss,i}$, and channel current $i_{ss,i}$ using.

A. PULSATING CURRENT FORMAT: CONTINUOUS OR DISCONTINUOUS MODE

Fig. 2 illustrates the pulsating current in discontinuous conduction mode (DCM), where each current pulse resets to zero at each switching cycle. Although the packet engine's output can also be a continuous conduction mode (CCM) current source as inductor currents can also operate at CCM in most converter topologies, it comes with severe drawbacks for the targeted USB-PD application.

The most important drawback is related to the safe operation of the de-MUX switches. In multi-USB-C chargers, depending on the device types and its charging phases, each port can have a wide voltage range dynamically. It means it is impossible to pre-determine the relative voltage level between any two ports at the design phase. For instance, Port USB-C1's voltage can be either higher or lower than that of USB-C2 depending on different use cases. This requires that each de-MUX switch should be capable of blocking voltage in both directions (voltage bi-directional switches). Otherwise, any conduction of one de-mux channel can forward bias the voltage-uni-directional switch in the other channel, shorting the two output capacitors which were at different voltages and causing tremendous shoot-through current, which may damage the de-MUX switches at those two channels.

Fig. 3 illustrates the de-MUX switches operation under CCM and DCM conditions of the pulsating current source (i_s), in a dual-output case. $v_{g,ss,i}$ shows the gate voltages of the de-MUX switches where i numbers the output. In order to avoid shoothrough between the two de-MUX switches, a certain dead time has to be inserted between the two gate signals ($v_{g,ss,1}$ and $v_{g,ss,2}$). This dead time creates a "all OFF" state which let the de-MUX switches to complete the switching transition. However, this "all OFF" state also interrupts and open the current source, which charges the packet engine output (v_x) with an overshoot voltage equals to ($Is \cdot T_d/C_p$), where T_d is the dead time and C_p is the equivalent capacitance at the v_x node in the "All OFF" state, including mostly the aggregated C_{oss} of all the de-MUX switches. In the case of CCM mode (shown as Fig. 3(a)), the voltage v_x may experience an overshoot of 625 V (assume $I_s = 5\,A$, $T_d = 50\,ns$, and $C_p = 400\,pF$), which is enough to cause over-voltage failures of the de-MUX switches that are often rated around 30–40 V. By contrast, the DCM mode operation (shown in Fig. 3(b)) always ensures the de-MUX switching actions completed within the zero-current interval of the DCM current waveform, so no overshoot exists at the v_x node.

In summary, using voltage-bidirectional switches at all de-MUX positions leaves no freewheeling path for the pulsating current source. Therefore, DCM mode operation should be used to avoid opening a non-zero current source.

B. PULSATING CURRENT FORMAT: UNIFORM VS. NON-UNIFORM PACKET SIZE

The function of the de-MUX circuit is to control the switch conduction time at each port such that the number of energy packet delivered to each output to achieve the required output regulation. Fig. 4 illustrates the de-MUX schemes for a triple-output case, which shows the packet engine output current i_s, de-MUX control signal $v_{g,ss,i}$, and channel current $i_{ss,i}$ using non-uniform packets and uniform packets.

Conventional de-MUX scheme for energy packet dispatching employs non-uniform packet size using a fixed time frame length for all output ports as shown in Fig. 4(a). The $v_{g,ss,i}$ waveform shows the de-MUX switch gate signals for each port, demonstrating an equal length of time frame and equal

energy packet numbers. In case of uneven output power required among the ports, the packet size, which relates to the peack current of i_s, must be adjusted to deliver the desired amount of power. For example, the port with the highest power demand (blue) requests higher energy packets than those with lower power levels (red and green). Note that in multi-port USB PD charger applications, dramatic power imbalance among output ports can occur. For example, in the single port mode, one port delivers the full power and the other ports only consume standby power of tens of milliwatts. Therefore, the major drawback of the non-uniform packet scheme is the abrupt and dramatic changes of the packet size, which causes design challenges of the packet engine including unfavorable transient response and controller malfunction.

In comparison, a uniform packet scheme (see 4(b)) is proposed herein where the energy packet size is constant regardless of the de-MUX operation. The peak current of i_s stays constant so the energy storage components experience no transient response. Meanwhile, the controller of the AC/DC converter or packet engine will stay in one stable operating mode without erroneous mode transitions. Therefore, the uniform packet scheme decouples the packet engine from the de-MUX, which significantly simplifies the implementation and improves robustness for practical commercial adoptions.

Employing the uniform packet scheme for a two-output case, the total power P_s and output power at Port i ($P_{o,i}$) under lossless assumptions are established by

$$P_s = \frac{N \cdot E_s}{T_m} \tag{1}$$

$$P_{o,i} = \frac{M_i \cdot E_s}{T_m} \quad (i = 1, 2) \tag{2}$$

$$P_{o,1} : P_{o,2} = M_1 : M_2 \tag{3}$$

where

$$N = M_1 + M_2 \tag{4}$$

$$T_m = M_1 T_{s,1} + M_2 T_{s,2}, \; f_m = \frac{1}{T_m} \tag{5}$$

and

$$P_{o,i} = \frac{M_i \cdot P_s}{N}, \; i = 1, 2 \tag{6}$$

$$P_s = P_{o,1} + P_{o,2} \tag{7}$$

In (5), M_i is the energy packet number received by the i^{th} port, and T_m and f_m are the demultiplexing period and frequency, respectively. It should be noted that M_i can be any integer as long as they satisfy the output-power ratio in (3). Equation (6) suggests that the output power for port i is determined by the number of packets this port has received (M_i) from the overall packet stream (N).

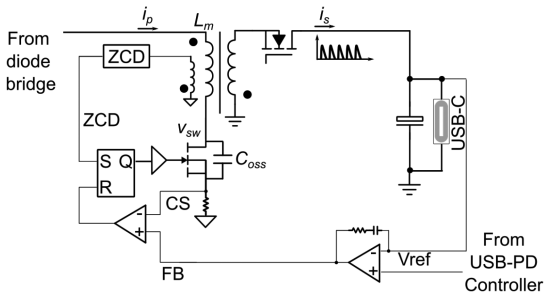

FIGURE 5. Key control architecture of a quasi-resonant flyback.

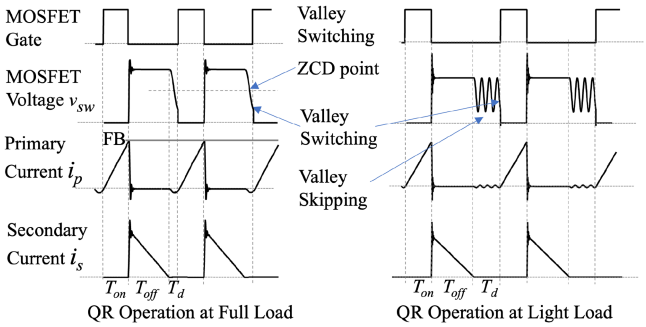

FIGURE 6. Quasi-resonant flyback key waveforms.

III. PRINCIPLES OF QUASI-RESONANT FLYBACK OPERATION

Quasi-resonant (QR) flyback topology has been widely researched, developed, and adopted commercially for isolated AC/DC converters. Over the years, analog QR-flyback controllers have been well optimized with high efficiency across wide load (zero to full load) and input/output voltage (5-6 folds at input, 6 folds at output) ranges. In order to facilitate the discussion on the proposed TDM-QR flyback implementation in the next Section, this section explains the key principles of QR flyback operations based on commercial analog controllers. More information can be found in [21], [22], [23].

The system architecture of a QR flyback is depicted in Fig. 5 with the key waveforms shown in Fig. 6.

A. VALLEY SWITCHING IN QUASI-RESONANT FLYBACK

The QR flyback uses boundary conduction mode (BCM) at heavy load so the inductor current drops to zero in every switching cycle, this means:

$$I_{P,pk} = \frac{V_{in}}{L_m} T_{on} = \frac{nV_o}{L_m} T_{off} \tag{8}$$

where L_m is magnetizing inductance, $I_{p,pk}$ is the flyback transformer peak current at primary side, V_{in} and V_o are the input and output voltages, and T_{on}, T_{off} represent the magnetizing inductor charging and discharging time, respectively. n is the transformer turns ratio from primary to secondary side. QR flyback intentionally utilizes the resonance between L_m and the switch output capacitance C_{oss} at the end of the inductor

current discharging phase (T_{off}). The MOSFET drain-to-source node voltage can be expressed as

$$v_{sw} = V_{in} + nV_o \cos(\omega_r t) \tag{9}$$

where

$$\omega_r = \frac{1}{\sqrt{L_m C_{oss}}} \tag{10}$$

At $\omega_r t = \pi$, v_{sw} reaches the valley point with a value of $V_{in} - nV_o$. If the MOSFET is turned on at this instant, the switching loss is minimized. This is commonly designated as "valley switching". The extra resonance time needed before the valley point can be derived as

$$T_d = \pi\sqrt{L_m C_{oss}} \tag{11}$$

The switching period and switching frequency can therefore be obtained as

$$T_s = T_{on} + T_{off} + T_d,\ f_s = \frac{1}{T_s} \tag{12}$$

After the zero-crossing point of transformer current, the resonance between L_m and C_{oss} brings the switch voltage down to as low as $V_{sw} = V_{in} - nV_{o,i}$ at the first valley. The flyback switch turning on at this instant will benefit most with reduced switching loss, designated as "valley-switching" (see Fig. 3).

In practical implementations, instead of directly searching for the valley point, the zero-crossing of the transformer voltage is easier to be detected by adding an auxiliary winding to the transformer. Most QR controllers have integrated the zero-crossing detection (ZCD) function, as shown in Fig. 5. Although the ZCD point does not match the valley point as marked in Fig. 6, most controllers allow inserting a programmable delay after the ZCD instant by using a simple resistor so valley switching can be achieved [21].

B. WIDE LOAD-RANGE MANAGEMENT FOR HIGH EFFICIENCY

Since the inductor energy accumulated during the T_{on} phase is fully released to the secondary side during the T_{off} phase. The energy released E_s is then established by

$$E_s = \frac{1}{2} L_m I_{P,pk}^2 \tag{13}$$

and the output power is

$$P_o = \frac{1}{2} L_m I_{P,pk}^2 \cdot f_s \tag{14}$$

Combining (8), (12), and (14) and solving for f_s reveals that f_s is approximately inversely proportional to the output power P_o. This relationship is plotted as the BCM QR region in Fig. 7. As the output power reduces, continuing to operate in BCM mode will lead to excessively high switching frequency which deteriorates the efficiency. In this case, skipping the first valley and selecting one of the subsequent resonant valleys to turn on has been adopted by [21] to effectively reduce the switching frequency and maintain the valley-switching and low turn-on switching loss. Fig. 6 depicts the exemplary

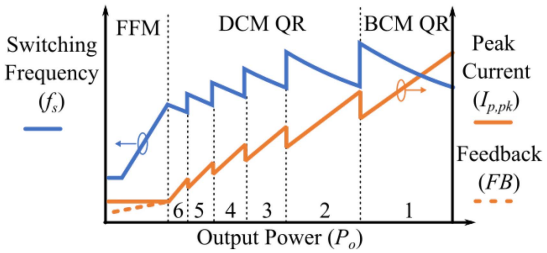

FIGURE 7. Switching frequency and peak current at different load conditions, reflecting flyback's different operating modes.

waveforms of skipping the first three valleys and turning on at the fourth valley. Fig. 7 shows the switching frequency is kept low by choosing the 2nd to 6th valleys. Since the flyback now operates in discontinuous conduction mode (DCM) with QR features, the delay time T_d previously derived in (11) is updated as

$$T_d = \left(k_{valley} - \frac{1}{2}\right) \cdot 2\pi\sqrt{L_m C_{oss}} \tag{15}$$

where k_{valley} is the order of valley at which the main switch is turned on.

As the load power continues to decrease, it would benefit the efficiency the most if the peak current is maintained constant and the output is controlled by modulating the switching frequency, which is designated as the Frequency Foldback Mode (FFM). With a constant peak current setting, lighter load is supported with lower switching frequency. The switching frequency keeps reducing with the load until it reaches the lower frequency limit (mostly set by the controller at a few kHz higher than 20 kHz) in order to avoid audible noise. After this, the controller will lock the switching frequency and only activate the flyback to switch for a few cycles at this locked frequency to replenish the output capacitors and maintain the voltage. For the rest of the time, the flyback converter is shut down and in sleep mode to minimize the power consumption. This is often referred as burst mode or skipping mode.

C. CONTROL IMPLEMENTATION

Regardless of the operating modes, since the QR flyback will always satisfy (14), its output power directly relates to the peak current $I_{p,pk}$ once the converter design including L_m is fixed. Fig. 7 also shows the peak current reduces with lower output power until it reaches the preset minimal value. Fig. 5 shows the brief control diagram of such system, including two control loops: an voltage loop for output regulation, and an inner current loop based on peak current mode control. A simple proportion-integral (PI) controller can be used for the voltage loop and its output FB, after passing the opto-cupler isolation barrier (not shown), serves as the most important control signal for the flyback controller, reflecting the output power needs. In BCM QR and DCM QR modes, the FB signals works as the reference to regulate the primary peak current. The primary current is sensed by a resistor R_{sen} in series with the switch, and the sensed voltage (CS) is compared with the

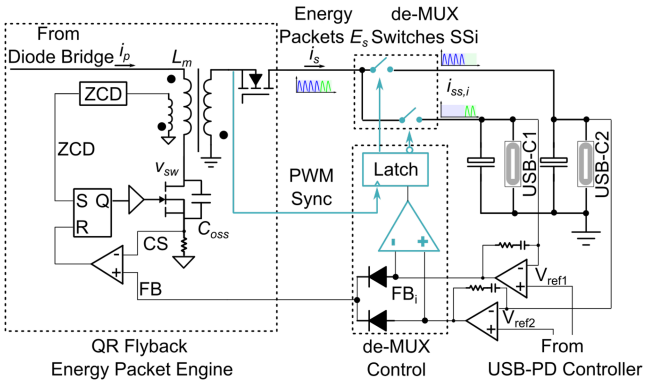

FIGURE 8. Multiplexing-based Quasi-Resonant flyback for a dual-port USB-PD charger. EMI filter and input diode-bridge are ignored in the schematics for concise illustration but included in the designed prototype.

current reference FB. Once the sensed current exceeds the FB voltage level, the primary switch is turned off, which leads to

$$FB = I_{P,pk} \cdot R_{sen} \tag{16}$$

Due to this correlation, the FB signal shows a similar relationship against output power as the peak current, as shown in Fig. 7 in both DCM QR and BCM QR regions. It also generally reduces with less output power with multiple zigzags due to valley skipping. In FFM mode, since the peak current is fixed, the FB signal does not regulate peak current, but correlate with switching frequency so it will continue drop with lowered output power. In skip or burst mode, the FB signal will set the threshold for start and stop of flyback switching pulses. In fact, commercial controllers normally use the FB signal to determine its operating mode (BCM QR, DCM QR, or FFM).

To summarize, QR flyback can operate in multiple different modes to optimize efficiency across full load to light load, and commercial QR-flyback controllers generally relies on the FB voltage level to determine the operating modes. In addition, QR flyback can achieve valley switching for low switching loss by using the ZCD signal from an auxiliary winding. With both signals exhibiting similar behaviors as a regular single-output QR flyback, we propose a dual-output TDM-QR flyback implementation, so that a commercial QR controller can be directly used without any modifications, and the valley switching and load management features are both reserved. This will be discussed in the following section.

IV. PROPOSED TIME-DIVISION MULTIPLEXED QUASI-RESONANT FLYBACK IMPLEMENTATION

The proposed dual-port implementation of the TDM-QR flyback scheme (see Fig. 8) is detailed in this section that synthesizes the discussions in previous sections. The powertrain consists of two major stages: the first stage is a QR flyback converter generating the energy packets that is identical to the one shown in Fig. 5 as discussed in Section III; the second stage is a demultiplexer (de-MUX) circuit to distribute the energy packets following each port's power

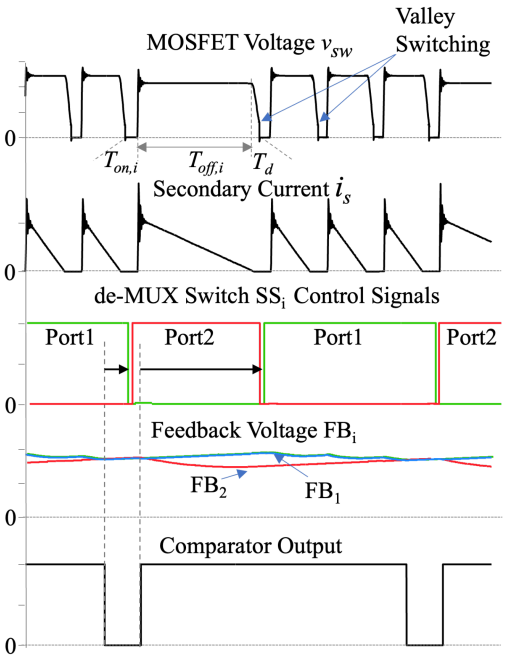

FIGURE 9. Simulated waveforms of the TDM-QR flyback under the condition of $P_{o,1} : P_{o,2} = 3 : 1$.

demand, comparable to the case of Fig. 2 using the discontinuous mode (Fig. 3) and uniform TDM scheme (Fig. 4). The proposed Mux-based single-stage implementation realizes a universal input, dual-USB-C output charger with simple analog controllers and components, which achieves high efficiency performance across entire load range and low cost.

A. QUASI-RESONANT FLYBACK AS ENERGY PACKET ENGINE

Section III shows that the QR flyback always adopts discontinous inductor current with the three operating modes in Fig. 7, which makes it suitable to serve as a TDM packet engine according to the discussion in Section II-A. In each T_{off} phase, the flyback inductor current fully discharges to the load, delivering the amount of energy that equals to (13), rewritten here as $E_s = L_m I_{P,pk}^2/2$. As the switching cycles continue, those current delivery events constitute a series of energy packets with constant energy level per packet regardless of the output voltage, since the peak current $I_{P,pk}$ is the same. By using this QR flyback as the energy packet engine, Equation (13) quantifies the energy packet size. It is worth mentioning that when the two output voltages are different, the discharge time T_{off} and slew rate will be different, which are clearly shown by the Secondary Current i_s waveform in Fig. 9. However, those energy packets still have the same energy level.

B. DE-MUX SWITCHES IMPLEMENTATION

As discussed in Section II-A, in order to prevent shoot-through between the outputs, each de-MUX switch SS_i must be able to block bi-directional voltages. Each de-MUX switch

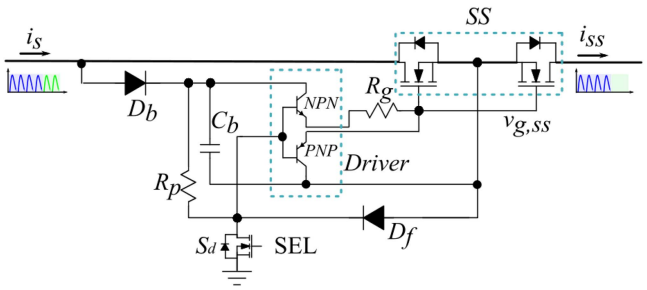

FIGURE 10. De-MUX Switches Implementation with back-to-back connected MOSFET pair and level-shifted drivers.

shown in Fig. 8 can be implemented with a back-to-back connected MOSFETs pair with shared source terminal as shown in Fig. 10. While it is possible to achieve similiar functions by replacing the MOSFET at the output side with a diode for lower cost, the power loss will increase due to higher voltage drop. It is often not straightforward to drive a NMOS switch pair since the PWM signal and the common source terminal do not share the common ground. Therefore, a level shifting circuit is needed as shown in Fig. 10 where a low-cost circuitry is used to implement the required level-shifter together with the gate driver. Fig. 10 exemplifies only one de-MUX switch implementation with the other one being the same.

The gate driver consists of a complementary pair of bi-polar transistors (NPN and PNP) as the drive-current boosters at turn-on and turn-off, respectively. The bypass capacitor C_b stores the energy for driving SS_1. The driving circuit uses gate resistor $R_g = 100\Omega$ at turn-on, and zero Ohm at turn-off. The PWM signal SEL for SS_1 is ground referenced so needs to be level-shifted to the source of the switch-pair. The level-shifter is realized by a simply pull-up resistor R_p and a low-voltage small pull-down MOSFET S_d. When SEL signal is high, S_d turns on and pulls the gate driver input to ground level. A clamping diode D_f prevents the voltage between the driver input and SS_1 source (gate driver's floating ground) from getting too negative. Since the gate driver sees a low input voltage, the PNP transistor will turn on and discharge the gate capacitance of SS_1 and shut it off. Meanwhile, since S_d is on, the packet engine output voltage will charge C_b through D_b, D_f, and S_d, refreshing the energy stored in C_b. When SEL signal is low, S_d turns off, so R_p can pull the driver input to the voltage of C_b. This will turn on the NPN transistor and SS_1 eventually. It should be noted that the driving logic of the SEL signal to SS is inverted, so the de-MUX control design should consider the polarity change. In addition, the circuit is realized with low-cost discrete components with low-voltage (<40 V) and low-current ratings, it can be easily integrated in an integrated circuit for further footprint and cost savings.

C. DE-MUX SWITCHES CONTROL WITH PACKET ENGINE SYNCHRONIZATION

The purpose of the de-MUX control is distributing the pulsating current source at the output of the energy packet engine, to individual output ports so that each output voltage can be independently regulated. To achieve this, each output voltage is compared with a reference voltage according to the USB-PD controller's command, and it is fed to a PI compensator which in turn generates independent feedback signals FB_i, as shown in Fig. 8. Since the FB_i signal is the output of the PI controller that integrates and amplifies the output-voltage error against the regulation voltage target, a deeper output voltage drop will eventually raise its own FB_i signal, exposing its needs for energy refreshment. A simple comparator circuit tells which port has a higher FB_i signal and respond to its energy refreshment request by turning on the corresponding de-MUX switch SS_i. Meanwhile, the other port's de-MUX switch is turned off to prevent shoot-through. The bottom two subplots in Fig. 9 show the FB_i signals and the comparator outputs.

When $FB_1 > FB_2$, the comparator flips to high, and vice versa. However, the comparator output cannot be directly used to control the de-MUX switches. As discussed in Section II-A, the channel switching should occur at zero current of the packet engine output. In Fig. 9, the high-to-low transition of the comparator output (highlighted by the dashed vertical line on the left) occurs when the secondary current i_s is non-zero. Therefore, the on/off control of de-MUX switch should be synchronized with the energy packet engine to find the zero-current time interval.

Thanks to the boundary mode or discontinuous mode operation of the flyback converter, the secondary current always falls to zero where the current crossing information can be readily determined from the transformer secondary winding voltage. A diode is used to pick up and rectify this voltage to provide a synchronization signal. A latch component in Fig. 8 is used to memorize the comparator output level but will not change its output states until it receives a falling edge from the synchronization signal. Fig. 9 illustrates how the latch circuit delays its output states (the SS_i control signals) with respect to both the rising and falling edges of the comparator output to avoid de-MUX switching at non-zero secondary currents.

Another benefit of this synchronization is the zero-current-switching (ZCS) of the de-MUX switches. The current in the conducting de-MUX switch drops to zero simultaneously with the secondary current, so the de-MUX switch is turned off with ZCS with minimal switching loss. Similarly, the turning-on of the other de-MUX switch after a deadtime also complies ZCS condition that incurs minimal switching loss. The soft switching of the de-MUX switches not only improves efficiency and reliable operation with low voltage overshoot, but also make it possible to use lower on-resistance MOSFETs to further improve efficiency without concerns of increased switching loss.

D. ADAPTIVE ENERGY PACKET SIZING FOR OPTIMIZED WIDE LOAD-RANGE EFFICIENCY

In order to achieve independent output regulation for both USB ports, both output voltages must be sensed and pass its

corresponding FB_i signal back to the primary flyback controller. It is often challenging to determine how to pass multiple feedback signals FB_i into one PWM controller. Instead of weighted combination of feedback signals which increases regulation errors [24], we adopts an OR'ing function of the two FB_i signals using two diodes, as Fig. 8 shows. As a result, the final FB signal to the flyback controller always represents the FB_i signal with higher voltage level. As a higher FB_i signal indicates that corresponding output has more voltage drop and needs more energy refreshment, this OR'ing scheme maintains both output voltages independently. Thanks to the proposed FB_i signals combination and de-MUX implementations, we can notice that during the time frames assigned to one particular output, with the corresponding de-MUX switch conducting and FB_i signal passed through, the TDM-QR converter operates exactly as a regular single-output QR flyback converter. Therefore, the commercial QR flyback controller can be directly adopted in the solution with modifications.

The OR'ing connection of the FB_i signals ensures the final FB signal stay at a relatively stable level across the TDM time frames, as shown in Fig. 9. In case of one FB_i signal dropping too low, its corresponding output voltage will keep sagging due to lack of assigned time frames. The PI error amplifier will gradually bring this signal higher until it is sufficient to overtake the other channel's feedback signal. As a result, both the two FB_i and the final FB will stay at a stable level in steady state. This essentially achieves the uniformed packet size scheme as discussed in Section II. The primary side peak current for both BCM and DCM QR modes, can therefore be solved as:

$$I_{P,pk} = I_{m,avg} + \sqrt{I_{m,avg}^2 + \frac{2T_d \cdot \left(P_{o,1} + P_{o,2}\right)}{L_m}} \tag{17}$$

where $I_{m,avg}$ is the average magnetizing current given by

$$I_{m,avg} = \frac{P_{o,1} + P_{o,2}}{V_{in}} + \frac{I_{o,1} + I_{o,2}}{n} = I_{in} + \frac{I_{o,1} + I_{o,2}}{n} \tag{18}$$

Equation (17) and (18) suggest that the peak current $I_{P,pk}$ changes with the output combinations ($I_{o,1}$, $I_{o,2}$, and $P_{o,1}$, $P_{o,2}$). A reduction on output power and output current will shrink the peak current, so does the FB signal according to (16)). The QR flyback controller will in-turn respond to the FB signal and reduce the peak current, effectively reducing the energy packet size. Therefore, the proposed TDM-QR flyback implementation achieves adaptive energy packet size with load changes. As the FB signals drops with load, the flyback operation will follow the same pattern in Fig. 7 and switch to DCM QR and then FFM modes, so efficiency can be optimized across all load range.

V. CONVERTER DESIGN

A dual-USB-C converter design is complicated due to various output combinations. The component and key parameter selection is determined by the worst-case current, voltage, and thermal (or power losses), which has to be identified first. When selecting component voltage ratings, traditional QR flyback's practice can be conveniently followed [22] by considering highest input and output voltage conditions, so will not be detailed herein. This section focuses on the semiconductor device sizing and transformer design, which needs power loss modeling. We will see that the TDM dual-USB-C converter does has unique loss models, different from traditional single-output flyback.

A. POWER LOSS MODELING

The loss models of the proposed converter topology are derived in this subsection. The multiplexing operation of the proposed solution requires unique loss models, different from traditional single-output flyback, and correlated to demultiplexing scheme. To be concise, only the critical power losses that differentiate the proposed architecture from the traditional solution are analyzed. Other common power losses shared by both architectures such as those from diode bridge, EMI filters, etc., can be derived easily following existing flyback design practice [22], so will not be discussed in this work.

The below key equations are derived considering multiple output conditions. The RMS values for the primary side winding (switch) current and the secondary side winding (rectifier) current in the dual-output configuration are derived as

$$I_{p,rms} = \sqrt{\frac{I_{P,pk}^2}{3} \cdot \frac{I_{in}}{I_{m,avg}}} \tag{19}$$

$$I_{s,rms} = \sqrt{\frac{I_{P,pk}^2 \cdot n^2}{3} \cdot \frac{I_{o,1} + I_{o,2}}{nI_{m,avg}}} \tag{20}$$

Considering the overall primary resistance R_p comprises resistances from the main switch $R_{ds(on)}$, primary winding $R_{w,p}$, and current sense resistor R_{sen}, the primary side conduction loss $P_{con,p}$ is lumped as

$$P_{con,p} = I_{P,rms}^2 R_p,\ R_p = R_{ds(on)} + R_{w,p} + R_{sen} \tag{21}$$

Similarly, the secondary conduction loss $P_{con,s}$through all resistances of the secondary side including resistances from secondary winding $R_{w,s}$, synchronous rectifier (SR) $R_{sr(on)}$, and de-MUX switches R_{dem} are calculated as

$$P_{con,s} = I_{S,rms}^2 R_s,\ R_s = R_{sr(on)} + R_{w,s} + R_{dem} \tag{22}$$

Note that the above equations already account for the multiplexing operation and represent the overall RMS values for a dual port application. For other power losses discussed below, the power loss is derived separately for each individual port as it is difficult to get concise formulas for the total power loss. The individual port number is designated by the subscript letter i in the below deductions, and the demultiplexing law is applied in the end.

The snubber loss for port i can be determined as

$$P_{sn,i} = \frac{L_{lk} \cdot \left(\alpha I_{P,pk}\right)^2}{2T_{s,i}} \cdot \frac{V_{sn}}{V_{sn} - nV_{o,i}} \tag{23}$$

where V_{sn} is the snubber capacitor voltage; α is the ratio depending on the current division effect of the primary and

secondary parasitic capacitance C_p and C_s:

$$\alpha = \frac{C_p}{C_p + C_s/n^2} \tag{24}$$

Capacitance C_p consists of the MOSFET C_{oss} and the primary winding capacitance, and C_s is the lumped capacitance of the SR C_{oss} and the secondary winding capacitance. The primary switch switching loss is related to the input and output voltages by

$$P_{sw,i} = \frac{1}{2} C_{oss} \left(V_{in} - nV_{o,i}\right)^2 f_{s,i} \tag{25}$$

The SR switch driving loss can be derived below, where V_{cc} is the supply voltage of the SR controller, $V_{drv,i}$ is the SR MOSFET driving voltage, and Q_g is the gate charge of the SR MOSFET which needs to be scaled at its driving voltage $V_{drv,i}$.

$$P_{drv,sr,i} = V_{cc} \cdot Q_g \left(V_{drv,i}\right) \cdot f_{s,i} \tag{26}$$

The transformer core loss can be determined by the Steinmetz Equation as

$$P_{core,i} = c \cdot \left(\frac{L_m I_{P,pk}}{2N_p A_e}\right)^a \cdot f_{s,i}^b \tag{27}$$

Since equations (23)–(27) only calculate the power loss for each port, the demultiplexing law below has to be applied to obtain the dual-port power loss for each category:

$$P_x = \frac{P_{x,1} M_1 T_{s,1} + P_{x,2} M_2 T_{s,2}}{M_1 T_{s,1} + M_2 T_{s,2}} \tag{28}$$

or

$$P_x = \frac{P_{x,1} P_{o,1} T_{s,1} + P_{x,2} P_{o,1} T_{s,2}}{P_{o,1} T_{s,1} + P_{o,1} T_{s,2}} \tag{29}$$

where P_x represents P_{sn}, P_{sw}, $P_{drv,sr}$, or P_{core}.

B. WORST-CASE IDENTIFICATION

It is possible to apply the power loss models for all the operating conditions, but the procedure will include five variables including $I_{o,1}$, $I_{o,2}$, $V_{o,1}$, $V_{o,2}$, and V_{in}, rendering the results difficult to interpret and present. One way to simplify this problem is to only concentrate on the worst cases, which occur at the conditions with relatively high output power and low input voltage, implicated by (17) and (18) which suggest that the peak current $I_{P,pk}$ increases with the output current and power ($I_{o,1}$, $I_{o,2}$, and $P_{o,1}$, $P_{o,2}$), and reduces with input voltage. We can use the lowest input voltage to eliminate one variable (V_{in})and only select relatively high power conditions. But for the dual-USB-C converter, those cases still include multiple voltage and current combinations. In this work, those cases are represented according to (30). The assumption is that the output current at port 1 is fixed at 3 A and the total output power is 60 W for an USB PD charger, the output current at port 2 under different combinations of port voltages ($V_{o,1}$ and $V_{o,2}$) can be calculated. With each port's current determined, the variable quantity have reduced to two, therefore a color contour chart can be drawn to illustrate a target quantity.

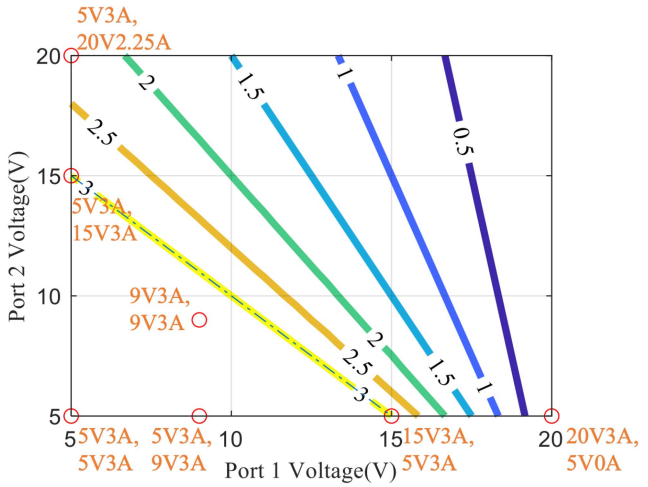

FIGURE 11. Port 2 output current $I_{o,2}$ versus port voltages calculated according to (30).

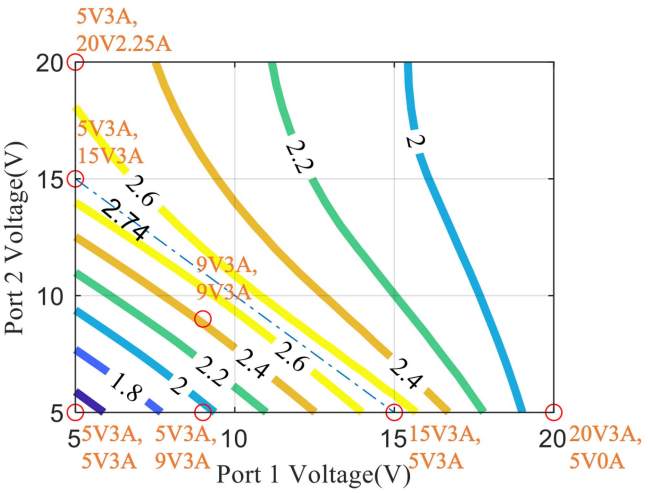

FIGURE 12. Modeled total critical power losses across different output combinations defined in (30) at Vin = 100 V with other parameters defined in Table 1.

Fig. 11 shows the port 2 current. Note that the representation is equivalent to assume port 2 current as 3 A and vary port 1 current since both ports' output capability are identical.

$$I_{o,1} = 3A, I_{o,2} = \max\left(3A, \frac{60W - V_{o,1} I_{o,1}}{V_{o,2}}\right) \tag{30}$$

This representation can therefore be used to show the overall power loss at different output combinations, as shown in Fig. 12, using the derived loss model and the component parameters provided in Table 1. We can clearly see the worst-case power loss occurs at full 60 W output power with both ports delivering full 3 A (dot-dash line), and the most common output combination in this case is 15 V/3 A and 5 V/3 A. Component sizing and transformer design needs to be optimized at this operating condition.

TABLE 1. Designed TDM Dual-USB-C Charger Key Components and Parameters

Quantity	Values
Input voltage V_{in}	90 – 264 Vac
Output voltage / port $V_{o,i}$	5V, 9V, 15V, 20 V
Output current / port $I_{o,i}$	0 – 3 A*
Magnetizing inductance L_m	120 μH
Leakage inductance L_{lk}	2 μH
Main GaN Switch	Navitas NV6115, 170 mΩ
Sync Rectifier MOSFET	Infineon BSC040N10NS5
de-MUX MOSFET	Infineon BSZ0506NS
Transformer core	RM7 ML27D
Transformer windings	Turns: P:S:P = 12:4:12 (n=6) Wire: #44x60(P), #44x360(S)
QR flyback controller	Onsemi NCP1342
SR controller	Onsemi NCP4306
USB PD controller	WT6615

*Total output power $<$ 63 W

C. TRANSFORMER DESIGN AND COMPONENT SELECTION

Flyback transformer design invovles the selection of turns ratio, inductance, winding, and layer structure for optimized efficiency, size, and EMI performance. Thanks to the decoupled packet engine and deMux circuit operation, the flyback transformer design is similar to that of existing QR flyback. For example, the turns ratio selection is based on the concept of balancing the voltage stress between primary and secondary switches; the inductance value is determined by the desired switching frequency due to boundary mode operation; the layer structure needs to be designed with common mode EMI balancing. It's worth mentioning that due to single secondary winding, the EMI design for the flyback transformer is identical to that of traditional single-output QR flyback. The winding design requires optimization on the turns number and wire gauge to minimize the total loss (winding and core) while filling one layer as much as possible, in order to achieve the best EMI shielding and balancing purposes. The resultant transformer design details are shown also in Table 1. The turns ratio is 24:4 and the primary side is segmented to two 12-turn layers with the secondary winding in between, which forms an interleaved structure for the benefits of low leakage inductance and AC resistance. AWG44 gauge litz wire with 60 strands and 360 strands were used for primary and secondary windings, respectively.

The breakdown voltage of the primary GaN switch is selected as 650 V for off-line AC/DC converter applications to account for universal input requirement (90–264 V AC). Lower voltage rated off-the-shelf GaN devices will be 300 V, which becomes impossible to handle 264 V AC input. Regarding current rating or on-resistance selection, a lower on-resistance will lead to lower conduction loss but not too much smaller until its impact is dwarfed by the sensing resistor's dominance. Also, a GaN device with too low resistance comes with higher output capacitance C_{oss}, which will induce switching loss at high line input condition, limiting the switching frequency and increasing the transformer size, similar to traditional QR flyback. A design optimization shows 170 $m\Omega$ GaN device provides balanced loss at low line and high line input conditions.

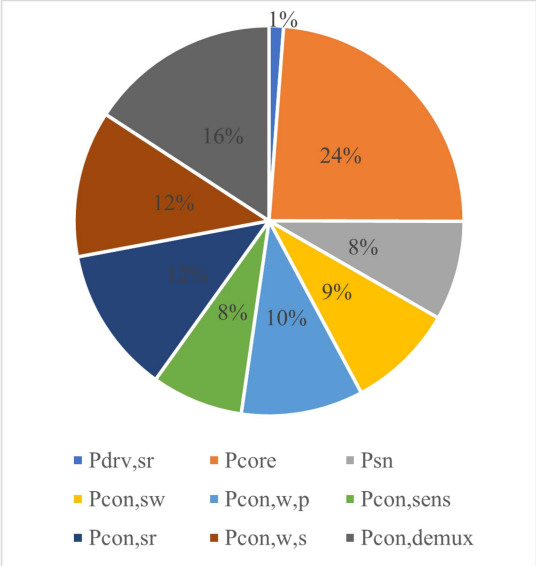

FIGURE 13. Loss breakdown of the proposed Mux solution, at 100 V DC input, 15 V3 A/5 V3 A output combination.

Similarly, the SR MOSFET's selection needs to balance the conduction loss and high-frequency related losses. For instance, lower on-resistance comes with higher gate charger, increasing driving loss. Moreover, for a low on-resistance SR switch, the voltage drop across the on-resistor becomes so low that it becomes comparable to that of the MOSFET package inductance, especially under high dv/dt condition. Since most SR controller senses the current by measuring the voltage drop across the drain and source terminals, this error can cause the SR switch turn-off prematurely before the actual current drops to zero. As a result, the current flows through its body diode, inducing higher conduction loss. After a few design iterations, a SR MOSFET with 4 $m\Omega$ on-resistance is selected.

The de-Mux MOSFETs only needs to block the voltage difference between the two ports. Although each port's voltage ranges from 5 V–20 V, a worst-case can occur when one port is short-circuited ($V_{o,i} = 0$), so a blocking voltage higher than 20 V is still required. Thanks to zero-current switching, the de-Mux switches benefit from both low switching loss, so a relatively low on-resistance devices can be used to optimize for efficiency. A 30 V, 4.4 $m\Omega$ MOSFET is selected.

With the derived loss model and optimization logic mentioned above, components are selected as shown in Table 1. Loss breakdown of the proposed TDM dual-USB-C converter, at 100 V DC input, 15 V3 A/5 V3 A output combination (power loss and thermal worst-case) is shown in Fig. 13.

VI. EXPERIMENTAL VALIDATION

A 60 W GaN-based TDM charger with dual-USB-C ports is built with the key components and parameters listed in Table 1, and the prototype photo is shown in Fig. 14. It worth

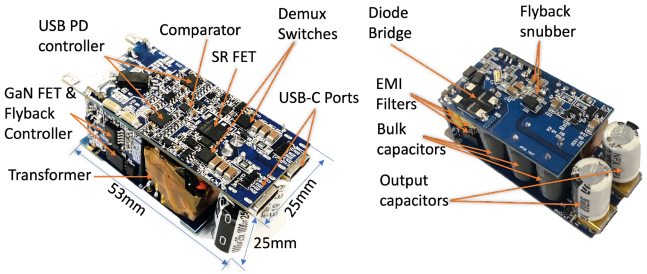

FIGURE 14. Prototype of a 60 W GaN-based TDM-QR Dual-USB-C charger.

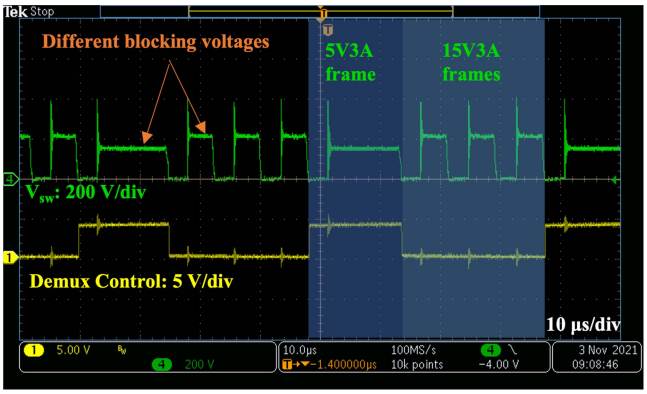

FIGURE 15. Full load waveforms of the flyback primary switch voltage and the de-MUX switch control signal at dual-port output with 15 V/3 A and 5 V/3 A.

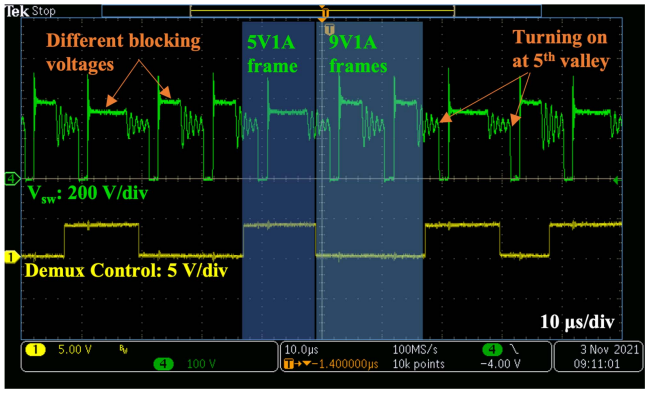

FIGURE 16. Light load waveforms of the flyback primary switch voltage and the de-MUX switch control signal at 5 V/1 A and 9 V/1 A outputs.

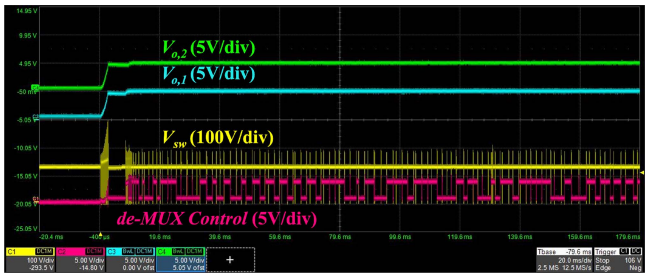

FIGURE 17. Converter startup waveforms when AC line applies. Converter starts to 5 V at both ports, in compliance with USB-PD controller's command before any charging negotiation starts. The V_sw waveform shows a clear burst-mode operation and the *SEL* signal alternates the conduction channel of the de-MUX.

pointing out that the proposed implementation can be directly used for higher power applications, as the concept is generic regardless of the power level.

A. STEADY STATE TEST RESULTS

Fig. 15 shows the experimental waveforms of the flyback primary switch voltage and the de-MUX switch control signal with an output combination of 15 V/3 A and 5 V/3 A. A high "de-MUX control" signal indicates the 5 V port is selected to receive power, and vice versa. The flyback packet engine works as expected in the BCM mode with valley switching ensured. When different ports are selected, the primary switch's steady-state blocking voltage varies accordingly by $V_{sw} = V_{in} + nV_{o,i}$. This varying blocking voltage can be taken as an indicator for the time-frame allocation as highlighted in Fig. 15. The ratio of the pulse number between the 15 V and 5 V ports equals 3, which is consistent with their output power ratio as analyzed in Section II.

Fig. 16 shows the light load waveforms under 5 V/1 A and 9 V/1 A outputs. The flyback operates in valley skipping mode where the primary switch turns on at the fifth valley, improving the light load efficiency. In addition, according to Fig. 6, the secondary current drops to zero before the quasi-resonant phase (T_d) starts. So we can see from the experimental waveform in Fig. 15 and Fig. 16 that, the de-MUX control signal always transits at the T_d or T_{on} phases, after the completion of the secondary-side current delivery, validating the function of the packet engine synchronization.

B. START-UP AND TRANSIENT VALIDATION

Fig. 17 shows the converter startup waveforms when AC line applies. Converter starts to 5 V at both ports, in compliance with USB-PD controller's command before any charging negotiation starts. Since the converter operates at no load condition, the V_sw waveform shows a clear FFM burst-mode operation where the spikes indicate switching events and the rest of the period with a straight horizontal line is the standby waiting time. The *SEL* signal alternates the conduction channel of the de-MUX to replenish both outputs capacitors.

Fig. 18 shows the Load current step-up waveforms. Port 1 stays at 5 V/3 A, and port 2 goes through a load current step-up from 20 V/0 A to 20 V/2.25 A. Fig. 19 shows the Load current step-up waveforms. Port 1 stays at 5 V/3 A, and port 2 goes through a load current step-down from 20 V/2.25 A to 20 V/0 A. Fig. 20 USB-PD output voltage change: Port 1 stays at 9 V/3 A, and port 2 goes through reference voltage change from 5 V to 20 V. Fig. 21 USB-PD output voltage change: Port 1 stays at 9 V/3 A, and port 2 goes through reference voltage change from 20 V to 5 V.

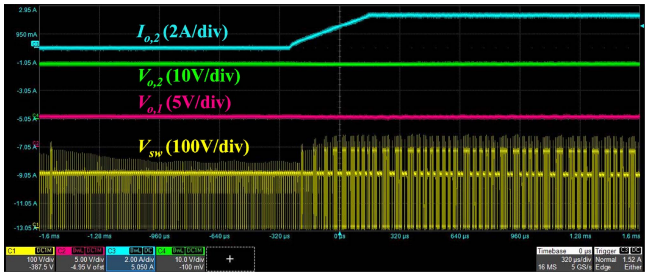

FIGURE 18. Load current step-up waveforms. Port 1 stays at 5 V/3 A, and port 2 goes through a load current step-up from 20 V/0 A to 20 V/2.25 A. Both port voltages remain stable during the load transient.

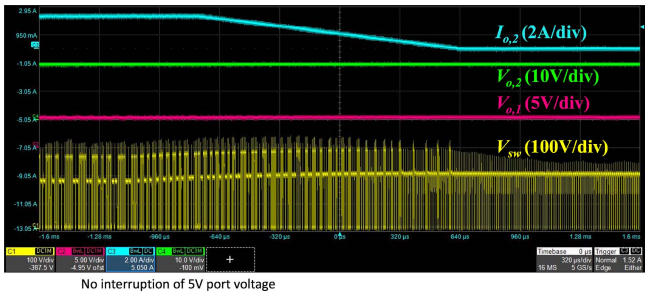

FIGURE 19. Load current step-up waveforms. Port 1 stays at 5 V/3 A, and port 2 goes through a load current step-down from 20 V/2.25 A to 20 V/0 A. Both port voltages remain stable during the load transient.

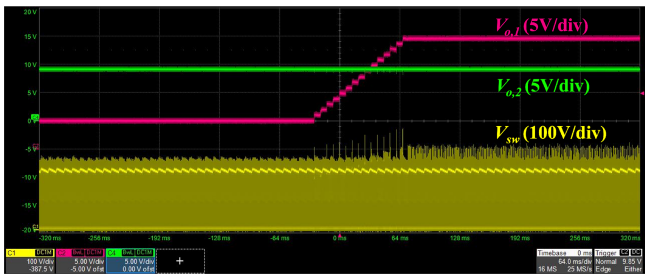

FIGURE 20. USB-PD output voltage transient: Port 1 stays at 9 V/3 A, and port 2 goes through reference voltage change from 5 V to 20 V.

C. EFFICIENCY PERFORMANCE ACROSS WIDE LOAD RANGE

Light-load efficiency for external power adapters becomes increasingly important in recent years to reduce overall energy consumptions for all energy sectors. Both U.S. DOE Level VI and EU's CoC Tier 2 standards define a 4-point average efficiency at 25%, 50%, 75%, and 100% loads for single output power supplies [19]. Since EU's CoC Tier 2 standard is more stringent than U.S. DOE Level VI, so only the former is plotted as the red dot-dashed line in Fig. 22). In addition, DOE Level VI regulates the average efficiency for multiple output voltage external power supplies (the limit shown as the red line in Fig. 22), which is much lower than the single output voltage standard (dot-dashed line). This is based on the perception that multi-output power supplies are inherently more lossy than single output ones.

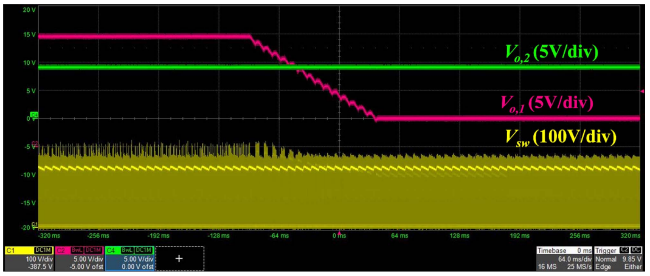

FIGURE 21. USB-PD output voltage transient: Port 1 stays at 9 V/3 A, and port 2 goes through reference voltage change from 20 V to 5 V.

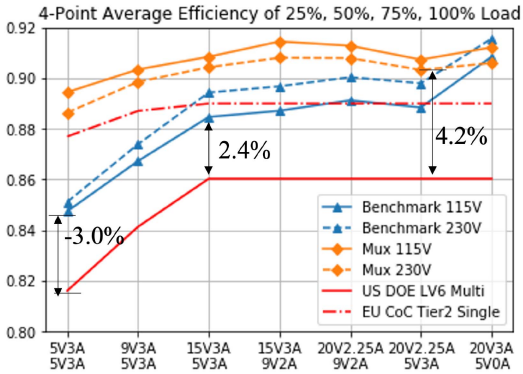

FIGURE 22. Comparison of 4-point average efficiency of the proposed (Mux) and a benchmark charger, against international efficiency standards.

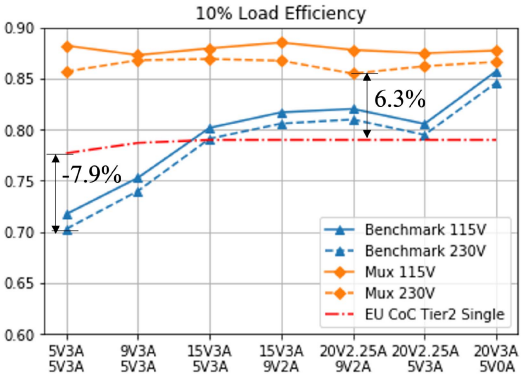

FIGURE 23. Comparison of 4-point average efficiency of the proposed (Mux) and a benchmark charger, against international efficiency standards.

Due to the lack of research on multi-port USB-PD chargers, a state-of-the-art GaN dual-USB-C charger was tested as a benchmark to compare with the proposed solution. While both the benchmark charger [25] and the proposed designs can meet the standard for multi-output, the proposed solution ("MUX" curves in Fig. 22) shows larger worst-case margin (4.2% at 20V2.25 A/5 V3 A) than that of the benchmark design (2.4% at 15 V3 A/5 V3 A). The proposed design can even meet the more stringent EU efficiency standard for the single-output case with 0.9% margin. In contrast, the benchmark charger's efficiency fails this EU limit by 3.0%.

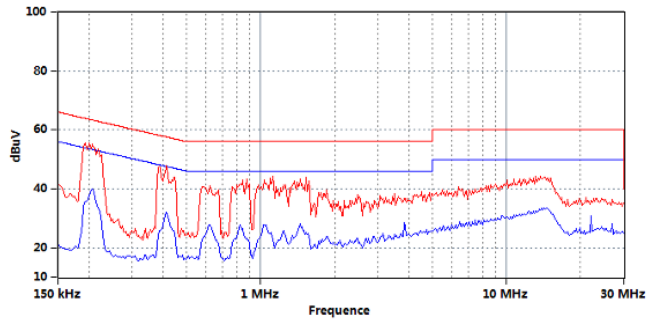

FIGURE 24. Conducted EMI measurement at low line 115 V_{AC}. Port 1: 20 V/3 A, Port 2: 5 V/0 A.

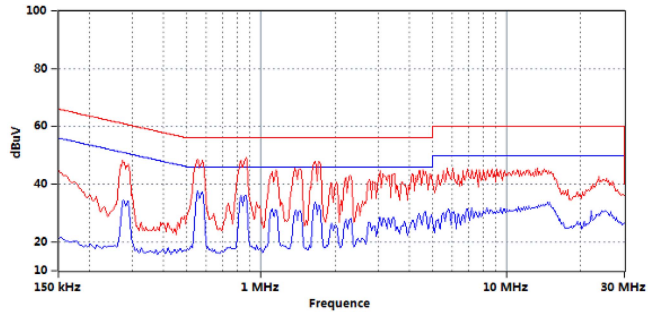

FIGURE 25. Conducted EMI measurement at high line 230 V_{AC}. Port 1: 20 V/3 A, Port 2: 5 V/0 A.

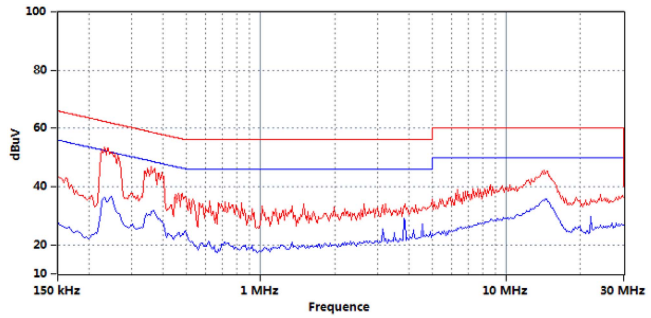

FIGURE 26. Conducted EMI measurement at low line 115 V_{AC}. Port 1: 9 V/3 A, Port 2: 9 V/3 A.

In addition, EU's CoC Tier 2 also regulates the efficiency for 10% load condition. Although this limit in fact only applies to single output power supply, the proposed solution meets this limit with larger than 6.3% margin in all cases comparing to the benchmark design that fails most of the operating conditions, as shown in Fig. 23. At the 5 V3 A/5 V3 A output combination, the efficiency value lacks the standard limit by 7.9%.

D. CONDUCTED EMI EMISSION MEASUREMENT

Fig. 24 and Fig. 25 show the conducted EMI emmission measurement in single-port mode (20 V/3 A) at 115V_{AC} and 230V_{AC}, respectively. The other port has no USB-C cable plugged-in so the output voltage stays at the default 5 V without load current. Fig. 26 and Fig. 27 show the conducted EMI

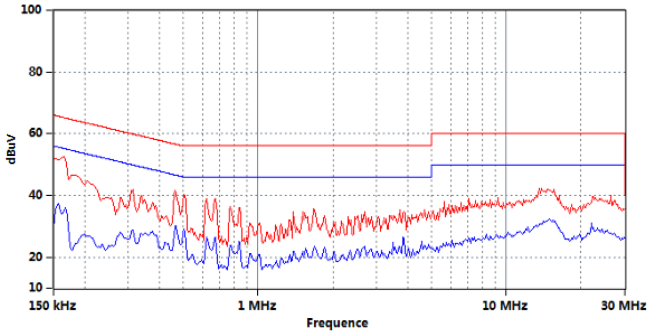

FIGURE 27. Conducted EMI measurement at high line 230 V_{AC}. Port 1: 9 V/3 A, Port 2: 9 V/3 A.

TABLE 2. GaN-Based USB-PD Charger Design Comparison

Parameters	[2]	[3]	[25]	**Proposed**
USB-C Outputs	Single	Single	Dual	**Dual**
Topology	QR	ACF	QR+Buck	TDM-QR
USB-C 1 Power[1] (W)	65	65	65	60
USB-C 2 Power[1] (W)	-	-	65	60
USB-C 1+2 Total Power (W)	-	-	63	63
Avg. Eff. Margin (multi)[2] (%)	-	-	2.4	**4.2** (1.8%↑)
Avg. Eff. Margin (single)[3] (%)	2.5	3.3	-3.0	**0.9** (3.9%↑)
10% Load Eff. Margin[3] (%)	-	2.5	-7.9	**6.3** (14.2%↑)
EMI Margin[4] (dBμV)	0	0	-	**7.4**
Uncased volume (cm^3)	31	27	-	**33**
Cased Volume (cm^3)	-	45	81	**58** (28%↓)

All margin numbers are at worst case. Avg. Eff. represents the average efficiency at 25%, 50%, 75%, and 100% loads.
[1]Maximum power in single port mode.
[2]Against DOE Level VI standard on multi-output power supply .
[3]Against EU CoC Tier 2 standard on single-output power supply.
[4]Conducted EMI emission against EN55032 standard.

emmission measurement in dual-port mode at 115V_{AC} and 230V_{AC}, respectively. Both ports are supplying 9 V/3 A. Each figure shows the Quasi-Peak (red) and Average (blue) results. In all four conditions, the converter can pass with more than 7.4 dB margin against the EN55032 standard requirement.

E. COMPARISON AND DISCUSSION

The comparison between the proposed and benchmark chargers are summarized in Table 2. Besides the efficiency benefit discussed earlier, the proposed charger measures 25 mm x 25 mm x 53 mm or 33 cm^3 without a converter case. To consider a converter case, assuming 5 mm is added at each short edge and 9 mm at the long edge to account for a foldable AC-plug, the charger will be 30 mm x 30 mm x 64 mm or 58 cm^3. This is 28% smaller than the benchmark charger (81 cm^3).

The table also listed the performance data for two single output GaN-based USB-PD chargers, one uses QR flyback and the other uses active clamp flyback (ACF) topology. Both chargers have passed the EU CoC Tier 2 standard on average efficiency with margins (2.5% and 3.3%, respectively). We can also see the proposed dual-USB-C charger has almost the same uncased volume as the singe-USB-C design in [2], due to the elimination of buck converters especially the inductors.

VII. CONCLUSION

A time-division multiplexing (TDM) quasi-resonant (QR) flyback converter for multi-port USB-C power delivery is proposed. The MUX solution eliminates the buck converter stages that are commonly used in state-of-the-art solutions to increase power density, efficiency, and reduce cost. The paper detailed the operating principles and also focused on the practical implementations of the TDM scheme integrated with a commercial QR flyback controller, including the flyback operation as an energy packet engine, the de-MUX design and control, as well as the interaction between the two. The designed GaN dual-USB-C charger experimentally validated the TDM-QR concept, demonstrated USB-PD compliant operation with each output voltage adjustable from 5–20 V and 0–3 A, and passed conducted EMI against EN55032 standard. The measured efficiency met the international standard on the average efficiency of multi-output power supply by more than 4.2% margin. Thanks to the elimination of additional buck DC-DC stages, the converter's efficiency even surpassed the efficiency standard limits for single-output power supplies, which bears a much higher requirement than the multi-output counterparts. In particular, at 10% of load, the converter can pass the standard limit with 6.3% margin, while the benchmark dual-USB-C charger fails by −7.9%. The dual-USB-C GaN charger achieves similar power density of a GaN single-USB-C charger. The implementation details of the TDM-QR were provided, which includes only a few additional low-voltage, low-cost analog components compared to a traditional QR flyback. They can be easily realized with an integrated circuit compatible with mature low-voltage silicon process for further cost and power density benefit. The proposed solution will be more advantageous at higher port numbers, which will be further research topics. Multi-USB-C chargers with indistinguishably powerful ports will enable standardized power interface for broader electronics in buildings, potentially revolutionizing building electrical infrastructure.

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