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Control Scheme for Leading Power Factor Operation of Single-Phase Grid-Connected Inverter Using an Unfolding Circuit

YASUHIKO MIGUCHI (Life Member, IEEE), HADI SETIADI (Member, IEEE), YOSHIKI NASU (Student Member, IEEE), HIDEMINE OBARA (Member, IEEE), AND ATSUO KAWAMURA (Life Fellow, IEEE)

Yokohama National University, Yokohama, Kanagawa Prefecture 240-8501, Japan

CORRESPONDING AUTHOR: ATSUO KAWAMURA (e-mail: kawamura@ynu.ac.jp)

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ABSTRACT A single-phase grid-connected inverter with an unfolding circuit consists of a first-stage dc/dc converter, which generates fully rectified sinusoidal waveforms, and a second-stage unfolding inverter, which switches every 180° of line frequency waveform. This converter exhibits low switching loss and high efficiency. Digitally controlled unfolding inverters can be used in numerous applications, such as power supplies to resistive loads and single-phase grid-connected inverters. The operating principle of an unfolding inverter is typically synchronous voltage and current. However, a reactive power supply function with a leading power factor (pf) (lagging pf from the grid perspective) is typically required for grid-connected inverters to suppress the terminal overvoltage. Limited studies have been focused on the operation of inverters with pf less than unity. Such an operation results in large overshoot and oscillation in the output voltage because of the difficulty in coping with large current fluctuations after voltage zero crossing. To this end, we propose a novel control scheme that enables leading pf operation without additional circuitry and overcomes the aforementioned limitations. When the unfolding inverter is operated with leading pf, a special mode called "all-conduction mode" occurs after voltage zero crossing. The proposed scheme implements appropriate dc current control to terminate this mode, resulting in a smooth transition to the normal mode steady state with pf less than unity. The scheme verifiably showcases exceptional efficiency in the conducted simulations and experiments.

INDEX TERMS All-conduction mode, high efficiency, power factor, single-phase grid-connected inverter, sinusoidal wave observer, unfolding inverter, voltage suppression.

I. INTRODUCTION

TYPICALLY, an inverter with an unfolding circuit consists of a first-stage dc/dc converter, which generates a fully rectified sinusoidal voltage or current waveform, and a second-stage unfolding inverter, which switches every 180° of the line frequency waveform and generates a sinusoidal voltage or current [1].

Initial research on unfolding inverters was focused on isolation and miniaturization of passive components. Schlecht [2] proposed an unfolding inverter with a first-stage flyback converter. Pitel [3] used a combination of phase-modulated converters, high-frequency transformers, and an LCL filter to generate a fully rectified sinusoidal voltage.

Numerous investigations have since been conducted to achieve the same output through other approaches [11]–[18].

The use of unfolding inverters with low switching loss has received considerable attention [4]–[7] with the purpose of realizing such converters with low total loss. In general, a tradeoff exists between conduction and switching losses as characteristics of semiconductor switching devices. Devices with superior conduction loss characteristics can be used in unfolding inverters, and devices with superior switching loss

characteristics can be utilized in dc/dc converters. For further loss reduction, non-isolated (transformer-less) dc/dc converters have been used, and various topologies can be employed in this approach. Other prominent approaches that have been proposed are: Zhao *et al.* [4] used boost-buck converters; Husev *et al.* [5] employed buck-boost converters; Lei *et al.* [33] employed a 7-level converter; and Kawamura *et al.* [6], [20] proposed a new multi-level chopper, called HEECS (high efficiency energy conversion system) circuit topology, and a high efficiency of 99.75% was reported in [7], [29].

In unfolding inverters, inverter devices are switched at every half cycle in synchronization with voltage zero crossing [1], [6], [7]. Thus, in the case of a unity power factor (pf), synchronous voltage and current zero crossing occurs in the unfolding inverter. If photovoltaic power is connected to a grid, lagging pf operation from the grid perspective (leading from the grid-connected inverter perspective) is critical for suppressing the overvoltage on the receiving terminal [19]. In such applications, the unfolding inverter needs to be operated with non-unity pf. However, in that case, a voltage transient response becomes oscillatory after unfolding [6], [20], as described in Section III, therefore, appropriate control is required. Few studies have focused on non-unity pf control of an unfolding inverter. Tian *et al.* [8] realized leading and lagging pf operation by adding a special circuit, namely, a "reverse dc/dc converter." Fonkwe *et al.* [9] also added a "current decoupling circuit" such that the circuit could support reactive power control. Li *et al.* [10] proposed a first-stage converter that generates fully rectified quasi-sinusoidal waveforms and a second-stage synchronous voltage and current zero crossing, which avoids additional circuit and PWM losses; however, total harmonic distortion (THD) of the output current is significantly large; moreover, operation pf range is limited to 0.86 or larger. Han *et al.* [34] connected a circuit called as "dc link" (combination of a switch and numerous capacitors) to an unfolding inverter. When the inverter generates reactive power, the dc link is connected, and the unfolding inverter operates in pulse-width modulation (PWM) mode, which increases switching loss. Min *et al.* [35] and Han *et al.* [36] operated an inverter in PWM mode for some period before and/or after the voltage zero crossing, which increased switching loss as well. In [20], the transient response of the HEECS can be improved by adjusting the voltage pulses after voltage zero crossing in case of a unity pf. However, in the case of a non-unity pf, overshoot and oscillation occur in the transient response.

In this paper, a novel control scheme is proposed to realize waveforms with low transient fluctuations after zero crossing in leading pf operations without additional circuits in unfolding inverters. First, Section II introduces the control principle of HEECS inverter. Next, Section III describes the circuit behavior in leading pf operation and control method corresponding to that circuit behavior. After voltage zero crossing, a special mode, called the "all-conduction mode," occurs as explained in Section III-A. Current control during this special mode is explained in Section III-B. Since the capacitor voltage is fixed at zero during this mode, it is uncontrolled. In the control method proposed in [20], the all-conduction mode was neglected and capacitor voltage was controlled, which resulted in significantly wide pulse that caused excessive inductor current and voltage overshoot. To this end, we applied a novel current control method in this mode to lead the inductor current to an appropriate value. In Section III-C, the control method of the normal mode after the all-conduction mode is explained. Additionally, the deadbeat voltage control law (DBVCL) in [20] caused an oscillatory response when the pf was less than unity. Therefore, we adopted a dead beat current control law + voltage control loop (DBCCL + VC) to stabilize this phenomenon. Moreover, Section IV presents the simulation and experimental results of the new control scheme and verifies the voltage waveform with a small fluctuation in the case of an unfolding inverter with a pf of less than unity while retaining high efficiency. Finally, Section V presents the conclusions.

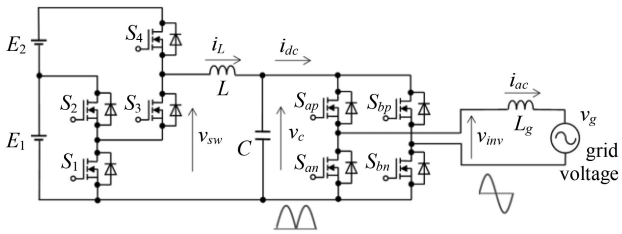

FIGURE 1. Grid-connected inverter based on HEECS.

TABLE 1. Relationship Between DC/DC Converter Switch States and Output Voltage

S_1	S_2	S_3	S_4	v_{sw}
ON	OFF	ON	OFF	0
OFF	ON	ON	OFF	E_1
OFF	ON	OFF	ON	$E_1 + E_2$

II. CONTROL PRINCIPLE OF HEECS INVERTER

A. HEECS INVERTER OPERATION [6]

Fig. 1 depicts a HEECS-based inverter circuit that is connected to the grid through an ac inductor [6], [21], [24].

Note that the multi-level dc/dc converter consists of switching devices S_1, S_2, S_3, and S_4 as well as an LC filter. Table 1 lists relations between switch states and the output of the switching network, v_{sw}.

If voltage command to the dc/dc converter is smaller than E_1, S_1 and S_2 operate in PWM mode. However, if voltage command is larger than E_1 and smaller than $E_1 + E_2$, S_2 is always ON; moreover, S_3 and S_4 operate in PWM mode. The dc/dc converter is controlled such that the capacitor voltage v_c follows the fully rectified sinusoidal reference voltage. The unfolding inverter consists of switching devices S_{ap}, S_{an}, S_{bp}, and S_{bn}. It switches every 180° electrical degrees of the line frequency waveform. The inverter output voltage v_{inv} is also a sinusoidal waveform. Voltage waveforms for the circuit in Fig. 1 are depicted in Fig. 2.

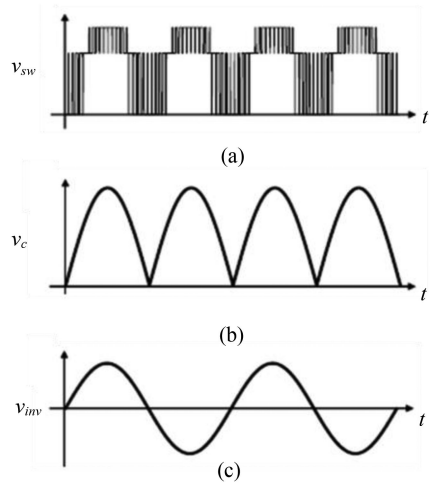

FIGURE 2. Voltage waveforms of HEECS: (a) dc/dc converter switching circuit output voltage, (b) dc capacitor voltage, (c) inverter output voltage.

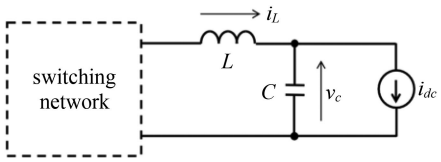

FIGURE 3. Equivalent circuit of HEECS.

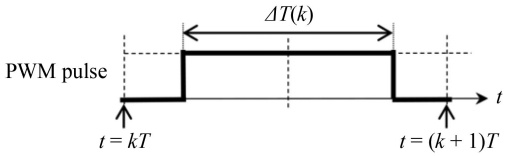

FIGURE 4. PWM pulse waveform.

B. CONTROL LAWS

1) DIGITAL CONTROL MODEL

Fig. 3 depicts the equivalent circuit of HEECS inverter [20], [21]. The resonance frequency of the LC filter is in the order of kilohertz, which is considerably higher than line frequency of 50 or 60 Hz. Furthermore, the sampling control frequency of the dc/dc converter (20 kHz) is high. The ac side transient phenomena are considerably slower than that of the dc-side. Thus, the ac output circuit of the inverter is replaced by a dc current source i_{dc}. The circuit equation [25], [26] for the equivalent circuit in Fig. 3 is:

$$\frac{\mathrm{dx}}{\mathrm{dt}} = Ax\,(t) + B_1 u\,(t) + B_0 i_{dc} \tag{1}$$

where $\mathrm{x}(t) = \begin{bmatrix} v_c(t) \\ i_L(t) \end{bmatrix}$, $u(t) =$ output of the switching network

$$\mathrm{A} = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix},\ B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix},\ B_0 = \begin{bmatrix} -1/C \\ 0 \end{bmatrix}$$

The voltage pulse of the dc chopper is assumed as centered in the sampling time, as shown in Fig. 4. The width is defined as $\Delta T(k)$ during the sampling period (kT to $(k+1)T$). Consequently, the sampled-data model [25], [26] of Eq. (1) is

$$\mathrm{x}\,[k+1] = Fx\,[k] + G_1 \Delta T\,[k] + G_0 i_{dc}\,[k]$$

$$\mathrm{F} = e^{AT} = \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \end{bmatrix},\ G_1 = e^{AT/2} B_1 E = \begin{bmatrix} g_{11} \\ g_{12} \end{bmatrix},$$

$$G_0 = A^{-1}\left(e^{AT} - I\right) B_0 = \begin{bmatrix} g_{01} \\ g_{02} \end{bmatrix} \tag{2}$$

where F can be expressed as :

$$F = e^{AT} = \begin{bmatrix} cos\omega_n T & \sqrt{\frac{L}{C}} sin\omega_n T \\ -\sqrt{\frac{C}{L}} sin\omega_n T & cos\omega_n T \end{bmatrix}$$

$$\omega_n = \frac{1}{\sqrt{LC}}$$

The capacitor voltage v_c can be controlled in two ways: DBVCL [6], [20] and DBCCL+VC [22], [23]. These approaches are discussed next.

2) DBVCL

The pulse width $\Delta T(k)$ of DBVCL is decided such that the output voltage $v_c(k+1)$ at the next sampling instant $(k+1)T$ matches the voltage reference $v_{cref}(k+1)$ [6], [21].

Considering the first row of Eq. (2), we get

$$v_c\,(k+1) = F_{11} v_c\,(k) + F_{12} i_L\,(k) + g_{11} \Delta T\,(k) + g_{01} i_{dc}\,(k) \tag{3}$$

and solving for $\Delta T(k)$ after replacing $v_c(k+1)$ with v_{cref} yields DBVCL as

$$\begin{aligned} \Delta \mathrm{T}\,(k) &= \left(v_{cref} - F_{11} v_c\,(k) - F_{12} i_L\,(k) - g_{01} i_{dc}\,(k)\right)/g_{11} \\ &= \left[-\tfrac{F_{11}}{g_{11}} \ -\tfrac{F_{12}}{g_{11}}\right] x\,(k) + \frac{1}{g_{11}} v_{cref} - \frac{g_{01}}{g_{11}} i_{dc}\,(k) \\ &= K_1 x\,(k) + \frac{1}{g_{11}} v_{cref} - \frac{g_{01}}{g_{11}} i_{dc}\,(k) \end{aligned} \tag{4}$$

The first, second, and third terms of Eq. (4) represent the state feedback, reference input, and disturbance feedforward compensation, respectively. Fig. 5 depicts the control block diagram of DBVCL. The transfer functions as well as locations of poles and zeros for this control system are analyzed in Appendix A1.

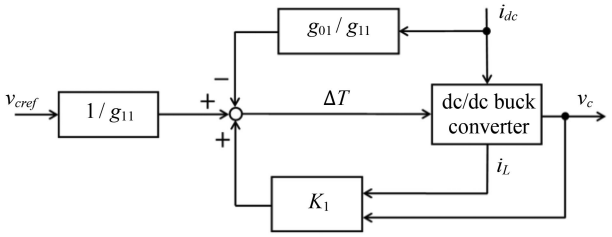

FIGURE 5. Control block diagram of DBVCL.

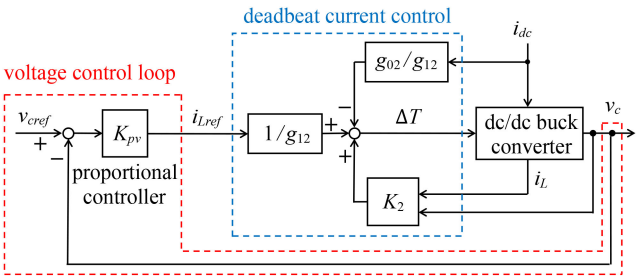

FIGURE 6. Control block diagram of DBCCL + VC.

3) DBCCL

The pulse width ΔT(k) of DBCCL is decided such that the inductor current i_L(k+1) at the next sampling instant $(k+1)T$ matches the current reference $i_{Lref}\,(k+1)$ [22]–[24].

Considering the second row of Eq. (2), we get

$$i_L\,(k+1) = F_{21} v_c\,(k) + F_{22} i_L\,(k) + g_{12}\Delta T\,(k) + g_{02} i_{dc}\,(k) \tag{5}$$

and solving for $\Delta T(k)$ after replacing $i_L(k+1)$ with i_{Lref} yields DBCCL as

$$\begin{aligned}\Delta \mathrm{T}\,(k) &= \left(i_{Lref} - F_{21} v_c\,(k) - F_{22} i_L\,(k) - g_{02} i_{dc}\,(k)\right)/g_{12} \\ &= \left[-\frac{F_{21}}{g_{12}} \; -\frac{F_{22}}{g_{12}}\right] x\,(k) + \frac{1}{g_{12}} i_{Lref} - \frac{g_{02}}{g_{12}} i_{dc}\,(k) \\ &= K_2 x\,(k) + \frac{1}{g_{12}} i_{Lref} - \frac{g_{02}}{g_{12}} i_{dc}\,(k)\end{aligned} \tag{6}$$

The first, second, and third terms of Eq. (6) represent the state feedback, reference input, and disturbance feedforward compensation, respectively. Furthermore, a voltage control loop is added as an outer control loop, which is discussed next.

4) DBCCL+VC LOOP

A VC loop is added as an outer control loop around the current control, as shown in Fig. 6. The current reference i_{Lref} is generated by the proportional controller as

$$i_{Lref} = K_{pv}\left(v_{cref} - v_c\right) \tag{7}$$

The combination of Eqs. (6) and (7) is designated as DBCCL + VC. The transfer functions as well as the locations of poles and zeros for DBCCL + VC are analyzed in Appendix A2.

The application of DBCCL + VC to dc/dc converter has been reported [22], [23]. This paper reports the first application of this control strategy to inverter ac voltage control.

5) CURRENT CONTROL OF GRID-CONNECTED INVERTER USING HEECS

Considering the applications of grid-connected inverter, the inverter output voltage shall be synchronized with the grid voltage, and the output power shall be controlled to match the commanded value, as showcased by the control block diagram in Fig. 7. The current reference generator calculates

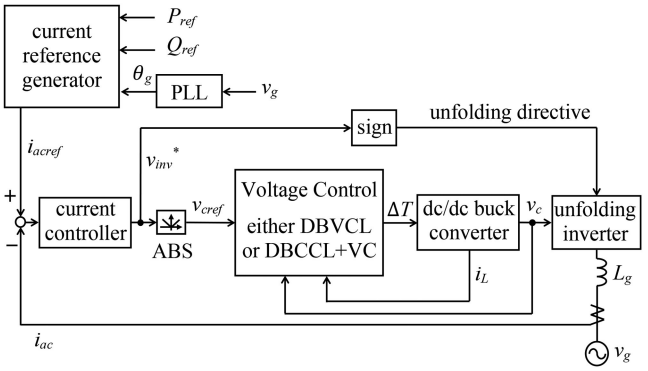

FIGURE 7. Control block diagram of current control for the grid-connected inverter based on HEECS.

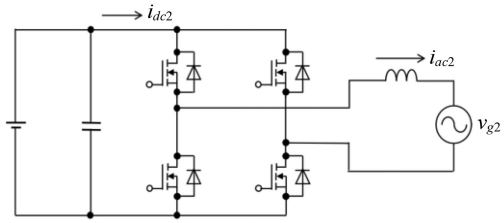

FIGURE 8. Grid-connected inverter using a conventional PWM voltage source inverter.

the current reference i_{acref} from the real power reference P_{ref}, reactive power reference Q_{ref}, and the grid electrical angle θ_g detected by phase-locked loop (PLL). The current i_{ac} to the grid is compared with the current reference i_{acref}, and the error becomes the input to the current controller. Further details of the current control are discussed in Appendix A3. The output signal $v_{inv}{}^*$ of this current controller becomes the inverter voltage command. The sign of $v_{inv}{}^*$ is used for selecting the switching pattern of the unfolding inverter. The absolute value of $v_{inv}{}^*$ becomes the voltage reference to the voltage controller of the dc/dc converter.

The voltage control block in Fig. 7 generates fully rectified sinusoidal voltage synchronized with the grid voltage. This block can be realized by either of two types of control laws: DBCVL (Fig. 5) or DBCCL + VC (Fig. 6). In Section I both these control methods are investigated further and compared in case of leading pf operation.

III. PROPOSED CURRENT CONTROL METHOD AFTER VOLTAGE ZERO CROSSING AND VOLTAGE CONTROL METHOD IN STEADY STATE OF HEECS INVERTER IN LEADING PF OPERATION

A. PROBLEM OF LEADING PF OPERATION IN HEECS INVERTER AND ITS ANALYSIS

For reference, the conventional PWM voltage source inverter connected to the grid is displayed in Fig. 8; moreover, typical simulated waveforms of grid voltage v_{g2}, ac current i_{ac2}, and dc current i_{dc2} of the circuit with leading pf in ideal condition are depicted in Fig. 9. In the PWM inverter waveforms in Fig. 9, the dc current changes from negative to positive at

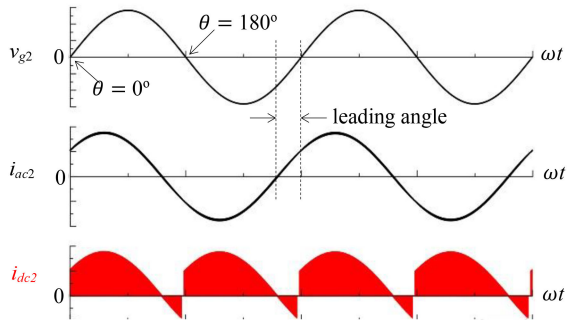

FIGURE 9. Simulated waveforms of the conventional PWM grid-connected voltage source inverter in leading pf operation.

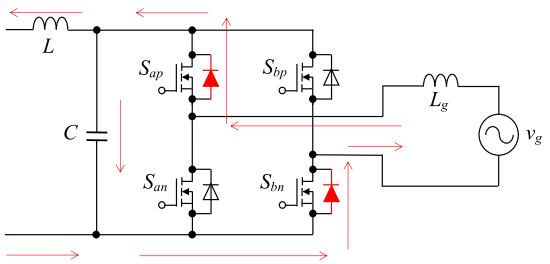

FIGURE 10. Current path before voltage zero crossing.

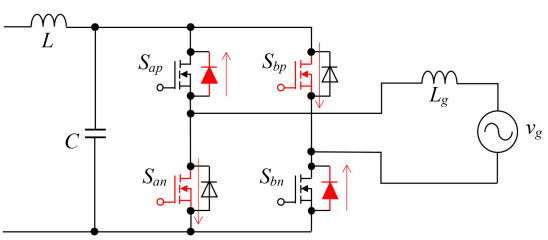

FIGURE 11. Device conduction states after voltage zero crossing.

voltage zero crossing because of the leading pf. Since voltage zero crossing occurs twice in every period of the ac line voltage, the voltage changes from negative to positive at 0° electrical angle, and from positive to negative at 180°. Herein, the 180° case is discussed in detail.

Fig. 10 shows the current path before zero crossing. The current paths are through the anti-parallel diodes of S_{ap} and S_{bn}. At zero crossing timing, the unfolding control circuit gives the ON gate signals to devices S_{an} and S_{bp}. Fig. 11 displays the device conduction states just after zero crossing. The current still flows through the anti-parallel diodes, which results in the "all-conduction mode" in which all four devices are conducting. The shoot-through of the bridge legs S_{ap}–S_{an} and S_{bp}–S_{bn} occurs, but the devices do not break down, and the circuit continues its operation. This phenomenon does not occur in the conventional PWM voltage source inverter with a high-capacitance capacitor on the dc side. Thus, the all-conduction mode is unique to unfolding inverters.

Analyzing the circuit behavior in the all-conduction mode, note that the capacitor is shorted. The resulting equivalent circuit of the dc/dc converter in the all-conduction mode as well as the dc inductor current flow are shown in Fig. 12. However,

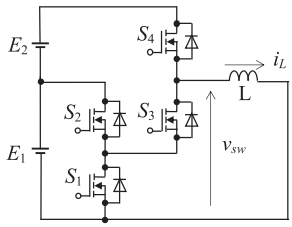

FIGURE 12. Equivalent circuit of the dc/dc converter in the all-conduction mode.

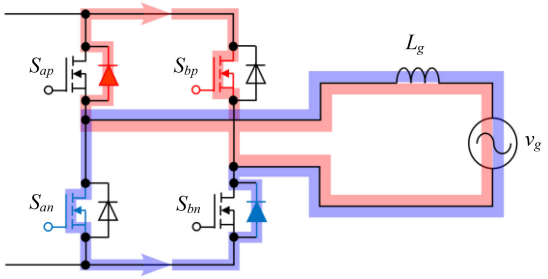

FIGURE 13. Ac current paths in the all-conduction mode.

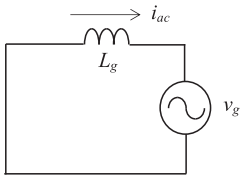

FIGURE 14. Equivalent circuit of the ac side in the all-conduction mode.

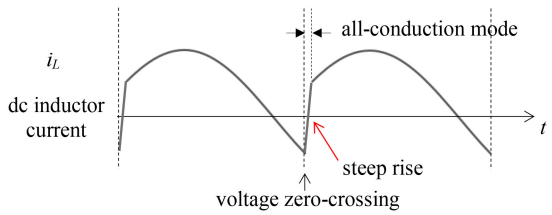

FIGURE 15. Ideal dc inductor current waveform after voltage zero crossing.

the ac current flow through the two paths as free-wheeling current is depicted in Fig. 13. Additionally, the equivalent circuit of the ac side in the all-conduction mode as well as the ac current flow are illustrated in Fig. 14. Thus, the two circuits behave independently. When the dc current increases and reaches the level of the ac current, the currents flowing through anti-parallel diodes are neutralized, which ends the all-conduction mode.

If the inductor current is controlled as described, the dc inductor current waveform exhibits a steep rise after voltage zero crossing as shown in Fig. 15.

B. PROPOSED CURRENT CONTROL METHOD IN THE ALL-CONDUCTION MODE

Fig. 16 illustrates the timing chart for current behavior analysis. At $t = t_1$, the voltage at the receiving end becomes zero,

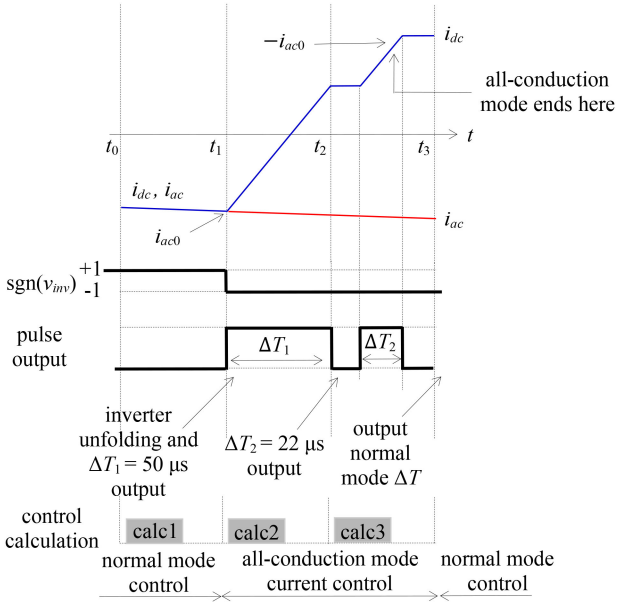

FIGURE 16 Example of current control in all-conduction mode.

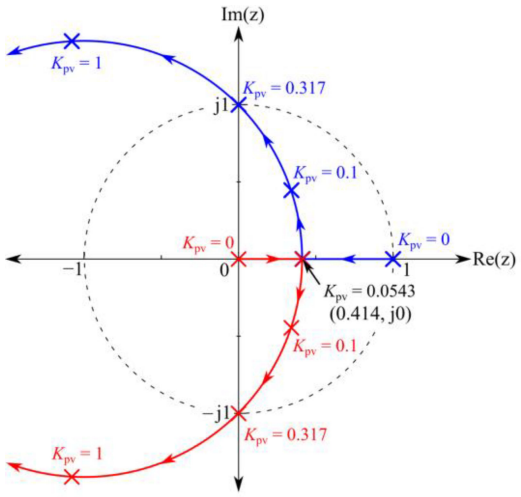

FIGURE 17 Root loci of voltage control loop.

and the ac current value at t_1 is i_{ac0}. As the time required for changing the dc current is sufficiently short, the ac current during this mode can be assumed constant. Fig. 11 shows that the dc current increases after $t = t_1$ and reaches -i_{ac0}; subsequently, the all-conduction mode ends. The time elapsed for this change is calculated next. The equation of the equivalent circuit in Fig. 12 can be expressed as

$$L\frac{di_L}{dt} = v_{sw} \tag{8}$$

where L is the inductance [H] and v_{sw} is the PWM pulse voltage with its pulse width assumed to be ΔT_{sum}. ΔT_{sum} can be pulse width of a single pulse, or can be sum of pulse widths of two or more pulses depending on i_{ac0} value. The inductor current starting from the initial value i_{ac0} evolves as

$$\begin{aligned} i_L(\Delta T_{sum}) &= i_{ac0} + \frac{1}{L}\int_0^{\Delta T_{sum}} E\,dt \\ &= i_{ac0} + \frac{E}{L}\Delta T_{sum} \end{aligned} \tag{9}$$

The time for the inductor current to reach $-i_{ac0} > 0$ can be calculated by

$$i_L(\Delta T_{sum}) = -i_{ac0} \tag{10}$$

The result is

$$\Delta T_{sum} = -2i_{ac0}L/E \tag{11}$$

Fig. 16 explains PWM voltage pulse generation during the all-conduction mode through a concrete example. The circuit parameters are: the carrier and sampling frequency are 20 kHz each; control period is $T = 50\mu s$; inductance of dc inductor is L = 2.43 mH; and dc voltage sources are E_1 = 280 V, E_2 = 125 V, and $E = E_1 + E_2$ = 405 V. Assuming that the ac current at voltage zero crossing is i_{ac0} = –6 A, in Eq. (11), pulse width is 12 A ∗2.43 mH/405 V = 72 μs. Since this value is longer than $T = 50\,\mu$s, more than one cycle is required for the all-conduction mode to end. Additionally, 72μs can be divided as

$$\Delta T_{sum} = 50\mu s + 22\mu s = \Delta T_1 + \Delta T_2 \tag{12}$$

where full duty (50 μs) and partial duty (22 μs) are the outputs of the first and second cycles, respectively. The pulse sequence corresponding to this numerical example is depicted in Fig. 16. If the absolute value of i_{ac0} is larger, more cycles are required. In contrast, if i_{ac0} is smaller, one cycle is sufficient. Thus, the dc inductor current can be controlled to reach an arbitrary value in the all-conduction mode by combining full and partial duty pulses (called as full duty and partial duty combination control, FDPDCC). For actual control, the partial duty is extended marginally (e.g., 2 μs) to ensure that the anti-parallel diodes turn off.

C. PROPOSED CONTROL METHOD DURING NORMAL MODE

Although the DBVCL has been used in HEECS control [6], [20], [21], the inductor current i_L and ac output voltage v_{inv} exhibit transient fluctuation even with unity pf, as described in [20]. Since i_L is not controlled properly, the voltage v_{inv} (output voltage of the unfolding inverter or receiving terminal voltage) fluctuates. Moreover, overshoot and oscillation become more significant with leading pf operation.

DBCCL + VC, as described in Section II-B-4, is used in this study. The voltage control loop gain K_{pv} is designed by using the root loci method, as displayed in Fig. 17. The poles of the voltage control loop start from the origin and 1 + j0 with $K_{pv} = 0$, approach each other with increasing gain, and become duplex roots with $K_{pv} = 0.054$. Note that $K_{pv} = 0.06$ is selected for the response to be non-oscillatory and realizing a smooth transition from the all-conduction mode

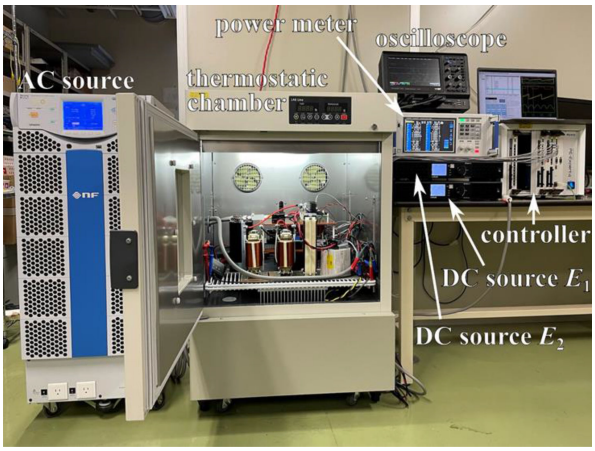

FIGURE 18. Experimental set-up.

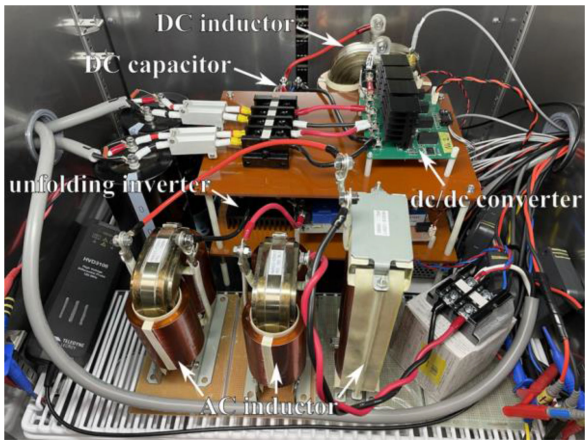

FIGURE 19. Circuit under test.

TABLE 2. Circuit Parameters

Grid voltage	280 Vrms, 50 Hz
Grid-tie inductor	L_g = 3.77mH (%impedance = 3.01%)
Dc capacitor	C = 8 μF
Dc inductor	L = 2.43mH
Dc source voltage	E_1 = 280 V, E_2 = 125 V
Dc/dc converter devices	SCT3017AL (Rohm)
Inverter devices	CAS325M12HM2 (Wolfspeed)
Carrier frequency	20 kHz

to the normal mode in leading pf operation. Design detail is described in Appendix A2.

IV. SIMULATION AND EXPERIMENT RESULTS

A. SET-UP

Figs. 18 and 19 show the experimental set-up and circuit under test, respectively. The circuit under test is implemented in a thermostatic chamber. Table 2 lists the circuit parameters used in the simulation and experiments. Moreover, Table 3 lists the equipment used in the experiment.

TABLE 3. List of Equipment

Ac voltage source	NF Corporation: DP060RS
Dc voltage source	Headspring: biATLAS-D HBPS-A2D525-502
Controller	PE Expert4
Oscilloscope	Teledyne Lecroy: Wavesurfer 3034z
Current sensor	Hioki: CT6862-05
Power meter	Hioki: PW6001

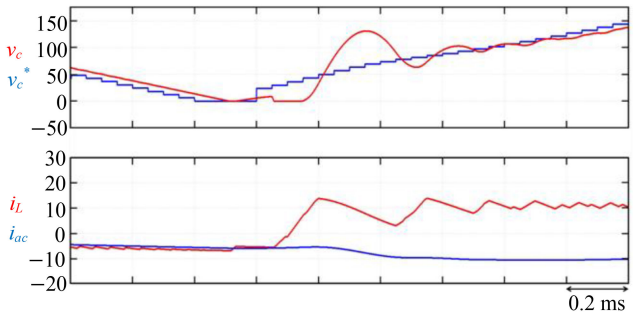

FIGURE 20. Capacitor voltage and inductor current waveforms near zero crossing with DBVCL (simulation).

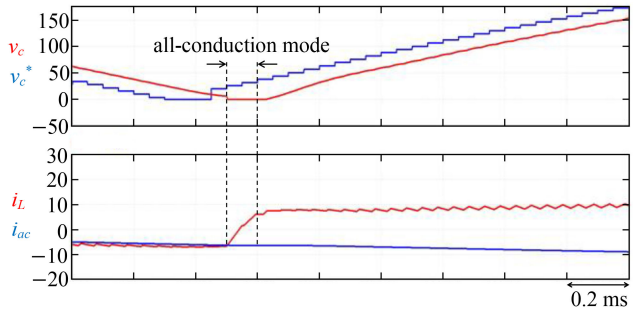

FIGURE 21. Capacitor voltage and inductor current waveforms near zero crossing with proposed control (simulation).

B. SIMULATION

First, the waveforms near voltage zero crossing of the DBVCL [20] and devised control (combination of FDPDCC and DBCCL + VC) are compared. The waveforms simulated with DBVCL are displayed in Fig. 20 in which P_{ref} = 1600 W, Q_{ref} = 1200 var, and pf = 0.8.

Overshoot and oscillation are observed in the capacitor voltage waveform. The controller neglects the all-conduction mode and attempts to achieve deadbeat voltage control. However, the terminals of the capacitor are shorted, causing deadbeat control to fail. The voltage pulse is significantly wide, and the inductor current becomes significantly large, which affects the waveforms. Oscillation is observed after the all-conduction mode because the pole allocation of DBVCL is intended for quick response, but the response is quicker than intended.

Fig. 21 displays the simulated waveforms near voltage zero crossing with the proposed control method (FDPDCC in the all-conduction mode and DBCCL + VC in the normal mode).

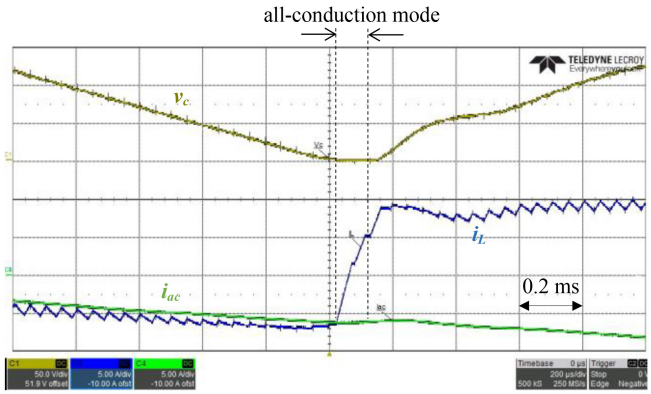

FIGURE 22. Experimental results: waveforms near zero crossing.

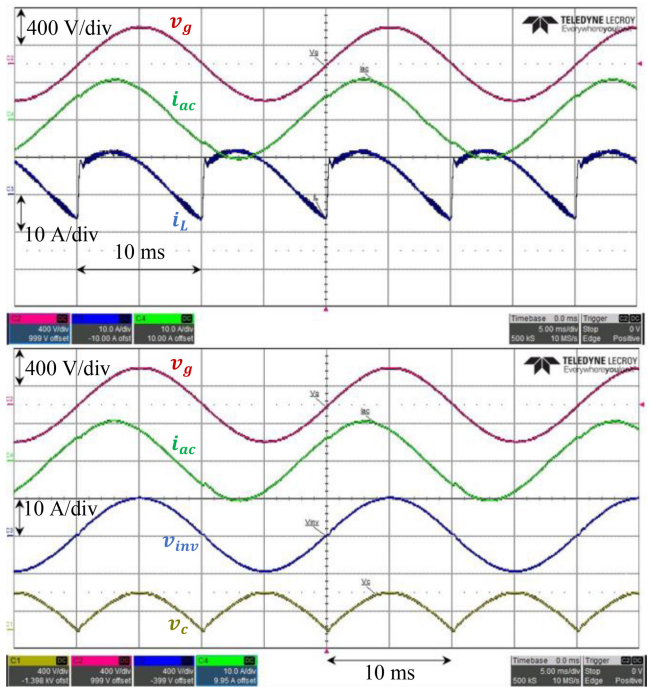

FIGURE 23. Experimental results: steady-state waveforms.

Note that the waveforms are realized with neither overshoot nor oscillation.

C. EXPERIMENTAL VERIFICATION

Fig. 22 illustrates the waveforms near zero crossing in the experiment, which are similar to the simulated waveforms in Fig. 21. Note that the circuit parameters are the same for simulation and experiment.

Fig. 23 illustrates the steady-state waveforms with $P_{ref} = 1600$ W, $Q_{ref} = 1200$ var, and pf $= 0.8$.

Fig. 24 shows the zoomed-in ac current of the second curve in Fig. 23 with an added ac current reference $i_{ac}{}^*$. The ac current is marginally distorted near zero crossing, but the THD is 3.1%, which is sufficiently small.

Table 4 lists the steady-state characteristics with various real and reactive powers with a total VA $= 2000$ VA, with

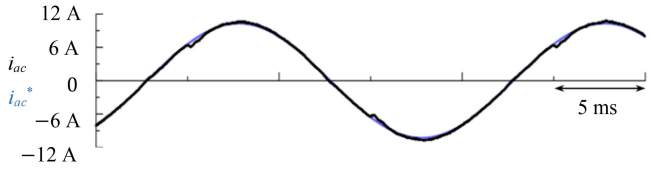

FIGURE 24. Experimental results: zoomed-in ac current from Fig. 23(in black) and ac current reference (in blue).

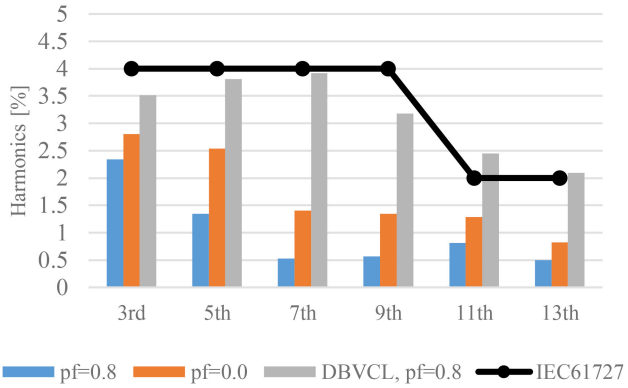

FIGURE 25. Harmonic contents of the ac current.

the left and right halves of the table showcasing the powering and regenerating modes, respectively. The efficiency is measured using a very accurate virtual transformer-based back-to-back asynchronous loss measurement method [29]. The measurement accuracy is approximately 0.006%. The efficiency decreases with decreasing pf, but still exceeds 99% even with pf $= 0.5$.

The harmonic contents of the ac current for the cases of pf $= 0.8$ and pf $= 0.0$ are described with upper limit values specified by IEC61727 in Fig. 25. Moreover, the harmonic contents of the ac current controlled by DBVCL with pf $= 0.8$ are shown in the figure. Fundamental component (100%) is abbreviated. The black line shows upper limits by IEC61727. Harmonic contents of pf $= 0.8$ case are in blue, those of pf $= 0.0$ case are in orange, and those of DBVCL are in grey. Therefore, the harmonic contents by the proposed scheme are well under the limit. Part of the harmonics by DBVCL (11^{th} and 13^{th}) exceed the limits and significantly worse than the proposed scheme.

Fig. 26 illustrates the transient response from $P_{ref} = 1600$ W and $Q_{ref} = 1200$ var to $P_{ref} = -1600$ W and $Q_{ref} = 1200$ var. As discussed in Appendix A3, dq-axis current control is conducted by estimating the virtual orthogonal component using a sinusoidal wave observer. The d- and q-axis currents are shown in Fig. 26. Note that the d-axis current follows the d-axis current reference within 5 ms.

Fig. 27 shows the relationship between the reactive power and inverter voltage (receiving terminal voltage) using the data in Table 4. The measured (red) and theoretical values (blue) are largely consistent. By using the proposed control method, the HEECS inverter can provide sufficient leading

TABLE 4. Experiment Result: Steady-State Characteristics (Total VA=2000VA)

Powering:					Regenerating:					
P [W]	Q [VAR]	Power Factor	$V_{ac\ rms}$ [V]	$I_{ac\ THD}$ [%]	P [W]	Q [VAR]	Power Factor	$V_{ac\ rms}$ [V]	$I_{ac\text{-}THD}$ [%]	Average Efficiency* [%]
2001.3	59.8	1.000	280.1	2.36	-1997.5	53.2	-1.000	279.6	1.49	99.75
1890.0	659.2	0.944	277.3	3.11	-1909.1	589.7	-0.955	276.8	2.89	99.70
1785.5	903.9	0.892	276.2	3.21	-1813.6	838.1	-0.908	275.7	3.14	99.67
1579.6	1227.4	0.790	274.7	2.92	-1619.7	1170.4	-0.811	274.3	3.98	99.59
1390.0	1438.5	0.695	273.7	3.51	-1437.8	1387.7	-0.720	273.3	4.21	99.51
970.1	1748.5	0.485	272.2	3.70	-1029.5	1712.0	-0.515	271.9	3.77	99.23
-34.7	1998.7	-0.017	270.9	4.91						77.26**

*The average efficiency is calculated using the measured efficiencies during the powering and regenerating operations based on [29]
**Measured conversion efficiency by direct measurement method [7]

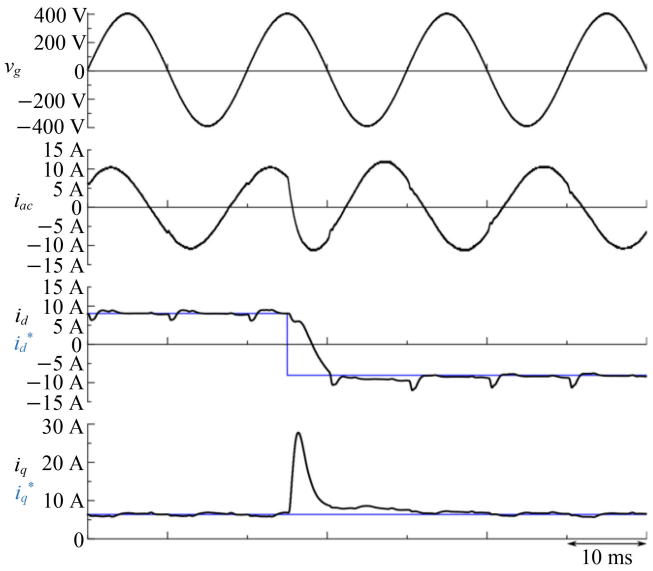

FIGURE 26. Experimental results: transient response.

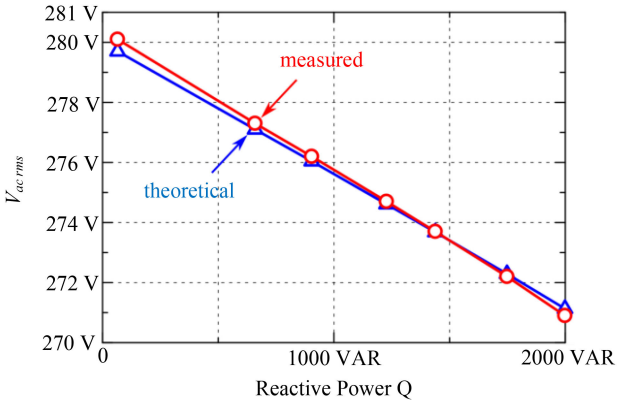

FIGURE 27. Relationship between the reactive power and receiving terminal voltage for powering mode (red: experimental, blue: theoretical).

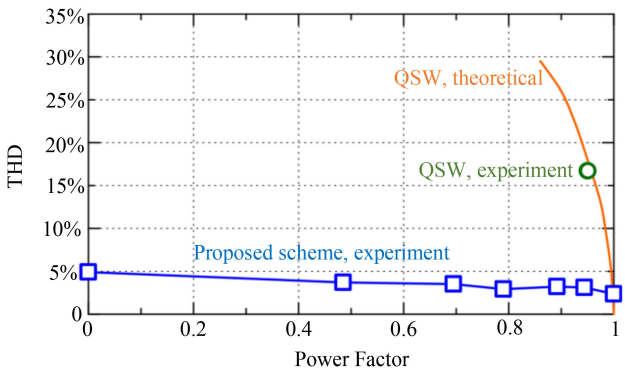

FIGURE 28. Comparison of THD.

reactive power such that the overvoltage of the receiving terminal is suppressed.

D. COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED SCHEMES

As stated in Section I, research on the non-unity pf operation of the unfolding inverter without additional circuits is lacking. Only two studies could achieve a variable pf without the use of additional circuits [10], [35]. A comparison of the pf–THD relation is shown in Fig. 28. Li [10] applied the quasi-sinusoidal waveform (QSW) current reference to handle reactive power. The curve in orange shows the theoretical THD by the QSW scheme. The green dot shows the experimental data by the QSW method with pf = 0.95 and THD = 16.7%. The blue curve is a plot of the THD data in the powering mode of the proposed method in Table 4. For the QSW scheme, the THD exceeds 5% with pf > 0.995. Additionally, the range of pf operation is limited to >0.86. In contrast, the THD of the proposed method is <5% within the range of pf operation of 0–1.

Furthermore, research presenting efficiency data is scarce. Fig. 29 depicts a comparison of the efficiency data. The orange curve with upward triangle marks shows the data reported by Min [35], which requires no additional circuit. The green curve with circle marks shows the data reported by Han [36], and the red curve with downward triangle marks shows those by Renaudineau [37]. The black diamond mark shows one

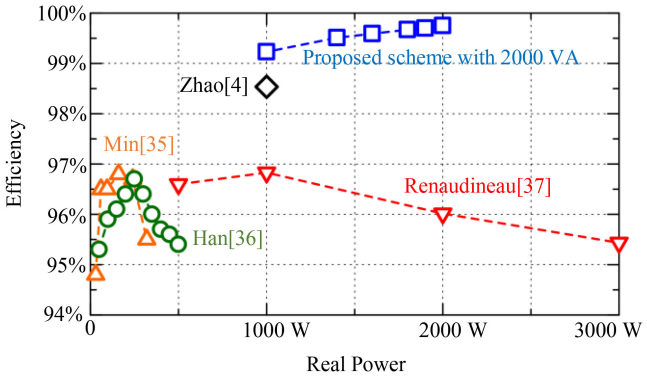

FIGURE 29. Comparison of efficiency.

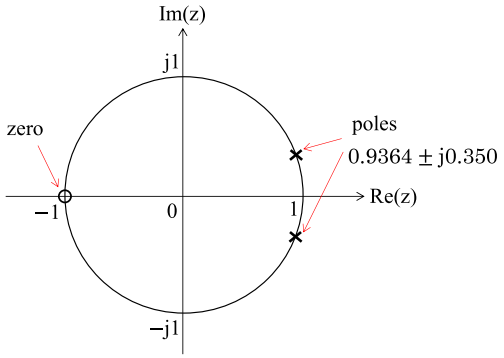

FIGURE 30. Pole-zero locations of the open-loop transfer function $v_c/\Delta T$.

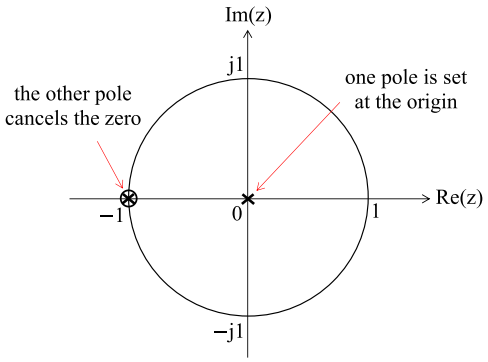

FIGURE 31. Pole-zero locations of the closed-loop transfer function v_c/v_{cref}.

point measurement by Zhao [4]. The data in [35], [36], [37], and [4] are measured at unity pf. The data in [37] contain measurements for more than 3000 W, but these efficiency values are lower and omitted in this graph. The blue curve shows the data of the proposed scheme plotted using Table 4 with total VA = 2000 VA, indicating variable pf. For instance, at 1579.6 W on the horizontal axis (real power), the pf is 0.79, which can be verified from Table 4. The inverter ratings in [35], [36], [37], and [4] were 320, 500, 5600, and 1000 W, respectively. Hence, comparing the efficiency of inverters with different ratings in the same condition is difficult. Nonetheless, the efficiency of the proposed inverter is significantly higher than those reported in previous studies.

V. CONCLUSION

Theoretical analysis and simulation are performed to clarify that the proposed novel control scheme can be used to operate grid-connected HEECS-based unfolding inverters with a leading pf. Furthermore, experiments are conducted to verify the simulation results. When the unfolding inverter is operated with a leading pf, the all-conduction mode occurs after voltage zero crossing. Transient dc current is controlled by FDPDCC in this mode, and the inverter smoothly returns to the normal mode operation after this mode by DBCCL + VC control. Furthermore, the overvoltage of the receiving terminal is suppressed by reactive power control. The conventional schemes require either additional circuitry or PWM operation as well as result in a large THD; however, our novel method requires neither. The operation pf range is 0 to 1, although limited to leading. Additionally, THD is small, and harmonics are compliant with grid code IEC61727. The efficiencies are 99.75% with pf 1.0 and 99.2% with pf 0.5, which are significantly better than other methods in literatures. Lagging pf operation will be discussed in a next opportunity.

APPENDIX A1

Analysis of the control system governed by DBVCL [6], [20], [21]

The output equation is

$$y_1 = v_c = H_1 x = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \tag{A1-1}$$

The open-loop transfer function from ΔT to v_c is

$$v_c/\Delta T = H_1(zI - F)^{-1}G_1$$

$$= \frac{g_{11}\left\{z - \left(F_{22} - F_{12}\frac{g_{12}}{g_{11}}\right)\right\}}{z^2 - (F_{11} + F_{22})z + F_{11}F_{22} - F_{12}F_{21}} \tag{A1-2}$$

If C = 8 μF and L = 2.43 mH, poles are at 0.9364±j0.350. The zero is at

$$z_{0v} = F_{22} - F_{12}\frac{g_{12}}{g_{11}} = -1$$

The pole and zero locations are depicted in Fig. 30. Additionally, the closed-loop transfer function is

$$v_c/v_{cref} = H_1(zI - (F + G_1K_1))^{-1}G_1\frac{1}{g_{11}}$$

$$= \frac{z+1}{z(z+1)} = \frac{1}{z} \tag{A1-3}$$

Thus, one pole is assigned at the origin of the z-plane, and the other pole cancels the zero of the open-loop transfer function.

The pole-zero locations of the closed-loop transfer function is shown in Fig. 31.

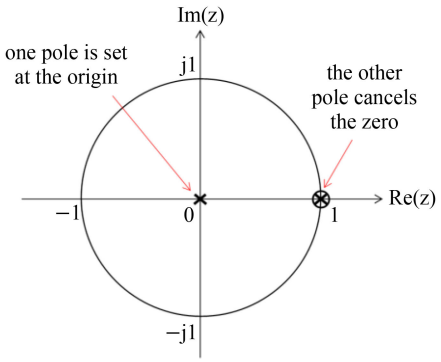

FIGURE 32. Pole-zero location of the transfer function i_L/i_{Lref}.

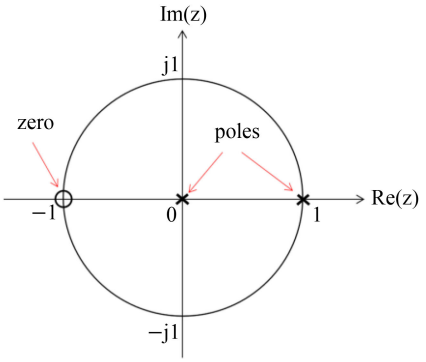

FIGURE 33. Pole-zero location of the transfer function v_c/i_{Lref}.

APPENDIX A2

Analysis of the control system governed by DBCCL + VC [22]–[24]

The output equation is

$$y_2 = i_L = H_2 x = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \tag{A2-1}$$

The open-loop transfer function from ΔT to i_L is

$$\begin{aligned} i_L/\Delta T &= H_2(zI - F)^{-1} G_1 \\ &= \frac{1}{z^2 - (F_{11} + F_{22})z + detF} g_{12}{}^* \\ &\quad \left\{ z - \left(F_{11} - F_{21} \frac{g_{11}}{g_{12}} \right) \right\} \end{aligned} \tag{A2-2}$$

Here, the zero of Eq. (A2-2) is

$$z_{0c} = F_{11} - F_{21} \frac{g_{11}}{g_{12}} = 1$$

If DBCCL is applied, the closed-loop transfer function from i_{Lref} to i_L becomes

$$\begin{aligned} i_L/i_{Lref} &= H_2(zI - (F + G_1 K_2))^{-1} G_1 \frac{1}{g_{12}} \\ &= \frac{z - z_{0c}}{z(z - z_{0c})} = \frac{1}{z} \end{aligned} \tag{A2-3}$$

Thus, one pole is assigned at the origin of the z-plane, and the other pole cancels the zero of the open-loop transfer function.

The pole-zero locations of the closed-loop transfer function are shown in Fig. 32. A VC loop is added around deadbeat current control (Fig. 6) to regulate the capacitor voltage. Additionally, the transfer function from the current reference i_{Lref} to the capacitor voltage v_c is

$$\begin{aligned} v_c/i_{Lref} &= H_1(zI - (F + G_1 K_2))^{-1} G_1 \frac{1}{g_{12}} \\ &= \frac{g_{11}}{g_{12}} \cdot \frac{z+1}{z(z-1)} = g_r \frac{z+1}{z(z-1)} \end{aligned} \tag{A2-4}$$

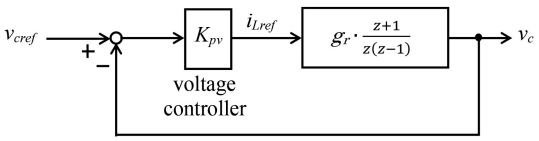

FIGURE 34. Simplified block diagram of the voltage control loop.

The two poles of Eq. (A2-4) are set at the origin and 1 + j0. The corresponding pole-zero locations are shown in Fig. 33. Next, Fig. 6 can be simplified as shown in Fig. 34.

The root loci of Fig. 34 are shown in Fig. 17. The root loci start from the origin and 1 + j0 with gain $K_{pv} = 0$. Two roots occur at 0.414 + j0 with gain 0.054, which subsequently separate upwards and downwards with a larger gain. The system becomes unstable with gain larger than 0.317. In the experiment, $K_{pv} = 0.06$ is used.

K_{pv} is calculated based on the energy balance between the dc inductor and capacitor [22], [23], but the basis for stability is ambiguous. This appendix clarifies the relationship between the stability of the discrete-time control system and gain.

APPENDIX A3

Dq-axis current control of single-phase grid-connected inverter

The three-phase to two-phase (abc to xy) transformation [30] and rotational (xy to dq) transformation [30] are used in the dq-axis current control in three-phase grid-connected inverter. These transformations are not feasible in a single-phase inverter. However, some schemes, such as orthogonal signal generator [31] and quadrature signal generator [32] have been proposed to generate virtual orthogonal components. A sinusoidal wave observer [27], [28] is used in this study to produce the orthogonal component. The state equation of the sinusoidal current wave generator for the state to be estimated (state variables i_x and i_y, output y, and radial frequency ω) is

$$\frac{d}{dt} \begin{bmatrix} i_x \\ i_y \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} i_x \\ i_y \end{bmatrix} \tag{A3-1}$$

$$y = i_{ac} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ i_y \end{bmatrix} \tag{A3-2}$$

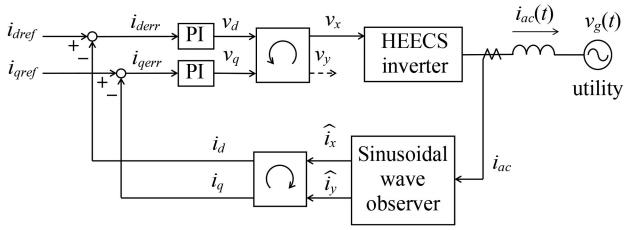

FIGURE 35. Current control block diagram with a sinusoidal wave observer.

where $i_{ac} = i_x$ is the ac current i_{ac} in Figs. 1 and 7, and i_y is a virtual orthogonal component. With estimated states $\hat{i}_x$, $\hat{i}_y$ and gain K_{sin}, a sinusoidal wave observer for Eqs. (A3-1) and (A3-2) can be constructed as

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_x\\ \hat{i}_y\end{bmatrix} = \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\begin{bmatrix}\hat{i}_x\\ \hat{i}_y\end{bmatrix} + K_{sin}\left(i_x - \hat{i}_x\right) \qquad \text{(A3-3)}$$

Subsequently, these two-phase components can be converted into dq components through rotational transformation as

$$\begin{bmatrix}i_d\\ i_q\end{bmatrix} = \begin{bmatrix}cos\omega t & sin\,\omega t\\ -sin\,\omega t & cos\,\omega t\end{bmatrix}\begin{bmatrix}\hat{i}_x\\ \hat{i}_y\end{bmatrix} \qquad \text{(A3-4)}$$

Thus, dq-axis current control becomes feasible for a single-phase inverter. The current control block diagram with sinusoidal wave observer is shown in Fig. 35.

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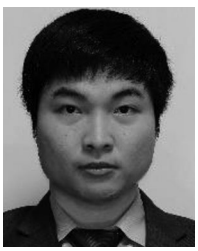
Yasuhiko Miguchi (Life Member, IEEE) received the master's degree in systems engineering from Kobe University, Kobe, Japan, in 1979. From 1979 to 1998, he was with Toshiba Corporation, Fuchu Works, Tokyo, Japan. He was a Visiting Researcher with the University of Missouri-Columbia, Columbia, MO, USA, from 1984 to 1986. He was a Researcher with United Technologies Research Center, East Hartford, CT, USA, from 1998 to 1999. He was with Nippon Otis Elevator Company, Shibayama, Chiba, Japan, from 2000 to January 2020. He is currently a Researcher with Yokohama National University, Yokohama, Japan. His research focuses on power electronics and its control. He is a Member of the Society of Instrument and Control Engineers, Institute of System, Control, and Information Engineers, and IEE of Japan.



Hadi Setiadi (Member, IEEE) received the B.Eng. degree in electrical power engineering from the Bandung Institute of Technology, Bandung, Indonesia, in 2014, and M.S. and Ph.D. degrees in electrical and electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2016 and 2020, respectively. He is currently a Postdoctoral Researcher with Yokohama National University, Yokohama, Japan.

Yoshiki Nasu (Student Member, IEEE) received the B.E. degree in electrical and computer engineering from Yokohama National University, Yokohama, Japan, in 2020. He is currently working toward the M.E. degree in electrical and electronics engineering from Yokohama National University. His research focuses on power electronics.

Hidemine Obara (Member, IEEE) received the Ph.D. degree in electrical and electronics engineering from Chiba University, Chiba, Japan in 2015. From October 2015 to March 2016, he was a Postdoctoral Researcher with Tokyo Metropolitan University, Tokyo, Japan. Since April 2016, he has been with Yokohama National University, Yokohama, Japan. He is currently an Associate Professor. His research interests include multi-level-topology-based linear amplifiers, multi-level power converters, and digital active gate drivers.

Atsuo Kawamura (Life Fellow, IEEE) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1981. After a five-year-stay with the University of Missouri-Columbia, Columbia, MO, USA, as a Faculty Member, he joined the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama, Japan, in 1986. After he retired there as a Professor Emeritus in 2019, he became a Professor of Power Electronics Endowed Chair. His research interests include power electronics, digital control, electric vehicles, train traction control, and robotics. He is a Fellow with the IEE Japan. He was the recipient of several transactions paper awards from the IEEE and IEE of Japan, as well as International Power Electronics and Motion Control Conference Award.