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Constant Delay-Line Repetitive Control Analysis for Variable Frequency Operation

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ABSTRACT The proposed paper deals with the complete analysis which is the basis of the common tuning procedure of variable sampling Repetitive Controllers for adjustable output frequency applications. The described approach can be applied without limitations to grid-tied inverters (narrow frequency variations), as well as to AC waveform generators (wide frequency variations). The operation of the proposed approach is to keep the Repetitive Control main delay line at a constant size, resulting in a very suitable implementation on FPGA-based control platforms. The effects of the desynchronization between the PWM modulator and the Control Loop will be accurately described, and the inherent delays will be expressed in closed form. Additional effects, like beating frequencies, are illustrated as well and described by closed-form expressions. Experimental verification is carried out to prove the effectiveness of the presented analysis.

INDEX TERMS Desynched operation, FPGA, repetitive control, variable frequency.

NOMENCLATURE

RC	Repetitive Control.
n	Length on the RC delay line.
PWMM	PWM Modulator.
CA	Control Algorithm.
N	Number of switching periods (at F_{SW}) where both the CA and the PWMM return to be synchronous.
M	Number of CA iterations during N switching periods.
GCD	Greatest Common Divisor.
LCM	Least Common Multiple.
MTM	Minimum Trigger Mismatch.
k	Maximum delay samples to be considered from the CA point of view.
MaxTotDelay	Maximum delay to be considered from the CA point of view.
w	Generic switching period.
γ	CA iterations within the timeframe w.
CTM	Control Triggers Mismatch.
ATM	Acquire Triggers Mismatch.
TotDelay	Delay to be considered from the CA point of view, for the generic switching period.
MaMS	Maximum Mismatches Step.
MiMS	Minimum Mismatches Step.

I. INTRODUCTION

In grid tied applications, where the grid frequency changes or even in stand-alone mode when the output fundamental harmonic must be modified, a conventional repetitive controller requires an interpolation method or additional memory to achieve frequency adaptability. It results in very complicated control structures, which in many cases tend to favor alternative control strategies. On the other hand, Repetitive Control (RC) at a fixed frequency could offer much better performance combined with implementation simplicity [1]. Moreover, the RC can be combined with additional controller topologies to build very high-performance structures as in [2], [3].

The family of fixed sample rate RC strategies includes several different approaches. In [4], the control variables are updated depending on the phase of the grid voltage to reflect the grid frequency deviations in the average period delay unit. In [5] the Virtual Variable Sampling (VVS) method, which creates an adjustable virtual delay unit to closely approximate a variable sampling delay, is proposed to allow the discrete Fourier transform based selective harmonic RC to be frequency adaptive. In a quite similar manner, a frequency

adaptive virtual variable sampling-based RC is proposed in [6], considering an integer ratio between the fundamental frequency and the RC sampling. Unlike VVS, such a control scheme accommodates frequency fluctuations by replacing fixed sampling period delays with VVS period delays. In [7] the same authors proposed a very similar control structure to be applied to a full-bridge inverter instead of a three-phase inverter.

A different approach to managing the operation of RC under frequency variation is called the fractional delay method. In [8], the mentioned method is applied to electrical drives for the torque ripple compensation. It is straightforward the extension to the general variable frequency operation of power inverters. Another technique is about the implementation of a delay z^{-N} with non-integer N, according to Fractional Delay (FD) filters design theory [9]. In practice, denoting with F the fractional part of the controller order N [10], the fractional delay z^{-F} can be well approximated by a Finite Impulse Response (FIR) Lagrange interpolation [11]. A similar approach uses to define N as a coefficient D plus an offset d, so that, as the reference frequency changes keeping D constant, it is possible to manage the variation through the offset d using Pasues have been clarified and analyzed in [15], with a specific approach that performs a sort of oversampling between measure acquisition and Repetitive Control action. This method introduces several drawbacks due to the oversampling technique, which requires high performance analog inputs in the control board. Moreover, the oversampling reduces the available time that can be used to perform the calculations related to the control algorithm.

In [16] the effects of having a variable output fundamental frequency have been compensated thanks to the usage of a very high switching frequency SiC inverter. However, that approach is very limited to a certain device and for medium to low power applications. A possible application of the proposed approach could improve the effectiveness of the method in [17], where the RC is used to compensate the dead-time distortion in grid-tied inverters without taking into consideration the frequency variations.

On the other hand, for all the techniques that use a delay-line of constant length, thus varying the execution time of the RC as a function of the variable fundamental frequency, an analysis relating to the effects of desynchronization has not been carried out. Therefore, the lack of synchronization between the sampling time and the RC period, requires a detailed analysis aimed at highlighting the drawbacks that this type of operating mode entails and any possible corrective actions. With the aim of filling this gap, a very thorough investigation on the effects of desynchronization will be provided in this article.

The previously proposed control structure [18], where the RC is executed at variable frequency to compensate the variation of the output frequency, needs an accurate analysis about delays, beating frequencies as well as benefits and drawbacks. In fact, being the RC desynched from the main scheduler, the desired control bandwidth could be affected by the introduced

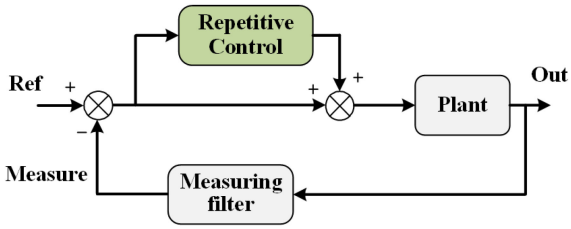

FIGURE 1. Plug-in type RC.

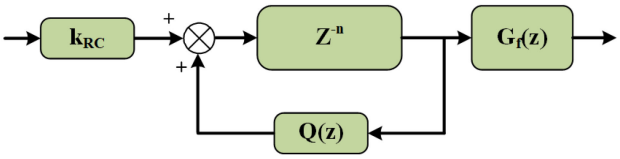

FIGURE 2. Discrete form repetitive controller.

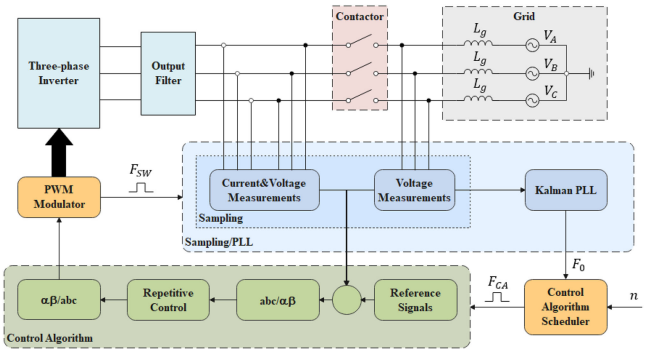

FIGURE 3. Block scheme for the frequency adaptive repetitive control.

control delay. The proposed analysis is at the basis of any future task as deriving a suitable tuning procedure or finding actions to fix the issues that will be illustrated.

The present work is organized into three main sections. Initially, the proposed control architecture is briefly illustrated in Section II. Section III shows the analysis for de-synchronized operation between the control loop and modulation loop. Finally, the proposed theoretical approach has been experimentally validated and the results are shown in Section IV.

II. CONSTANT DELAY-LINE REPETITIVE CONTROL

Plug-in type Repetitive Control can be represented as shown in Fig. 1 considering its integration with plant and feedback. Moreover, the RC discrete form can be summarized as illustrated in Fig. 2, where n is the ratio between the period of the reference signal and the digital sampling time, z^{-N} is the main delay line, $G_f(z)$ is the stability compensator (i.e., in many cases it is an additional constant delay) and $Q(z)$ is a quality factor for the feedback.

When it is necessary to deal with variable fundamental frequency signals, while an RC based control algorithm is implemented and intended to work with a constant delay line length (n), the structure illustrated in Fig. 3 lets to achieve very

high performances with negligible additional computational efforts or memory usage [18].

In this method three loops are realized to execute the control algorithm with a variable frequency, which is generally different from the switching and sampling main frequency. The first loop contains two decoupled and totally independent structures, the *PWM Modulator* (PWMM) used to provide opening/closing signals to the inverter's switches and to send the trigger signal to the *Sampling/PLL* block according to the switching frequency. This guarantees that measures acquisition task can sample the instantaneous average values.

The *Control Algorithm* scheduler has been specifically intended to provide the trigger signal for the *Control Algorithm* (CA) according to the PLL estimated fundamental frequency. As shown in Fig. 3, the *Control Algorithm* is tight to the synch signal which has the same frequency of the *PWM Modulator* only when the output frequency is the rated one. In fact, that loop runs at a variable F_{CA} frequency, calculated from the delay line length n and the PLL fundamental frequency F_0 (or the desired output frequency when in stand-alone mode):

$$F_{CA} = n \cdot F_0 \tag{1}$$

Before starting to illustrate the effects of the RC desynched operation, control implementation must be briefly described. This will help the reader to better understand the quantities that will be introduced to describe each specific cause-effect ratio.

Complete control code including the main scheduler, the PLL for grid synchronization and the *Control Algorithm* synch signal generation have been placed on the FPGA of the PED-Board controller. Each part has been implemented using 32-bit single-precision floating-point arithmetic thanks to the supported LabVIEW environment.

To carry out the experimental tests at the variable frequency when operating in grid-connected mode, the electrical grid was emulated by a dedicated 3-phase 4-leg inverter working in UPS mode. Both switching frequency and *Control Algorithm* frequency have been derived considering the FPGA core clock, and then the ticks to be counted to obtain the desired frequencies.

Specifically, considering the FPGA clock of 120 MHz, the PWM carrier generated by an up/down counter, 15 kHz as the rated switching frequency, and 50 Hz as the rated output fundamental frequency, the maximum value to be counted is 4000 ticks resulting in a period of 8000 ticks. Accordingly, the RC delay line length will be fixed to 300 (i.e., 15 kHz over 50 Hz). Fig. 4 depicts the carrier waveform used in the FPGA to generate the PWM signals.

Desynched operation does not significantly increase FPGA resources. Additional logics and DSP cores are used to call the Repetitive Control Loop and to calculate the proper sampling time according to the output fundamental frequency. Specifically, two FPGA VIs have been compiled, where RC worked at constant and variable sampling mode. The assets related to the desynched operation can be estimated respectively in 1.4% of additional Slices and 2.7% of extra DSP cores. No incremental usage of FPGA Block RAMs.

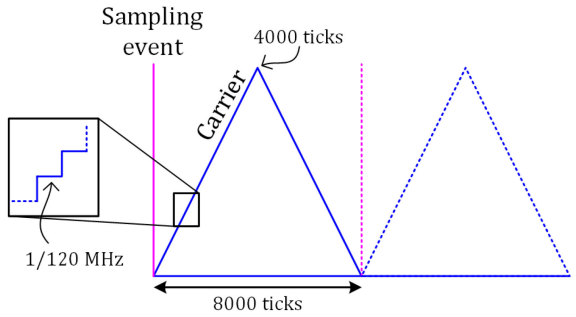

FIGURE 4. Illustration of the digitally generated PWM carrier.

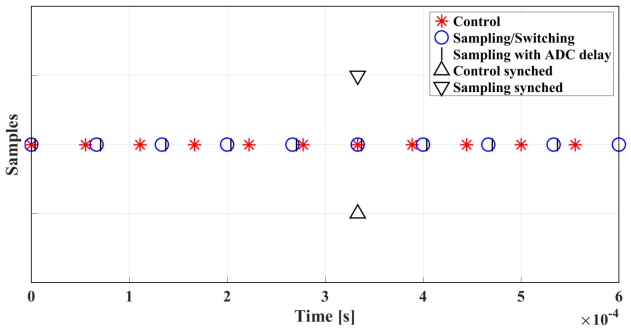

FIGURE 5. Trigger signals mismatch with $F_{SW} = 15$ kHz, $n = 300$, $F_0 = 60$ Hz and $F_{CA} = 18$ kHz.

III. ANALYSIS FOR DESYNCHED OPERATION

Even if the aforementioned control structure can allow to maintain very high RC's performance dealing also with a wide range of output frequencies, some considerations must be carried out in order to achieve a comprehensive analysis and then to perform a suitable RC's gains tuning. Due to the time shift between the *CA* and the *PWMM*, the delay evaluation is a mandatory task before any tuning consideration. It can be considered that the *Control Algorithm* at F_{CA} and *PWMM* at F_{SW}, start with a condition where their triggers are aligned. As shown in Fig. 5, it is possible to notice that after N switching periods (at F_{SW}) both the *Control Algorithm* and the *PWMM* return to be synchronous (for one sample only). During these N switching periods the *Control Algorithm* has been executed M times. For each of the N periods, the time mismatch between the main scheduler and the *CA* changes.

This leads to a total delay that changes cycle-by-cycle, maintaining a periodic behaviour characterized by a frequency equal to F_{SW} divided by N, or F_{CA} divided by M. Moreover, in the presented analysis, additional terms must be included. The delay required by the *CA* to provide the updated modulating signals after it has been triggered is Δt_{MODg}, and the delay from the *Sampling/PLL* trigger to the instant when all required measures are available is Δt_{ACQ}. Both negatively affect the total delay and then the system stability.

The next step is the calculation of the maximum delay which affects the *Control Algorithm* concerning the specific operating conditions, such as switching period and fundamental output frequency.

A. MAXIMUM DELAY EVALUATION (MAXTOTDELAY)

Analytically, it is possible to obtain a closed-form expressions for N (at F_{SW}), and M (at F_{CA}), after which the tasks return to be synchronous:

$$N = \frac{F_{SW}}{GCD\{F_{SW}, F_{CA}\}} = \frac{LCM\{F_{SW}, F_{CA}\}}{F_{CA}} \tag{2}$$

$$M = \frac{F_{CA}}{GCD\{F_{SW}, F_{CA}\}} = \frac{LCM\{F_{SW}, F_{CA}\}}{F_{SW}} \tag{3}$$

where *GCD* and *LCM* represent respectively the *Greatest-Common-Divisor* and the *Least-Common-Multiple* between F_{SW} and F_{CA}.

Moreover, once N and M have been calculated the *Minimum-Triggers-Mismatch* (*MTM*) between the *Control Algorithm* and *PWM Scheduler* can be evaluated according to (4). This gives the minimum amount of time the *CA* lags the *PWMM* synch signal for a certain output fundamental frequency.

$$MTM = \frac{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}}{M - N} \tag{4}$$

Consequently, according to the quantities Δt_{MOD_g} and Δt_{ACQ}, two parameters can be defined as shown in (5) and (6), representing how large these delays are with respect of the period identified in (4).

$$y = Floor\left\{\frac{(M-N)\cdot \Delta t_{MOD_g}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}}\right\} \tag{5}$$

$$u = Floor\left\{\frac{(M-N)\cdot \Delta t_{ACQ}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}}\right\} \tag{6}$$

where *Floor* operator returns the integer part without rounding.

It can be noticed that both (5) and (6) yield an indeterminate 0/0 form when the output frequency is equal to the rated one. However, by defining Δt_{MOD_g} as the *CA* period minus a quantity that at least can be assumed equal to a δ-part of the *CA* period ($\delta > 1$), the expression (7) can be written:

$$\Delta t_{MOD_g} = T_{CA} - \frac{T_{CA}}{\delta} = \frac{1}{F_{CA}} - \frac{1}{\delta \cdot F_{CA}} = \frac{\delta - 1}{\delta} \cdot \frac{1}{F_{CA}} \tag{7}$$

Rewriting M as follows:

$$M = \frac{F_{CA}}{F_{SW}} \cdot N \tag{8}$$

and using de l'Hôpital theorem the indeterminate form can be solved leading to the result reported in (9):

$$\lim_{F_{CA}\to F_{SW}} \frac{(M-N)\cdot \Delta t_{MOD_g}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}} = \frac{\delta - 1}{\delta} \tag{9}$$

It must be noticed that when F_{CA} matches F_{SW}, both N and M are equal to 1. Moreover, in the previous analysis, Δt_{MOD_g} has been defined as the portion of the *CA* period. When the two frequencies match, Δt_{MOD_g} must not exceed the carrier period $1/F_{SW}$ (δ must be greater than 1). This allows representing the Δt_{MOD_g} delay as a function of the switching period, and N as a function of M.

Noticed that the same conclusion can also be reached for the indeterminate form of (6) when $M = N$:

$$\lim_{F_{CA}\to F_{SW}} \frac{(M-N)\cdot \Delta t_{ACQ}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}} = \frac{\delta - 1}{\delta} \tag{10}$$

According to (9) and (10), when the *Control Algorithm* rate matches the switching frequency, y and u must be forced to be zero as in (11) and (12):

$$\begin{aligned} y &= Floor\left\{\lim_{F_{CA}\to F_{SW}} \frac{(M-N)\cdot \Delta t_{MOD_g}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}}\right\} \\ &= Floor\left\{\frac{\delta - 1}{\delta}\right\} = 0 \end{aligned} \tag{11}$$

$$\begin{aligned} u &= Floor\left\{\lim_{F_{CA}\to F_{SW}} \frac{(M-N)\cdot \Delta t_{ACQ}}{\frac{1}{F_{SW}} - \frac{1}{F_{CA}}}\right\} \\ &= Floor\left\{\frac{\delta - 1}{\delta}\right\} = 0 \end{aligned} \tag{12}$$

The additional parameter in (13) can be defined as the maximum delay samples at the main switching frequency F_{SW}, from the measure acquisition trigger signal and the instant when the modulating signals are loaded into the *PWM Modulator*. The k quantity must be intended as the maximum delay samples to be considered from the *Control Algorithm* point of view. Accordingly, the time delay can be obtained from (14) for a direct comparison with F_{SW}.

$$k = \left[Floor\left(\frac{N + y + u}{M}\right)\right] + 1 \tag{13}$$

$$MaxTotDelay = \frac{k}{F_{SW}} \tag{14}$$

Fig. 6 graphically highlights the previously defined quantities. The upper triangular waveform shows the carrier related to F_{SW} that is used to trigger the *Sampling/PLL*. The bottom triangular waveform is related to F_{CA} for a 70 Hz fundamental output frequency. Triggers mismatches have been represented to show *MTM* and *MaxTotDelay*. Finally, Δt_{MOD_g} and Δt_{ACQ} have been also shown in Fig. 6 to achieve a comprehensive view. According to the previous analysis, Fig. 7 illustrates the value of k when the output fundamental frequency F_0 changes from 20 Hz to 80 Hz.

Notice that the reported Δt_{MOD_g} and Δt_{ACQ} values are related to the implemented LabVIEW FPGA control software, they are measured when the complete control structure is running: maximum jitters have been considered to include the worst-case scenario.

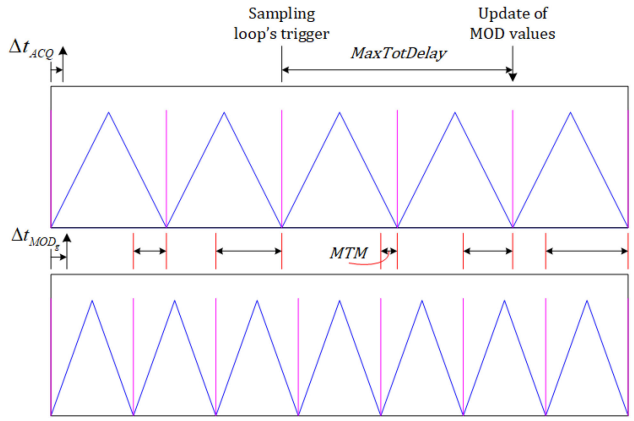

FIGURE 6. Triggers mismatch with $F_{SW} = 15$ kHz and $F_{CA} = 21$ kHz.

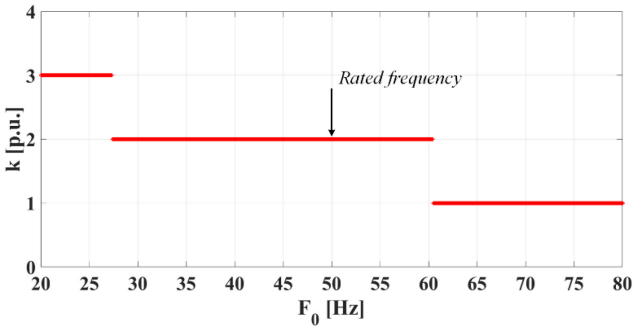

FIGURE 7. k vs output fundamental frequency F_0 with $F_{SW} = 15$ kHz, $n = 300$, $\Delta t_{MODg} = 7.6$ µs and $\Delta t_{ACQ} = 3.975$ µs.

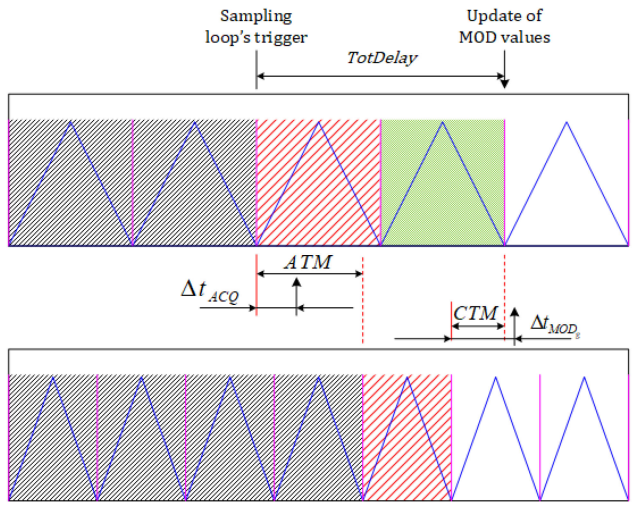

FIGURE 8. Main parameters for *MaxTotDelay* alternative calculation. $F_{SW} = 15$ kHz and $F_{CA} = 21$ kHz, $w = 4$, $\gamma = 5$, $q = 2$, $k = 2$.

B. MAXTOTDELAY ALTERNATIVE CALCULATION

As doublecheck, *MaxTotDelay* has been also evaluated with respect to the estimated fundamental frequency, following a different approach.

Considering the generic switching period w (in Fig. 8 filled in green), where w can vary from 1 to N (being N the amount of switching period where both *CA* and *PWMM* are in phase again), the elapsed *CA* iterations until the timeframe w can be obtained as:

$$\gamma = Floor\left\{\frac{wT_{SW}}{T_{CA}}\right\} = Floor\left\{\frac{wF_{CA}}{F_{SW}}\right\} \tag{15}$$

With reference to the w switching period, the *Control-Triggers-Mismatch* (*CTM*) between the trigger of the $w+1$ switching period and the trigger of the $\gamma+1$ *CA* will be equal to (graphically from Fig. 8):

$$CTM\,(w) = wT_{SW} - \gamma T_{CA} = \frac{w}{F_{SW}} - \frac{\gamma}{F_{CA}} \tag{16}$$

If the *CA* is fast enough to update the modulating signals before the $w+1$ period (or $CTM(w)$ is greater than Δt_{MODg}), the updated modulating signals will be related to the γ +1 *CA* iteration. On the contrary, the modulating signals will be related to the γ *CA* iteration (this is the case represented in Fig. 8 where the *CA* iteration to be considered has been dashed in red). The q quantity shows how many switching periods have elapsed in a timeframe equal to γ *or* γ-1 *CA* periods:

$$\begin{cases} q = Floor\left\{\frac{\gamma F_{SW}}{F_{CA}}\right\}\Big|_{CTM(w)>\Delta t_{MOD_g}} \\ q = Floor\left\{\frac{(\gamma-1)F_{SW}}{F_{CA}}\right\}\Big|_{CTM(w)\leq\Delta t_{MOD_g}} \end{cases} \tag{17}$$

Fig. 8 shows the case $CTM \leq \Delta t_{MODg}$ where the second equation of (17) must be used in order to calculate the q quantity, which graphically will be equal to the number of the switching periods (dashed in black).

Moreover, with reference to the w switching period, the *Acquire-Triggers-Mismatch* (*ATM*) between the trigger of the $q+1$ switching period and the trigger of the γ *or* γ-1 *CA* periods will be equal to (graphically from Fig. 8):

$$\begin{cases} ATM\,(w)|_{CTM(w)>\Delta t_{MOD_g}} = \frac{\gamma}{F_{CA}} - \frac{q}{F_{SW}} \\ ATM\,(w)|_{CTM(w)\leq\Delta t_{MOD_g}} = \frac{(\gamma-1)}{F_{CA}} - \frac{q}{F_{SW}} \end{cases} \tag{18}$$

The next step imposes the comparison between $ATM(w)$ and Δt_{ACQ} quantities to identify the coherent switching period which provides the measurements. If Δt_{ACQ} is lower than $ATM(w)$, sampling will be related to the $q+1$ switching period: this is the case represented in Fig. 8 where the switching period to be considered has been dashed in red. Otherwise, when Δt_{ACQ} is greater than $ATM(w)$, measures will be provided by the q switching period. Finally, the quantity $k(w)$ indicates the instantaneous delay linked to the number of switching periods:

$$\begin{cases} k(w) = w - q|_{ATM(w)>\Delta t_{ACQ}} \\ k(w) = w - (q-1)|_{ATM(w)\leq\Delta t_{ACQ}} \end{cases} \tag{19}$$

After all, the total time delay seen by the *CA* entering the $w+1$ switching period will be equal to:

$$TotDelay(w) = \frac{k\,(w)}{F_{SW}} \tag{20}$$

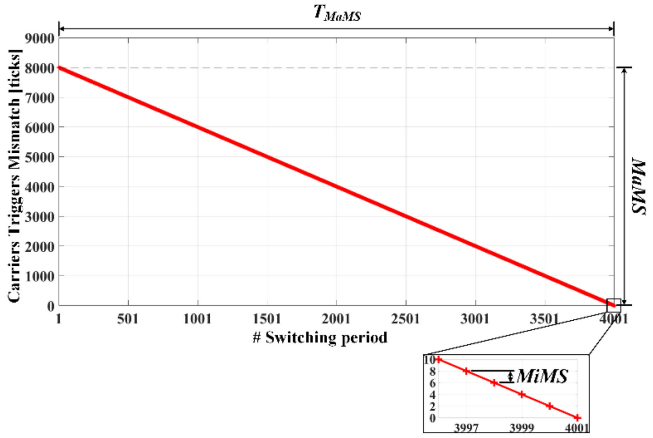

FIGURE 9. Beat on the AC currents when $T_{SW} = 8000$ ticks, $T_{CA} = 8002$ ticks, N = 4001, M = 4000.

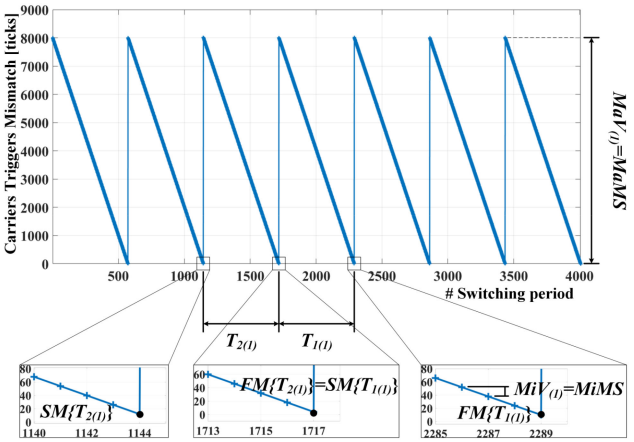

FIGURE 10. Mismatch variation between two synch events: main output beating frequency set to $F_0 = 49.91$ Hz, $T_{CA} = 8014$ ticks and $T_{SW} = 8000$ ticks. $f_{(I)} \approx 26.2$ Hz.

Varying w from 1 to N, it is possible to calculate the maximum total time delay (*MaxTotDelay*):

$$MaxTotDelay = \frac{MAX\{k(w)\}}{F_{SW}} \tag{21}$$

Comparing the result provided by (21) with the previously obtained in (14), the same *MaxTotDelay* value has been observed whatever was the considered fundamental frequency. This proves the effectiveness of the proposed analysis, where the first approach could be preferred due to its simplicity.

C. EFFECTS OF VARIABLE DELAY

Because the delay between the *CA* and *PWMM* triggers signals is not constant, additional effects are present in the output waveforms. The presented behavior is different from the maximum delay, which is used to tune the controllers.

Due to the variable delay of the triggers mismatch during the N switching periods, beat frequencies are introduced into the output waveforms producing in some cases a very high distortion. Before taking any action to solve or at least mitigate this problem, an accurate analysis concerning the generated beating must be carried out.

It is important to point out that, in order to characterize the distortions introduced in the output waveforms, it is necessary to characterize the effects that produce such distortions: variable temporal misalignment between the *CA* and the *PWMM*. To address this problem, two additional parameters should be defined. The *Maximum-Mismatches-Step* (*MaMS*) is the maximum variation between two consecutive triggers delays, whereas the *Minimum-Mismatches-Step* (*MiMS*) is the minimum variation. *MaMS* and *MiMS* are respectively shown in Fig. 9 and in Fig. 10, which highlight the related quantities.

The *MaMS* value can be evaluated from N, M and the *MTM* as in (22):

$$MaMS = MTM \cdot (N - |M - \alpha \cdot N|) \tag{22}$$

where:

$$\alpha = Round\left(\frac{M}{N}\right) \tag{23}$$

Round operator returns the rounded value to the nearest integer.

The *MiMS* can still be evaluated from N, M and the *MTM* as shown in (24):

$$MiMS = MTM \cdot |M - \alpha \cdot N| \tag{24}$$

From the ratio of *MaMS* and *MiMS* it is possible to discriminate the number of beat frequencies starting from one.

$$R_{MM} = \frac{MaMS}{MiMS} \tag{25}$$

When R_{MM} is an integer value, there will be only one beat frequency in the output waveforms (i.e., triggers between *CA* and *PWMM* having variable mismatch), whereas, if that ratio is not an integer, there will be more than one beating frequency.

1) R_{MM} INTEGER

Assuming an R_{MM} integer, which occurs only when the *MiMS* is equal to the *MTM*, the resulting *MaMS* will be periodic with period T_{MaMS}.

$$T_{MaMS} = \frac{N}{F_{SW}} = \left(\frac{MaMS}{MiMS} + 1\right) \cdot \frac{1}{F_{SW}} \tag{26}$$

One harmonic only will be introduced into the output waveforms. Fig. 9 shows the single frequency beating having a period equal to the T_{MaMS}. Operating conditions are obtained for a *Control Algorithm* ticks period equal to 8002, with respect to the rated 8000 ticks at 50 Hz output fundamental frequency. The same condition will be replicated to validate the analysis in the experimental campaign.

2) R_{MM} NOT INTEGER

However, when the R_{MM} value is not an integer value, additional beatings (i.e., harmonics) are present in the output waveform. In fact, a non-integer result will cause the same *MaMS* to not appear with the same period every time: there are two distinct periods $T_{1(1)}$ and $T_{2(1)}$. Under the operating condition of output fundamental frequency equal to $F_0 = 49.91$ Hz, Fig. 10 illustrates $T_{1(1)}$ and $T_{2(1)}$ periods, which can be evaluated as in (27) and (28) for the very first beating $(h) = 1$:

$$T_{1(1)} = [Floor\,(R_{MM}) + 1]\,\frac{1}{F_{SW}} \tag{27}$$

$$T_{2(1)} = [Floor\,(R_{MM}) + 2]\,\frac{1}{F_{SW}} \tag{28}$$

That specific operating condition was selected to make the effects graphically visible.

With reference to the first beating effects $(h) = 1$, the number of events $p_{(1)}$ between the two synchronous events where the *MaMS* appears with a period equal to $T_{1(1)}$, and the number of events $r_{(1)}$ where the *MaMS* appears with a period equal to $T_{2(1)}$, can be obtained from (29) and (30) without lacks of generality for the higher beatings:

$$p_{(h)} = \frac{\frac{MiV_{(h)}}{MTM} \cdot T_{2(h)} - N}{T_{2(h)} - T_{1(h)}} \tag{29}$$

$$r_{(h)} = \frac{MiV_{(h)}}{MTM} - p_{(h)} \tag{30}$$

where $MiV_{(1)}$ (*Minimum-Variation*) in the case of the main beating is equal to the *MiMS*. For the additional harmonics, $MiV_{(h)}$ calculation will be shown later.

According to the first beating frequency, the output waveforms are affected by a harmonic whose magnitude is related to the *MaMS* and whose period can be calculated as the weighted average of $T_{1(1)}$ and $T_{2(1)}$ where the weights are represented by $p_{(1)}$ and $r_{(1)}$. Regarding Fig. 10, when a non-integer R_{MM} is considered, the triggers mismatch at the end (*Final-Mismatch*, *FM*) of $T_{1(1)}$ or $T_{2(1)}$ periods is not equal to that one at the beginning (*Starting-Mismatch*, *SM*) of $T_{1(1)}$ or $T_{2(1)}$. Moreover, the difference between the *Final-Mismatch* (*FM*) and the *Starting-Mismatch* (*SM*) during $T_{1(1)}$ will differ from the same difference appearing during $T_{2(1)}$. This will cause at least one additional beating frequency to be present in the output waveforms.

As shown in Fig. 11, the second frequency is highlighted in yellow. It can be seen also that further beating is present in this specific case, which is shown by the orange line.

The following analysis shows how to characterize the second beating (i.e., yellow trace in Fig. 11), and how to check if additional harmonics will be present. This results in the complete correlation between the *CA* and *PWMM* time mismatch and the output quantities effects.

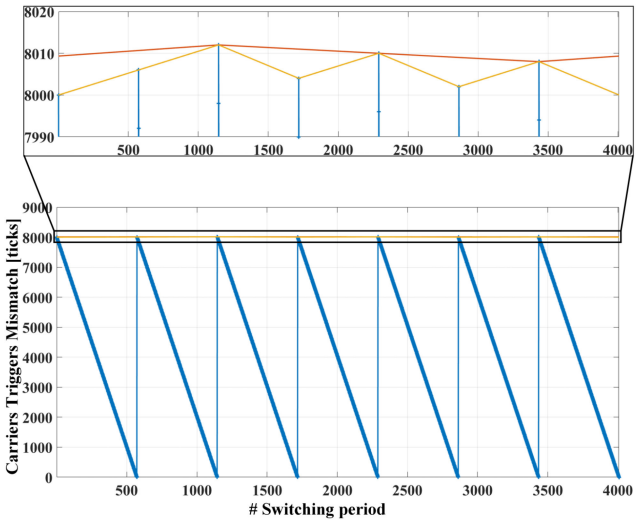

FIGURE 11. Complete beating frequencies for $F_0 = 49.91$ Hz.

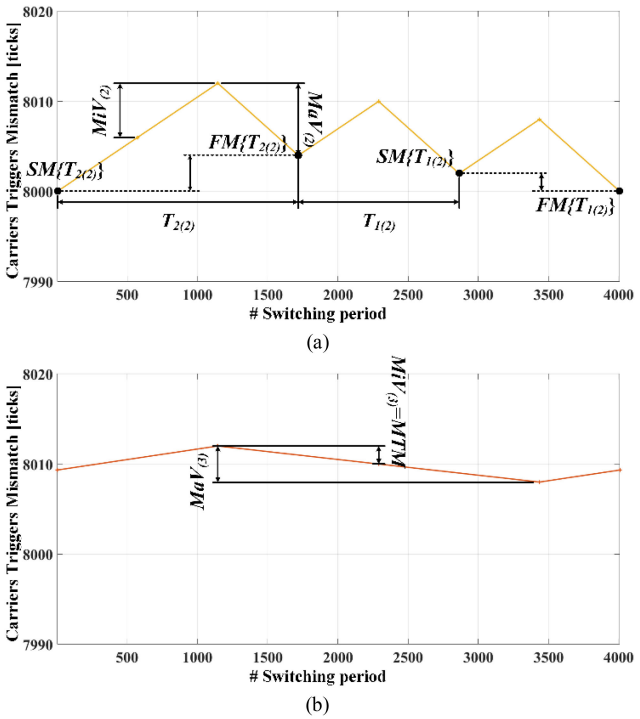

FIGURE 12. Temporal behavior of the trigger mismatch between *CA* and *PWMM* for $T_{CA} = 8014$ ticks and $T_{SW} = 8000$ ticks (i.e., $F_0 = 49.91$ Hz). (a) Second harmonic beating at $f_{(2)} \approx 11.23$ Hz. (b) Third harmonic beating at $f_{(3)} \approx 3.74$ Hz.

The *Maximum-Variation* (*MaV*) of the time mismatch for the main beating at $(h) = 1$ can be achieved as in:

$$MaV_{(1)} = MaMS \tag{31}$$

The second harmonic is characterized by a *Maximum-Variation* $MaV_{(2)}$ and a *Minimum-Variation* $MiV_{(2)}$ between the triggers of *CA* and *PWMM*. Hence, except the case of $(h) =$

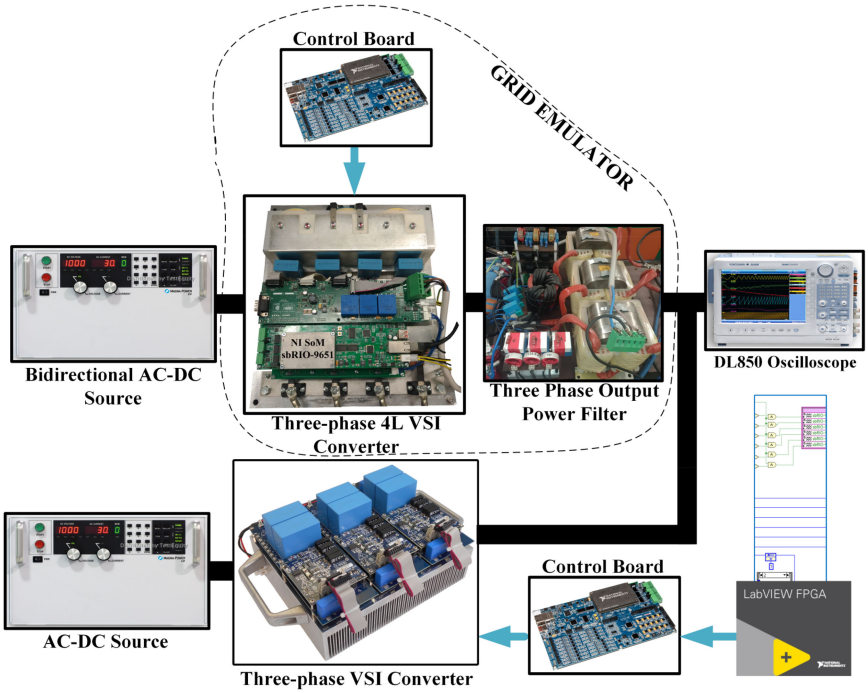

FIGURE 13. Experimental setup.

1, the related quantities can be computed knowing the results of the previous iteration:

$$MaV_{(h)} = \left| MaV_{(h-1)} - \left[Floor\left(\frac{MaV_{(h-1)}}{MiV_{(h-1)}} \right) + \beta_{(h)} \right] MiV_{(h-1)} \right| \tag{32}$$

$$MiV_{(h)} = \left| \left[Floor\left(\frac{MaV_{(h-1)}}{MiV_{(h-1)}} \right) + \varepsilon_{(h)} \right] MiV_{(h-1)} - MaV_{(h-1)} \right| \tag{33}$$

where:

$$\left\{ \begin{array}{l} p_{(h-1)} < r_{(h-1)} \rightarrow \ \beta_{(h)} = 0, \varepsilon_{(h)} = 1 \\ p_{(h-1)} > r_{(h-1)} \rightarrow \ \beta_{(h)} = 1, \varepsilon_{(h)} = 0 \end{array} \right|_{h>1} \tag{34}$$

The quantities $MaV_{(h)}$ and $MiV_{(h)}$ are shown in Fig. 12 for the same operating conditions of $F_0 = 49.91$ Hz, and the second and the third beatings. Fig. 12a shows the beating related to the second harmonic, whereas Fig. 12b shows the quantities related to the third beating. Subsequently, it is necessary to verify the presence of further beats by calculating the ratio between $MaV_{(h)}$ and $MiV_{(h)}$. As reported before, the procedure is iterative: if the ratio between $MaV_{(2)}$ and $MiV_{(2)}$ leads to a non-integer value, there will be at least an additional beating frequency with a lower frequency in the output quantities. In (35) and (36) are reported the analytical derivations to be used for calculating the current beating frequency.

$$T_{1(h)} = \left\{ \left[Floor\left(\frac{MaV_{(h)}}{MiV_{(h)}} \right) \right] \left(\beta_{(h)} T_{1(h-1)} + \varepsilon_{(h)} T_{2(h-1)} \right) + \left(\varepsilon_{(h)} T_{1(h-1)} + \beta_{(h)} T_{2(h-1)} \right) \right\} \frac{1}{F_{SW}} \tag{35}$$

$$T_{2(h)} = \left\{ \left[Floor\left(\frac{MaV_{(h)}}{MiV_{(h)}} \right) + 1 \right] \left(\beta_{(h)} T_{1(h-1)} + \varepsilon_{(h)} T_{2(h-1)} \right) + \left(\varepsilon_{(h)} T_{1(h-1)} + \beta_{(h)} T_{2(h-1)} \right) \right\} \frac{1}{F_{SW}} = = T_{1(h)} + \left(\beta_{(h)} T_{1(h-1)} + \varepsilon_{(h)} T_{2(h-1)} \right) \frac{1}{F_{SW}} \tag{36}$$

The quantities $p_{(h)}$ and $r_{(h)}$ for the new harmonic can be obtained from (29) and (30). After that, a completely iterative approach should be used for the next step: checking if additional beating is present until the ratio $MaV_{(h)}/MiV_{(h)}$ is integer. This allows to obtain analytically the harmonics which will be present in the output waveforms (currents or voltages).

IV. EXPERIMENTAL RESULTS

The suitable test-rig shown in Fig. 13 has been developed to prove the effectiveness of the proposed theoretical analysis. In order to operate with variable grid frequency, a 3-Phase 4-Leg inverter with an output power filter has been used as grid-emulator. The constant delay line Repetitive Control runs on the PED-Board controller, and it has been coded by using

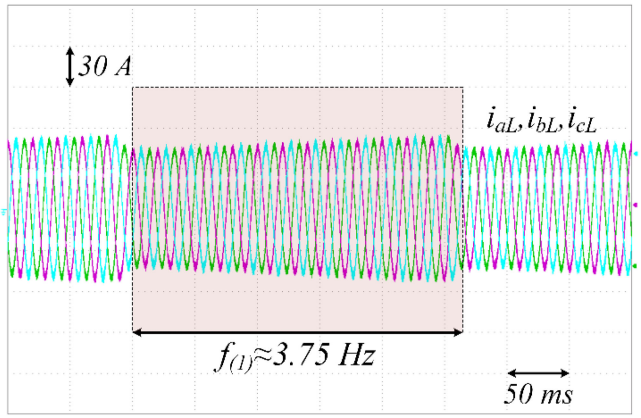

FIGURE 14. Beating frequency when $T_{CA} = 8002$ ticks, $T_{SW} = 8000$ ticks.

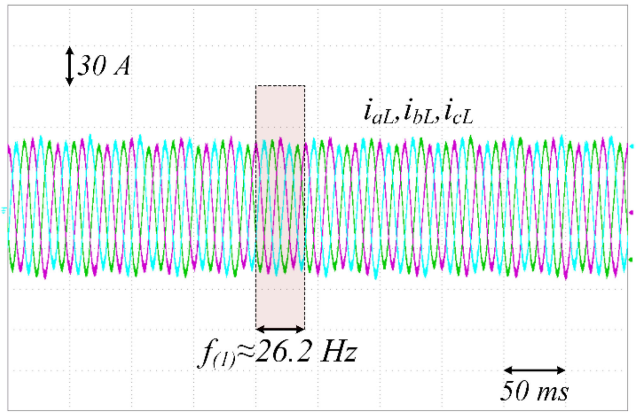

FIGURE 15. Highest beating frequency when $T_{CA} = 8014$ ticks, $T_{SW} = 8000$ ticks.

the LabVIEW environment. A 3-Phase inverter has been connected to the grid emulator at the output of the power filter.

Tests have been performed according to the system scheme illustrated in [18]. The experimental campaign was carried out under different operating conditions to graphically highlight the effect predicted in the previously shown analytical derivation.

The presence of the beating frequencies in the output waveforms has been observed by properly varying the fundamental frequency F_0, considering a grid-tied operation mode. First, a specific F_0 has been imposed leading the software to set a maximum counted value for the *CA* carrier equal to 4001. In this way, it has been possible to replicate the condition represented in Fig. 9. The results illustrated in Fig. 14 clearly show the presence in the output current waveforms of a beating with $f_{(1)}$ frequency. This distortion can be related to the trend of the misalignment between *CA* and *PWMM*, the period of which can be determined by (26).

Furthermore, the case represented in Fig. 14 concerns the circumstance in which the R_{MM} is an integer value that leads to a single beating frequency. In fact, no further frequencies have been detected for this operating condition in the output waveforms.

To observe more than one beat frequency in the acquired quantities, the fundamental frequency F_0 was imposed at 49.91 Hz to obtain a maximum value counted for the *CA* carrier equal to *4007* ticks (thanks to the variable frequency AC generator). In this way, three beat frequencies can be discriminated thanks to the proposed analysis, as shown in Figs. 10, 12(a) and (b).

Consequently, three main beating frequencies should appear in the output waveforms.

The first one is introduced by a very small mismatch as shown in Fig. 10. The analytical procedure provides an average weighted period corresponding to a frequency equal to 26.2 Hz.

Analyzing the output current waveforms with a suitable timeframe as shown in Fig. 15, an $f_{(1)} \approx 26.2$ Hz beating frequency can be observed. Being the output a pure three-phase

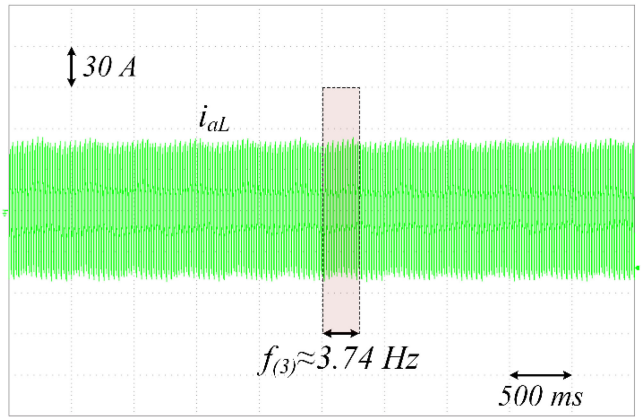

FIGURE 16. Lowest beating frequency when $T_{CA} = 8014$ ticks, $T_{SW} = 8000$ ticks.

arrangement, currents are still balanced, even if they exhibit an envelope at a frequency lower than the fundamental.

Furthermore, concerning a single current waveform to better highlight the effect, and by selecting an appropriate time range as shown in Fig. 16, it is possible to highlight another evident beat frequency equal to about 3.74 Hz. This frequency corresponds to that relating to the third beat shown in Fig. 12(b).

The intermediate beating frequency, related to the condition illustrated in Fig. 12a, is not as easily seen in the output waveforms as it is for the other two.

However, what has already been done shows a relationship between the trend relating to the misalignment of the variable triggers between *CA* and *PWMM* and the distortions detectable in the output waveforms. The method for determining the amplitude of these harmonics will be illustrated in subsequent work.

V. CONCLUSION AND FUTURE WORK

Concerning variable frequency applications managed by RC based control algorithms, it could be very effective to operate according to the control structure presented in [18], which

allows taking advantage of an incredibly good tracking of sinusoidal references. This permits to go beyond RC's weakness related to variable frequency operations, without any noticeable effects in terms of increased computational efforts or memory usage, while still operating with a constant delay line that makes it suitable for FPGA implementation. However, unrelating the operation of Repetitive Control to the main PWM scheduler, which represents the core of this technique, leads to a time mismatch between the *Control Algorithm* and *PWM Modulator* which needs to be evaluated.

Moreover, the trend concerning the variable triggers mismatch between *CA* and *PWMM* negatively affects the output waveforms introducing in some cases distortions, which are not tolerable. Hence, this paper reached two main goals.

The first one concerns the analytical evaluation of the maximum delay introduced in the control chain: the basis of any tuning procedure. The second objective concerned the analytical characterization of the beat frequencies introduced by the relative misalignment of the triggers relating to the *CA* and the *PWMM*. To prove the correctness of the proposed approach, a dedicated experimental campaign has been carried out. Results show the effectiveness of the illustrated mathematical approach, which allows determining the presence and the frequency of any beating it may arise, thanks to the reported closed form expressions. The determination of the amplitude of the shown beating frequencies represents the next step that will be treated in a further paper where some possible solutions to solve or at least mitigate the problem will also be presented.

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