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A Modular Multilevel DC-DC Converter With Auxiliary Inductor Circuits for Cell Voltage Balancing and Fast Output Response

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ABSTRACT Battery-equipped apparatuses, such as electric vehicles (EVs), renewable energy generations, and mobile devices, are widely used and still being developed. For the design and evaluation of these devices, there is a growing demand for dc power supplies to test the charge-discharge characteristics and lifetimes of batteries. As the voltage and performance of the batteries increase, the power supplies for the battery test must be able to handle higher voltages and have a faster output transient response. To handle a high voltage, multilevel converters that use multiple power devices with lower voltage ratings have often been used in recent years, in addition to using a single power device with high-voltage ratings. Among various circuit topologies, modular multilevel converters (MMCs) have been actively studied and developed. However, unlike dc-ac and ac-dc conversions, dc-dc conversion in MMCs has a problem in that the cell capacitor voltages cannot be balanced in principle because of less redundancy of operation states. Therefore, most MMC-based dc-dc converters achieve voltage balancing control by combining a dc-ac conversion, isolation transformer or inductor, and ac-dc conversion. However, these circuit configurations tend to have a large equivalent inductance and are unsuitable for achieving a fast output response. In this study, we analyze the dc-dc operation and its problems in the MMC circuit. Based on the analysis, a circuit topology using auxiliary inductor circuits and a control method suitable for a dc-dc converter are proposed. A prototype of a 6-cell MMC-based dc-dc converter using SiC-MOSFETs was designed and implemented, and it was demonstrated that cell voltage balancing control and fast output response could be realized.

INDEX TERMS Auxiliary inductor circuit, cell capacitor voltage balance, dc-dc converter, modular multilevel converter (MMC).

I. INTRODUCTION

In recent and future power networks, where renewable energy sources, such as photovoltaic (PV) and wind power are massively introduced into the power grid, batteries are one of the most important elements for maintaining the stability of the power system and utilizing energy effectively. In the development of products containing batteries, such as electric vehicles (EVs), uninterruptible power supplies (UPS) in data centers, and renewable energy generation, the batteries must be tested to obtain various characteristics using dc power supplies. Thus, the demand for dc power supplies for battery testing is increasing [1], [2]. In the automotive field, in particular, the global shift from gasoline-powered vehicles to EVs is accelerating rapidly, and the demand and specification requirements of dc power supplies for battery testing are becoming more stringent [3]. To charge as faster as possible, EV battery voltages are becoming higher year by year [4]. However, it has been reported that very fast charging and steep current waveforms negatively affect battery life [5]. Therefore, dc power supplies for battery testing are required

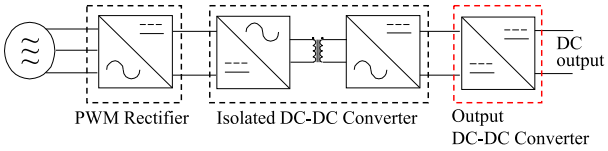

FIGURE 1. System configuration of a typical DC power supply for battery testing.

to have a higher performance to achieve higher voltage, larger power capacity, lower ripple, higher efficiency, and lower cost [4]. Fig. 1 shows the system configuration of a typical dc power supply for battery testing: a PWM rectifier converts grid ac power to dc with power factor correction, and isolation is achieved by an isolated dc-dc converter, such as a dual active bridge (DAB) converter. The performance of the final stage dc-dc converter is critical for determining the output characteristics of the dc power supply. This study aims to achieve a higher voltage, faster response, and lower output ripple of final-stage dc-dc converters in a dc power supply for battery testing. It is also important to achieve lower costs by applying the same design methodology to products with various voltages and power capacities. Considering the above requirements, in this study, we propose the application of a modular multilevel converter (MMC) topology as an output stage dc-dc converter. The MMC is configured using multiple cascaded modular H-bridges, and the handling voltage of the entire circuit can be determined by changing the number of bridge cells. It is well known that the MMCs are suitable for high- or medium-voltage dc-ac/ac-dc power conversion and are used in applications, such as HVDC and solid-state transformers (SST) [6]–[11]. However, in general MMC topologies, voltage balancing control for cell capacitors is possible at twice the fundamental frequency in dc-ac and ac-dc conversions. However, in dc-dc conversion, unlike in the case of power conversion involving ac, the voltage balance control for each cell capacitor cannot be achieved. Thus, there are issues to be addressed for the extension of dc-dc converters in the MMC topology. Based on this background, most MMC-based dc-dc converters are configured by combining a dc-ac converter, an isolation transformer or inductor, and an ac-dc converter to achieve cell voltage balance control [12]–[14]. However, such circuit configurations tend to have large inductances and are not suitable for a fast output response, which is determined by their time constants. Other solutions for realizing MMC-based dc-dc converters have been reported, where multiple MMC legs provide balanced voltage control of the capacitors [15]–[17]. A control scheme for an MMC-based dc-dc converter configured by multiple phase legs was reported to minimize the amplitude of the ac circulating current in [15]. In [17], a transformer-less dc-dc converter topology combining two legs of the MMC with capacitors to produce a physical ac current path was proposed. A multiport dc output converter using individual cell voltages was reported in [18]. In [19], various MMC-based dc-dc converter topologies with transformers were introduced. However, these circuits are controlled based on the capacitor voltage-balancing method using the ac component of the circulating current. Thus, they are not suitable for achieving fast responses.

In this study, the issue of cell capacitor voltage balancing control in dc-dc operation was clarified based on an analysis of the MMC operating modes. Based on this analysis, an MMC-based dc-dc converter topology with fast response and cell voltage balancing capability without the use of transformers, dc-ac, and ac-dc conversion is proposed [20]. The simulation and experimental results validate the effectiveness of the proposed circuit and capacitor voltage-balancing control. Furthermore, the proposed converter configuration provides a faster dynamic response than conventional MMC-based dc-dc converters with transformer combinations.

II. ISSUE OF VOLTAGE BALANCING IN GENERAL MMC TOPOLOGY ON DC-DC CONVERSION CASE

A typical 4-cell MMC leg with chopper cells has 14 operation modes, and Fig. 2 shows the typical current paths for some of them. For example, when the output voltage is E, no current flows through any of the cell capacitors in the upper arm, and current flows through the two cell capacitors in the lower arm, as shown in Fig. 2(a). In other words, the cell capacitors in the lower arm are charged or discharged, depending on the direction of the output current. In the modes shown in Fig. 2(b)–(d), it is impossible to always maintain all capacitor voltages at the normal value of $E/2$ because the direction of the current in each cell capacitor depends on the output voltage and current. For example, when the converter maintains the output voltage constant at $3E/4$, the capacitor in the upper cell #1 can only be discharged by the circulating current i_{cir} and the voltages converge to 0, as shown in Figs. 3(a) and (b). On the other hand, the capacitors in the lower arm can only be charged by the circulating current i_{cir} through the buffer inductors, and the voltages converge to E as shown in Figs. 3(c) and (d). Moreover, in the case of the output voltages $E/2$ and $E/4$, as shown in Figs. 2(c) and (d), respectively, each capacitor in the upper and lower arms can realize only one state between charging and discharging. There are four operating modes for each output voltage, except for cases where the output voltage is E or 0. Even if all operating modes are combined and controlled, the degrees of freedom of the charge and discharge operations for the capacitors are not sufficient for a fixed output voltage. Furthermore, even if H-bridge cells are applied instead of chopper cells, the degree of freedom is still not sufficient to realize voltage balancing control. Thus, the general single-stage dc-dc power conversion using the MMC leg does not provide sufficient redundancy in operating modes and cannot output a constant dc voltage while achieving capacitor voltage balance in principle.

Various topologies and control methods have been reported to realize dc-dc converters using MMC topology [12]–[19]. However, as noted above, most of these topologies utilize ac components of the circulating current and tend to have a relatively large buffer inductance, making it impossible to achieve the fast output response required for battery characteristic tests. To achieve a fast output response, the time constant of the current path determined by the buffer and filter

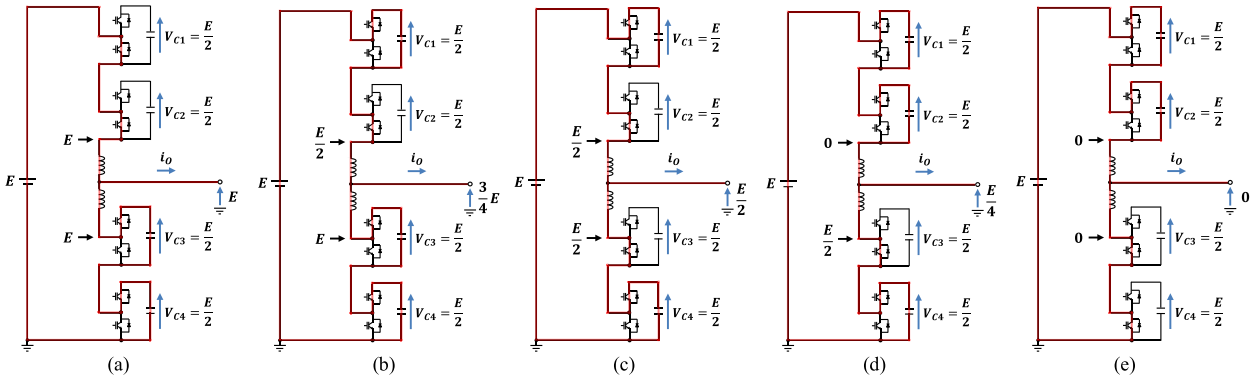

FIGURE 2. Part of operation states in general modular multi-level converter with 4-cells as a simplest example. (a)$v_{PWM} = E$ (1 mode). (b)$v_{PWM} = 3E/4$ (4 modes). (c)$v_{PWM} = E/2$ (4 modes). (d)$v_{PWM} = E/4$ (4 modes). (e)$v_{PWM} = 0$ (1 mode).

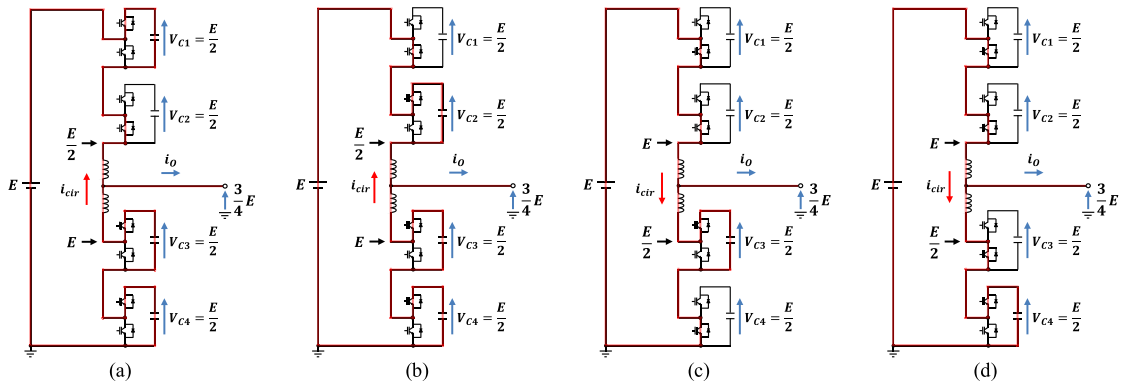

FIGURE 3. Operation states for the output voltage of $3E/4$ in general modular multi-level converter with 4-cells.

inductances and capacitances should be as small as possible. Therefore, a solution that includes a new voltage-balancing method with small passive components to realize a fast output response is required.

III. PROPOSED MMC-BASED DC-DC CONVERTER WITH AUXILIARY INDUCTOR CIRCUIT

A. CIRCUIT CONFIGURATION

In this study, we propose a single-stage dc-dc converter topology and its control that achieves capacitor voltage balancing and fast output response by adding auxiliary inductor circuits to the general MMC topology with chopper cells. Fig. 4 shows a circuit schematic of the proposed converter with 6-cells as an example. Each cell consists of a general chopper cell and an auxiliary circuit (L_{a1}–L_{a5}) comprising the same chopper cell and inductor, which can practically be implemented using an H-bridge cell. The lowest cell does not require an auxiliary circuit and can comprise only a chopper cell. The chopper cells and buffer inductors (L_u and L_l) between the upper and lower arms operate similarly to the general MMC topology shown in Fig. 2, combining each cell capacitor voltage to output an arbitrary voltage. The auxiliary inductor circuit is utilized to provide a circulating current to the cell capacitors (C_1–C_6) for charging and discharging operations to achieve voltage balance in each cell. The output filter using capacitor

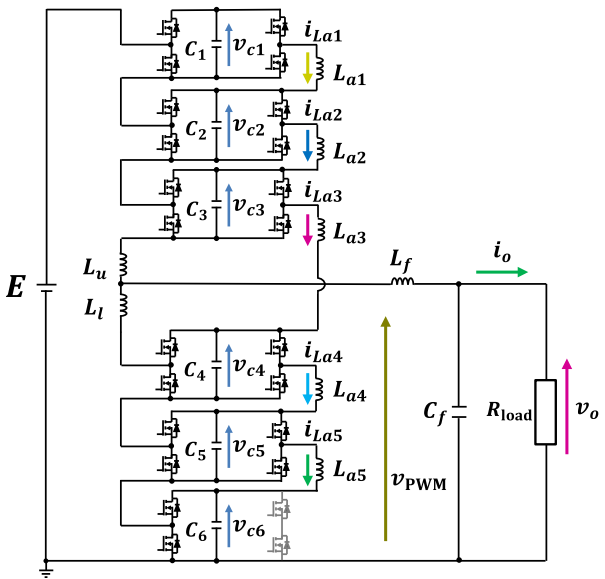

FIGURE 4. Proposed circuit configuration of MMC-based DC-DC converter (ex. 6-cells, 7-level output case).

C_f and inductor L_f is utilized to obtain a smooth dc output waveform and can be relatively smaller using the multilevel output voltage with lower harmonics.

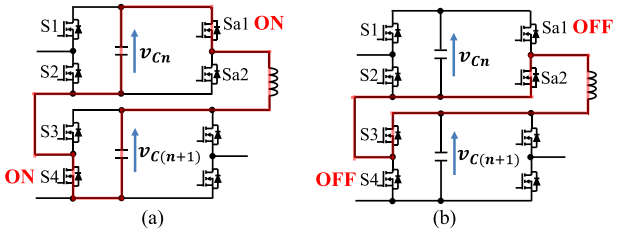

FIGURE 5. Operation states of each auxiliary circuit. (a) Balancing operation. (b) Circulation operation.

As shown in Fig. 5, the auxiliary circuit always operates in synchronization with the chopper cell and performs a voltage balancing operation by circulating current between the adjoining two cells. When switches Sa1 and S4 are in the on-state, as shown in Fig. 5(a), both cell capacitors are connected in parallel through an auxiliary inductor connected in series. At this time, the circulating current for charging and discharging flows through both capacitors, and the voltage of each capacitor automatically becomes the average of the sum of their voltages. In the operating state shown in Fig. 5(b), when switch S4 is in the off-state, switch Sa1 must also be in the off-state to prevent short circuit. Thus, this auxiliary inductor circuit realizes fast voltage balancing of all cell capacitors at each switching cycle. In this regard, the resonant operations are not actively used in this auxiliary circuit. Furthermore, the operation of the auxiliary circuit does not affect the operation of the main circuit. As a result, the buffer inductor inductance can be reduced, and a faster output response can be achieved compared with general MMC circuits.

B. POSITIONING OF THE PROPOSED TOPOLOGY AMONG RELATED TOPOLOGIES

The assumed application of the proposed MMC-based converter is not infrastructure, but a power supply with a dc voltage of 500 to 1500 V for battery tests in the product design phase. In this application, the performance of the high-speed response, high accuracy, and low ripple is more important than cost and efficiency. Redundancy design is not necessary, unlike infrastructure applications. Even if it breaks down, there is no problem if it is stopped safely by using a fuse etc.

Compared with the general dc-ac and ac-dc MMCs in applications, such as HVDC and SST [6], [11], the proposed converter in this work is better for achieving high-speed output response using higher switching frequency and faster cell voltage control at a relatively lower voltage and smaller power capacity as the dc-dc converter for battery testing. Various MMC-based dc-dc converters have also been reported thus far [12]–[21]; however, most of the converters use ac circulating current with the output fundamental frequency inside the circuit to realize the cell voltage balance, which causes slower voltage control and slower output response. In [14], a model predictive control was introduced to an MMC-based dc-dc converter. However, the output response was discussed in units of several [s] orders owing to the relatively higher capacity for HVDC applications. This output response may be good for large-capacity and high-voltage applications; however, it does not seem to be sufficient for battery testing. In [21], the output response time of an MMC-based dc-dc converter has been discussed in the order of several [ms] for several hundred volts. This is also insufficient for the high-speed response of the power supply for battery testing.

Compared with the general 2-level converters in this application, the proposed converter has the advantages of faster response, lower ripple, and applicability of power devices with lower rated voltage and better characteristics. Furthermore, compared to multilevel converter topologies, such as diode-clamped converters that cannot achieve the self-voltage balance of the capacitors, the proposed converter has the advantage that the self-voltage balance can be achieved by only additional circuits with small inductors. An active neutral clamped converter with one MHz switching for battery charger applications was reported in [22]. The objective for the realization of the high-speed response is similar to that in this study; however, a discussion of the response speed was limited in this literature.

C. CONTROL METHOD

Fig. 6 shows the block diagrams of the control, including the cell capacitor voltage control and the overall duty calculation for the proposed converter. The overall duty ratio d_{larm} of the lower arm can be expressed as

$$d_{larm} = \frac{v_o}{E}\left\{K_p\left(v_o^* - v_o\right) + K_i\int\left(v_o^* - v_o\right)dt\right\} \tag{1}$$

Here, v_o^* is the command for the output voltage. The overall duty ratio d_{uarm} of the upper arm is given by

$$d_{uarm} = N - d_{larm} \tag{2}$$

In (2), N is the number of cells in each arm. The duty ratio d_u of the upper arm cell and that d_l of the lower arm cell are obtained using (3) and (4), respectively.

$$d_u = \frac{d_{uarm}}{N} \tag{3}$$

$$d_l = \frac{d_{larm}}{N} \tag{4}$$

The voltage-balancing control assists the individual capacitor voltage v_{cj} to follow its command v_c^*, as shown in Fig. 6. The duty ratio commands d_{cju}^* and d_{cjl}^* obtained by the voltage-balancing control for the upper and lower arms, respectively, are given as follows:

$$d_{cju}^* = K_{pc}\left(v_c^* - \frac{v_{c1} + v_{c2} + \cdots + v_{cN}}{N}\right) \tag{5}$$

$$d_{cjl}^* = K_{pc}\left(v_c^* - \frac{v_{cN+1} + v_{N+2} + \cdots + v_{c2N}}{N}\right) \tag{6}$$

Finally, the duty ratio commands d_{ju}^* and d_{jl}^* of the upper and lower arms, respectively, are expressed by the following

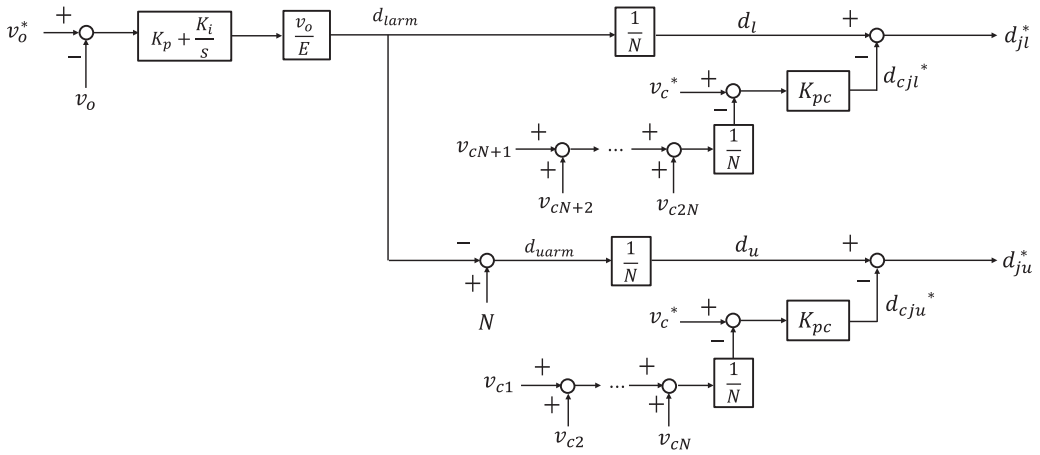

FIGURE 6. Block diagram of modular multi-level dc-dc converter control.

TABLE I Simulation and Experimental Condition

DC supply voltage	E	500 V
Load resistance	R_{load}	50 Ω
Load current	i_o	0 ~ 10 A
Buffer inductance	L_u, L_l	154 μH
Auxiliary inductance	$L_{a1} - L_{a5}$	3.3 μH, 3.3 μH, 300 μH, 3.3 μH, 3.3 μH
DC capacitance	$C_1 - C_6$	4.7 mF
Filter inductance	L_f	1.2 mH
Filter capacitance	C_f	3.9 μF
Carrier frequency	f_C	20 kHz
Proportional gain	K_p, K_{pc}	0.015, 0.02
Integral gain	K_i	3

equations:

$$d_{ju}^* = d_u - d_{cju}^* \tag{7}$$

$$d_{jl}^* = d_l - d_{cjl}^* \tag{8}$$

The duty ratio commands were compared with the phase-shifted carriers, and PWM signals for each switch were generated.

IV. SIMULATION INVESTIGATION

A. SIMULATION CONDITION

The operation of the proposed converter was validated through a simulation. The proposed circuit configuration with 6-cells shown in Fig. 4, was dealt with using the simulation software PSIM. Table I lists the simulation condition. The dc input voltage E and voltage reference v_c^* of each cell capacitor are 500 V and 166.7 V, respectively.

B. SELECTION CRITERIA OF AUXILIARY INDUCTORS

In the proposed circuit, the inductance of each auxiliary circuit is relatively small. This is because the applied voltage of each auxiliary inductor becomes the difference in the voltages between the capacitors of the adjacent cells, and this voltage difference is small in a balanced condition. In addition, because the auxiliary circuits operate synchronously with the chopper cells, the ripple frequency of the circulating current is relatively high, which is the same as that of the PWM carrier frequency. The current ripple of the auxiliary inductor L_{an} (n=1, 2, …, 2N-1) can theoretically be calculated as follows:

$$\Delta i_{Lan} = \frac{\{V_{Cn} - V_{C(n+1)}\}\{1 - d_{(n+1)}\}}{f_c L_{an}} \tag{9}$$

The current ripple Δi_{Lan} reaches the maximum value when the duty ratio $d_{(n+1)}$ of each cell is 0. Therefore, the maximum current ripple of the auxiliary inductor is derived as (10).

$$\Delta i_{Lan\_max} = \frac{V_{Cn} - V_{C(n+1)}}{f_c L_{an}} \tag{10}$$

From (10), the required inductance of L_{an} to satisfy the maximum current ripple Δi_{Lan_max} can be obtained as follows:

$$L_{an} = \frac{V_{Cn} - V_{C(n+1)}}{f_c\ \Delta i_{Lan\_max}} \tag{11}$$

In this simulation, the inductance is selected to be 3.3 μH for the maximum current ripple of 7.6 A under the voltage difference of 0.5 V between the capacitors in the simulation condition listed in Table I.

However, among the auxiliary inductors, only the inductance of L_{aN}, which is connected between the upper and lower arms shown in Fig. 2(L_{a3} in the 6-cells case.) cannot be applied with significantly small inductance. This is because L_{a3} is applied by a voltage equal to the total voltage of the two series buffer inductors, as shown in Fig. 7. To suppress the circulating current ripple, L_{a3} requires an inductance that is twice that of buffer inductors L_u and L_l. The current ripple of L_{aN} can be calculated using (12).

$$\Delta i_{LaN} = \frac{2E d_{(N+1)}\{1 - d_{(N+1)}\}}{N^2 f_c L_{aN}} \tag{12}$$

The maximum current ripple at a duty ratio of 0.5 and the required inductance L_{aN} can be derived from (13) and (14),

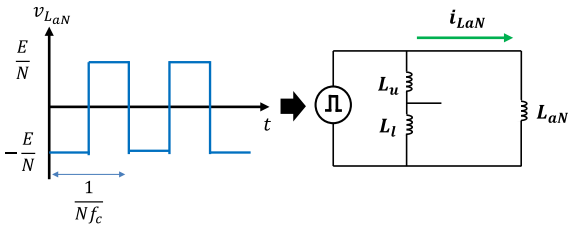

FIGURE 7. Equivalent circuit for circulating current through L_{aN} in auxiliary circuit.

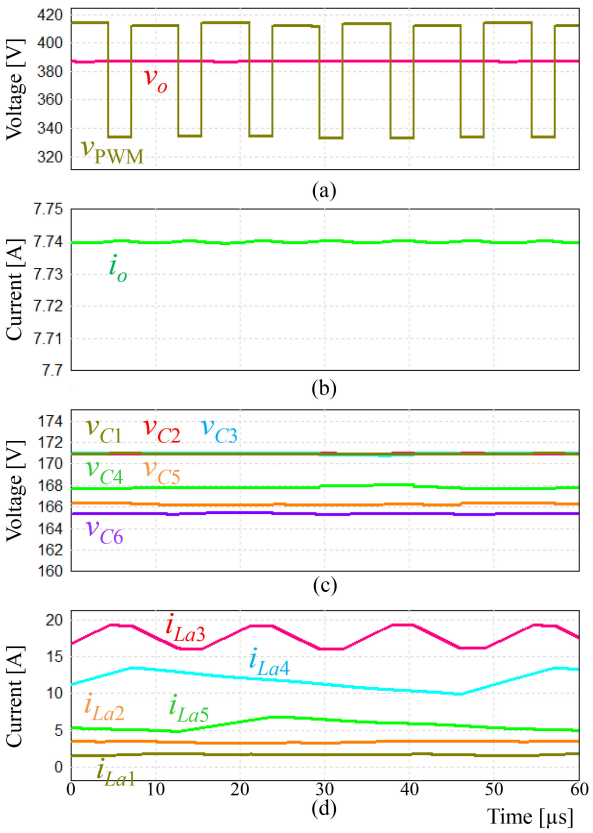

FIGURE 8. Simulation waveforms of steady state operation. (a) Output voltage v_0 and PWM voltage v_{PWM}. (b) Output current i_0. (c) Voltages of each capacitor C_1 to C_6. (d) Currents i_{La1} to i_{La5} of auxiliary inductors.

respectively.

$$\Delta i_{LaN\_max} = \frac{E}{2N^2 f_c L_{aN}} \tag{13}$$

$$L_{aN} = \frac{E}{2N^2 f_c \ \Delta i_{LaN\_max}} \tag{14}$$

In this simulation, L_{a3} of 300 μH was selected for a maximum current ripple of 4.6 A.

C. SIMULATION RESULT

Fig. 8 shows the steady-state simulation results when the output voltage v_o is 387 V and the output power is 3 kW. The output PWM voltage v_{PWM} was confirmed to have sufficient multilevel voltages of approximately $5E/6 = 417$ V and $4E/6 = 333$ V as the 7-level operation. The capacitor voltages of each cell were stable; however, there were slight differences for the normal voltage of 166 V. The capacitor voltages in the upper arm tend to be higher than the normal voltage, and those in the lower arm become lower than the capacitor voltages in the upper arm. The capacitor voltage errors between the theoretical and measured voltages appear to originate from the voltage drop in the auxiliary inductors and MOSFETs. Cell voltage control that uses only P control instead of PI control is also one of the reasons for the voltage errors. These voltage errors did not have a large effect on the total output voltage, and an adequate output voltage of 387 V could be obtained.

For the operation of the auxiliary circuits, the currents flow through the auxiliary inductors to achieve voltage balance of the cell capacitors, as shown in Fig. 8(d). The current through L_{a3} becomes the largest and have the ripple with the frequency of $Nf_c = 60$ kHz and peak-to-peak value of 3.24 A. From the simulation result in this condition, the duty ratio d_4 becomes 0.778 for the operation of L_3. The theoretical ripple current of i_{L3} can be calculated as 3.20 A using (12).

Excepting i_{La3}, it is seen that the current i_{La4} becomes the largest and have the ripple of 3.62 A. From the simulation result, the voltage difference between C_4 and C_5 is 1.09 V and the duty ratio d_5 becomes 0.777 for the operation of L_4. By using (9), the current ripple of L_4 is calculated as 3.68 A. Thus, the validity of the theoretical equations from (9) to (12) has been confirmed and each auxiliary inductor can be designed considering the current ripple. From the simulation results, the operation of the proposed dc–dc converter with cell voltage balance using auxiliary circuits was validated.

In the proposed topology, because an auxiliary circuit exists through which a large current flow exists, the loss in the auxiliary circuits cannot be ignored. However, because the auxiliary inductor is comparatively small, the power device losses are usually dominant. There is a trade-off relationship between obtaining a high-speed response and reducing the number of such components for a suitable selection of a converter topology. The proposed circuit topology is a promising candidate, particularly for applications that require high-speed response, such as power supply for battery testing. However, this circuit topology may not be selected for applications where fast response is not required and cost is a priority.

V. EXPERIMENTAL VALIDATION

A. EXPERIMENTAL CONDITION

Fig. 9 shows the configuration of the experimental setup using a prototype of the proposed MMC-based dc-dc converter with 6-cells. Each cell with a chopper cell and auxiliary inductor circuit is arranged in each section of the rack. Fig. 10 shows a photograph of each cell. The cell board consists of SiC-MOSFETs, gate drivers, isolated power supply, signal conversion circuits from optical fiber signals, current sensors, etc. SiC-MOSFETs (SCT3022ALGC11) are used in both the chopper-cell and auxiliary circuits. A control system was configured using DSP and FPGA on a digital control system

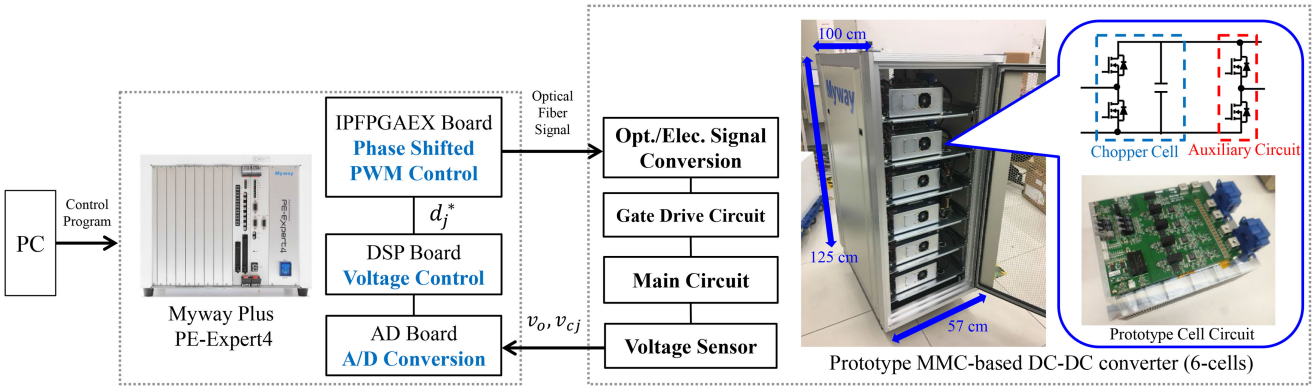

FIGURE 9. Experimental setup.

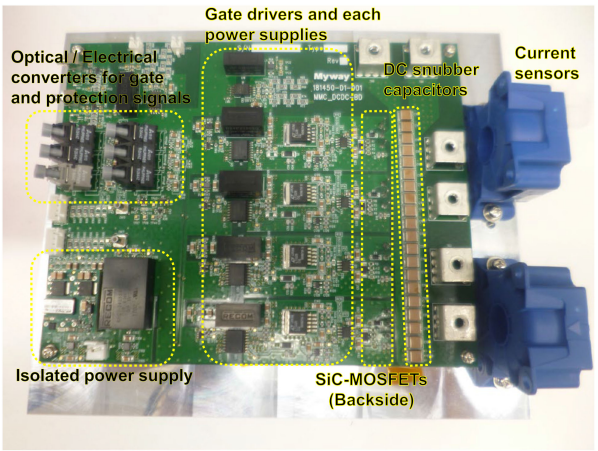

FIGURE 10. Experimental setup of each cell circuit.

PE-Expert IV manufactured by Myway Plus Corporation, as shown in the left part of Fig. 9.

The experimental conditions for validation were the same as the simulation conditions listed in Table I. As discussed above, the inductance of the auxiliary inductors can be small. The output filter of the whole converter is designed to satisfy a requirement of the current ripple of 0.01 A [23]. The individual carrier frequency of each cell was set to 20 kHz. This implies that the equivalent output PWM frequency using the carrier phase-shifted modulation becomes 120 kHz using the 6-cells. The switching frequency affects the output response speed because it determines the time constant of the output filter.

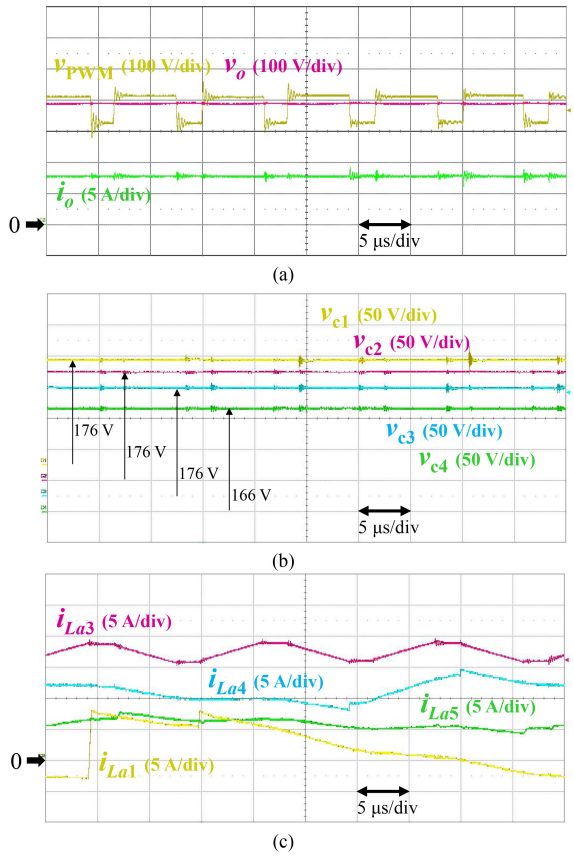

FIGURE 11. Experimental waveforms on steady state operation (387 V, 3 kW). (a)Output voltage v_o, PWM voltage v_{PWM} and output current i_o. (b)Voltage of each cell capacitor v_{c1} to v_{c4}. (c) Currents i_{La1} to i_{La5} of auxiliary inductors.

B. STEADY STATE OPERATION

Fig. 11 shows the experimental result in the steady-state operation with an output voltage of 387 V and an output power of 3 kW. Fig. 11(a) shows the output voltage v_o, the output PWM voltage v_{PWM}, and the output current i_o. It is confirmed that the v_{PWM} repeats $5E/6 = 417$ V and $4E/6 = 333$ V adequately as the 7-level operation. The voltages had a small error for the normal values of the capacitor voltages, similar to the simulation result. It is observed that slight ringing in the voltage v_{PWM} occurs owing to the stray inductance and capacitance. Although this ringing does not have a significant effect on the output response of the converter, it should be considered in the circuit design to prevent unintentional overvoltage in power devices. Such a practical design procedure is discussed in detail in section VI.

Fig. 11(b) shows the capacitor voltage for each cell. The theoretical regulated value of each capacitor voltage is $E/3 =$

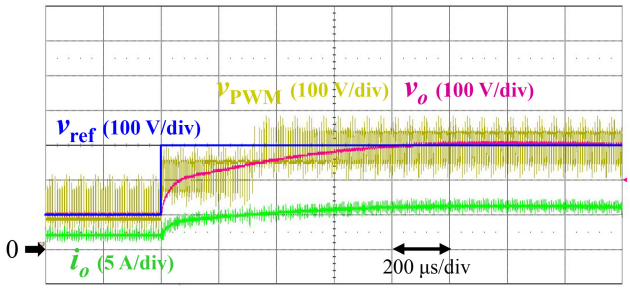

FIGURE 12. Experimental result of step response on the output voltage from 100 V to 300 V.

166 V. From these results, the capacitor voltages are 176 V in the cells of the upper arm and 166 V in the cells of the lower arm. The reason for the small error between the theoretical and measured voltages is the same as that in the simulation discussed in section IV-C. However, the capacitor voltage error is small enough for the entire converter operation, and an output voltage v_o of 387 V is suitably obtained through the output filter, as shown in Fig. 11(a). In an actual battery test power supply, there is another circuit before the proposed MMC-based converter, as shown in Fig. 1. The initial voltages depend on the circuit operation, and it is considered that a significant initial imbalance does not occur if the circuit in the previous stage operates normally. In the experiment in this study, each capacitor voltage could be controlled to a balanced condition from 0 V in the initial startup condition without an external initial charging circuit.

Fig. 11(c) shows the waveforms of the auxiliary inductor currents. It can be observed that these waveforms are in good agreement with the simulation waveforms shown in Fig. 8 and satisfied the designed maximum ripples. Only i_{La1} shows a small difference in the simulation result, and it becomes larger owing to a larger error in the capacitor voltages and parasitic parameters in the experimental circuit. However, it can be confirmed that this difference does not have a large effect for the overall operation. In this way, it is verified that voltage balancing control is achieved in the proposed MMC based dc-dc converter. The efficiency at an output power of 3 kW was measured as 95.8% in the prototype circuit, including the output filter.

C. PERFORMANCE OF OUTPUT RESPONSE

Fig. 12 shows the experimental waveform in a step change of the output voltage from 100 V (200 W) to 300 V (1.8 kW). It can be observed that the response time becomes approximately 0.80 ms (0.25 kV/ms) for 90% of the target voltage value and it is significantly faster compared with the reported studies of the MMC-based dc-dc converters using the isolation transformer this far. For example, in [21], the response time was discussed in units of several [ms] order on a step response of several hundred volts. However, the conventional MMC-based dc-dc converter with an isolation transformer cannot minimize the time constant of the output and cannot realize

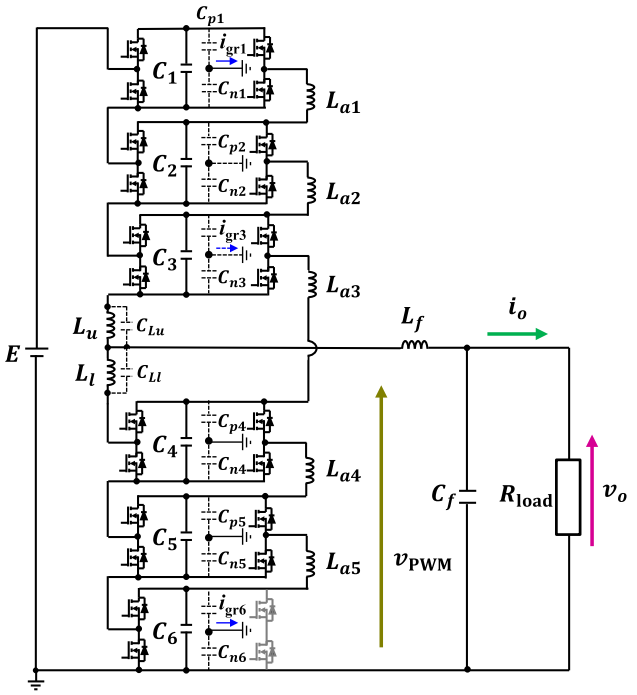

FIGURE 13. Detailed circuit schematic of the proposed MMC-based dc-dc converter with 6-cells considering critical parasitic capacitances.

such a fast output response. This implies that the result of this study improves by more than ten times compared with the above literature by realizing a smaller equivalent inductance for the output. Thus, it is verified that the proposed MMC-based dc-dc converter, as shown in Fig. 4, and its control method are suitable for high-voltage and high-speed responses, assuming power supplies for battery testing.

In this regard, in the case of the battery load, a voltage dip does not occur, and the evaluation of the load voltage change is not needed in such applications, unlike dc-dc converters for general loads.

VI. DISCUSSION OF CIRCUIT IMPLEMENTATION CONSIDERING NOISE REDUCTION

Generally, the mutual effect between high-speed switching and parasitic parameters in the circuit causes ringing and noise in power converters. Fig. 13 shows a practical circuit model of the proposed MMC-based dc-dc converter considering parasitic capacitances. In all MMC-based converters, the cell voltage is sufficiently low, and the normal mode noise becomes sufficiently low. However, the common-mode voltage between each cell and the ground potential cannot be reduced, even by increasing the number of cells. Thus, even MMC circuits with lower divided multilevel voltages and lower normal mode noise must be considered for common-mode noise reduction to handle a high input voltage for the entire circuit. Based on the experimental waveforms, a noise-prevention procedure for MMC-based converters is discussed in this section. It was clarified that the parasitic parameters

negatively affect the ringing and noise of the output voltage by the following matters.

A. PARASITIC CAPACITANCES FOR THE GROUND POTENTIAL OF EACH CELL

The most critical reason for ringing and noise are parasitic capacitances, such as $C_{\rm px}$ and $C_{\rm nx}$ in Fig. 13 for the ground potential of each cell. As discussed above, the voltage between the top cell and ground potential is the highest and is the same as the input dc voltage. Noise problems occur because of the interaction between the common-mode voltage and the stray capacitances, even in the case of a sufficiently low voltage in each cell without a suitable countermeasure. From the experimental results in the previous section, it was observed that a small ringing in the output PWM voltage occurs, as shown in Fig. 11(a). The measured values of the stray capacitances were $C_{\rm p1} = 1.38$ nF and $C_{\rm n1} = 1.39$ nF in the prototype converter, and it is considered that they affected the ringing. Here, the frame ground cables for the heatsinks of each cell were removed to reduce stray capacitances and common-mode noises. Although the switching speed of the power devices should be adjusted and lowered to reduce the ringing, the effect of each stray capacitance on the noise was studied here. Fig. 14 shows the measured waveforms of the leakage currents under the three conditions. When the frame ground cable of only cell 1 was connected, the ringing voltage became slightly higher compared with the non-grounded condition shown in Fig. 11, and some large current ringing occurred, as shown in Fig. 14(a). Second, when only cells 1 and 6 are grounded, the ringing of the output voltage further increases, and the ringing current flows through the ground cables, as shown in Fig. 14(b). Third, when cells 1, 3, and 6 were grounded, no significant change was observed from the above condition, as shown in Figs. 14(b) and (c). From the results, the ringing current flows through the ground cables and circulates through several cells. To reduce ringing, the parasitic capacitances of each cell to the ground potential should be reduced by a suitable implementation considering the switching speed and heat dissipation of the power devices.

B. PARASITIC CAPACITANCES AT THE BUFFER INDUCTORS

The second reason for ringing is the parasitic capacitances, such as C_{Lu} and C_{Ll} between the buffer inductors. Fig. 15 shows the simulation waveforms under the various conditions listed in Table II. Fig. 15(a) and (b) show the simulation waveforms for conditions with and without parasitic capacitances. It can be observed that the parasitic capacitances of the buffer inductors negatively affect the ringing of the output voltage. When there is a difference in the parasitic capacitance, the output voltage, which is the neutral-point voltage of the buffer inductors, has high-frequency ringing owing to [pF] order parasitic capacitances. This point is difficult to solve entirely because accurate design and measurement of such small stray capacitances in an inductor are practically impossible.

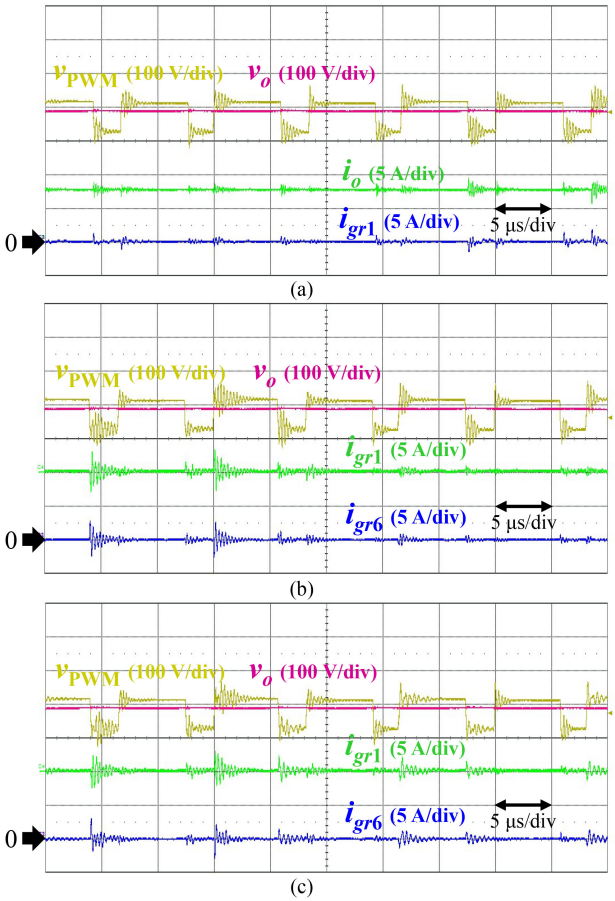

FIGURE 14. Experimental waveforms of output voltage v_o, PWM voltage v_{PWM}, leakage currents i_{gr1} and i_{gr6} in the ground lines of each cell to consider the effect of stray capacitances (387 V, 3 kW). (a) when only cell 1 is ground. (b) when only cells 1 and 6 are grounded. (c) when only cells 1, 3, and 6 are grounded.

C. UNBALANCE OF INDUCTANCE BETWEEN THE BUFFER INDUCTORS

The third reason for the ringing is based on an imbalance of inductance in both the buffer inductors, L_u and L_l. Fig. 15(c) shows the simulation results under the condition of 10% imbalanced buffer inductances with balanced parasitic capacitances. When there is an imbalance between buffer inductances, the voltage of each inductor becomes unbalanced, as shown in Fig. 15(c). When both the parasitic capacitances and inductances are unbalanced, the ringing of the output voltage deteriorates significantly, as shown in Fig. 15(d).

D. HIGH-SPEED SWITCHING CHARACTERISTICS

The high-speed switching capability of SiC-MOSFETs is an essential issue of ringing and noise. It triggers ringing with the stray capacitance of each cell, buffer inductors, and auxiliary inductors. Even if there is an imbalance in the parasitic capacitances and inductances, the ringing voltage will not increase if the switching speed is not high.

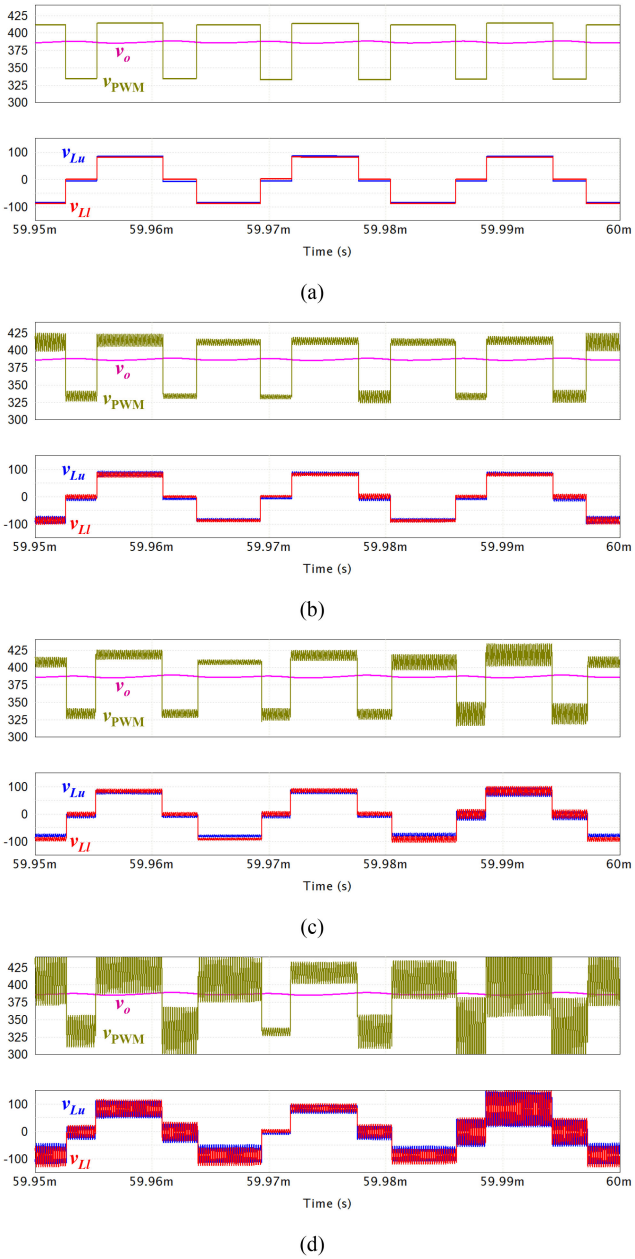

FIGURE 15. Simulation waveforms of output voltage and inductor voltages under the conditions of balanced and unbalanced parasitic capacitances and buffer inductances. (a)balanced condition without parasitic capacitance. (b)with parasitic capacitances. (c)unbalanced inductances with parasitic capacitances. (d)unbalanced parasitic capacitances and inductances.

In this way, it is clarified that the ringing in the output PWM voltage is caused by the mutual influence of the above three reasons. To prevent ringing, the parasitic capacitances of each cell should be reduced, and an imbalance between the parasitic capacitances and inductances in the buffer inductors should be designed to be sufficiently small. In the practical implementation of the proposed circuit, attention should be paid to the above design procedures to prevent noise problems.

TABLE II Simulation Conditions in Fig. 15

Parameter	(a) Balanced	(b) With stray capacitances	(c) Unbalanced inductances	(d) Both unbalanced
Inductance of upper buffer inductor L_u	154 μH	154 μH	139 μH	139 μH
Inductance of lower buffer inductor L_l	154 μH	154 μH	154 μH	154 μH
Parasitic capacitance of upper buffer inductor C_u	0	5 pF	5 pF	5 pF
Parasitic capacitance of lower buffer inductor C_l	0	5 pF	5 pF	8 pF

VII. CONCLUSION

In this study, first, the circuit operation of the general MMC is analyzed, and the issue of the unavailability of capacitor voltage balancing on dc-dc conversion is pointed out. As a solution, an MMC-based dc-dc converter with auxiliary inductor circuits has been proposed to realize capacitor voltage balancing and fast output response. The design procedure of the auxiliary inductors was theoretically clarified, and it was clarified that the inductances can be significantly smaller. The simulation and experimental results demonstrate the validity of the proposed dc-dc converter and control method. Finally, an implementation procedure is discussed to reduce ringing and noise in MMC-based converters with high-speed switching capability based on experimental waveforms. It has been confirmed that the proposed MMC-based dc-dc converter can output an arbitrary constant dc voltage with capacitor voltage balancing and achieve a fast output response.

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