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An Efficient Electro-Thermal Compact Model of SiC Power MOSFETs Including Third Quadrant Behavior

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ABSTRACT This paper presents an efficient physics-based electro-thermal model that solves some advanced problems of modeling Silicon Carbide (SiC) power MOSFETs. It is the first electro-thermal model that simulates the temperature dependency of the first and the third quadrant characteristics, including the reverse recovery of the body diode accurately and efficiently. It extends from a previous work that demonstrated the isothermal physics-based model of the gate-dependent body diode. Physics-based temperature scaling of the first and third quadrant allows simulation of the self-heating effect in a wide range of temperatures (27 °C–200 °C), even for the synchronous operation. Moreover, a physics-based modeling approach is taken to include gate-voltage dependent non-linearity of the gate to source capacitance (Cgs). Also, a physic-based segmented cascaded method is taken to accurately model the Miller (Crss), and the output (Coss) capacitances at the low and very high drain to source voltage regions. Further, the temperature-dependent breakdown mechanism is included for reliable system design. Double Pulse Tests (DPTs) at various temperatures up to 200 °C validate the model's accuracy. Lastly, a synchronous buck converter test demonstrates the model's ability to predict junction temperatures, validating the model's accuracy and efficiency in a continuous operation with self-heating.

INDEX TERMS Silicon Carbide, Power MOSFET, Body diode, Reverse recovery, Synchronous rectification, Freewheeling diode.

I. INTRODUCTION

The objective of compact modeling is to predict the behavior of the device as a function of the applied terminal biases (voltage, current, charge, etc.), environmental conditions (temperature, radiation, etc.), and physical parameters (channel length, doping, oxide thickness, etc.) [1]. According to [1], SPICE compatible compact models can be broadly categorized into three levels: Behavioral, Semi-physics based, and Physics-based. Though behavioral models are simple to develop and fast to simulate, these models cannot predict the variation of the device behavior due to variations of different physical parameters. For example, the channel length of power MOSFETs varies from device to device, even within the same wafer. As a result, there will be variations in threshold voltage, transconductance, on-resistance, etc. Empirical equations used in behavioral models cannot predict these variations in device behavior due to the lack of co-relation of their parameters to device physics.

On the contrary, the parameters of a physics-based model can be co-related to the variations in different physical parameters to get predictive statistical simulations [2]. However, traditional physics-based models often suffer from convergence issues and slow simulation speed [1]. So, there is a need to develop efficient physics-based compact models that can be used for statistical simulations as well as for simulations of large circuit topologies. This is more important for emerging technologies like Silicon Carbide power MOSFETs which suffer from variations in characteristics due to fabrication limitations.

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There has been much progress in the area of compact modeling of SiC power MOSFETs. References [1], [3], and [4] list the previous notable works done in this field. However, some challenging aspects are less addressed due to the complexity of their physics and slow computational speed when included in the model.

One such advanced issue is self-heating. Due to operations in the high voltage and high current range, SiC MOSFETs dissipate a significant amount of power in the form of heat. Though the thermal conductivity of SiC is almost double that of Si (3.7 vs. 1.5 $\mathrm{Wcm^{-1}\ K^{-1}}$), the compact size of SiC chips decreases heat dissipation. The thermal impedance of the package also limits heat dissipation. Hence, the junction temperature of the device rises with operation time. It is called self-heating. The device characteristics are heavily dependent on the junction temperature. Efficiency and Reliability both depend on the junction temperature of the device. So, the self-heating phenomenon needs to be modeled to accurately predict the overall system. Existing physics-based models like [5] and [6] include temperature dependencies of the model parameters. However, the models are not verified by experimental data at the self-heating condition. These models' linear formulations with no proper physics-based feedback mechanisms cause convergence issues in electro-thermal simulation. The paper in [7] presents an electro-thermal model that can predict the device behavior inside and outside the Safe Operating Area (SOA). However, it does not describe the third quadrant behavior. Without accurate third quadrant behavior, circuits performing synchronous operations will suffer from inaccuracy [4].

Another advanced issue of the compact modeling of SiC power MOSFETs is the accurate modeling of interelectrode capacitances. In reference [8], it was shown that the interelectrode capacitances are substantially more influential than the conduction branch in determining the dynamic behavior of the MOSFET model. This necessitates very accurate interelectrode capacitance modeling in the device's operating range. Reference [8] also presents an extensive literature study on the existing capacitance models of the power MOSFET. According to [8], current physics-based and semi-physical models lag in capacitance modeling compared to the Look-Up Table (LUT) based models. However, as described earlier, LUT-based models are behavioral and cannot predict device scaling. Similarly, reference [7] uses a purely empirical approach to model capacitance-voltage (CV) characteristics. Reference [9], a model developed by STMicroelectronics, uses LUT based approach to model CV characteristics. Reference [10] presents a physics-based model for miller capacitance (Cgd). Nevertheless, it does not provide the gate voltage dependency of the gate to source capacitance (Cgs). Recently published [11] addresses the non-linearity of interelectrode capacitances more extensively, albeit using a behavioral approach.

While switching loss plays the most significant role in determining the system's efficiency, it is necessary to have breakdown characteristics to design reliable systems, especially with the high dv/dt of wide bandgap devices, which gives a significant voltage overshoot. Moreover, the breakdown voltage changes with junction temperature. So, the inclusion of temperature-dependent breakdown characteristics for electro-thermal modeling allows reliable system designs. Most of the existing models avoid including breakdown characteristics due to convergence issues. The paper in [12] presents an electro-thermal model with self-heating and body diode characteristics. However, the breakdown mechanism is not included in that model. Also, extraction of the model's parameter set requires information related to the device's physical characteristics. For circuit designers, this information is difficult to access. Moreover, the gate dependency of the body diode is not explicitly described. The paper in [13] presents a Fourier series based electro-thermal model of the body diode. The model also includes a latch-up induced breakdown mechanism, but this body diode robustness model is not embedded in a complete power MOSFET model. Reference [14] describes an electro-thermal model and validates the static characteristics at different temperatures. Nevertheless, the switching characteristics are not validated. Moreover, there is no mention of third-quadrant characteristics in the paper. Reference [15] accurately models the non-linear miller capacitance (Crss). The model has excellent convergence properties despite having temperature dependencies of different parameters. But the model of [15] is a behavioral model. Also, the body diode of that model has no gate-voltage dependency. The model also has constant Cgs characteristics. Temperature dependencies of the switching losses are quite accurately addressed by behavioral models of [16] and [17]. But behavioral nature of these models always raises the question of their predictability with device scaling.

This work is an extension of the prior model presented in [4], in which an isothermal model of SiC power MOSFETs was presented. The model of [4] shows the gate-dependent third quadrant behavior, including the reverse recovery of the body diode. The model accurately predicts the first and third quadrant behavior of the SiC power MOSFET without compromising the simulation efficiency. It was validated that the presented model of [4] improves the accuracy and simulation speed significantly compared to the vendor-provided behavioral model, despite being physics-based. Moreover, a unique smoothing technique was introduced, allowing the inclusion of computationally expensive equations (example: reverse recovery of body diode) without causing convergence problems. Hence extension of the model of [4] addressing the advanced issues of compact modeling of SiC power MOSFETs is a logical progression.

In this paper, the interelectrode capacitance-voltage (CV) characteristics have been modified from [4]. The physics-based modification aims to include the gate-bias dependency in the gate to source capacitance (Cgs), and increase the Miller capacitance's (Cgd) accuracy, especially in the low voltage region and in the very high voltage region. Moreover, the leakage current-induced avalanche breakdown characteristics have been included. Lastly, physics-based temperature dependencies have been established for the first and the third

quadrant characteristics, including the body diode. As a result, stable and accurate electro-thermal simulation, including self-heating, can be performed with the developed model. The model's accuracy in predicting the switching characteristics has been proven by Double Pulse Tests (DPTs) at different ambient temperatures up to 200 °C. Finally, a synchronous buck converter continuous test was performed to validate the model's overall accuracy and simulation efficiency in a self-heating included electro-thermal environment. The key contributions of this paper can be listed as:

1) Inclusion of gate bias dependent gate to source capacitance (Cgs)
2) Accurate miller capacitance (Crss) modeling at very low and high voltage region
3) Inclusion of the temperature dependency in the first and third quadrant behavior with the body diode's reverse recovery
4) Inclusion of the leakage induced temperature-dependent breakdown characteristics
5) Verification of the model's temperature scaling in predicting switching loss by Double Pulse Tests at different temperatures
6) Validation of the electro-thermal model's accuracy and simulation efficiency by a synchronous buck converter continuous test

The paper is organized as follows: Section II presents the description of the interelectrode capacitance modeling. This section also validates the capacitance model by overlaying simulation results on measured data. A parameter extraction process for the updated CV model is also included in the section. Section III describes the breakdown modeling, its validation, and extraction guidelines for the breakdown related parameters. Section IV models the temperature dependencies of the first and third quadrant characteristics. This section also describes how different parameters of the isothermal model [4] vary with temperature and the device physics behind these trends. Section V verifies the model's accuracy in predicting the switching characteristics at different temperatures by double pulse tests (DPT). Section VI describes the synchronous buck converter continuous test, which validates the model's overall accuracy and efficiency. Section VII concludes the paper.

This work's measured data is from a commercial SiC power MOSFET (C2M0045170D). From this point on, the model parameters are differentiated from the text by using bold *italic* (example: ***Cox***). The simple *italic* font has been used for the other terms in the model equations. Two types of subscripts are used in the model equations. Subscript $x = l$ or h stands for the low and high gate voltage regions, respectively. Subscript $y = f$ or r stands for the forward (first quadrant operation) and reverse (third quadrant operation) conduction. Details about these regions of operation are described in [4].

II. CV MODEL DEVELOPMENT

In reference [4], the gate to source capacitance (Cgs) was modeled with a constant value. This approach is followed in most compact models due to the negligible variation of Cgs with the drain to source voltage (Vds). This is the only way to model input capacitance in the datasheet-based modeling approach [6] because most datasheets only provide the variation of interelectrode capacitances with Vds. However, as shown in Fig. 1, the measured data has a significant variation of Cgs with the gate voltage (Vgs). This variation in Cgs is important since a significant gate voltage sweep is applied from turn-off to turn-on. To the best of the authors' knowledge, there is no physics-based model of SiC power MOSFETs that includes gate-dependent input capacitance characteristics.

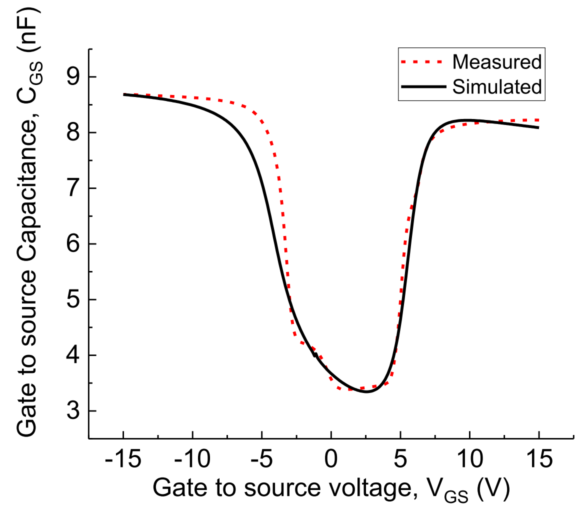


FIGURE 1. Gate to source capacitance (***Cgs***) vs Gate to source voltage (***Vgs***). The nonlinear dependency of ***Cgs*** on ***Vgs***. Modified model can accurately capture the nonlinear behavior of the measured result.

Cgs depends on the charge distribution in the channel region. There are three states of charge distribution in the channel region depending on the Vgs. At negative Vgs, the p-doped channel region shows accumulation of positive charges. As a result, Cgs is equal to the intrinsic oxide capacitance (***Cox***). As Vgs shifts from a negative value to a more positive value, the channel region enters the depletion state. The depletion layer forms below the gate oxide, which acts as an insulator. This depletion layer grows thicker with the increasing positive voltage, and the Cgs decreases. However, at the onset of inversion, the inversion charges at the surface again make Cgs ≈ ***Cox.***

Cgs is modeled at the accumulation state using the equations (1)–(3). Here, ***Vacc*** is a model parameter standing for the transition point voltage between the accumulation and depletion state. ***Cgsacc***depicts the constant capacitance at the accumulation state. Qgs_{acc} stands for the total charge in the accumulation state.

$$Vgs_{acc} = \frac{1}{2}\left[Vgs + \boldsymbol{Vacc} + \sqrt{(Vgs + \boldsymbol{Vacc})^2 + 4\partial^2}\right] \tag{1}$$

$$Vgs_{acceff} = Vgs + \boldsymbol{Vacc} - Vgs_{acc} \tag{2}$$

$$Qgs_{acc} = \boldsymbol{Cgsacc} \cdot Vgs_{acceff} \tag{3}$$

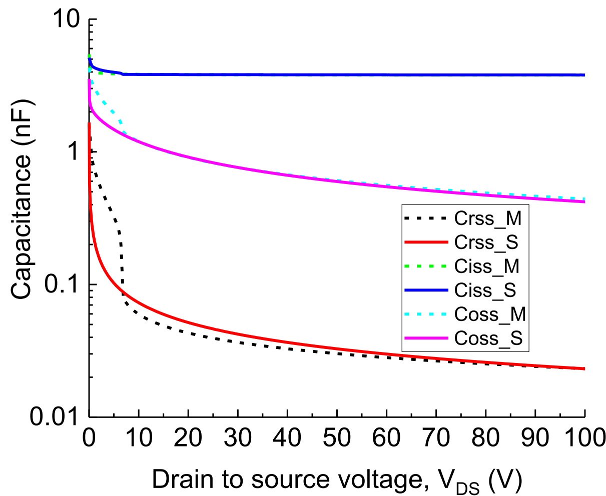


FIGURE 2. Simulated CV characteristics of the model [4] and its significant mismatch with the measured results at low *Vds* region.

$$Vgs_{dep} = \frac{1}{2}\left[V_{gs} - \boldsymbol{Vth_{lf}} + \sqrt{\left(V_{gs} - \boldsymbol{Vtd}\right)^2 + 4\partial^2}\right] \quad (4)$$

$$Vgs_{depeff} = Vgs - Vgs_{dep} + \frac{\boldsymbol{Gp}}{2} \quad (5)$$

$$Qgs_{dep} = \boldsymbol{Cgsinv} \cdot Vgs_{depeff} \quad (6)$$

The gradual drop of the Cgs in the depletion state is modeled by the equations (4)–(6). This drop continues until the inversion of the channel charge occurs at the threshold voltage. The threshold voltage is denoted by the parameter $\boldsymbol{Vth_{lf}}$. $\boldsymbol{Vthl_f}$ is extracted from the static output characteristics as described in [4]. $\boldsymbol{Cgsinv}$ is a parameter equal to the nearly constant capacitance at the inversion state. $\boldsymbol{Gp}$ is a model parameter that determines the slope of the Cgs drop. Qgs_{dep} is the total gate charge in the depletion and inversion states. Equations (1), (2), (4), and (5) are used for making a continuous expression of the driving voltage at different states instead of using any conditional statements. Vgs_{acceff} and Vgs_{depeff} are effective gate voltages at the accumulation and depletion+inversion states, respectively. Vgs_{acc} and Vgs_{dep} are intermediary terms. ∂ is the smoothing parameter. The total channel charge (Qgs) that leads to the Cgs is expressed as:

$$Qgs = Qgs_{dep} + Qgs_{acc} \quad (7)$$

The Miller capacitance (Crss) is a depletion capacitance caused by the gate electrode's overlap on the drain region. Since the capacitance is between the device's input and output terminals, it plays a negative feedback role in slowing down the transition of Vgs [10]. In [10], it was shown that the traditional SPICE models have about 50% error in predicting the Miller capacitance at the low drain voltage region. Fig. 2 shows the simulated CV characteristics of the model of [4]. It has a maximum error of 72% and an overall RMS error of 21% with the measured results. The reason behind this mismatch is the approximation that there is only one continuous depletion region. For more accurate modeling of the miller capacitance, [10] adopted a concept called segmented-cascaded depletion regions. In this paper, the concept is implemented in a different method. Cdg is formed with a series combination of oxide capacitance, and drift region depletion capacitors. The oxide capacitance ($\boldsymbol{Cox}$) is a fixed component, and the depletion capacitance varies with the Vdg bias.

The JFET and following drift region have multiple doping concentrations and thicknesses in advanced SiC MOSFET device structures [18], [19]. Current spreading layer (CSL), for example. So, there may exist multiple layers of depletion regions. Each depletion region sees the previous depletion region as a fixed capacitor and varies with the applied Vdg. Hence the model requires multiple depletion capacitances with their own doping concentrations and overlap areas to capture the total Cgd accurately. Information on these regions is rarely available to circuit designers. So, instead of multiple doping concentrations and overlap areas, the effect can be modeled with different initial capacitances ($\boldsymbol{Cox_i}$). If the device structure information is available, $\boldsymbol{Cox_i}$ can be correlated to those physical parameters.

The miller capacitance, Cgd is expressed with the equations (8)–(15):

$$\sum_{i=0}^{k} Qgd_i = Qgd_{ni} + Qgd_{pi} \quad (8)$$

$$Qgd_{ni} = Vdgeff_{ni} \cdot Coxi \quad (9)$$

$$Qgd_{pi} = Vdgeff_{pi} \cdot Cgd_{ji} \quad (10)$$

$$C_{gd_{ji}} = \frac{\boldsymbol{Cox_i} \cdot Cgd_i}{\boldsymbol{Cox_i} + Cgd_i} \quad (11)$$

$$Cgd_i = \varepsilon_{sic} \cdot \frac{\boldsymbol{agd}}{wgd_i} \quad (12)$$

$$wgd_i = \sqrt{2 \cdot \varepsilon_{sic} \cdot \frac{Vdgeff_{pi}}{q \cdot \boldsymbol{nd}}} \quad (13)$$

$$Vdgeff_{pi} = \frac{1}{2}\left[Vdg - \boldsymbol{vtd_i} + \sqrt{(Vdg - \boldsymbol{vtd_i})^2 + 4\partial^2}\right] \quad (14)$$

$$Vdgeff_{ni} = Vdg - \boldsymbol{vtd_i} - Vdgeff_{pi} \quad (15)$$

For $\boldsymbol{i} = 0$, parameter $\boldsymbol{Cox}$ signifies the gate oxide capacitance. Cox_i depicts the previous stage's fixed minimum capacitance at the transition voltage parameter ($\boldsymbol{vtd_i}$) for the following cascaded structures. For DMOS structure, only two cascaded capacitors are enough to fit the measured Cgd characteristics accurately. Qgd_i depicts the charge associated with Miller capacitance at the $\boldsymbol{i}$ th cascaded capacitor. Physically, Qgd_{ni} and Qgd_{pi} represent charges associated with Cgd for voltages lower or higher than $\boldsymbol{vtd_i}$. $Vdgeff_{ni}$ and $Vdgeff_{pi}$ stand for effective Vgd at those respective regions. wgd_i stands for the depletion width associated with each cascaded structure.

With large enough applied Vdg, the depletion region reaches the N+ substrates. From there on, the depletion width does not change much before the breakdown. The Cdg takes a minimum value fixed by the parameter ***Cdgmin***. Here ***nd*** is the doping concentration of the drift region and ***agd*** is the overlap area between gate and drain. The presented model's simulated Crss shows less than 10% maximum error and less than 5% RMS error with the measured results.

The cascaded depletion regions also affect the drain to source capacitance (Cds) and, ultimately, output capacitance (Coss). Hence, instead of one depletion capacitance equation, the total Cds combines i number of depletion capacitances. Equations (16)–(21) express the modeling approach for Cds. Here Qds_i is the total charge related to the drain to the source junction. For each cascade component, Qds_{ni} and Qds_{pi} represent charges associated with the voltages lower or higher than $\boldsymbol{vtd_i}$. *Vbi* is the built-in voltage, and *Vbdiode* is the voltage across the drain to the source junction after the drop in the p-body resistance. ***nb*** is the body region doping concentration.

$$\sum_{i=0}^{k} Qds_i = Qds_{ni} + Qds_{pi} \tag{16}$$

$$Qds_{ni} = \boldsymbol{cds_i} \cdot Vbdiode\,eff_{ni} \tag{17}$$

$$Qds_p = \boldsymbol{cds_i} \cdot Vbi^m \cdot \frac{(Vbi + Vbdiode\,eff_{pi})^{1-\boldsymbol{m}} - Vbi^{\boldsymbol{m}}}{1-\boldsymbol{m}} \tag{18}$$

$$Vbi = \frac{kT}{e} \ln\left(\frac{\boldsymbol{nb} \cdot 10^{16}}{n_i^2}\right) \tag{19}$$

$$Vbdiode\,eff_{pi} = \frac{1}{2} \times \left[Vbdiode - \boldsymbol{vtd_i} + \sqrt{(Vbdiode - \boldsymbol{vtd_i})^2 + 4\partial^2}\right] \tag{20}$$

$$Vbdiode\,eff_{ni} = Vbdiode - \boldsymbol{vtd_i} - \frac{1}{2} \times \left[Vbdiode - \boldsymbol{vtd_i} + \sqrt{(Vbdiode - \boldsymbol{vtd_i})^2 + 4\partial^2}\right] \tag{21}$$

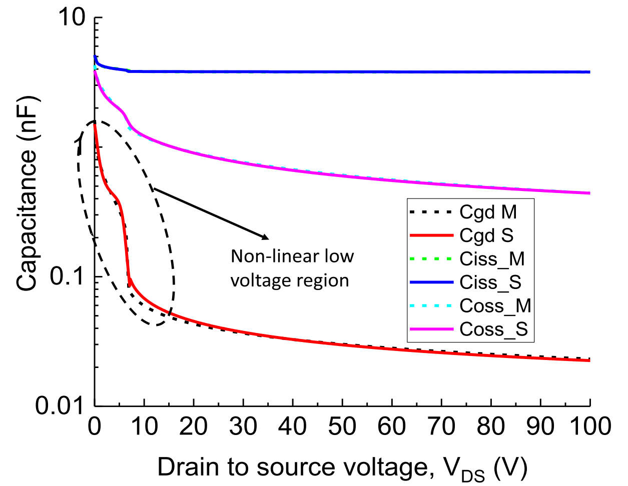


FIGURE 3. Comparison of the presented model's simulated CV characteristics with the measured results.

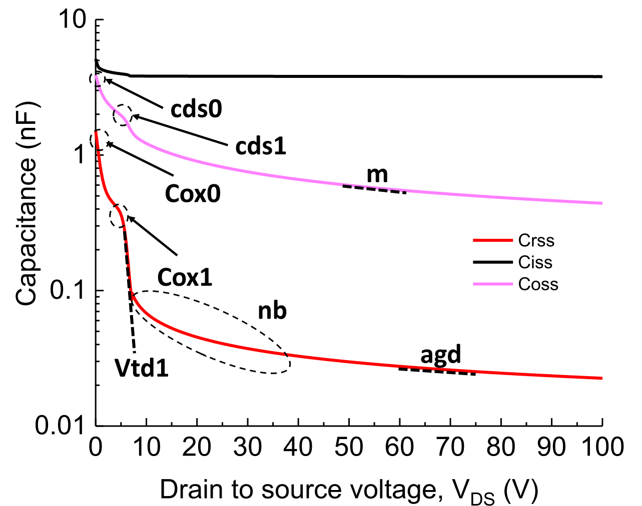


FIGURE 4. Drain voltage dependent capacitance parameters extraction procedure.

The simulated CV characteristics of the developed model overlaid on the measured results are shown in Fig. 3. The parameters related to CV characteristics are listed in Table 1. The parameters are extracted using the curve-fitting technique. Fig. 4 highlights the areas in the CV curve where the parameters' impact is maximum. So curve fitting of the simulation

$$I_{leakage} = \boldsymbol{I_{leakage0}} \cdot \sqrt{\frac{2\varepsilon_{sic}}{\boldsymbol{q}} \cdot \left(\frac{\boldsymbol{nb} + \boldsymbol{nd}}{\boldsymbol{nb} \cdot \boldsymbol{nd}}\right) \cdot abs\,(Vds)} \tag{22}$$

$$M = \begin{cases} \dfrac{1}{1-\left(\frac{Vds}{vbr}\right)^{\boldsymbol{bvn}}}, & Vds < (\boldsymbol{Fc_{BV}} \cdot vbr) \\ \dfrac{1}{\left(1-\boldsymbol{Fc_{BV}^{bvn}}\right)^2} \cdot \left[\left(\frac{Vds}{vbr}\right) \cdot \boldsymbol{Fc_{BV}^{bvn-1}} \cdot Vds + 1 - \boldsymbol{Fc_{BV}^{bvn}} \cdot (\boldsymbol{bvn}+1)\right], & Vds \geq (\boldsymbol{Fc_{BV}} \cdot vbr) \end{cases} \tag{23}$$

$$I_{mult} = (M-1) \cdot I_{mos} + M \cdot I_{leakage} \tag{24}$$

TABLE 1. Parameters for CV Modeling

Notation	Definition	Value	Unit
Cgsacc	Gate to source capacitance *at the accumulation state*	2.888E-09	F
Cgsinv	Gate to source capacitance *at the inversion state*	9.336E-09	F
Vacc	Accumulation state onset voltage	5.531	V
Gp	voltage gradient parameter	0.3623	V
vtd_0	First gate drain overlap depletion transition voltage	0	V
vtd_1	Second gate drain overlap depletion transition voltage	6.5	V
Cox_0	Gate oxide capacitance	1.543E-09	F
Cox_1	Initial constant capacitance at the onset of second depletion region	3.802E-10	F
Cgdmin	Constant capacitance at the high voltage region	5.703E-12	F
cds_0	First depletion capacitance between drain to source junction	5.88E-09	F
cds_1	Second depletion capacitance between drain to source junction	2.482E-10	F
m	Junction grading coefficient	0.7947	-
agd	Gate length overlap active area	0.0002272	cm^2
nd	Doping concentration of the drift region	7.44E+16	cm^{-3}
nb	Effective doping in the body region	1E+17	cm^{-3}
∂	Smoothing parameter	0.001	-

results with the measured data at a highlighted area will give the particular parameter value.

Extraction of the CV parameters begins with the Crss curve. Cox_0 is assigned equal to the value of Crss at $Vds = 0$ V. Cox_1 is tuned to match the first plateau region of the Crss curve at the low *Vds* region (usually < 20 V). vtd_0 is assigned to 0. vtd_1 is the second depletion voltage, and its value is extracted from the onset of the abrupt downward transition of the Crss curve. ***Cgdmin*** is extracted from the near-constant value of the Crss at the very high Vds region. The capacitance-voltage

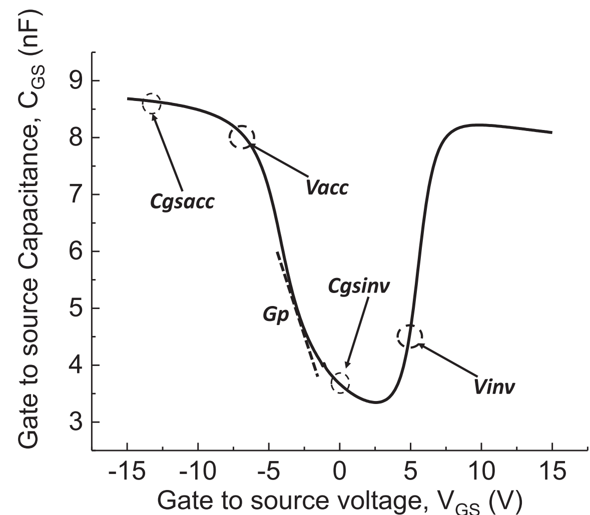


FIGURE 5. Gate voltage dependent *Cgs* related parameters extraction procedure.

characteristic described in this work is a modified version of [6], and [4]. Hence, there are some common parameters, namely: ***agd***, ***a***, ***nd***, ***nb,***and ***m***. The extraction process also remains the same as described in [6] for these parameters.

After the extraction of the Crss related parameters, the parameters related to Coss can be extracted. cds_0 is used to fine-tune the zero-voltage value of the Coss curve, and cds_1 is used to fine-tune the plateau region part of the Coss curve.

Once the Vds dependent parameters are extracted, *Vgs* dependent parameters can be extracted from Cgs vs. Vgs curve. Parameters ***Cgsacc*** and ***Cgsinv*** are extracted from the accumulation and inversion state of the curve. ***Vacc*** and *Vinv* parameters depict the onset of the accumulation and inversion, respectively. *Vinv* is equal to the threshold voltage and extracted from the output characteristics. Extra care needs to be taken to fit the value at Vgs = 0. This value also determines the initial value of the Ciss vs. Vds curve. Fine-tuning areas for different Vgs dependent parameters are shown in Fig. 5.

III. LEAKAGE CURRENT AND BREAKDOWN MODELING

The developed model includes the leakage current-induced breakdown characteristics instead of the mechanical damage induced breakdown. The leakage current is caused by three major reasons: thermal generation, diffusion, and avalanche multiplication [20]. But all these mechanisms are temperature-dependent and proportional to the square root of Vds. Instead of using different expressions for these leakage currents, a unified expression (22), shown at the bottom of the previous page, is used to include the leakage current characteristics in this model. Here, $I_{leakage0}$ is the leakage current at zero drain voltage. It depends on the device geometry, intrinsic carrier concentration, and effective carrier lifetime at the depletion region.

The breakdown is modeled with avalanche effect. At high electric field, the avalanche effect is expressed with (23), (24), shown at the bottom of the previous page. The concept of

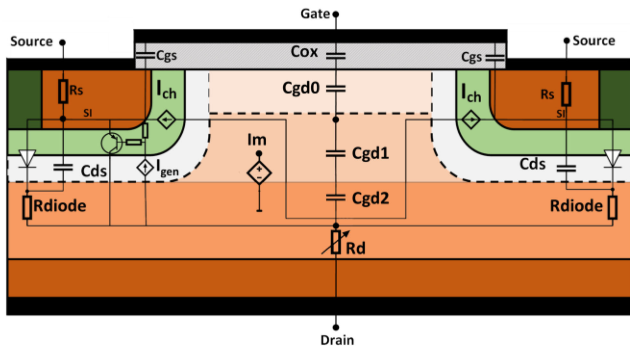


FIGURE 6. Subcircuit representation of the model components of the different parts of SiC power MOSFET.

TABLE 2. Parameters for Breakdown Characteristics Modeling

Notation	Definition	Value	Unit
$I_{leakage0}$	Intrinsic leakage current at the room temperature	1E-10	A
vbr0	Breakdown voltage at room temperature	1780	V
bvn	Avalanche multiplication exponent	0.642	-
Fc_{BV}	Smoothing parameter of the breakdown voltage	0.99	-

these equations are from [21]. In this work, avalanche breakdown equations are modified to be continuous across the first and third quadrant operations. Here, *vbr* is the temperature-dependent breakdown voltage. ***bvn*** is the avalanche multiplication exponent, and $\boldsymbol{Fc_{BV}}$ is a smoothing parameter. I_{mult} is the avalanche multiplication current. M is the multiplication factor that depends on the electric field. The channel current I_{mos} includes the gate dependency of the breakdown voltage with its inherent Vgs dependency.

The inclusion of thermal runway in the model is accomplished with a generic SPICE *npn* as the parasitic bjt. This *npn* is formed between the power MOSFET's source contact, body, and drift region, as shown in Fig. 6. This figure also represents the presented model's sub-circuit view as an extension of the model presented in [4].

Table 2 lists the parameters related to the breakdown characteristics. Initially, the breakdown voltage parameter (***vbr0***) can be assigned the value mentioned in the datasheet. If measured data is available, the value is extracted from fine-tuning the simulated result with the measured data. Parameter ***bvn*** is fine-tuned to match the slope of the current rise. Fig. 7 highlights the specific area where each parameter plays the most significant role.

IV. TEMPERATURE SCALING FOR SELF-HEATING MODELING

The most critical effect of the junction temperature is seen on the threshold voltage. The threshold voltage decreases in the SiC power MOSFET as the temperature increases. The reason behind this decrease is the increase in the thermal

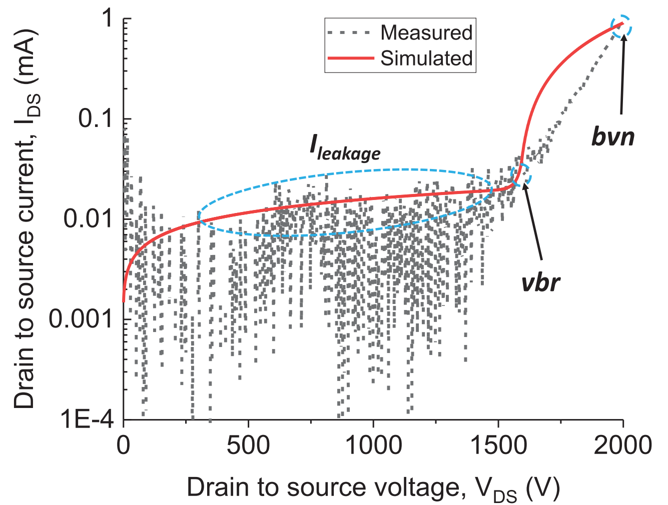


FIGURE 7. Leakage current and breakdown characteristics related parameter extraction.

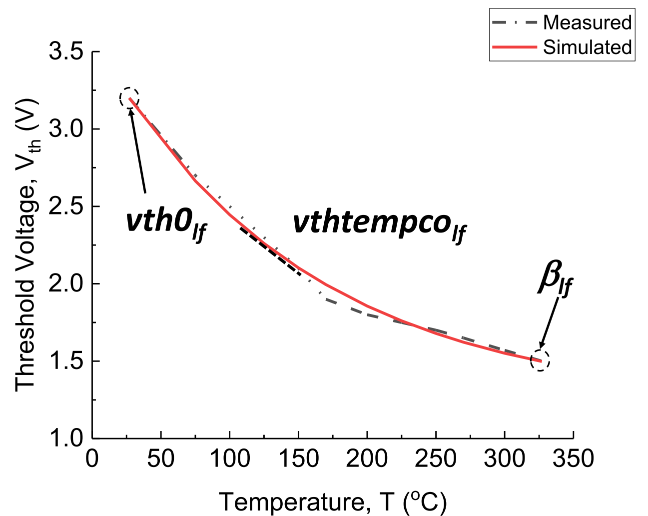


FIGURE 8. Threshold voltage variation with temperature in SiC power MOSFET and related parameters extraction.

generation of minority carriers in the channel region. Previous models like [6], [22], and [5] used linear equations to include this characteristic. However, such formulations cause non-convergence in electro-thermal simulations as the threshold voltage might become negative in the iterative simulation process. The linear decrease of threshold voltage with temperature is not physics-based either. Reference [23] presents experimental data proving that at temperatures higher than 200 °C, the threshold voltage decreases at a much slower rate than lower temperatures. This means that a linear decreasing relation will not predict correct behavior in electro-thermal simulation. This non-linear decrease of the threshold voltage with increasing temperature is shown in Fig. 8. This non-linearity is modeled with (25) modifying the method described in [7]. In [7], the effect of the interface charges is included by the mobility equation. However, as described in

TABLE 3. Threshold Voltage Related Temperature Parameters

Notation	Definition	Value ($y = f/r$)	Unit
$\boldsymbol{vth0_{ly}}$	Low gate voltage region's threshold voltage at the room temperature	3.414 / 1.681	V
$\boldsymbol{vth0_{hy}}$	High gate voltage region's threshold voltage at the room temperature	7.361 / 7.361	V
$\boldsymbol{\beta_y}$	Minimum threshold voltage	1.302 / 0.5	V
$\boldsymbol{vthtempco_{ly}}$	Tuning parameter of the slope for $\boldsymbol{vth_{ly}}$	0.003808 / 0.00875	°C^{-1}
$\boldsymbol{vthtempco_{hy}}$	Tuning parameter of the slope for $\boldsymbol{vth_{hy}}$	0.001/0.001	°C^{-1}

[3], the effect of interface charge is included in the model by separate threshold voltages ($\boldsymbol{vth_{ly}}$, $\boldsymbol{vth_{hy}}$) for low and high gate voltage regions, respectively.

$$vth_{xy} = \boldsymbol{\beta_y} + \left(\boldsymbol{vth0_{xy}} - \boldsymbol{\beta_y}\right) \cdot \exp\left[-\boldsymbol{vthtempco_{xy}} \cdot tempdiff\right] \quad (25)$$

$$tempdiff = temperature - \boldsymbol{tnom} \quad (26)$$

Here $\boldsymbol{vth0_{xy}}$ stands for the threshold voltage at room temperature. β_y represents the minimum threshold voltage at very high temperatures (>300 °C). The measured threshold voltage at the maximum measured temperature is assigned as its value. $\boldsymbol{vthtempco_{xy}}$ is the tuning parameter that controls the slope. Table 3 lists the parameters related to the temperature dependence of the threshold voltage.

The temperature dependence of the transconductance largely depends on mobility. As described in [4], the transconductance parameters are extracted from the drain current's saturation region. This current increases with the increasing temperature for the low gate voltage region. The saturation current decreases with the higher temperature for the high gate voltage region. The reason behind these opposite trends is the presence of two different controlling mechanisms of mobility [7]. The first mechanism is carrier scattering due to filled interface states. The second is lattice scattering. At the low gate voltage region, the interface state induced carrier scattering controls the mobility of the channel. The interface states are less likely to be filled with the increasing temperature. So, the contribution from this scattering mechanism drops. Increased mobility increases the low gate voltage transconductance. However, the trend is not linear as it saturates after a certain high temperature. The temperature dependence of the transconductance at the low gate voltage region (kp_{ly}) is expressed with (27). Fig. 9 shows the extracted kp_{ly}values at

TABLE 4. Transconductance Related Temperature Scaling Parameters

Notation	Definition	Value ($y = f/r$)	Unit
$\boldsymbol{kpl0_y}$	Saturation region transconductance parameter of low gate voltage region at the room temperature	3.568 / 27.01	A/V^2
$\boldsymbol{kph0_y}$	Saturation region transconductance parameter of high gate voltage region at the room temperature	226.9 / 226.9	A/V^2
$\boldsymbol{tnom}$	Room temperature	300	K
$\boldsymbol{kpltempco_y}$	Slope adjusting parameter for kpl	10 / 0.06858	A/V^2
$\boldsymbol{kphtempco_y}$	Slope adjusting parameter for kph	0.5309 / 0.5309	-

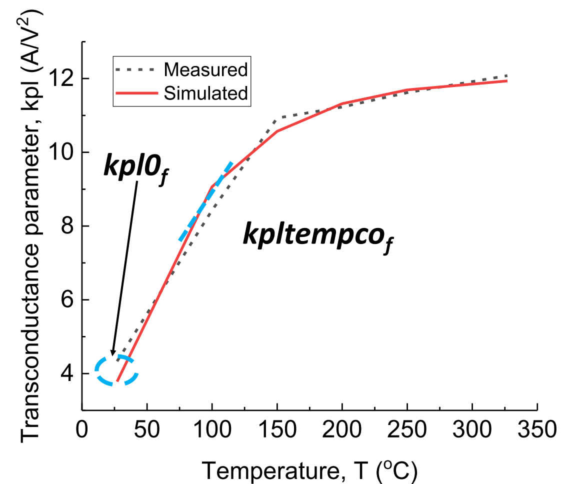


FIGURE 9. $\boldsymbol{kp_{lf}}$ variation with temperature in SiC power MOSFET and related parameters extraction.

different isothermal conditions. The expression (27) can accurately fit these extracted values, enabling temperature-scaling of transconductance parameter kp_{ly}.

$$kp_{ly} = \boldsymbol{kpl0_y} + \boldsymbol{kpltempco_y} \cdot \ln(tratio) \quad (27)$$

$$tratio = \frac{temperature}{\boldsymbol{tnom}} \quad (28)$$

In the high gate voltage region, the effect of the interface charge is less even at room temperature. The controlling mechanism for mobility is lattice scattering. This scattering increases with the increasing temperature. The transconductance at the high gate voltage region (kp_{hy}) decreases as the temperature increases. Even in this case, a weak saturation can

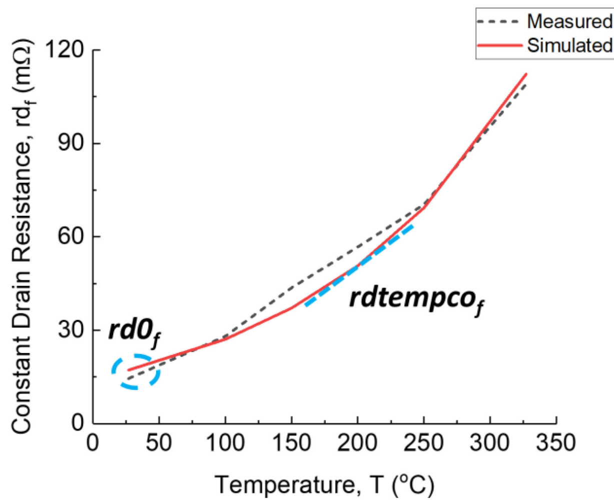


FIGURE 10. rd_f **variation with temperature and related parameters extraction.**

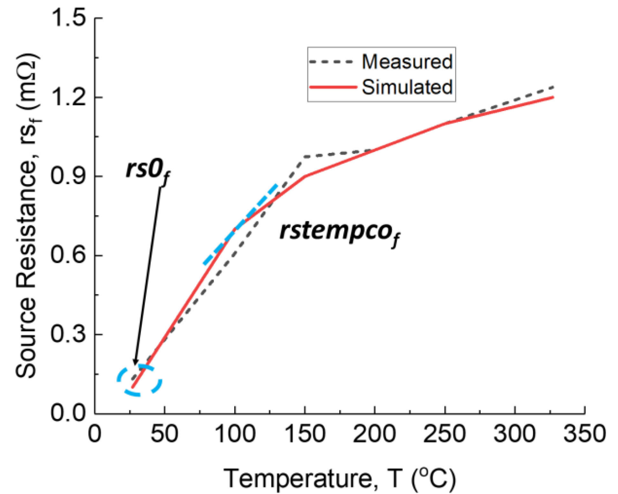


FIGURE 11. rs_f **variation with temperature and related parameters extraction.**

be noticed. This trend is incorporated in the model using (29).

$$kp_{hy} = \boldsymbol{kph}0_{\boldsymbol{y}} \cdot tratio^{-\boldsymbol{kphtempco_y}} \quad (29)$$

The on-resistance (Rds_{on}) varies significantly with temperature. The drift region resistance largely determines the total Rds_{on} at high current operation. With increasing lattice scattering at high temperatures, the drift region resistance increases. Moreover, the source terminal's contact resistance also increases due to increasing scattering at the heavily doped source contact. As can be seen from Fig. 10, the drain resistance shows an exponential rise with increasing temperature. It is expressed with (30).

$$rd_y = \boldsymbol{rd}0_{\boldsymbol{y}} \cdot \exp\left(\boldsymbol{rdtempco_y} \cdot tdiff\right) \quad (30)$$

The increase of the source terminal resistance is gradual and can be expressed with the logarithmic expression of (31), seen in Fig. 11.

$$rs_y = \boldsymbol{rs}0_{\boldsymbol{y}} + \boldsymbol{rstempco_y} \cdot \ln(tratio) \quad (31)$$

$$\Theta_{xy} = \boldsymbol{\Theta x}0_{\boldsymbol{y}} + \boldsymbol{\Theta xtempco_y} \cdot \ln(tratio) \quad (32)$$

The channel resistance variation is taken care of by the variations MOSFET parameters, namely threshold voltage, transconductance, transverse field.

Transverse electric field parameters (Θ_{xy}) increase with the temperature rise. Increased empty interface states decrease the blocking of the vertical electric field, which increases vertical compression of mobility at higher temperatures. More empty interface states enable the vertical electric field to affect the channel charges substantially. This temperature dependence can be expressed with (32). Table 5 lists the parameters related to on-resistance and transverse field variation with temperature.

In the third-quadrant operation, i.e., ($Vds < 0$) and ($Ids < 0$), there are two paths for the current flow. First, the current

TABLE 5. **Parameters for On-resistance and Transverse Field Temperature Scaling**

Notation	Definition	Value ($y = f/r$)	Unit
$\boldsymbol{rs0_y}$	Parasitic source resistance at the room temperature	0.005663 / 0.005663	Ω
$\boldsymbol{rd0_y}$	Constant drain resistance at the room temperature	0.009095 / 0.001838	Ω
$\boldsymbol{rdtempco_y}$	Temperature coefficient of the drain resistance	0.008514 / 0.01044	K^{-1}
$\boldsymbol{rstempco_y}$	Temperature coefficient of the source resistance	0.004847 / 0.004847	Ω
$\boldsymbol{\theta l0_y}$	Transverse electric field mobility factor for low gate voltage region at the room temperature	0.1204/1	V^{-1}
$\boldsymbol{\theta h0_y}$	Transverse electric field mobility factor for high gate voltage region at the room temperature	0.152/1	V^{-1}
$\boldsymbol{\theta ltempco_y}$	Temperature coefficient parameter of $\boldsymbol{\theta l0_y}$	0.1329/2.272	V^{-1}
$\boldsymbol{\theta htempco_y}$	Temperature coefficient parameter of $\boldsymbol{\theta h0_y}$	0.04948/0.521	V^{-1}

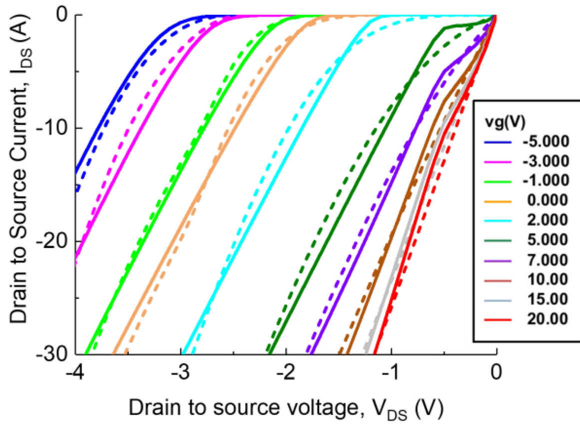


FIGURE 12. Third-quadrant output characteristics at room temperature. Symbols are the measured data, and solid lines are the simulated results.

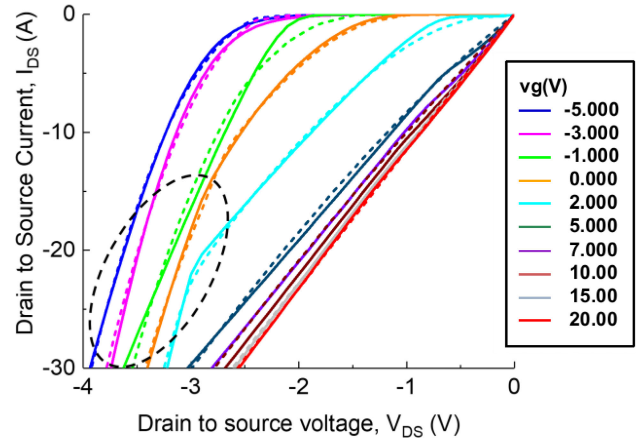


FIGURE 13. Overlay of measured (dashed) and simulated (solid) third-quadrant output characteristics at 200 °C.

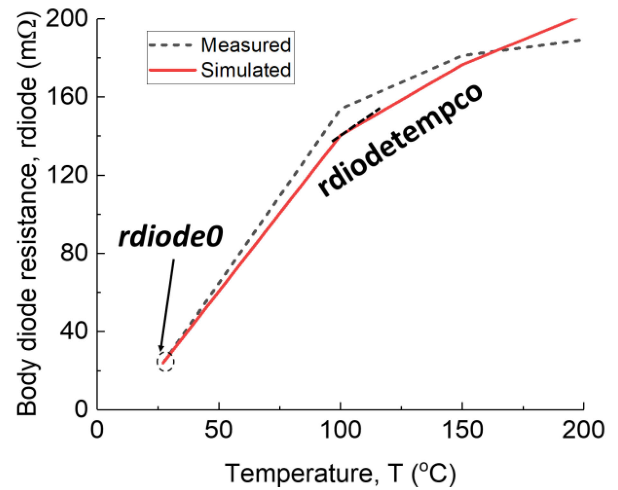


FIGURE 14. Logarithmic variation of diode resistance with increasing temperature.

can flow through the inversion channel as of the MOS operation. Second, the current can flow through the body diode formed between the p body and the n^- drift region. The first mechanism dominates for gate voltage higher than the threshold voltage and the drain voltage less than the forward drop of the *p-n* junction. As discussed in [4], the threshold voltage, transconductance, and on-resistance parameters of the MOS channel are different for the first and third quadrant operations and need different parameters set for accurate modeling. Though the parameters are different for the forward and reverse conduction of the MOSFET, the reverse conduction parameters' temperature dependences follow the same physics as their forward conduction counterparts. So the temperature dependencies of the third-quadrant MOS current related parameters are expressed by (25) through (32). The values of the temperature coefficients are different and are listed in the above tables with subscript $y = r$

The paper in [4] presents a unique modeling approach that includes the gate-dependent body diode characteristics and reverse recovery. The body diode conduction path sees different resistance than the MOSFET conduction path with no channel region or JFET region. Also, conduction modulation takes place due to the bipolar nature of the *p-i-n* body diode. Reference [4] addresses this issue by using a separate resistance parameter (***rdiode***) for the body diode on-resistance. This bias-independent parameter is enough for modeling the conduction modulation up to the rated current at room temperature.

However, the resistance becomes bias-dependent at higher temperatures (>150 °C). This can be seen in Figs. 12 and 13. In Fig. 12, the body diode curves' slopes at room temperature show minimal dependence on the gate bias. However, at 200 °C, the slopes of diode curves become significantly dependent on the gate voltages, as shown in Fig. 13.

An extensive inclusion of conduction modulation in compact model is a broad research scope itself. The conduction modulation effect has been incorporated in this work empirically, considering its significance for the model's overall efficiency and accuracy. The approach is to make the body diode's resistance gate dependent. The gate dependency of the body diode's resistance is expressed as:

$$rdiode = \frac{rdiode0_t}{1 + rdiovgs_t \cdot V_{gsnreffvk1}} \tag{33}$$

$$V_{gsnreffvk1} = Vgs - \boldsymbol{vk}1 - \frac{1}{2} \times \left[Vgs - \boldsymbol{vk}1 + \sqrt{(Vgs - \boldsymbol{vk}1)^2 + 4\partial^2} \right] \tag{34}$$

Here, *rdiode0_t* depicts the body diode's resistive slope at $Vgs = \boldsymbol{vk1}$. ***vk1*** is a model parameter that stands for the body diode's positive knee gate voltage. It is the positive most Vgs for which diode resistance determines the slope [4]. With increasing lattice vibration, the resistance of the conduction path rises with increasing temperature. This can be seen in Fig. 14. The increase of this resistance is logarithmic and

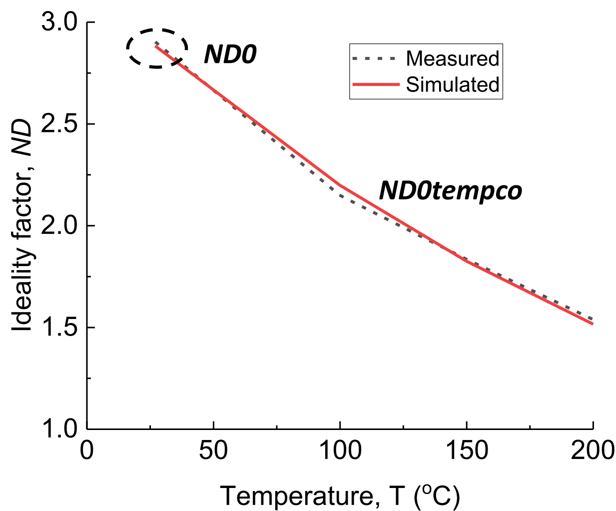


FIGURE 15. Body diode's ideality factor variation with temperature.

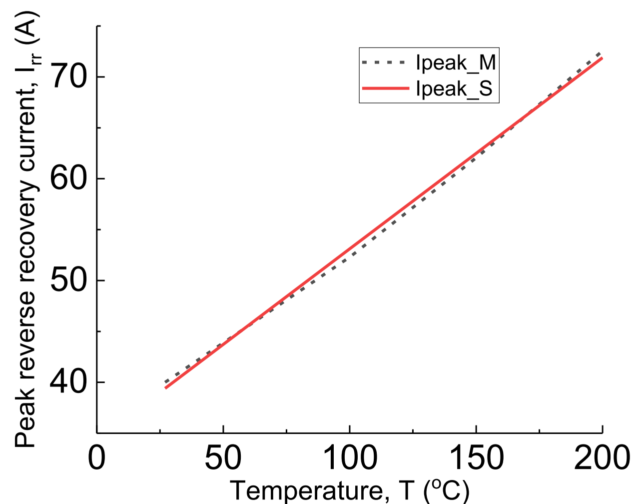


FIGURE 16. Peak reverse recovery current (I_{rr}) variation with temperature.

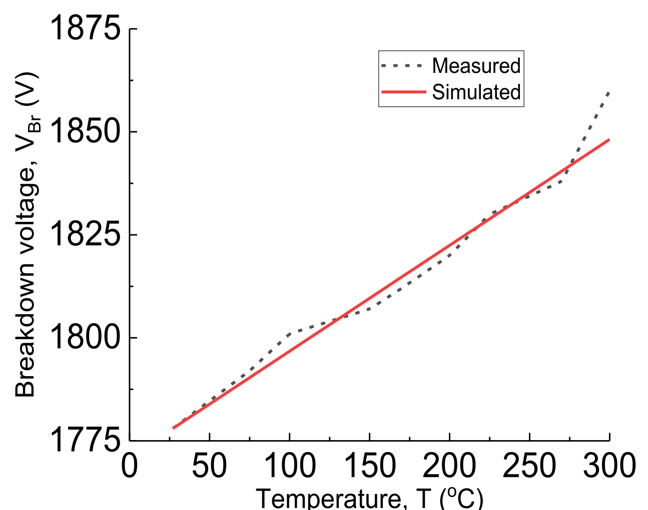


FIGURE 17. Breakdown Voltage (*vbr*) variation with temperature.

modeled with (35).

$$rdiode0_t = \boldsymbol{rdiode}0 + \boldsymbol{rdiodtempco} \cdot \ln(tratio) \tag{35}$$

rdiovgs_t incorporates the conduction modulation effect. It helps to fit the different slopes for different *Vgs* curves. $V_{gsnereffvk1}$ is the effective gate voltage for the body diode as described in [4].

Conduction modulation in the power MOSFET's drift region increases with the temperature due to increased minority carrier lifetime. The decrease in resistance at the diode conduction part is more prominent at higher temperatures than at room temperature. Hence the conduction modulation parameter *rdiovgs_t* becomes more significant with increasing temperatures. The temperature dependence of *rdiovgs_t* is modeled with the (36).

$$rdiovgs_t = \boldsymbol{rdiovgs}0 \cdot (tratio)^{\boldsymbol{rdiovgstempco}} \tag{36}$$

The forward voltage drop of the body diode decreases with the increasing temperature. This decrease is related to increased intrinsic carrier concentration at higher temperatures. The reduction can be more stably modeled with a linear relation for better simulation convergence. Eq. (37) shows the temperature dependence modeling of *ND*. *ND* is the constant part of the ideality factor of body diode [4]. The forward voltage drop of the body diode at $Vgs = \boldsymbol{vk1}$ is tuned with *ND***.** Fig. 15 shows the overlay of the expression (37) and the extracted values of *ND* at different temperatures. ***ND0***is the ideality factor at the room temperature, and ***NDtempco*** is the temperature co-efficient of *ND*.

$$ND = \boldsymbol{ND}0 \cdot (tratio)^{-\boldsymbol{NDtempco}} \tag{37}$$

Increasing temperature increases the carrier lifetime [24]. As a result, total reverse recovery time and peak reverse recovery current increase. Fig. 16 shows the variation of peak reverse recovery current with temperature. Temperature dependence of the carrier lifetime parameter (*tau*) can accurately model the temperature scaling of revere recovery peak current with the (38).

$$tau = \boldsymbol{tau}0 \cdot tratio^{\boldsymbol{tautempco}} \tag{38}$$

The breakdown voltage (*vbr*) of a SiC power MOSFET increases with temperature [25]. Measured results also support the linearly increasing trend, as shown in Fig. 17. This increase is practically linear and can be modeled with (39).

$$vbr = \boldsymbol{vbr}0 + \boldsymbol{vbrtempco} \cdot (tdiff) \tag{39}$$

Table 6 lists the parameters related to body diode and the breakdown voltage temperature scaling. The parameter set of an isothermal model can be extracted at any particular temperature following the process described in [4]. All the temperature coefficients' values are kept at zero during this extraction. Once parameter sets at different temperatures are extracted, the temperature coefficients can be extracted using a curve fitting tool like MATLAB or Python. Alternatively, only

TABLE 6. Parameters for Body Diode and Breakdown Voltage Temperature Scaling

Notation	Definition	Value	Unit
rdiode0	Body diode's series resistance at the room temperature	0.03163	Ω
rdiovgs0	Gate bias dependent conductivity modulation parameter at the room temperature	0.02101	V^{-1}
rdiodetemp	Temperature coefficient of the body diode's series resistance	0.003797	Ω
rdiodevgstemp	Temperature coefficient of the body diode's conduction modulation	4.684	-
tau0	The lifetime of the minority carriers in the drift region at the room temperature	1E-09	s
ND0	Body diode ideality factor at the room temperature	2.903	-
tautempco	Temperature coefficient of the carrier lifetime	7E-10	-
Ndtempco	Temperature coefficient of the ideality factor	0.274	-
vbrtempco	Temperature coefficient of the breakdown voltage	0.2564	$V\ K^{-1}$

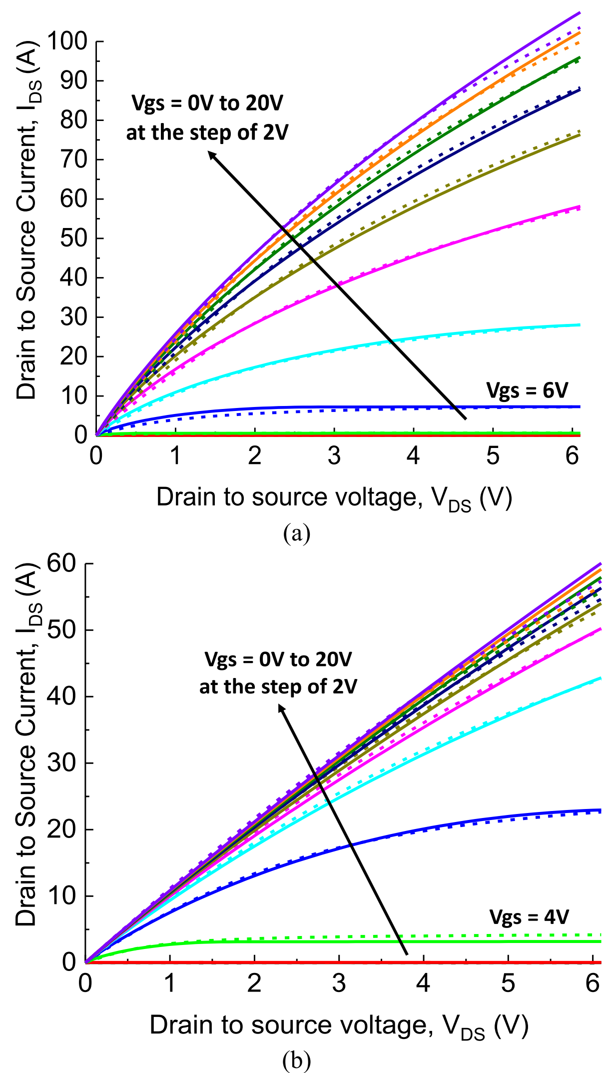


FIGURE 18. Measured (dashed) and Simulated (solid) output characteristics at (a) 27 °C and (b) 200 °C.

the room temperature parameter set is extracted following the procedure described in [4], the temperature parameters are used as tuning parameters to fit simulated results with the measured data at different higher temperatures using IC-CAP [26], an extraction tool built for compact model parameter extraction.

V. MODEL VALIDATION

A. STATIC CHARACTERISTICS

Fig. 18 shows the Ids-Vds curves at room temperature and 200 °C. The temperature scaled model can accurately fit the output characteristics from 27 °C to 200 °C. Even though the parameter extraction process relies solely on output characteristics, simulated transfer curves at different temperatures fit accurately with the measured results for the extracted parameter set. Fig. 19 shows the transfer curves at different temperatures from the room temperature up to 327 °C. It validates the model's accuracy in temperature scaling for the first quadrant.

Though the device is only rated to 150 °C, the static measurements are taken up to 327 °C to test the model's capability. No degradations (in terms of threshold voltage, on-resistance shift etc.) were seen after cooling down the device. Also the measured results follow the trend seen in [7], [23]. So the measured results can be considered reliable. Though these devices cannot sustain a stable operation at higher than the rated temperature, it did not pose any issues for static measurements.

The model's capability of capturing the third-quadrant output characteristics can be seen in Figs. 12 and 13, where the third-quadrant output characteristics are shown at room temperature and 200 °C. Figs. 1 and 3 validate the model's accuracy in simulating CV characteristics with *Vgs* and *Vds* variation, respectively. Lastly, Fig. 7 shows the model's capability in predicting the breakdown characteristics.

B. DYNAMIC CHARACTERISTICS

Double Pulse Tests (DPTs) were carried out at different temperatures to verify the switching characteristics of the model.

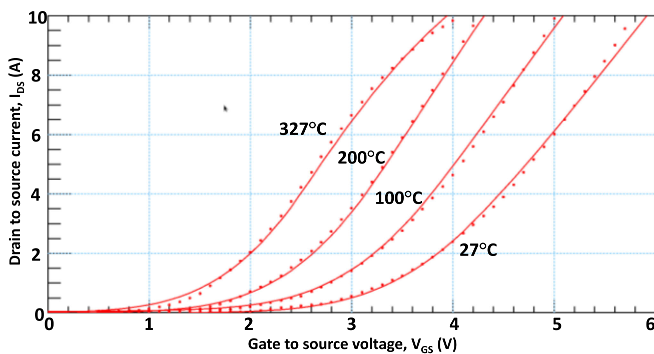


FIGURE 19. Transfer curves of C2M0045170D at different temperatures for *Vds* = 2V.

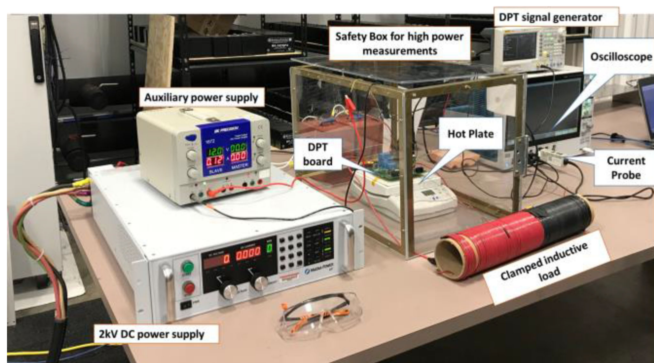


FIGURE 20. Double Pulse Test set up.

The DPT setup is shown in Fig. 20. A commercial evaluation board from CREE [27] is used for the test. The devices are mounted on the board's backside and are attached to the hot plate with Kapton tape. A safety shield surrounds the DPT board and the hotplate. An oscilloscope from Tektronix (MSO58) with a 6.25 GS/s sampling rate and 2 GHz bandwidth is used to measure the output waveforms. The lower side device's gate to source voltage is measured using a passive probe with 10x attenuation. The drain to source voltage was measured using Tektronix's TPP0850 passive high voltage probe. This probe has a bandwidth of 800 MHz and is rated to measure up to 2.5kV peak voltage. The drain to source current is measured using a Tektronix TCP0030A AC/DC current probe. This current probe has a very high bandwidth of 120 MHz. The switching is conducted at 1000 V, and 30 A. Magna-power's 2kV DC power supply is used for the test. A 320 μH inductor is used as the clamped inductive load. A thermocouple is used for measuring and controlling the temperature of the hotplate. Since the pulse durations are very small, self-heating can be neglected for a DPT. Hence the measurements can be termed isothermal at the temperature set at the hotplate. Due to the limitations of the DPT board, tests were performed only up to 200 °C. Besides the board's limitation, probe connectors melt at higher temperatures. Though 200 °C is still higher than the rated voltage of the device, no abnormality was observed. It was possible due to the short duration of DPT.

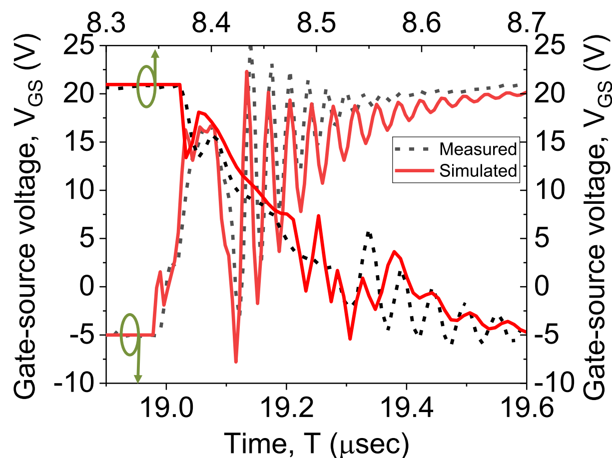
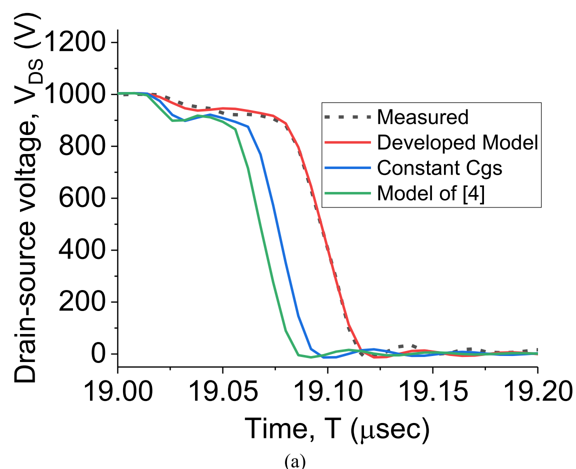
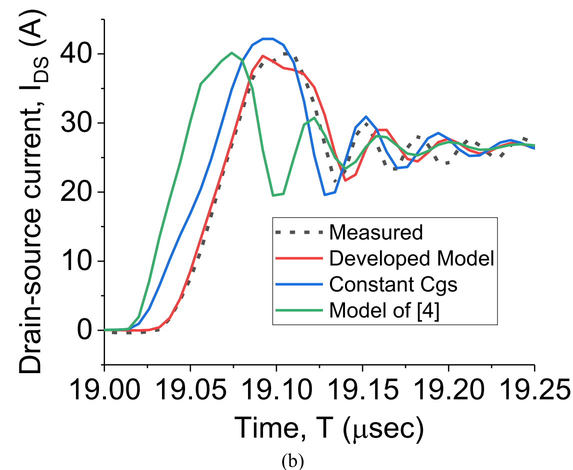


FIGURE 21. Turn-on and Turn-off transient of the gate voltage at room temperature.



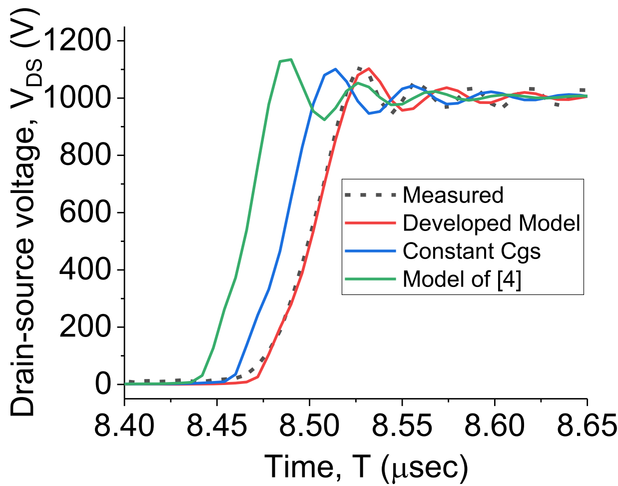
(a)



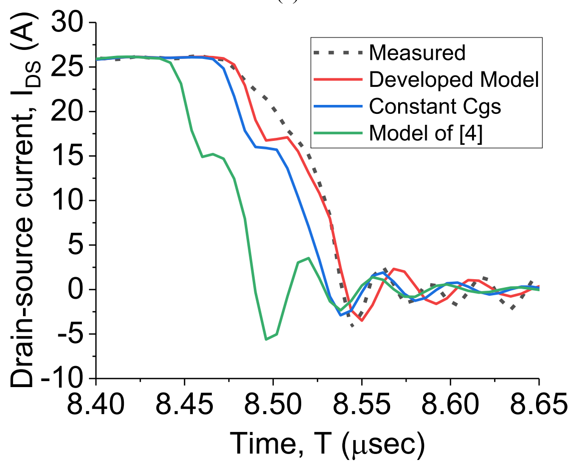
(b)

FIGURE 22. Turn-on (a) V_{DS} and (b) I_{DS} at room temperature.

Figs. 21–23 show the DPT results at room temperature. In Fig. 21, the turn-on and turn-off transitions of the gate voltage are shown. The model can accurately fit the gate voltage transient characteristics due to accurate CV and static



(a)



(b)

FIGURE 23. Turn-off (a) V_{DS} and (b) I_{DS} at room temperature.

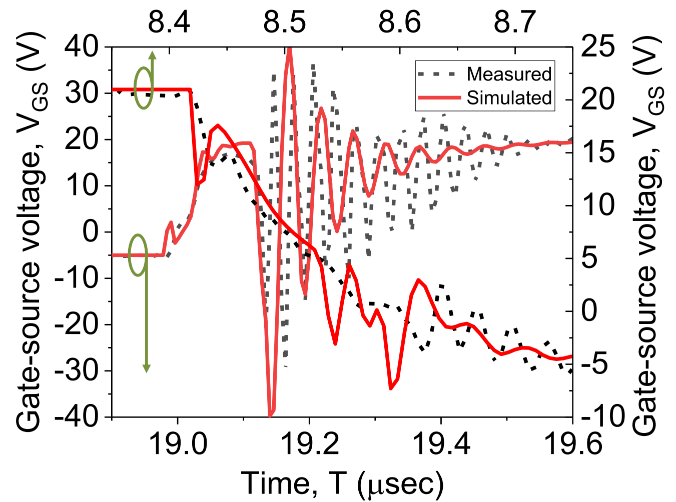


FIGURE 24. Turn-on and Turn-off transient of the gate voltage at 200 °C.

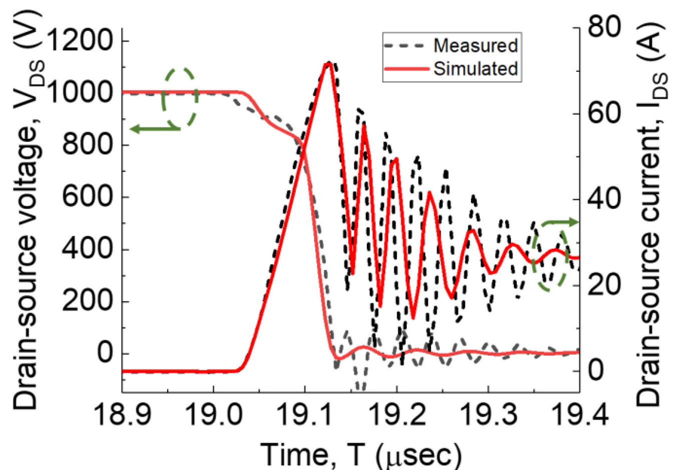


FIGURE 25. Turn-on V_{DS} and I_{DS} waveform at 200 °C.

characteristics. Because of precise modeling of *Cgd*, the simulated characteristics fit every sharp change in the gate voltage transition both in turn-on and turn-off state. The reverse recovery parameters were adjusted from the measured DPT results. The large negative spike at 19.1 μs in the turn-on gate voltage curve is accurately simulated. A close match in the gate voltage oscillation indicates the accurate modeling of the gate voltage dependent *Ciss*.

Fig. 22 shows the turn-on V_{DS} and I_{DS} waveforms at room temperature. The developed model has a more accurate expression of *Coss*. As a result, the dip in the *Vds* curve fits perfectly. The current overshoot at 19.1 μs, a summation of *Coss* discharge and reverse recovery, matches the measured result. The close match in the current oscillation frequency verifies the accurate extraction of the PCB layout parasitics. The parasitics of the board is extracted using ANSYS Q3D simulation. Fig. 23 shows the turn-off characteristics. The model predicted *dv/dt* and *di/dt* match closely with the measured result.

Two different versions of the model are also simulated with the same DPT circuit schematic to observe the effect of CV model modifications. The first is the model of [4] which does not have modified *Crss* characteristics or *Vgs* dependent *Cgs*. Another version that includes the modified *Crss* characteristics but does not have *Vgs* dependent Cgs characteristics (labeled as constant Cgs) is also simulated. As shown in Figs. 22 and 23 the model with constant *Cgs* characteristics causes a time shift with the measured data. This is because the simplified constant *Cgs* model underpredicts the capacitance's value at Vgs $>$ 0. As a result, dynamics between the power loop and gate loop do not match the actual circuit. A larger value of internal gate resistance can minimize this issue. But it creates gate oscillation magnitude and frequency mismatch due to mismatched dynamics. For reliable gate driver design accurate gate dynamics is required. The problem compiles when Crss is also undervalued for the low Vds region by the model of [4]. This causes faster switching (higher *dv/dt* and *di/dt*) and larger overshoot than the measured results [8].

Figs. 24–26 present the DPT results at 200 °C. Fig. 24 shows the gate voltage switching for turn-on and turn-off.

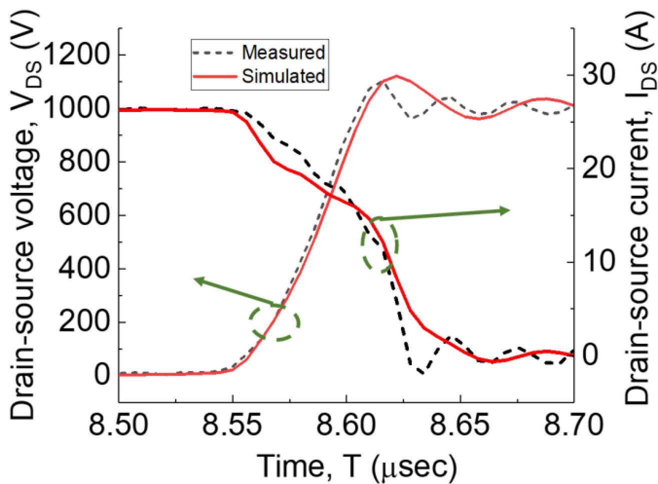


FIGURE 26. Turn-off V_{DS} and I_{DS} waveform at 200 °C.

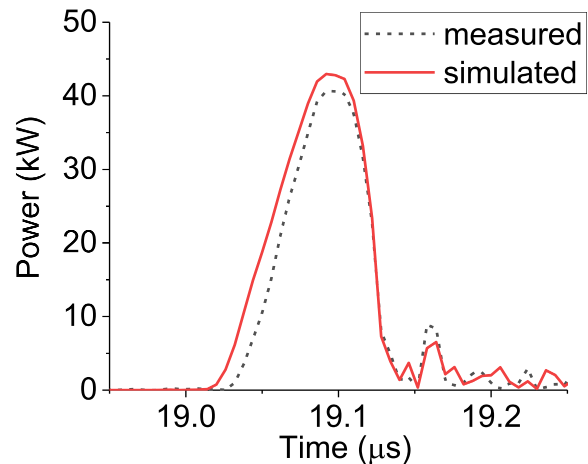


FIGURE 28. Turn-on switching loss at 200 °C.

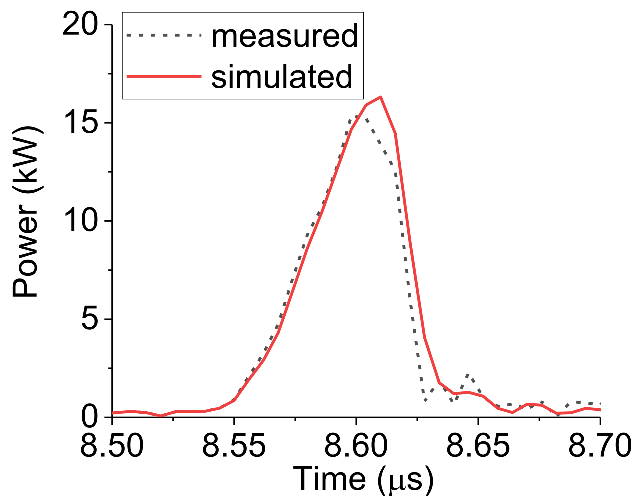


FIGURE 27. Turn-off switching loss at 200 °C.

TABLE 7. Switching Energy Loss At Different Temperatures

Temperature	Results	E_{off} (μJ)	E_{on} (μJ)	Total Error (%)
27 °C	Measured	693	1200	-
	Simulated	659	1400	8.0621
100 °C	Measured	750	2200	-
	Simulated	687	2500	7.4364
150 °C	Measured	772	2400	-
	Simulated	770	2700	8.5878
200 °C	Measured	784	2800	-
	Simulated	781	3200	9.9723

TABLE 8. Comparison of the Transition Times At the Room Temperature

Parameters	V_{DS} rise time (ns)	I_{DS} fall time (ns)_	V_{DS} fall time (ns)	I_{DS} rise time (ns)
Measured	37.082	67.797	65.58375	27.695
Simulated	38.27751	62.068	66.69287	27.726
Error (%)	3.224	8.449	1.691	0.1133
Error in [15] (%)	18.79	0.53	32.85	13.9

There is a slight mismatch in the significant downward spike and oscillation. This might be caused by the variation of PCB parasitics at higher temperatures. PCB parasitics are considered temperature-independent in the simulation.

The current overshoot magnitude matches the measured results during the turn-on switching (Fig. 25). The temperature scaling of the reverse recovery parameters was based on these measured DPT results. However, the oscillation frequency and the Coss dissipation loss have a slight mismatch. Possible causes are the variation of Coss with temperature or the change in package parasitics at high temperatures. In Fig. 26, the turn-off *dv/dt* and *di/dt* agree well with the measured result. However, the oscillation frequency is lower compared to the measured result.

Figs. 27 and 28 show a comparison between the measured and simulated switching power losses at 200 °C. These figures show that the model can predict the switching losses very accurately. Table 7 lists the measured and simulated switching energy losses at different temperatures. Due to temperature scaling, the developed model's accuracy exceeds the 90% mark at all temperatures.

Tables 8 and 9 show the simulated and measured transition times (rise and fall) of the drain voltage and the drain current at room temperature and at 200 °C, respectively. Reference [15] also describes a model of SiC power MOSFETs with

TABLE 9. Comparison of the Transition Times At 200 °C

Parameters	V_{DS} rise time (ns)	I_{DS} fall time (ns)_	V_{DS} fall time (ns)	I_{DS} rise time (ns)
Measured	37.93	65.93	60.02	23.75
Simulated	40.39	73.55	61.30	25.47
Error (%)	6.51	11.56	2.13	7.21
Error in [15] (%) At 125°C	3.21	8.81	1.87	3.66

temperature-dependent parameters and uses the same d evice (C2M0045170D) to validate the dynamic characteristics. So, a comparison between the two models is also presented here. At room temperature, the presented model of this paper can predict the transition times of the output voltage and currents with very low error. Though [15] is a behavioral model, the error percentages in predicting transition times are higher (except I_{DS} fall time). It should be mentioned that the DPT was performed at a lower voltage (700V compared to 1000V) and lower current (20A compared to 26A) in the experiment described in [15].

At 200 °C, the error percentage of the presented model increases. But the maximum error is still less than 12%. 125 °C is the maximum temperature at which [15] performed the DPT. The switching voltage and current were also lower (400V and 10A) compared to the DPT performed in this work. Still, the error percentages are close between these two models. This comparison proves that the physics-based presented model is at least on-par or more accurate in predicting dynamic characteristics at different ambient temperatures than a behavioral model of [15].

VI. SYNCHRONOUS BUCK CONVERTER TEST

A synchronous buck converter study has been performed to validate the presented model's convergence property and emphasize the importance of including self-heating electro-thermal modeling. A similar study is performed in [9]. In ref. [8], it has been shown that such simulation is important to predict the junction temperatures in a converter design. It is possible to add variations between different dies in a multi-chip power module and see the differences in junction temperatures with such electro-thermal simulations. However, no experimental data is provided in [9] to be used as a reference point for validation. This section validates the model's convergence property and predictability in an electro-thermal simulation with the measured results.

The synchronous buck converter has been designed using the half-bridge configuration of the DPT board [27]. It needs to be mentioned here that the objective of this experiment is not to design any efficient synchronous buck converter. The objective is to validate the model's capability with a safe and easy-to-measure circuitry.

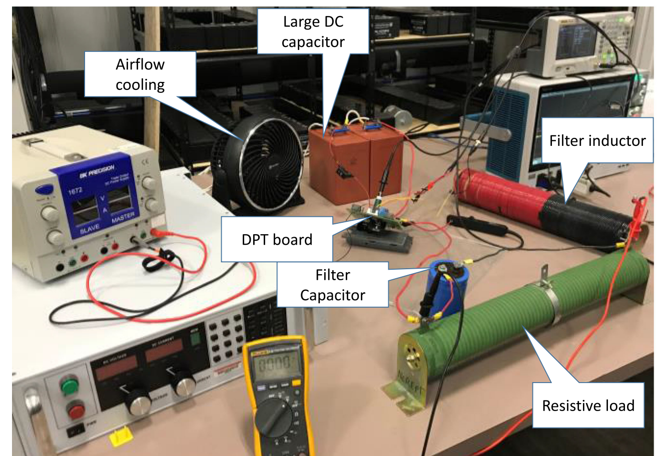


FIGURE 29. Synchronous Buck converter test set-up.

TABLE 10. Synchronous Buck Converter Parameters

Parameter	Value	Unit
Input voltage	600	V
Output voltage	60	V
Load current	13	A
Duty cycle	0.1	
Dead time	500	ns
Switching frequency	40	kHz
Output current ripple	±2	A
Filter capacitor	450	µF
Filter inductor	320	µH
Load resistance	4.1	Ω
Decoupling capacitor	4500	µF
Input Gate signal	+20/-5	V

The synchronous converter design is selected because part of its operation is in the third quadrant region. The input voltage for the converter is 600V. The expected output voltage is 60 V with a 10% duty cycle. A smaller blocking voltage is selected considering higher overshoot at high temperatures. The converter was switched with a frequency of 40 kHz. A slower frequency is deliberately chosen to validate both conduction loss and switching loss prediction capability of the model. The dead time between the two switches was set to 500 ns from the recommendation of the evaluation board's manual. Also, a larger dead time gives the body diode more conduction time. Since one of the uniqueness of the presented model is the extensive inclusion of body diode conduction characteristics, a longer body diode conduction time is required to validate the temperature modeling of the body diode. A large filter capacitor of 450 μF was selected for keeping the output voltage ripple small. A filter inductor of 320 μH and a load resistance of 4.1 Ω are used for the setup. The overall test setup is shown in Fig. 29. The simulation schematic of the test setup is shown in Fig. 30. The gate driving signal part of the circuit is simplified for ease of simulation. The converter specifications are listed in Table 10.

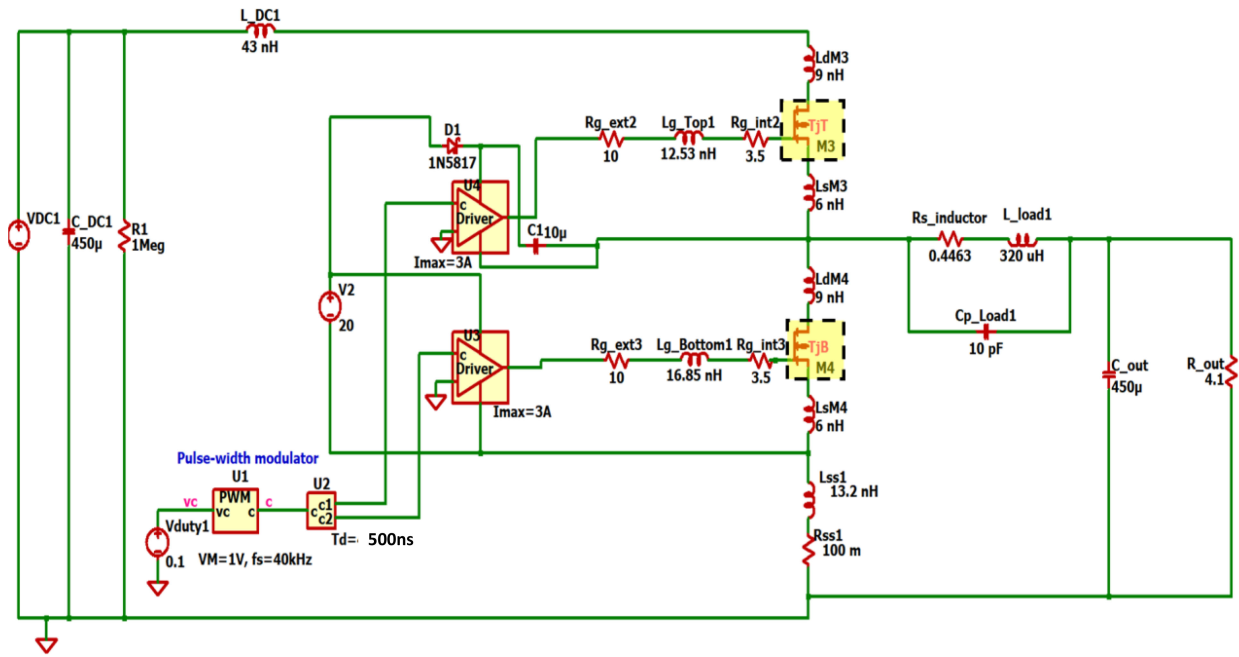


FIGURE 30. Simulation circuit for the synchronous buck converter.

One of the critical features of a power converter is self-heating. In the synchronous buck converter, both the high and low side devices of the half-bridge configuration are switched. Switching loss coupled with the conduction loss increases the junction temperature of the switching devices. The body diode conducts during the dead time and causes the device to heat up further. The temperature-dependent parameters of the presented model can accurately capture the device behavior in such self-heating conditions.

The model requires a thermal network (e.g., Cauer type) along with the temperature-dependent parameters for the electro-thermal simulation. A thermal network provided by the vendor is used from the device junction to the case. No external heatsink is used intentionally to increase the case temperature comparatively higher. The vendor-provided thermal network used in the simulation is shown in Fig. 31.

Fig. 32 shows the measured and simulated output voltage. There is a 0.6 Ω cable resistance, and the output voltage is close to 52.5 V. Fig. 33 shows the measured and simulated inductor current with ripple. Temperatures of the low and high side devices were measured using a thermocouple and DAQ (Data Acquisition) tool. Fig. 34 shows the measured temperatures of the high-side (input side) and low-side (output side) devices. Input voltage was gradually ramped up from 0 to 600V at 100V step. So the initial temperatures were different than the room temperature at the beginning of the 600V switching. Initial temperatures for the low and high side devices are 35 °C and 70 °C respectively. For simulation, these are assigned as ambient temperatures.

Power losses in the devices of a synchronous buck converter come mainly from four factors [28].

1) MOSFET switching loss, Psw

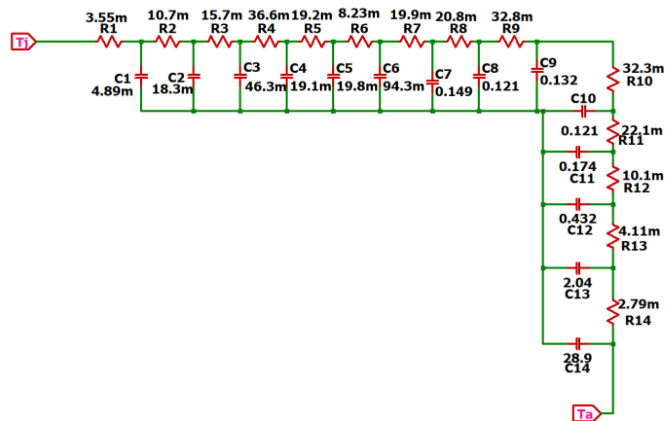


FIGURE 31. Vendor provided Cauer thermal network.

2) Dead time loss, P_D
3) Reverse recovery loss, Prr
4) Conduction loss caused by MOSFET on-resistance, P_{ON}

Switching loss is the major component of the total power loss in synchronous buck converter. This loss is generated when the high-side and the low-side MOSFETs are switched alternatively. However, the low-side device switches at a low drain to source voltage due to the conduction of body diode. So switching loss at the low-side device can be neglected.

During deadtime the body diode of the low-side device conducts the load current and this conduction loss is termed as the dead time loss. It is a conduction loss but different than the conduction loss of the MOS channel. Temperature dependent modeling of the body diode gives more accurate prediction of this dead time loss. During the turn-off of the body diode of

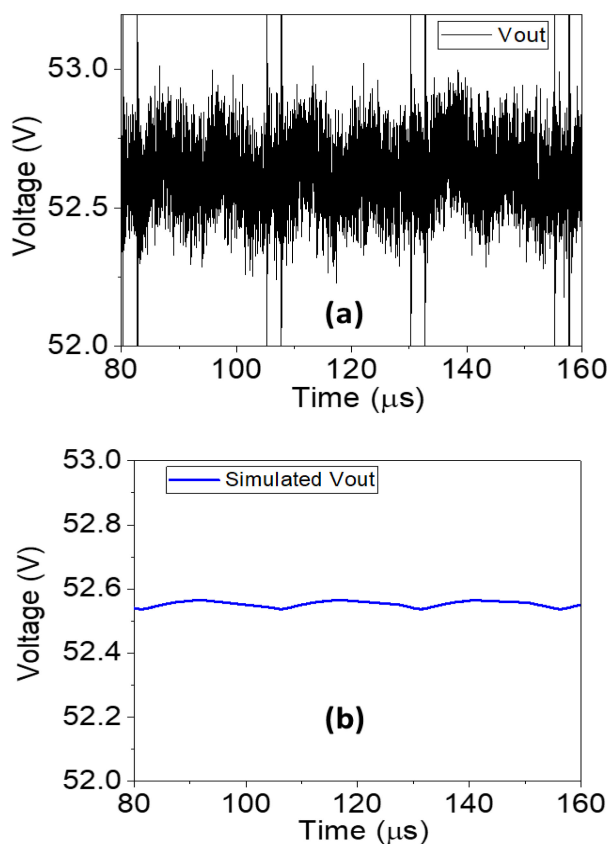


FIGURE 32. (a) Measured and (b) simulated output voltage.

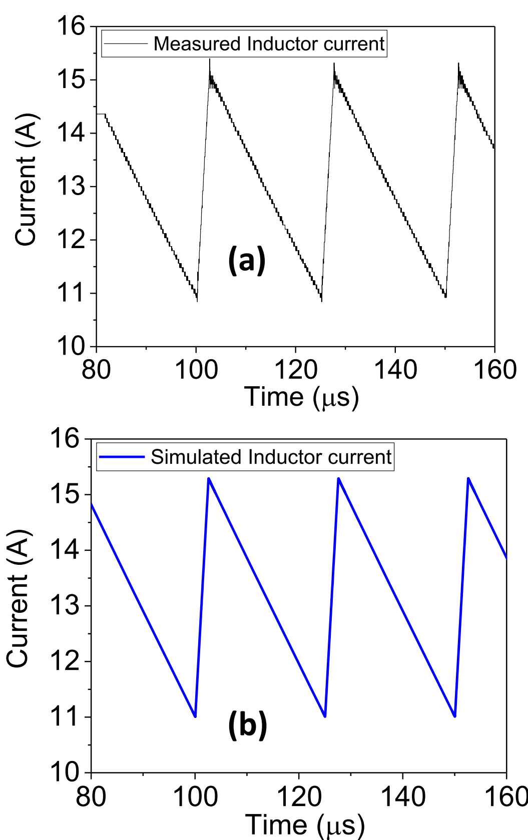


FIGURE 33. (a) Measured and (b) simulated inductor current.

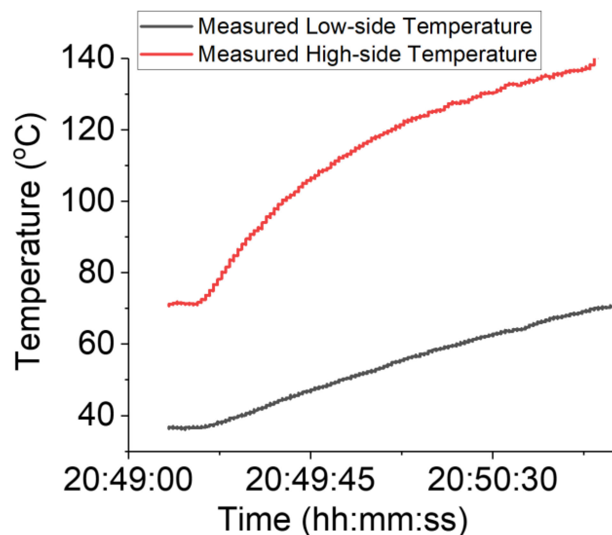


FIGURE 34. Measured temperatures at the high-side and low-side device.

the LS device, reverse-recovery loss of the body diode takes place. Temperature dependent body diode characteristics of the model allow accurate prediction of this loss.

The high-side and the low-side both generates conduction losses during their respective ON periods. Because of the duty cycle of just 10%, conduction loss in the low-side switch is higher at the same temperature compared to the high-side switch. But high-side switch heats up faster and it increases the on-resistance causing progressively higher conduction loss as the time progresses. This is one of the reasons why electro-thermal simulation is required for calculating the device temperature in a complex system.

Temperatures stabilize close to 140 °C for the high-side device and close to 70 °C for the low-side device. In the simulation, the steady-state temperatures for the devices are shown in Fig. 35. The high-side device has a steady-state temperature of 79.5 °C. For the low-side device, it is 134.15 °C.

Table 11 lists the simulated values of different losses at the initial temperature (35 °C for the low-side device and 70 °C for the top side device) and at the final temperatures (79.5 °C for the low-side device and 134.15 °C for the top side device).

The slight mismatch between measured and simulated results can be attributed to the vendor's provided Cauer thermal network. The simulated low-side device has a higher temperature than the measured result. However, the simulated high-side device has a lower temperature than the measured temperature. In the low-side device the bulk of the powerloss comes from conduction loss. In the intermediate temperatures, (27 °C<T<100 °C) on-resistance might be a little higher in the simulation model compared to the actual device as can be seen from Fig. 12. Hence, the low-side device is predicting higher junction temperature. In case of the

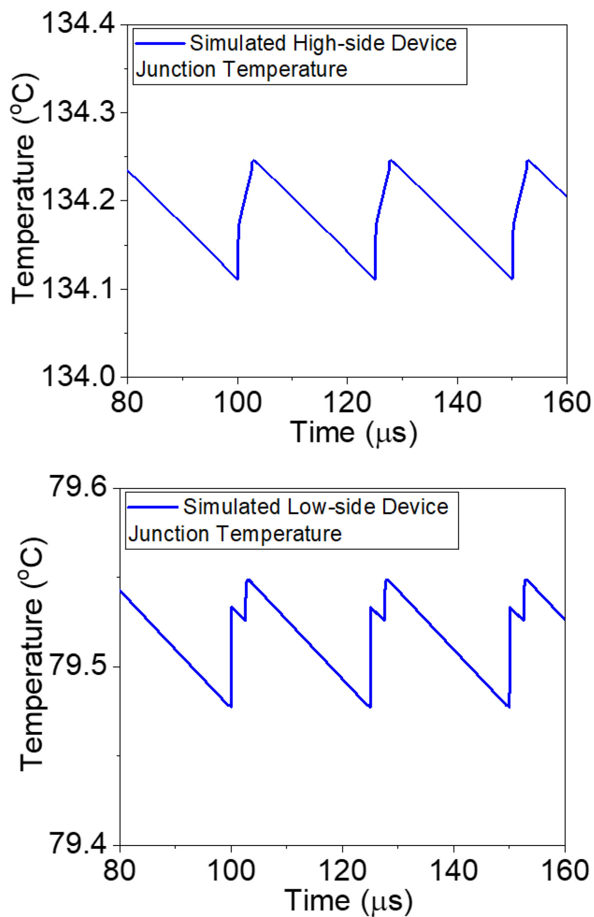


FIGURE 35. Simulated temperatures at the high-side and low-side device.

TABLE 11. Synchronous Buck Converter Parameters

Power Loss distribution (W)	At the initial temperature	At the final temperature
HS conduction loss	0.8780	1.1074
LS conduction loss	7.07	8.16
Dead-time loss due to diode conduction	2.0233	1.9214
Diode reverse-recovery Loss (reverse recovery charge)	7.19 (299.6nC)	15.31 (638nC)
HS switching loss (Switching energy loss)	18.88 (472 **µJ**)	25.68 (642 **µJ**)

high-side device, switching loss plays the major role. Simulated switching loss might be lower in low-current switching compared to the actual case. Though slightly different, a close match of the simulation results with the measured results validates the electro-thermal model's accuracy. Moreover, a long electro-thermal simulation vindicates the model's convergence property.

VI. CONCLUSION

In this paper, the physics-based isothermal compact model of a SiC power MOSFET, presented in [4], has been extended to a complete electro-thermal model. One of the first in elaborating the temperature dependencies of the third-quadrant characteristics, the model is accurate and efficient in circuit simulation with self-heating. The model includes enhanced accuracy in capacitance-voltage characteristics by including the input capacitance's gate voltage dependency. Moreover, the miller capacitance characteristics have been improved, especially for very low and high voltage regions. This improvement reduces the RMS error in simulated *Crss* from 21% to less than 5%. The model's accuracy in simulating switching characteristics is validated by performing double pulse tests (DPTs) at different temperatures. The presented model predicts switching losses with less than 10% error up to 200 °C of the ambient temperature. Comparison between simulated and measured results also show that the modified CV characteristics fix the dynamics between the power and gate loop and remove the time shift in the simulated result. This accurate CV model also gives more accurate gate oscillation results. Moreover, with physics-based temperature-dependent parameters, the presented model is at least equal or better than behavioral models in predicting switching losses at different temperatures. This has been validated by comparing it with the results of [15]. Lastly, the model closely predicts a synchronous buck converter's output waveforms and junction temperatures of the high side and low side devices. This electro-thermal simulation with self-heating will not be possible without physics-based and well-converged temperature dependencies of the parameters. Thus, the continuous test using synchronous buck converter validates the accuracy and convergence property of the developed physics-based advanced electro-thermal compact model.

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