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A Novel Modular Multilevel Converter With Ripple Current Elimination Channels Based on Isolated CLLC Resonant Circuits

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ABSTRACT This paper proposes a novel multilevel topology "Modular-Isolated-Multilevel-Converter" which achieves almost zero low frequency capacitor voltage fluctuation. It inherits the structure of MMC but replaces the half bridge module by the newly proposed Isolated Half-Bridge (IHB). The fundamental and 2^{nd} order harmonic frequency current originally in the MMC module capacitor have been eliminated through connecting the secondary sides of the IHB at the same level of the three phases together. The elimination is due to that the 1^{st} and 2^{nd} order components in the arm current are 120° phase shifted in three phases. Therefore, the module capacitance is reduced by more than 10 times since it only carries switching frequency ripple. Moreover, the arm inductance can also be significantly reduced since the 2^{nd} order harmonic current disappears. The topology is specifically suitable for variable frequency drive application, because its capacitance and inductance are not affected by the output frequency. The challenges of zero frequency start-up when MMC is adopted for VSD can be addressed here. In the paper, the operation principle of the proposed MIMC is fully analyzed and the mathematical model is built. Moreover, a methodology of capacitor sizing and arm inductor design for general MMC topology is proposed. The detailed design considerations for MIMC are also discussed and presented. The plant modeling and control strategy have been proposed for MIMC. A 55-kW simulation is carried out to verify the theoretical analysis. And a 6-kW downscaled hardware prototype is also developed to demonstrate the benefits of the new topology over the traditional MMC.

INDEX TERMS CLLC resonant converter, modular multilevel converter (MMC), planar transformer, submodule (SM) capacitor low frequency voltage ripple elimination.

I. INTRODUCTION

Typical future requirements at the system level include: inherent redundancy to make the availability of the whole power electronics system extremely high; modular design to improve the scalability of the power converter; eliminating large passive filters; eliminating bulky transformers; real power exchange from several systems through a common dc link. To overcome these challenges, the high-power Voltage Source Converters (VSCs) are taking higher and higher market share and faster developments compared with the current source and the matrix converters over the past decade [1]–[4] because of the problems of Current Source Converters (CSCs) and matrix converter such as resonances, non-controllable reactive currents, unclamped device voltage, requirement for reverse blocking semiconductors. As a result, to fulfill the future requirements for the converter, the essential improvement of VSC and multilevel VSC is most useful. The main issues to be improved are summarized as: the requirement of high-pulse frequencies – and, in consequence, high dv/dt of the semiconductors; the danger of short circuits at the dc side causing extremely high surge currents; the unfavorable, slow dynamic behavior of dc-voltage controllability; the complex construction and lack of scalability when increasing the voltage or power range. To address these problems, the

high-power modular multilevel converter (MMC) is widely accepted in industry and energy system since it features the low dV/dt, low expense for redundancy, small filter size, high modularity, excellent harmonic performance and high-power quality [5]–[9]. In order to limit the SM capacitor voltage ripple within acceptable range, the capacitance of each SM need to be large enough to compensate the highest voltage ripple under certain low frequency. This problem is further exacerbated under low fundamental frequency region, which is kind of universal situation during the startup of a motor. Under this situation, simply increasing the capacitance alone is no more a reasonable solution. Therefore, utilization of MMC in applications with variable frequency scenarios, such as adjustable speed drives, is not that popular as expected [10]–[13].

In recent years, many methods have been proposed to solve the capacitor size issue. One effective approach is low frequency circulating current injection [14]–[16]. A second-harmonic circulating current is introduced and controlled to minimize the energy fluctuation. However, this injected low-frequency current significantly increases the device power loss as well as the current stress. High frequency circulating current injection is proved to be another good method [17]–[19]. The low-frequency voltage ripple or the energy fluctuations are shaped into high-frequency components and thus the SM capacitor can be charged or discharged in a faster speed. Therefore, the voltage ripple can be effectively damped and the required SM capacitance is reduced. However, besides the increased current stress and device conduction loss, another drawback of this method is the additional inducted common mode (CM) voltage at the motor terminals.

One class of methods aim at reducing capacitor size by new module structure [20]–[28]. To reduce the inrush current in the dc short circuit failure, a common method is to replace the Half-Bridge (HB) module by a Full-Bridge (FB) module [20]–[23]. With the similar power level and output voltage, the FB module can reduce the arm energy ripple at most by half. Therefore, replacing HB module by FB module is an effective method to reduce the capacitor size. However, it will bring the disadvantages of the conduction loss and switching loss increase since the same arm current now flows through two times of devices. To reduce the loss, a clamp-double SM [24], [25] or semi-FB SM [26] have been proposed, in which the module can be configured into one FB or two HBs by modulating the middle switch. If DC short circuit happens, half number of FBs is enough to generate a negative ac voltage to cancel out the source voltage, so only half number of the clamp-double SM needs to be installed compared to the number of HBs. But then in normal operation, the capability of generating a negative arm voltage is limited. Therefore, the capacitor size reduction is limited. To overcome the challenge, a double-zero submodule has been invented to further reduce the conduction loss brought by FB modules, as well as reducing the capacitor size [27], [28]. The double connection of the double-zero submodule can reduce the capacitor size by exactly half.

Another class of methods focuses on topological configurations [29]–[31], [43]–[45]. Cross-connected power channels are introduced to help absorb and balance the energy fluctuation between the upper arm and lower arm by properly controlling the flowing ac current in these channels [29], [30]. Based on these, horizon-connected channels built by DHBs are further proposed in [31] to replace the original cross-connected channels. The pulsating energy ripple in the three adjacent SMs can be eliminated as the vectoral low frequency current sum is zero. However, many extra active DHB control loops are added to the control strategy and thus increase control complexity. The flying capacitor MMC (FC-MMC) is introduced in [43]. In this topology, a cross-connected capacitor is placed between the middle point of the upper and lower arms to achieve the power balance between arms to reduce the SM capacitor voltage fluctuations. However, large current that proportional to the injected high-frequency voltage must be conducted by this single capacitor. Another novel hybrid MMC is proposed in [44]. In this topology, the upper and lower arms are connected through an additional middle SM which helps the power balance between arms. However, the voltage balance control complexity among SMs is increased. Moreover, the redundancy for this middle SM is difficult to implement and thus do harm to the system reliability. Based on [44], a power module is further inserted in each arm converter as proposed in [45]. In this topology, the two power modules of each phase leg are respectively connected to the positive and negative ports of the upper and lower arms. Cooperating with the additional middle SM, these power modules help control the power balance among arms and also realizes smaller SM capacitor voltage ripple, which reduces the SM capacitor size. However, this hybrid topology again sacrifices the modularity and reliability.

In this paper, a new horizon-connected ripple current elimination approach based on CLLC circuit is proposed for variable-speed drives. The three SMs on same level but from three phase legs are connected to a common capacitor through a high-frequency half-bridge CLLC channel. As a result, the arm current flows into the CLLC channel instead of the original SM capacitor. On the secondary side, the current converges at the common capacitor and then get cancelled each other because the vectoral sum of the current is zero. On the other hand, the SM capacitor supports the dc-link voltage of the CLLC stage on the primary side while the common capacitor plays the same role on the secondary side. Therefore, the three SM capacitors are coupled together through the bidirectional CLLC stages, through which the energy-exchange enables a dynamic voltage-balance state between these three SMs. That is, the unexpected low-frequency energy ripples induced from both fundamental and second-order harmonic current almost disappear and the SM capacitance is significantly reduced.

This paper is presented as follows. Section II demonstrates the proposed MMC configuration and explain the operation mechanism in detail. The hardware design considerations and methodologies of sizing SM capacitance and arm inductance

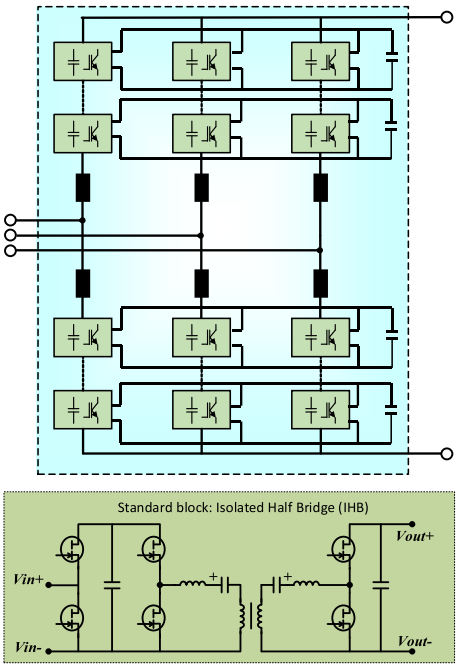

FIGURE 1. Circuit diagram of the proposed MIMC.

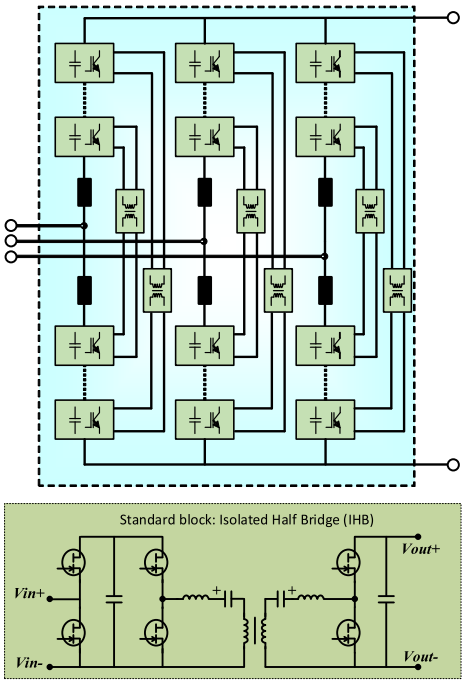

FIGURE 2. Circuit diagram of the alternative topology.

are discussed in Section III. The comprehensive control algorithms are demonstrated in Section IV. The simulation results for a whole MMC system and experimental results for a downscaled laboratory prototype are presented in Section V. Finally, Section VI concludes this paper.

II. PROPOSED MODULAR ISOLATED MULTILEVEL CONVERTER TOPOLOGY

The general architecture of the proposed MIMC is close to the traditional MMC, but each module is replaced by the new structure, as shown in Fig. 1. The parallel connection of three modules from three phases can lead to the cancellation of the ω and 2ω current originally in the module capacitor, so the capacitor at the end of the parallel connection is sized for the need of switching frequency ripple current absorption only. Compared to the original capacitor, its capacitance can be reduced significantly. Since the capacitance is the dominate factor for the size of the traditional MMC, the converter volume can be brought down significantly as well. Such excellent advantage tends to be more prominent as the system frequency is very low, especially in variable speed motor drive applications. However, if considering the grid connection in some applications, the proposed topology may lose the current elimination due to the three-phase unbalanced arm current. As a result, the capacitance of SM capacitor as well as the common capacitor are forced to be enlarged to damp the induced voltage fluctuations. Under this situation, an alternative topology is proposed as shown in Fig. 2. Each SM of upper arm and lower arm are linked together through an isolated DCDC converter. Although the three-phase interleaving is no longer existed in this topology, the low frequency pulsating energy ripple in SM capacitor can still be eliminated because the energy ripple in the coupled two SMs are pulsating in opposite direction. By transferring the excessive energy in one SM to the other one that is losing the energy, the SM capacitor voltages remains unchanged and ideally achieves the ripple free condition. Even under three-phase unbalance situation, the performance can be still maintained. It can be seen the methodology of constructing the new topology with energy ripple cancellation is to find out the modules that their AC energy ripple can add and cancel each other. The three-phase version of MIMC is more suitable for the motor drive application or others that the three-phase unbalance will unlikely happen. The two-phase version of MIMC is more suitable for the grid application where the unbalance is common. This paper will take the three-phase version of MIMC as an example to analyze.

A. PRINCIPLE OF CAPACITOR CURRENT CANCELLATION

Taking phase A as an example, the ideal equations of single arm converter output voltage and current can be expressed as equation (1) to (4). i_{C_up} is general expression of upper arm SM capacitor current in three phases. i_{aC_up} is Upper arm SM capacitor current of phase A. S_{up} and S_{low} are switching function of upper and lower arm converter in average model. i_{up} and i_{low} are arm current of upper and lower arm converter in average model. V_{up} and V_{low} are output voltage of upper and lower arm converter in average model. V_a and I_a are AC side output voltage and current amplitude of Phase A. V_{dc} and I_{dc} are dc bus voltage and current. M_1 is modulation index of each arm converter and M_0 is DC bus voltage variation index.

$$i_{up}(t) = \frac{I_{dc}}{3} + \frac{I_a(wt+\varphi)}{2} + \sum_{h=2\ldots k} i_h(t) \qquad (1)$$

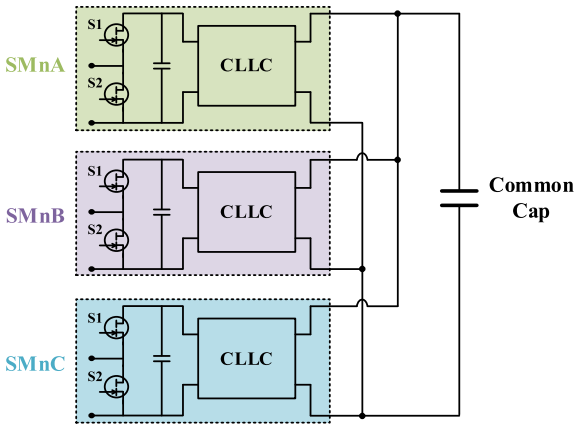

FIGURE 3. Illustration schematic of the ripple current elimination channels.

$$i_{low}(t) = \frac{I_{dc}}{3} - \frac{I_a(wt+\varphi)}{2} + \sum_{h=2\ldots k} i_h(t) \tag{2}$$

$$v_{up}(t) = \frac{V_{dc}}{2} - V_a \cos(wt) \tag{3}$$

$$v_{low}(t) = \frac{V_{dc}}{2} + V_a \cos(wt) \tag{4}$$

Also, it is assumed that the switching function can be expressed as equation (5) and (6), in which the PWM modulation does not consider arm dc bus voltage variations ($M_0 = 1$). M1 is the modulation index of each arm while M3 stands for the third harmonic injection:

$$S_{up}(t) = \frac{1}{2}M_0 + M_1 \cos wt \tag{5}$$

$$S_{low}(t) = \frac{1}{2}M_0 - M_1 \cos(wt) \tag{6}$$

Combining equation (1) (2) (5) (6), the arm capacitor current can be calculated as:

$$i_{C\_up}(t) = i_{up}(t) \times S_{up}(t) \tag{7}$$

$$i_{C\_low}(t) = i_{low}(t) \times S_{low}(t) \tag{8}$$

Moreover, considering only the dc and fundamental components of the arm current, combining the power balance equation (9) between the ac and dc side, the current flowing through the SM capacitor can be derived as shown in equation (10):

$$I_{dc} \times V_{dc} \times M_0 = \frac{3}{2} \times V_a \times I_a \times M_1 \tag{9}$$

$$i_{aC\_up}(t) = \frac{3}{16}I_a \cos(wt) + \frac{1}{8}I_a \cos(2wt) \tag{10}$$

Therefore, SM capacitor current contains fundamental frequency and 2nd order harmonic components, which further induce the voltage ripple of same frequencies on the SM capacitor. This is the root cause of the low frequency ripple across the SM capacitor.

Moreover, the resultant dc bus voltage spectrum can be derived by the equation (11):

$$V^e(t) = S_{up}(t) \times \frac{N}{C}\int S_{up}(t) \times i_{up}dt + S_{low}(t) \times \frac{N}{C}\int S_{low}(t) \times i_{low}dt \tag{11}$$

Generally, the dc bus voltage spectrum contains several spectral components, especially considering injected third harmonic. However, among them the most dominant component is the second order harmonics and can be expressed in equation (12).

$$V^e(t) = \frac{N}{wC}\left\{\begin{array}{l} \frac{I_a M_0 M_1}{8}\sin(\varphi) - \frac{I_{dc}M_1^2}{12}\sin(2wt) \\ \frac{3I_a M_0 M_1}{16}\sin(2wt+\varphi) + \frac{I_a M_0 M_1}{8}\sin(2wt-\varphi) \end{array}\right\} \tag{12}$$

This equation also presents the direct driving voltage for the circulating current. It needs to be pointed out that the effect of third harmonics injection is limited and therefore ignored in the calculation of dc bus voltage. Any higher order harmonics such as 4th and 6th order harmonics are also not counted in this due to their low amplitude.

In traditional MMC topology, the arm current absolutely flows through the SM capacitor. However, in the proposed MIMC topology, the arm current from three phase legs flow through the CLLC ripple current elimination channels instead and converge at the common capacitor located on the secondary side. By applying the equation (10) to both phase B and phase C, it can be concluded that the vectoral sum of the three-phase fundamental and second order current is zero, as expressed in equation (13). That is to say, neither the original SM capacitor nor the common shared capacitor needs to conduct low frequency ripple current. As a result. the sizing of the SM capacitance only depends on the high frequency switching ripple, which consists of the original SM switching ripple and the newly introduced CLLC resonance frequency switching ripple. In conclusion, the required SM capacitance is greatly reduced compared to the traditional case.

$$i_{aC\_up}(t) + i_{bC\_up}(t) + i_{cC\_up}(t) = 0 \tag{13}$$

B. OPERATION PRINCIPLE OF PROPOSED MIMC MODULE

1) SM Structure: The SM in MIMC is required to have three major features: (1) high voltage isolation: the isolation is the key to form the claimed parallel connection, and the isolation level here is as high as the dc link voltage of the whole converter; (2) bidirectional power flow: the original capacitor current is a AC current, so the following stage needs to be able to conduct bidirectional current; (3) low switching loss: the additional conduction loss is unavoidable since the full current will flow through each additional switch on the path to the final capacitor, but the switching loss can be minimized by employing soft switching topologies. Therefore, a SM composed of the half bridge and the CLLC converter is developed and simplified schematic of which is shown in Fig. 4.

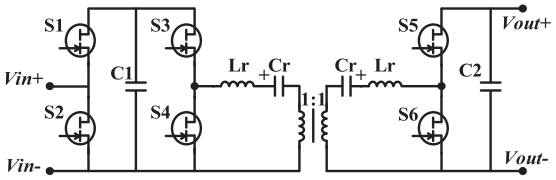

FIGURE 4. Simplified SM schematic.

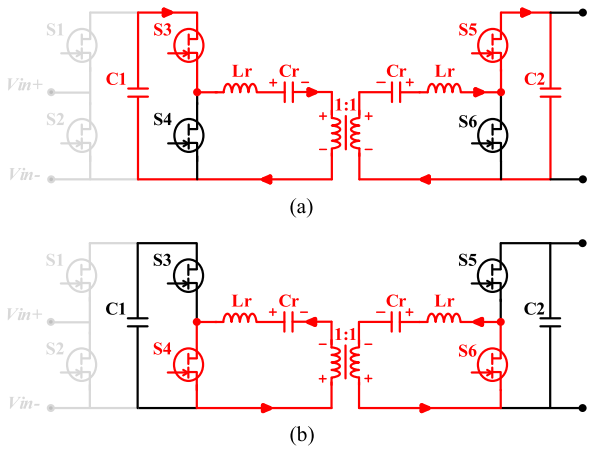

FIGURE 5. CLLC operation illustration schematic: (a) positive cycle (b) negative cycle.

The reason to select the CLLC converter as the isolation stage instead of Dual Active Bridge (DAB) is that CLLC/LLC operates at Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) at the same time, but DAB operates at ZVS with maximum current at turn-off [32]–[34]. In addition, there are two other major drawbacks of DAB. First, DAB loses the soft switching at light load because its load current is the main force to charge and discharge the junction capacitance. In the proposed topology, the dc link current after the first half bridge is equal to the original capacitor current, which is a pure AC value including fundamental and second order harmonic components. Therefore, the main ac current in the transformer will cross zero and stay close to zero for a long time. During this time, DAB will lose the soft-switching capability. Secondly, active phase angle control needs to be applied for all DABs to achieve bidirectional power flow as well as the gain adjustment. Therefore, the overall control becomes more complex. Moreover, the tradeoff between the phase angle and the switching loss needs to be considered, which means the energy transfer speed is limited. Compared to DAB, the ZVS in CLLC/LLC depends on the magnetizing current [36]. When operating under DCX mode, the load current is always zero during the dead-time. That's to say, the dc current profile deals no effect on soft switching on all load range. Another benefit of the DCX mode is the simplified control strategy. High frequency switching with fixed 50% duty cycle is sufficient to achieve the goal. Therefore, it is not necessary to be involved in the overall current control loops of MMC.

Among the resonant converters, CLLC is chosen over LLC because it features the symmetrical resonant architecture and symmetrical voltage gain curve in both power flow directions [37], [38]. As for CLLC converter, there are two types: Full-Bridge (FB) version and Half-Bridge (HB) version. Although the device current stress in FB is lower, the cost is the double switching devices. Another main issue is focused on the resonant capacitor. Half the SM capacitor voltage will drop on the resonant capacitor in HF-CLLC. In exchange, the winding voltage is also halved and lower the requirement on maximum flux density of transformer core. Therefore, the topology selection needs careful consideration. In the built downscaled prototype, the HF-CLLC is the preferred selection because of fewer switching devices, looser design of planar transformer and the comparable assembling of resonant capacitor bank [35].

2) CLLC Operation Principle: There are three GaN devices based half-bridges (HBs) in total. The first one follows the modulation command of normal MMC operation. The rest two HBs, together with two resonant tanks, form the bidirectional CLLC resonant circuit, in which a well-designed planar transformer is employed. The turns ratio of the transformer is set as 1:1 since the major task of the CLLC is bidirectional power transfer with galvanic isolation. In the HB version CLLC schematic shown in Fig. 5, the inverting switches S3 and S4 run at 50% duty cycle and 180° out of phase. On the secondary side, the S5 is synchronized with S3 while the S6 strictly follows the S4. There are generally two operation states as shown in Fig. 5. For the positive cycle, as the S1 and S3 are conducting, the resonant tank is kicked in and the resonant current increases in a sinusoidal shape. Since the switching frequency is set to be very close to the resonance frequency, the impedance of resonant tank can be regarded as zero. Therefore, the high-voltage square-waveform switching node voltage is applied on the magnetizing inductance and the induced magnetizing current increases in a triangular shape. The load current is carried by the resonant current and the power is transferred to the secondary side through the transformer. When transferred to the negative state, the S4 and S6 are conducting while the S3 and S5 are turned off. The resonant capacitor applies negative dc voltage on the primary winding. The resonant current is in a freewheeling mode and will not flow out. Therefore, the whole operation cycle demonstrates a half-wave rectification.

3) CLLC Transformer Design Guideline: For the CLLC resonant converter, the transformer design is very critical. High switching frequency introduces high core loss and winding loss. The planar transformer stands out for very high frequency applications ($\geq$500 kHz) because of some prominent merits [39], [40]. The PCB trace formed windings largely diminish the skin and proximity effects, which greatly reduced the ac winding loss. Unlike the Litz-wire wound transformer, better coupling minimizes the leakage inductance as well as the ac winding loss. Low-profile and high filling factor significantly improve the power density compared to the traditional design. Last but not the least, the easy fabrication

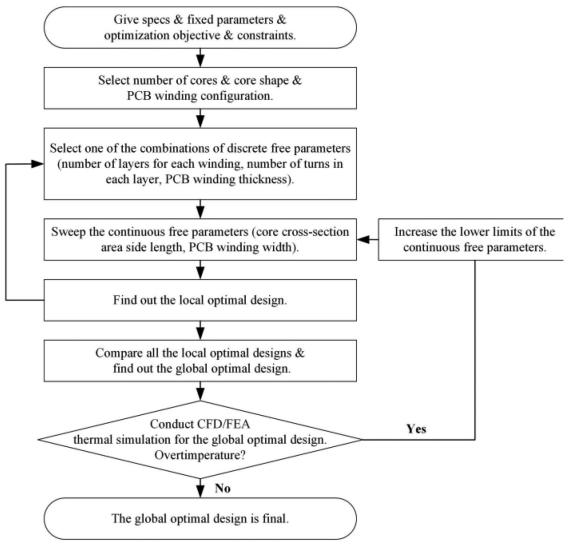

FIGURE 6. Generalized design methodology for high-power-density planar transformers [37].

and assembling process is also very important characteristics in modular design such as MMC. A comprehensive design methodology is fully explored in [37] and employed in the hardware development of proposed SM. The summarized flow chart of step-by-step design process is presented in Fig. 6.

First of all, the constraints for planar transformer design in proposed topology can be summarized as follows.

1) $B_{max} < B_{sat}$*:* The maximum flux density (B_{max}) determined by Volt-Second of transformer is normally much less than the saturation flux density (B_{sat}) of the core material.
2) $g < g_{max}$*:* The air-gap length (g) should be confined as well. If g is too large, the fringing flux causes more winding loss.
3) $J < J_{max}$*:* The current density (J) in the winding should be smaller than the maximum allowable current density (J_{max}). J_{max} is limited by the winding temperature rise.
4) *Insulation distance:* The two major concern in this part include the distance between two adjacent windings (δ_{ww}) and the distance between winding and magnetic core (δ_{cw}). Together with the number of turns, these two fixed parameters are closely related to iteration of effective window area calculation.
5) *Minimize* $L_{leakage}$: The leakage inductance ($L_{leakage}$) is not the priority here since an external inductor is employed. However, larger leakage inductance means stronger leakage magnetic field intensity, which can cause more ac winding loss.
6) *Minimize* C_{intra} *and* C_{inter}: Compared with traditional transformer, planar transformer has much higher winding stray capacitance, which may affect the soft switching. The high interwinding capacitance indicates larger common node noise crossing primary and secondary winding, especially in high voltage applications. Therefore, these two should also be minimized.

For the device selection in the half bridges, the voltage and current rating of the device is exactly the same as the front stage half bridge. For the resonant inductance and capacitance sizing, the guideline is to achieve the smallest possible leakage inductance, and then calculate the resonant capacitance according to the inductance. The reason is that the converter is working at DCX, so it doesn't require a certain ratio between the leakage inductance and the magnetizing inductance to form a gain curve that provides narrower frequency variation range to fulfill the voltage gain variation. Since the leakage inductance is formed inside the transformer, the leakage inductance should be sized as small as possible in order to reduce the loss of the transformer. In this case, the leakage inductance is calculated according to the specific winding structure which is discussed in later section III. In order to adapt to the non-ideal cases that the converter is not operating at exactly DCX, an external planar inductor is designed to provide the converter a gain variation range while operating in a reasonable switching frequency range.

In summary, the proposed MIMC module provides the capability for the parallel connection of the three phase modules. It features high efficiency and high-power density due to the employment of ZVS and planar transformer. However, the proposed MIMC still suffers from higher device power loss than the conventional MMC since the same current flows through more devices. Therefore, the utilization of MIMC and MMC is a trade-off between power density and the efficiency.

III. HARDWARE DESIGN CONSIDERATIONS

A. TRADITIONAL MMC SM CAPACITOR SIZING METHODOLOGY

In this subsection, an analytical method for calculation of minimum SM capacitance in HB-MMC is presented. The basic criteria considered in these calculations are maximum permissible repetitive voltage ripple and the required maximum converter voltage to avoid modulation in presence of dc bus ripple. Assuming that the circulating current is negligible, the stored energy in the arm converter can be expressed as:

$$\frac{dw_{Cup}}{dt} = -v_{up}(t)i_{up}(t) \tag{14}$$

$$\frac{dw_{Clow}}{dt} = -v_{low}(t)i_{low}(t) \tag{15}$$

Based on the mentioned arm voltage and current equation (1) (2) (3) (4), the time varying stored energy variations, for example the upper arm, can be derived. Combining the equation (9), an alternative expression for time varying energy ripple is further presented in (16):

$$\Delta w_{up}(t) = \frac{S}{12w}\left\{\begin{array}{l} 2\frac{M_1}{M_0}\sin(wt)\cos\varphi - \frac{1}{4}\frac{M_1}{M_0}\sin(wt+\varphi) \\ +\sin(2wt+\varphi) \end{array}\right\} \tag{16}$$

The SM capacitance selection must ensure that the energy variations do not produce excessive repetitive peaks. This

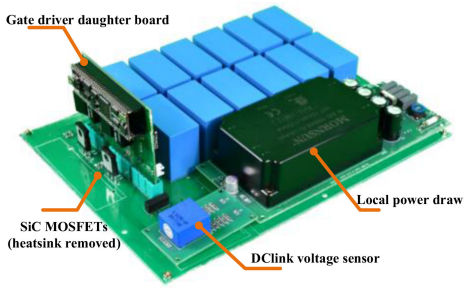

FIGURE 7. SM prototype of a 150kW traditional MMC system.

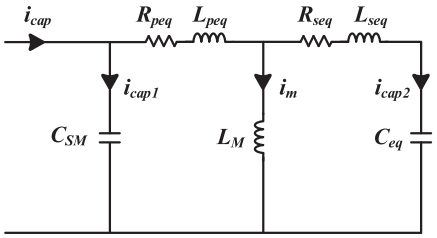

FIGURE 8. Simplified equivalent circuit model of SM-CLLC.

condition can be expressed in (17) via the stored energy decomposition:

$$\frac{1}{2}\frac{C}{N}V_c^2 + \Delta w_{up}(t) = \frac{1}{2}\frac{C}{N}V_{up}(t)^2 \tag{17}$$

From the instantaneous energy variation, the peak of the energy fluctuation can be found:

$$\Delta W_{\text{cmax}} = \max(\Delta w_{up}(t)) = \frac{1}{2}\frac{C}{N}V_{\text{cmax}}^2 - \frac{1}{2}\frac{C}{N}V_c^2 \tag{18}$$

The number of modules in HB-MMC can be calculated by:

$$N = \frac{V_c}{V_{\text{cnmodule}}} \tag{19}$$

In general, V_c equals to the dc bus voltage in HB based MMC configuration. $V_{cnmodule}$ is decided according to the switching devices voltage rating. The V_{cmax} in equation (18) is limited to be no more than k% of the V_c (the typical value of k% can be 105%–110%). Combining equation (18) and (19), the SM capacitance can be estimated as:

$$C > \frac{2N}{k^2 - 1}\frac{\Delta W_{\text{cmax}}}{V_{\text{cnmodule}}^2} \tag{20}$$

The SM capacitance sized in this way ensures that the dc bus voltage fluctuations are kept below the capacitor repetitive voltage rating and that sufficient voltage margin is provided in given operational conditions. However, it still needs to leave some margin in order to further increase the dc bus stiffness in case of large power system transients, load shading which are causes of large energy fluctuations.

By using the discussed capacitor sizing methodology, a standard HB-SM for a 150 kW traditional MMC platform is developed by authors and shown in Fig. 7. The bulky capacitor bank takes up almost 60% of the total volume of the whole SM, which verifies the huge influence of the capacitor size on the whole system volume.

B. SM CAPACITANCE SIZING IN PROPOSED MIMC

In traditional MMC topology, the major components in SM capacitor current are fundamental, second order harmonic and the high frequency SM switching ripple. Following the methodology mentioned above gives the required SM capacitance. However, this is no longer the case in proposed MIMC.

As discussed in Section II, the fundamental and second order harmonic get eliminated by the CLLC circuits. Therefore, the remaining current in SM capacitor is divided in following three parts: (1) The switching ripple of original SM. During the on period, the SM capacitor conducts the arm current and get charged. (2) The switching ripple of CLLC resonant tank. As the SM capacitor also forms the dc link bus of the CLLC stage, it provides the dc voltage applied on the transformer winding. Therefore, the sinusoidal resonant current flows through the capacitor and generate very high frequency voltage ripple. However, this part is dominated by the SM switching ripple. (3) Little low frequency ripple from arm current. Although this part ideally should be zero due to the current elimination, the actual hardware circuit of HB-CLLC is not perfect and behaves like a huge capacitor bank paralleled with SM capacitor, as shown in Fig. 8. Generally speaking, carefully designed and assembled CLLC circuits can maximize the C_{eq} and features several orders of magnitude difference between C_{SM} and C_{eq}. However, since the C_{eq} is close related to the physical circuit model, it is quite difficult to predict the accurate equivalent capacitance. According to actual experiments, few second-order harmonic ripple can still be observed on the SM capacitor, which dominates the switching ripple of CLLC resonant tank and SM. Therefore, it is quite necessary to leave enough margin when sizing the SM capacitance. Based on the experimental results, it is recommended to size the SM capacitance assuming 5% of original arm current still flow through the SM capacitor.

In conclusion, since almost all the low-frequency ripple is transferred to the CLLC stage, the major consideration of the SM capacitor selection should be absorbing the SM-HB switching ripple. However, the actual hardware circuit determines that the SM capacitance is still dominated by the few low frequency ripple flowing into the SM capacitor. Thus, appropriate margin when sizing the capacitance should be considered. Despite all the discussed concerns above, the SM capacitance is already significantly reduced.

C. SM CLLC RESONANT TANK AND TRANSFORMER DESIGN CONSIDERATIONS

As is known, the magnetizing current is the main charging/discharging current for the junction capacitor during the dead-time since the resonant current crosses zero at the device turn off moment. The biggest difference between the CLLC of MIMC and the traditional CLLC is that the flowing "load

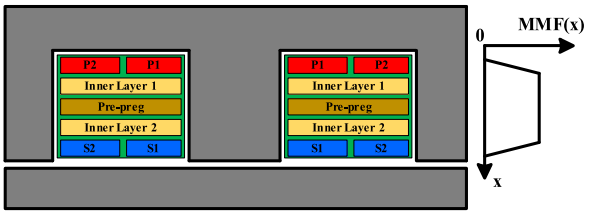

FIGURE 9. Winding structure of the planar transformer.

current", which is a mix of fundamental and second order harmonic currents. Thus, the envelope of the resonant current follows the shape of the "load current", which means the amplitude of the resonant current in the CLLC keeps changing. The detailed waveform will be shown in Section V. As a result, the load current for the CLLC can be as low as zero. At that moment, the junction capacitor energy needed in the soft switching will only be provided by the magnetizing current solely, which becomes a guideline for designing the magnetizing inductance. In summary, the peak magnetizing current needs to be able to fully charge or discharge the junction capacitors of switching devices.

In general, the sizing of leakage inductance is very important in some applications. However, it is not the first priority here due to two major reasons. First, an external inductor is employed to build the resonant tank. The excessive leakage inductance can be integrated in resonant inductance by flexibly adjusting the external inductor. Second, the isolation level between primary and secondary winding should be considered based on the whole dc bus voltage. This high isolation requirement enlarges the distance between the core and the winding as well as the distance between the primary winding and the secondary winding, which results in larger leakage inductance. Additionally, it is also preferred to minimize the inter-winding capacitance to reduce the induced common mode noise. Therefore, the interleaving winding structure, which is good for leakage inductance minimization at cost of higher inter-winding capacitance and short distance between two sides, is not adopted. Instead, parallel routing strategy is employed in the transformer design as shown in Fig. 9. Alternatively, the inner layer 1 and 2 can be set as shielding layer to further reduce the inter-winding capacitance.

As for the resonant tank, external inductors are employed to alleviate the thermal stress of the high-power-density planar transformer. For the design of independent resonant inductors, both the planar inductor and the Litz-wire wound inductor can be utilized. The low-profile less-labor-intense planar inductor is selected. The design and optimization of the planar inductor is very similar to the design of the planar transformer but two major differences. First, the maximum flux density (B_{max}) in a planar inductor is determined by the peak current rather than the volt–second. Second, uniformed current direction means no flux canceling between the adjacent turns in the inductor. Therefore, the number of turns for a planar inductor should be as few as possible to avoid the excessive ac winding loss.

TABLE 1. Key Parameters for CLLC Magnetics

Parameters	Values
Resonant frequency	500 kHz
Switching frequency	500 kHz
Operation mode	DCX
Planar transformer core material	E58/11/38-3F36
Planar transformer maximum flux density	80 mT
Turns ratio	1:1
Number of turns	2 (pri) ; 2 (sec)
Resonant tank inductor	1.15 μH
Resonant tank capacitor	88 nF

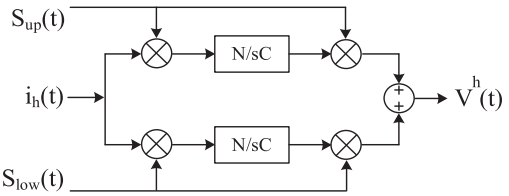

FIGURE 10. Arm converter voltage calculation diagram.

For the resonant capacitor, film capacitors and ceramic capacitors can be taken into consideration. The ceramic capacitors usually exhibit smaller size, lower equivalent series resistance, and higher corner frequency. Although the voltage rating of ceramic capacitors is limited compared to film capacitors, the selected half-bridge topology only utilizes half the capacitor voltage. Besides, the modularity of MMC enables lower voltage rating of single SM. Therefore, the voltage rating requirement of the capacitor is still significantly reduced. Meanwhile, multiple capacitors can be paralleled to reduce the thermal stress for each capacitor. Moreover, the capacitance value should be consistent under the operating temperature range. Eventually, the C0G/NP0 ceramic capacitors are employed in the design of proposed SM. The ultimate parameters of the resonant tank are also listed in Table 1.

D. ARM INDUCTOR SELECTION METHODOLOGY

To find the resultant voltage induced by a current harmonic in the circulating current, the arm current equation discussed before can be reshaped with following assumption, as shown in (21).

$$i_{up}(t) = i_{low}(t) = \sum I_h \cos(hwt + \varphi_h) \tag{21}$$

By repeating the calculation of arm converter voltage shown in Fig. 10, the ultimate expression of circulating current produced voltage is presented in (22):

$$v_h^h(t) = \frac{N}{2wC}\left(\frac{M_0^2}{h} + \frac{M_1^2}{2}\frac{h}{h^2-1} + \frac{M_3^2}{2}\frac{h}{h^2-9}\right) I_h \sin(h\theta + \varphi_h) \tag{22}$$

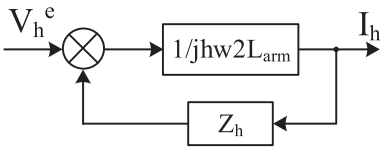

FIGURE 11. Block diagram between arm converter voltage and current.

Therefore, the impedance of the arm converter can be derived:

$$Z_h = \frac{V_h^h}{I_h e^{j\theta_h}} = \frac{N}{2jwC}\left(\frac{M_0^2}{h} + \frac{M_1^2}{2}\frac{h}{h^2-1} + \frac{M_3^2}{2}\frac{h}{h^2-9}\right) \tag{23}$$

From this result, it can be concluded that the arm converter behaves as a capacitor. The equivalent capacitance depends on SM capacitance, number of SM per arm and operation condition of MMC such as M_0, M_1. As the third order harmonic injection generates limited effect, the equation (23) can be further simplified as presented in equation (24):

$$Z_h = \frac{N}{2jwC}\left(\frac{M_0^2}{h} + \frac{M_1^2}{2}\frac{h}{h^2-1}\right) \tag{24}$$

The equivalent impedance of one phase leg is equal to the sum of Z_h and the impedance of two arm inductors. The major harmonic voltage in the phase leg generated from the fundamental frequency arm current is the ac component in the $V_h{}^e$ in equation (12). If involving the arm inductor, the related block diagram of whole phase leg can be derived as shown in Fig. 11.

According to the block diagram, the related transfer function is then presented in (25):

$$\begin{aligned} I_h &= \frac{V_h^e/(jhw2L_{arm})}{1 - \frac{N}{4w^2hL_{arm}C}\left(\frac{M_0^2}{h} + \frac{M_1^2}{2}\frac{h}{h^2-1}\right)} \\ &= \frac{V_h^e}{1 - \frac{N}{w^2L_{arm}C}\frac{2(h^2-1)M_0^2 + h^2M_1^2}{8h^2(h^2-1)h}} \end{aligned} \tag{25}$$

The denominator in (25) sends out a message that the circulating current harmonics can get very high value regardless of the excitation voltage in case when the following condition is met:

$$1 - \frac{N}{w^2L_{arm}C}\frac{2(h^2-1)M_0^2 + h^2M_1^2}{8h^2(h^2-1)h} = 0 \tag{26}$$

Therefore, to prevent the resonance, the arm inductor along with the arm capacitance should be carefully sized so that:

$$L_{arm}C > \frac{N}{(hw)^2}\frac{2(h^2-1)M_0^2 + h^2M_1^2}{8(h^2-1)} \tag{27}$$

To reduce the passive size, the inductor can be sized for h = 4. Meanwhile, the second harmonic circulating current can be suppressed using the circulating current control of the converter.

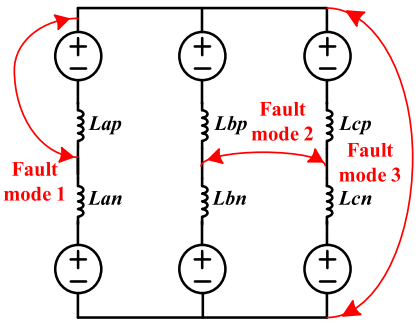

FIGURE 12. Short circuit fault modes of MMC.

Besides the circulating current suppression, inrushing current limitation during the dc fault is another tough task of arm inductor. Three general possible fault modes of MMC are shown in Fig. 12. Aimed at these fault cases, different equivalent circuit models can be derived to help determine the required inductance to limit the huge surge current. Theses short circuit loops may involve single arm inductor or both of them and the related equations the fault current di/dt in three fault cases are listed in equations (28) to (30). Therefore, the required inductance that can achieve mild fault current change slope can then be determined, which should be able to cover all three cases. This value is then compared with the one got from equation (27) and the larger one becomes the ultimately optimized inductance selection.

$$\text{Mode 1: } \frac{di_{sc1}}{dt} = \frac{\frac{V_{dc}}{2} + \sqrt{\frac{2}{3}}V_{LLrms}}{L_{arm}} \tag{28}$$

$$\text{Mode 2: } \frac{di_{sc2}}{dt} = \frac{\sqrt{2}V_{LLrms}}{L_{arm}} \tag{29}$$

$$\text{Mode 3: } \frac{di_{sc3}}{dt} = \frac{V_{dc}}{2L_{arm}} \tag{30}$$

E. ARM INDUCTOR SELECTION FOR MIMC

In proposed MIMC topology, major components of the circulating current, such as second order and forth order harmonics, are transferred from phase legs to the CLLC channels and get eliminated. As a benefit, almost zero voltage fluctuation can be observed on the SM capacitor voltage. Therefore, the dc bus voltage expressed in equation (12) becomes a constant value as presented in equation (31), which induces zero ripple on arm inductor.

$$V^e(t) = \frac{N}{wC}\frac{I_aM_0M_1}{8}\sin(\varphi) \tag{31}$$

Apparently, the sizing of arm inductance no longer depends on the circulating current. However, the inrushing current limitation during the dc fault is still indispensable in the proposed MIMC since the new configuration inherits the fault mode considerations and related equations in traditional MMC. Therefore, arm inductor sizing for inrushing current limitation is the same as that in conventional topology.

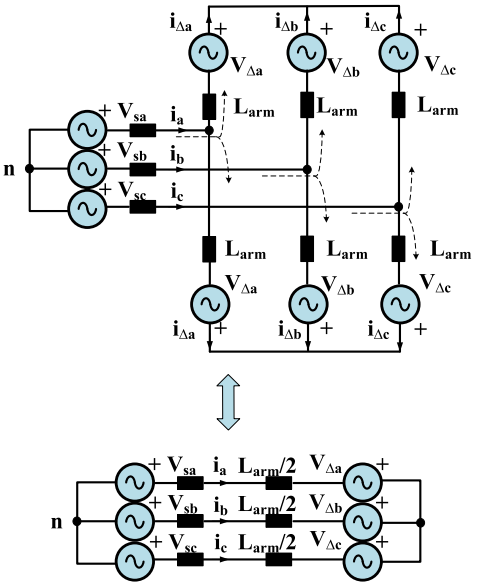

FIGURE 13. Equivalent scheme for differential asymmetric components.

In conclusion, the sizing of arm inductance in the proposed MIMC topology mainly depends on the requirement of dc fault current suppression because the low frequency circulating current is either eliminated or transferred in proposed MIMC.

IV. CONTROL ALGORITHMS

A. DECOMPOSITION OF ARM CURRENTS IN MIMC

In traditional HB-MMC, there are six arm converters. The arm currents are composed of a complex mixture of the ac side three phase currents, dc link current and circulating currents flowing internally within the converter structure. Due to mutual interconnections, each arm converter voltage affects the current of all converters and external ports. To achieve precise control of power exchange between the ac grid and dc link as well as energy balance among the submodule capacitors, it is of interest to decompose the original arm current into several new components attributed to particular power exchange.

The six converter arm currents can be split into five new components which are classified in following three types according to the path they are flowing in. (1) Asymmetrical or differential mode current space vector (two independent components, flowing in opposite directions in upper and lower arm converters) related to the grid current and exchange of energy between the arm converters and ac grid. (2) Symmetrical or circulating mode current space vector (two independent components, flowing in same direction in upper and lower arm converters) which is related to internal current power exchange between phases/arms. (3) Common mode current (single component) related to the dc link current and power exchange between the arm converters and the dc link.

The differential mode current vector is driven by an arm voltage space vector demonstrated in Fig. 13.

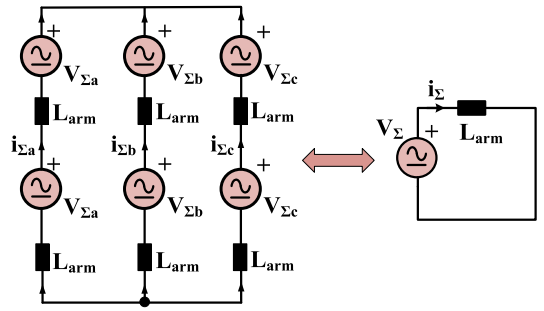

FIGURE 14. Equivalent scheme for circulating (symmetrical) system.

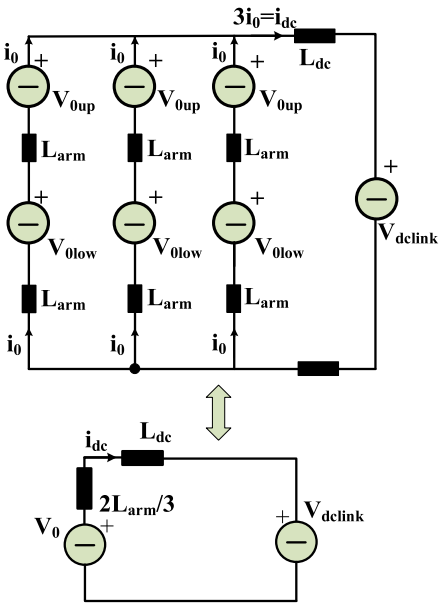

FIGURE 15. Equivalent scheme for the common mode system.

The symmetrical (circulating) mode current space vector can be calculated as:

$$I_\Sigma = \frac{i_{up} + i_{low}}{2} \tag{32}$$

$$V_\Sigma = \frac{v_{up} + v_{low}}{2} \tag{33}$$

These new vectors are called symmetrical mode vectors as they act is same directions in the upper and lower arms. As the consequence these current components constituting this vector are circulating within the converter. The circulating current and voltage vectors can be mutually interlinked via the equivalent circuit shown in Fig. 14.

In normal operation the circulating currents may have complex spectrum, dominated by the dc component, fundamental and second harmonic. The circulating currents should be ideally suppressed to zero. But they play a crucial role in transfer of energy between the arms and thus they should be carefully controlled in order to maintain arm dc bus voltages.

Fig. 15 presents the equivalent scheme for the common mode current and voltage. The common mode voltage/current

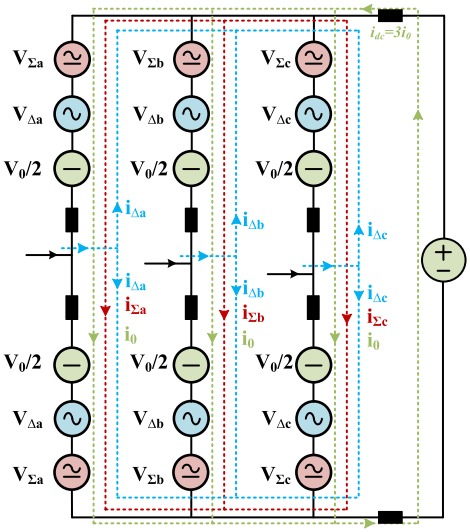

FIGURE 16. Equivalent circuit model of MMC.

component is responsible for building of the dc link voltage across the converter dc terminals and building the total dc current. The common mode voltage and current components are identical in all arms. As the consequence, the common mode sub-system is fully decoupled from the asymmetrical and symmetrical sub-systems.

Combining the driving voltage for the differential mode, common mode and circulating current components discussed above, an integrated equivalent circuit model can be derived as presented in Fig. 16. The addition of the three equivalent voltages will become the voltage command for the arm converter.

B. MMC INNER CURRENT CONTROL LOOPS

As discussed in previous Section A, the references for current control loops are already generated from the energy loops. The next thing is to find the appropriate circuit model to provide the plant for different current control loops. The equivalent circuit model shown in Fig. 16 tends to be the chosen one to illustrate MMC inner current control loops. The individual loops between each current and its corresponding voltage are already illustrated in Fig. 13-15. In the Fig. 16, each arm converter is replaced by three controlled voltage source which are responsible to their corresponding current components.

1) DC Current Control Loop: Each phase leg of MMC is modulated to generate required output power. That is to say, all the SM capacitors are inevitably discharged to provide the output power and thus the voltage will keep dropping without supplement. Therefore, the dc bus needs to inject sufficient dc current into these SMs to charge these capacitors and pull the reduced SM voltage back to its nominal level. The reference comes from the discussed total energy loop and a voltage feedforward of rating dc bus voltage is implemented.

2) Output Current Control Loop: The output current mainly comes from the fundamental component of arm current. The whole control is transferred to d-q frame and the PLL block is utilized to synchronize with the grid. The current reference in d-axis and q-axis control the real and reactive power, respectively.

3)Circulating Current Control Loop: The undesired circulating current increase the peak/RMS value of the arm current, which consequently increases the rating of devices, device power losses, and the SM voltage ripple. Although well designed arm inductors help suppress the circulating current, precise control strategy is the essential method to thoroughly solve the problem. The primary goal of circulating current control is to limit the pulsating second and forth order harmonics in the arm converter, which are the major components in arm current. The added arm inductors provide control freedoms for all six arms. A PR controller based integrated controller are utilized to help suppress or reshape the circulating current.

Ultimately, the complete control diagram is summarized and shown in Fig. 17.

C. CAPACITOR VOLTAGE BALANCE CONTROL

The SM capacitor voltage balance control is involved to ensure that the stored energy is equally distributed in all the SMs. On the other word, each SM capacitor voltage is regulated at the same value. This means a lot for the MMC to achieve low THD and high power-quality. A selection mechanism based on SM capacitor voltage measurement and current direction detection is employed at each switching cycle. Thus, the SM capacitor voltages of each arm is sorted and wait the central controller to choose which SMs to be inserted or bypassed [41], [42].

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed MMC topology with ripple current cancellation stages has been verified using PLECS simulation tool. The general operation performance has been demonstrated. The current waveforms at different positions of the module are fully investigated. Besides, a downscaled laboratory prototype is also built to realize the proposed topology and demonstrate the claimed benefits. The parameters for both the simulation and the hardware platforms are listed in Table 2.

A. SIMULATION VERIFICATION

In the simulation study, the circuit exactly follows the schematic described in Section II and supplies a three-phase RL load. Meanwhile, a comparison between the traditional MMC and the proposed one has been conducted in the simulation. The basic operation waveforms of the traditional MMC topology are shown in Fig. 18. At one point, the simulated topology will switch from MMC to MIMC. The basic operation waveforms of the proposed MIMC are shown in Fig. 19. The dynamic waveform when switching between these two topologies are presented in Fig. 20.

The two major differences between the waveforms of MMC and MIMC are: (1) MMC's capacitor voltage contains large

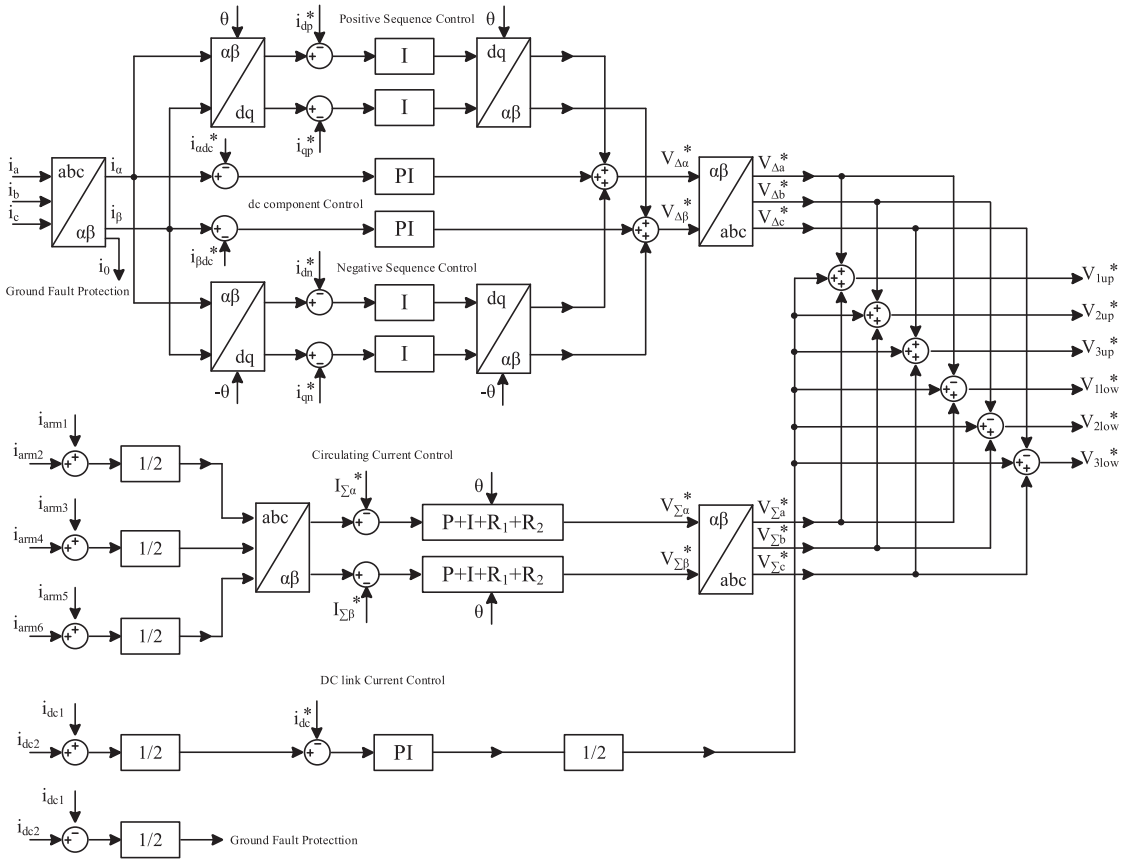

FIGURE 17. **Integrated control strategy. Not all blocks which are implemented in controllers are demonstrated in the figure, such as feed-forward, decoupling blocks, output limiter and anti-winding up.**

TABLE 2. **Key Parameters of Proposed MIMC**

Parameters	Simulation	Experiment
Rated power	55 kW	4.8 kW
Dc-link bus voltage	2.2 kV	400 V
Rated ac current amplitude	42 A	10 A
Number of SMs per arm	3	2
SM capacitance*	1 mF / 1 μF	240 μF / 10 μF
Nominal SM capacitor voltage	740 V	200 V
SM switching frequency	20 kHz	20 kHz
Common linked capacitor	1 μF	100 μF
Arm inductance	5 mH	2 mH
Nominal fundamental frequency	60 Hz	60 Hz

*Since the comparative tests are conducted for the traditional MMC and proposed MMC, two different sets of SM capacitor bank need to be prepared. The value on the left is the capacitance required in traditional MMC topology while the right one is for the proposed topology.

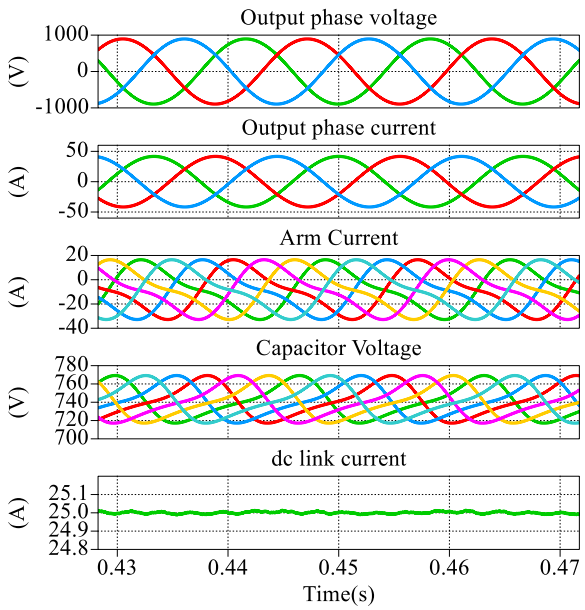

FIGURE 18. **Simulation results of the traditional MMC.**

fundamental and second order harmonics, but MIMC's capacitor voltage is almost only formed of dc component; (2) MMC's arm current contains significant second order harmonic, but MIMC's arm current has very little harmonics. It demonstrates that the low frequency currents from adjacent arms successfully converge at the common capacitor and cancels each other. The arm current, which supposes to flow through the SM capacitor, run all the way into the CLLC channels instead. The flat dc voltage and the switching function

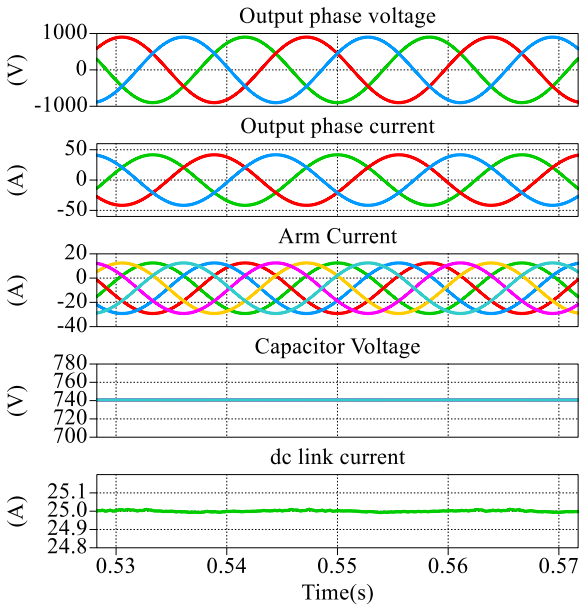

FIGURE 19. Simulation results of the newly proposed MIMC.

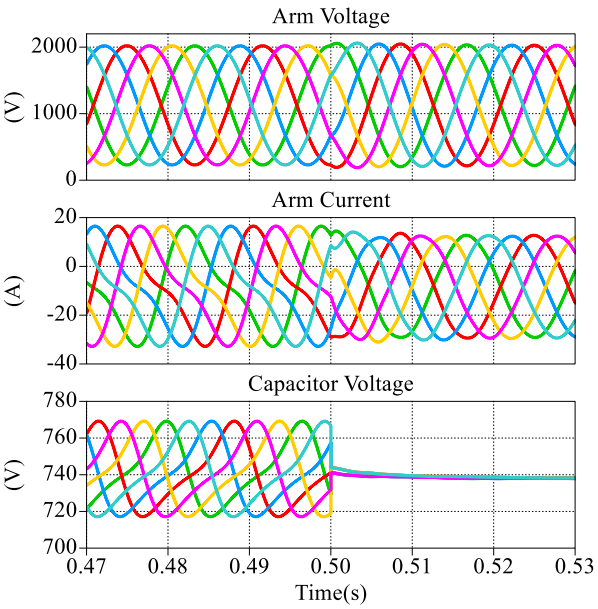

FIGURE 20. Simulation of topology switch from traditional MMC to the newly proposed.

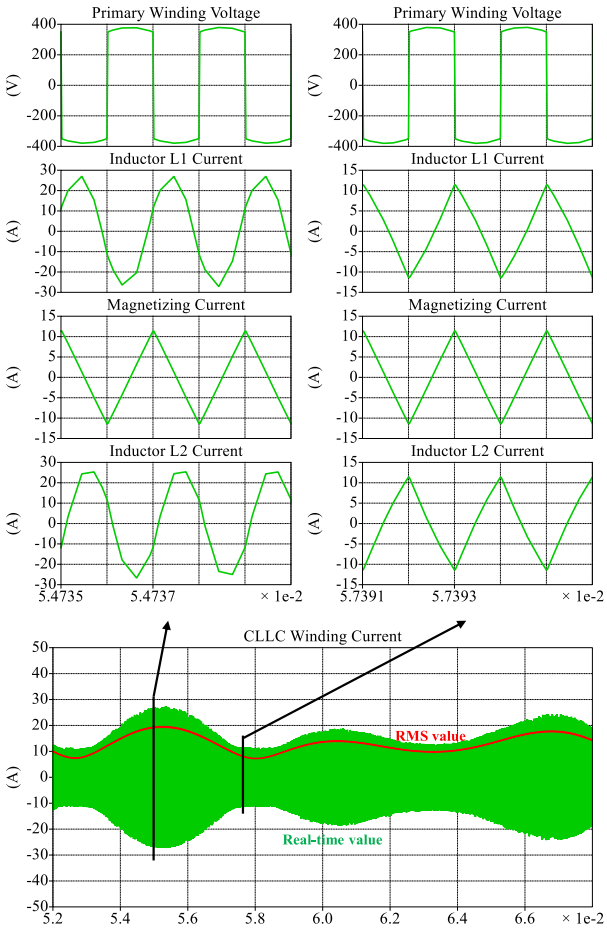

FIGURE 21. Simulation results of CLLC resonant circuit.

also will not generate second order current in the arm as well. As SM capacitance are the same in the simulations for both topologies, a perfect flat dc voltage can be observed on the SM capacitor in MIMC. Actually, the SM capacitance in MIMC can be sized much smaller.

The current detail in the CLLC current cancellation stage is also demonstrated in Fig. 21. Ideally, all the original fundamental and second-order harmonic capacitor current flows through this channel. From the current profile point of view, the magnetizing current presents a high-frequency triangular waveform while the resonant current appears to be a high-frequency sinusoidal waveform with changing amplitude, the envelope of which is formed by the low frequency ripple current. Since the SM capacitor is also involved in the resonant loop, the high-frequency ripple current flowing through the capacitor also follows the envelope. But the difference is that it is disconnected from the resonant loop during the negative resonant cycle. Therefore, the ripple current profile becomes a chopped high-frequency ac waveform.

Besides the RL load, the motor drive load is also simulated. The start-up process in the simulation is shown in Fig. 22, in which the fundamental frequency ramps up from 0 Hz to 60 Hz. The arm current presents a perfect sinusoidal and the SM capacitors keep zero low-frequency voltage ripple even when the frequency is close to zero. With the same capacitor, the MIMC can run from zero frequency to high frequency while keeping the output voltage and current always a perfect sinusoidal waveform. The benefit is significant compared to conventional MMC. The desired capacitance in MMC is reverse proportional to the output frequency. Ideally, it cannot start up from zero frequency. To avoid bulky capacitor, a high frequency current injection method is used to start up the MMC from zero frequency. However, it introduces large

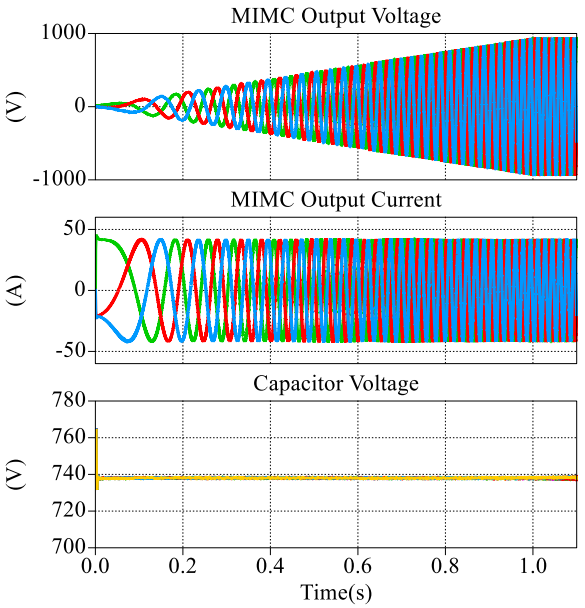

FIGURE 22 . Simulation of motor drive startup process using proposed MMC topology.

additional loss to the converter. A tradeoff analysis between size and efficiency will be conducted and the capacitor will be sized at a certain low frequency close to zero. Therefore, the capacitor size will be two or three times larger compared to that in grid-connected application. However, the capacitance in MIMC is independent from the system operation frequency. It is only sized to absorb the switching frequency ripple in SM. The capacitance will keep the same when operation frequency increases from low to high. At the same time, the capacitor voltage will always present negligible low-frequency harmonics. Therefore, in variable speed drive application, the proposed MIMC presents a significant reduction on the capacitor size compared to the traditional MMC.

B. EXPERIMENTAL RESULTS

The developed SM prototype is shown in Fig. 23 and the related operation waveforms of the CLLC are demonstrated in Fig. 24. The Fig. 24(a) is a zoom in session while the load current is zero. This happens when the load current flowing through the CLLC crosses zero. As discussed before, the load current of the CLLC is ac current that equals to the original capacitor current in the traditional MMC. In Fig. 24(a), V_{gsLS} represents the gate-source voltage of the low side switch; V_{dsLS} represents the drain-source voltage of the low side switch; $V_{primary}$ represents the voltage on the primary winding; $I_{primary}$ represents the current in the primary winding. The waveform of V_{gsLS} and V_{dsLS} during the dead-time demonstrates the ZVS operation. The winding current $I_{primary}$ now equals to the magnetizing current and presents as a triangular waveform. During the dead-time period, the magnetizing current reaches the peak value and helps charge and discharge the junction capacitor to achieve the ZVS. This

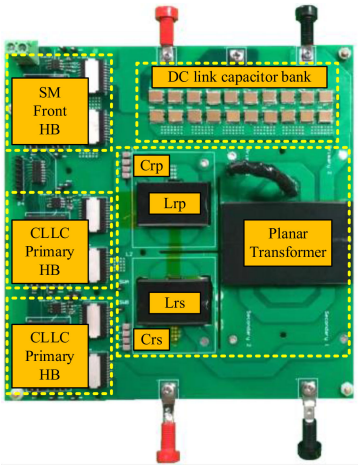

FIGURE 23. Newly proposed SM prototype of proposed MIMC.

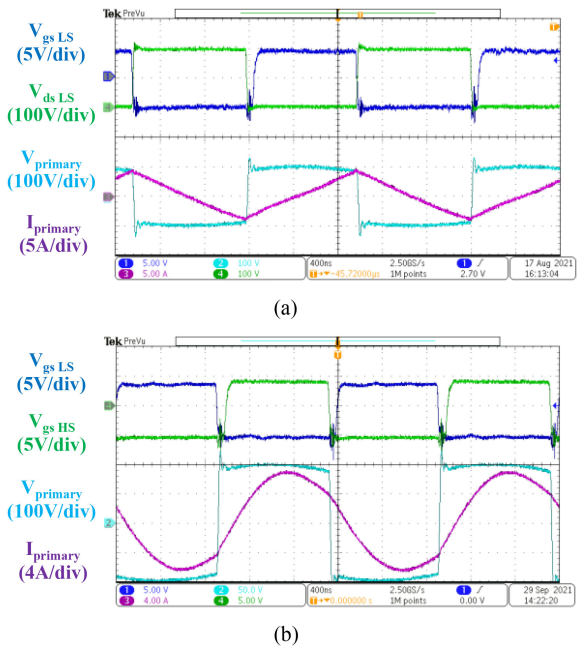

FIGURE 24. Basic operation states of CLLC circuit. (a) Primary side HB switching state when load current crosses zero; (b) Primary side HB switching state when load current is not around zero.

peak value can be adjusted by changing the magnetizing inductance to guarantee the ZVS of the HB-CLLC under all load range. Fig. 24(b) shows the waveforms when the load current is not around zero. When the current flows into the HB-CLLC channel, it gets modulated and shaped into a high-frequency sinusoidal resonant current by the resonant tank. At this time, the winding current becomes the combination of triangular magnetizing current and sinusoidal resonant current. The load current becomes zero at each turn on/off transient and the ZVS is always implemented by the magnetizing current.

A downscaled hardware platform of the proposed MIMC rated at 4.8 kW with 2 SMs per arm has been built and tested in the lab, as shown in Fig. 25. The experiment results with

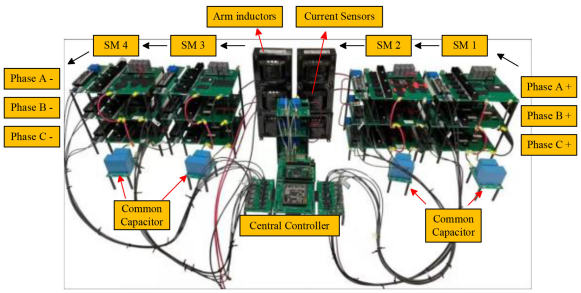

FIGURE 25. Downscaled 4.8 kW MIMC prototype.

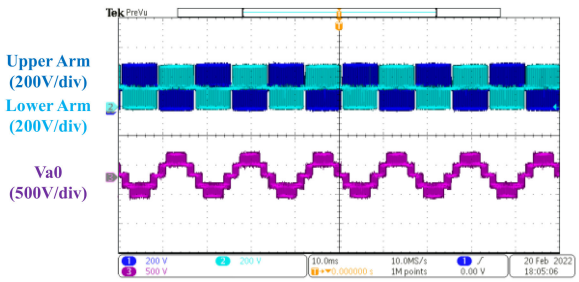

FIGURE 26. Phase leg voltage performance.

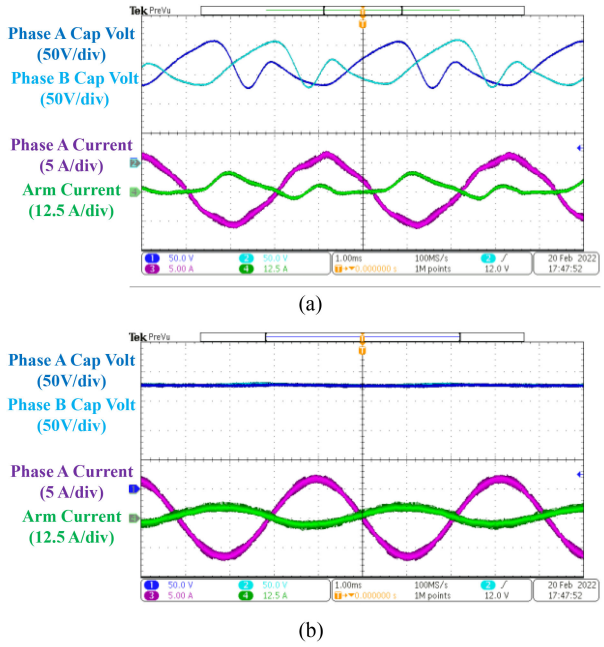

FIGURE 27. SM voltage fluctuation and arm current performance comparison between (a) the traditional MMC and (b) the newly proposed MIMC at 60 Hz.

three-phase RL load are obtained and shown in Fig. 26 to Fig. 30. The detailed specifications are listed in Table 2.

Fig. 26 shows the zoomed-out arm converter output voltage for upper and lower arms of phase A, and the output phase voltage V_{a0} at the middle point of the phase leg. The envelope of the PWM arm voltage is shown as a very flat square waveform, which verifies that the capacitor voltage in the module has no low frequency fluctuation, as claimed in the previous sections. The switching node voltage V_{a0} presents a very perfect sinusoidal multilevel waveform, which verifies that there is no second order harmonic voltage in the arm, as claimed before.

In order to present a more intuitive difference between the proposed MIMC and traditional MMC, the steady state performance of arm current and capacitor voltage for both topologies under same test conditions is shown in Fig. 27. 80 μF capacitor is used for MMC but only 20 μF capacitor is used for MIMC. The Fig. 27(a) presents the waveforms for the traditional MMC while the Fig. 27(b) presents the waveforms for the proposed MIMC. In each single plot, the upper two waveforms demonstrate the capacitor voltage of adjacent SMs in phase A and B. The following features can be observed: (1) the capacitor voltage in MMC has large fundamental and second order harmonic current of which the peak-to-peak value is nearly 40% of the rated voltage; but the capacitor voltage in MIMC is perfectly flat with negligible harmonics. Moreover, the capacitance in MIMC is only 25% of the capacitance in the MMC. (2) the arm current in MMC has significant low frequency harmonic distortion, but the arm current in MIMC contains very little harmonics. (3) the THD of the output current in MMC is much higher than the MIMC. These results verify the claimed benefits of MIMC over MMC: much smaller capacitance is needed to generate low THD output voltage and current.

With the amazing experimental results at 60 Hz as a basis, the experiments are further extended to variable frequency operation. Before conducting the tests, the SMs capacitance is increased to 240 μF in the MMC topology to stand huge voltage ripple under very low output frequency. But for the proposed MIMC topology, the SM capacitance is further reduced to 10 μF to demonstrate its prominent performance. The experimental waveforms of variable frequency operation are shown in Figs. 28–30. In each figure, the upper figure shows the capacitor voltage in three phases of the MMC converter; the lower figure shows the capacitor voltage in three phases of the MIMC converter. Figs. 28–30 show the results at output frequency equal to 30Hz, 15 Hz and 7 Hz respectively. At 30 Hz, MMC's capacitor voltage presents a 33% peak to peak voltage ripple, but MIMC's capacitor voltage presents only 4% peak to peak voltage ripple. At 15 Hz, the MMC's ripple quickly increases to 65%, but MIMC only goes up to 8%. At 7 Hz, MMC's ripple becomes as significant as 115%, but MIMC still keeps as low as 10%. As the MIMC hardware is not a perfect circuit model, a few low-frequency current components still flow into the SM capacitor and introduce this 4% to 10% ripple. It is also noted here SM capacitance in MMC is 240 μF but that in MIMC is as small as 10 μF. When system operation frequency decreases, the SM capacitor voltage ripple MMC increases linearly and exceeds the requirement in normal operation. Thus, larger capacitor needs to be installed to maintain the voltage ripple within 20%. It means a capacitance of 1440 μF is expected at 7 Hz. However, a 10 μF capacitance which is only 0.7% of the MMC

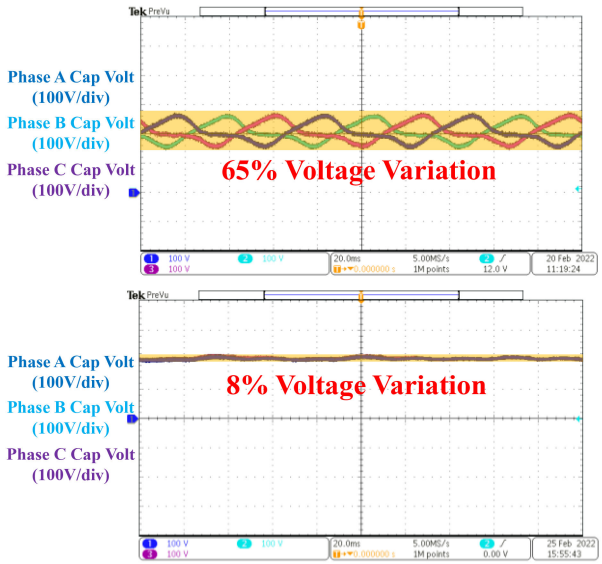

FIGURE 28. SM voltage fluctuation in three phase legs at 15 Hz.

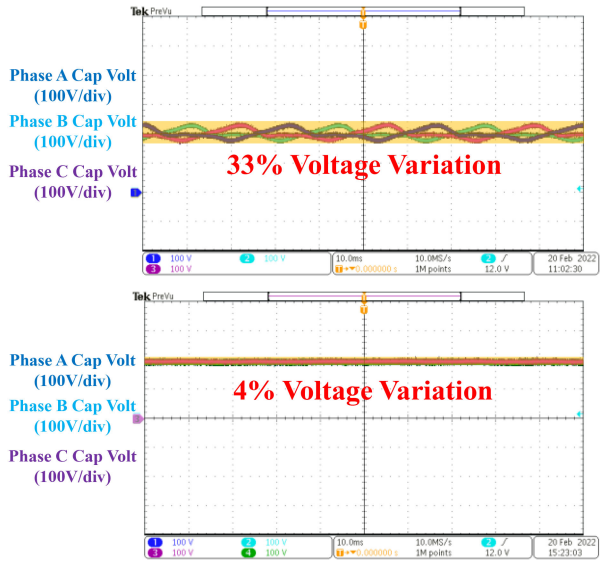

FIGURE 29. SM voltage fluctuation in three phase legs at 30 Hz.

capacitance can maintain 10% peak-to-peak voltage ripple in MIMC. It demonstrates that the capacitance can be reduced by almost one hundred times, and the capacitor size is estimated to be reduced by nearly ten times.

VI. CONCLUSION AND FUTURE WORK

In MMC, the side-effect of using distributed half-bridge modules to support the DC link instead of using series connected capacitor is the fundamental frequency energy ripple on the capacitor. To generate an arm voltage with low THD, a big capacitance needs to be used to suppress the ripple. In variable frequency operation, the capacitance is inversely proportional to the frequency. In order to reduce the capacitor size, the energy ripple cancellation technique through connecting the modules in three phases in parallel is adopted. Connecting

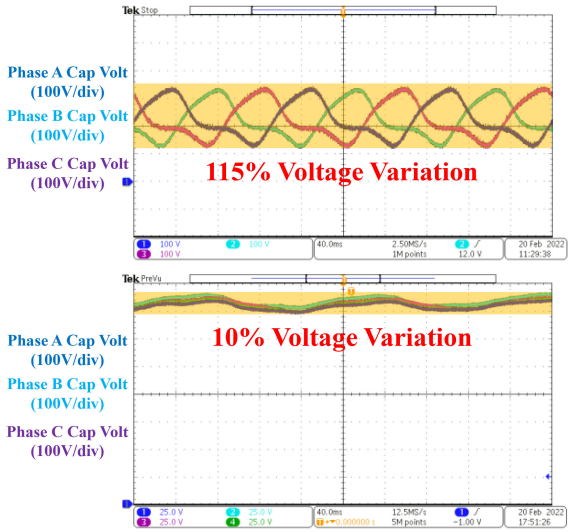

FIGURE 30. SM voltage fluctuation in three phase legs at 7 Hz.

the modules at different voltage potential together requires the module to be equipped with isolation. Therefore, an isolated half-bridge module is proposed to replace the original half-bridge module. By using the proposed MIMC topology, the capacitor size and the inductor size can be significantly reduced, which has been demonstrated through simulation and down-scaled experiments.

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