IEEE Open Journal of
Power Electronics

Received 18 February 2022; accepted 12 March 2022. Date of publication 16 March 2022;
date of current version 13 April 2022. The review of this article was arranged by Associate Editor Gab-Su Seo.

Digital Object Identifier 10.1109/OJPEL.2022.3160049

Isolated Flying Capacitor Multilevel Converters

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ABSTRACT This paper presents the topology known as the isolated flying capacitor multilevel flyback converter (FCMFC). The topology uses isolated flying capacitors (FC) for high-gain, DC-DC power conversion while maintaining primary-secondary isolation and improving the efficiency and capability of a standard flyback transformer circuit. Three converters have been developed and tested, one flyback as a control, a 3 level FCMFC, and a 4 level FCMFC to prove the gain and efficiency benefits of this new topology. The FCMFC prototypes achieve higher gain and efficiencies relative to a flyback design utilizing the same off-the-shelf transformer. The stress of the input and output switches is reduced because of the fractioning of the output voltage across multiple output stages, allowing future iterations to utilize lower-rated components. The operating parameters are 5V to 40V boosting for a 10W load at 250kHz. Utilizing the same semiconductor components, the flyback converter control prototype achieves 78% efficiency while the proposed FCMFC converters reach 85% and 82% efficiency, even with the added isolated power, gate drive, and bootstrap circuitry. The FCMFCs have a multiplying effect on the gain of the traditional flyback which also increases near the 90% duty cycle flyback threshold. Additional testing was done at light load and at 100kHz, 250kHz, 452kHz, and 500kHz.

INDEX TERMS Flyback, flying capacitors, multilevel, voltage boost.

I. INTRODUCTION

Direct current (DC) is a staple of the modern world. Not only is an ever-increasing majority of our loads powered with DC, but so are our renewable energy sources with photovoltaic energy in particular being DC. The power is processed using power electronics that can convert one DC voltage to another and then eventually invert that into usable AC power. A significant portion of that AC power will be rectified back to DC for use in consumer electronics such as televisions, gaming stations, cell phones, or even LED lighting. Power conversion using DC-DC converters is an expanding field that continuously demands smaller and more efficient products. The applications span from small implantable medical devices to renewable energy integration, to microgrids, all the way up to industrial power supplies and transportation [1], [2]. High frequency, flying capacitor multilevel (FCML) converters have been developed to maximize power density and efficiency. Flying capacitors (FC) have been used to enhance the capabilities of basic power electronic topologies such as the multilevel boost converter [3]. The multilevel structure spreads voltage gain across individual switching cells containing the FC and the benefits include increased efficiency, lower device stress, and higher power density [4]. Multilevel structures have also been implemented for the buck [4], [5] and buck-boost [7] converters with correspondingly high efficiencies. Until now, this technique has not been combined and proven with the flyback converter.

Flyback topologies are widely utilized for their low cost and high versatility in power conversion, boasting a wide input and output voltage range of operation [8], [9]. The flyback converter is a good candidate for high step-up voltage conversion that has the added benefit of electrical isolation. The flyback is a popular isolated converter for renewable applications but can suffer significant switch and diode stress, limiting its use [10]. Active clamp switching schemes are utilized to lower the stress on the primary switch that requires advanced control techniques to achieve zero-voltage/current switching for example [11], [12]. These active circuits work well to reduce primary FET stress but FCMFC does this inherently by utilizing the secondary flying capacitor voltage cells to reduce

the primary reflected voltage. Utilization of the proposed multilevel flying capacitor variation expands the power potential of this converter because of the decreased stress and increased efficiencies.

To achieve high voltage gain for new applications using flyback converters, designers utilize a high turns ratio [13], [14]. This requires detailed custom magnetic design and still yields high-stress ratings for the primary FET and secondary output diode. Transformers are often custom-made for a particular purpose, but many off-the-shelf options exist and can be utilized in an FCMFC structure to cover a broader application range than what a simple flyback could cover. This is made possible by the increased voltage gain and reduced primary FET stress of the proposed topology. Modifications to the flyback converter using boost converters and other voltage multipliers are also common in this space [15]–[19]. Modified boost converters are also utilized [20] but with limited gain. All the modified flyback converters will use a moderate turns-ratio and get the remaining gain from a separate converter stage, increasing control system complexity. The FCMFC can achieve high voltage gain using a phase-shifted pulse width modulation scheme for the switch-diode-capacitor (SDC) secondary side stages. FCMFCs have the benefit of increased voltage gain with additional stages independent of transformer turns ratio. In other FC topologies, gain is not directly dependent on the number of stages [3], [4]. This work proves that adding one flying capacitor stage will double the available voltage gain of the standard flyback converter, two will triple the gain and this trend continues for higher-order FCMFCs which also allows the main input switch to operate at lower duty cycle and stress compared to a flyback converter. For a given transformer and duty cycle, the proposed topology will always have double, triple, etc. the gain of any flyback converter and thus allows for more capability to be derived from existing flyback topologies.

Challenges arise with multilevel converters, particularly balancing the FC voltages. Voltage imbalance comes from variance in component values and gate triggering time delays, an issue that is exacerbated with higher-level converters. While some converters experience some natural balancing, any variation directly hinders the lower component stress requirements. Control methods have been developed to solve this issue and prevent the premature failure of an individual stage. Natural balancing has been achieved by varying the switching scheme [21]. Active balancing has been achieved through value valley current detection and a constant effective duty cycle to account for the light load condition [22]. This work presents the FCMFC and shows that it achieves natural flying capacitor voltage balance with *open-loop* phase-shifted pulse width modulation (PSPWM), which is key to the reduced voltage stress seen by the semiconductor devices.

A generalized FCMFC is shown in Fig. 1 with a single SDC stage outlined. Note that this is not a conventional voltage multiplier but a flying capacitor structure interfacing with the flyback converter. Multiple converters can be derived from this general form for N levels where (N-1) is the number of

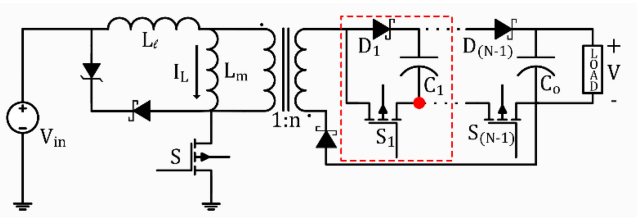

FIGURE 1. Flying capacitor multilevel flyback converter general form.

capacitors of a given converter. The double wound inductor ("*transformer*") provides for higher gain capability but is not the focus of this work. A higher turns ratio can be used to achieve more gain at the expense of increased voltage and magnetic stresses. This work derives an alternative way to increase gain which (1) will always be superimposed on the existing gain derived from the double wound inductor, (2) minimizes custom magnetic design, and, thus, (3) efficiency improvement can be focused on the secondary stage rather than the magnetics. Work has been done to explore the magnetic design in relation to flying capacitor stages but is not the focus here [23]. FCMFC can utilize the same off-the-shelf transformer originally intended for a flyback design and the use of that transformer for higher voltage gain, at the cost of more semiconductors and higher control complexity. However, the FCMFC can achieve higher output voltages because of the significant gain increase provided by flying capacitors, while maintaining high efficiencies shown in Section IV.

The contribution of this work is successful operational analysis, design, and testing of the first functioning FCMFCs for DC-DC power conversion. It proves the steady-state operating equations for gain, voltage, and current hold true and that natural voltage balance is achieved which allows for lower device voltage stresses, like other FCML converters. Unlike other FCML converters, the converters herein, achieve a higher voltage gain as a result of cycling flying capacitors with the transformer. Section II will lay out the switching operation of the topology and steady-state equations. Section III explains the design of the two FCMFC prototypes and the one flyback converter used as a control group for comparison. This allows direct verification that using the same active and passive devices improves the gain capability and efficiency of the converter which can be seen with a corresponding duty cycle decrease for the proposed design of 5V to 40V. Section IV presents the results and compares them to theoretical values.

II. CONVERTER OPERATION

A. SWITCHING STATES AND VOLTAGE GAIN

The operation of the FCMFC is shown in Fig. 2, Fig. 3, and Fig. 4. Note that this is the simplest FCMFC, $N = 3$ (or N3) voltage levels (2 capacitors: 1 flying and 1 output) but the operation would be the same for higher-level devices. Higher-level devices add 2 switching states per flying capacitor, one to charge the magnetizing inductance and another to discharge into the extra flying capacitor. The primary MOSFET (S) sets

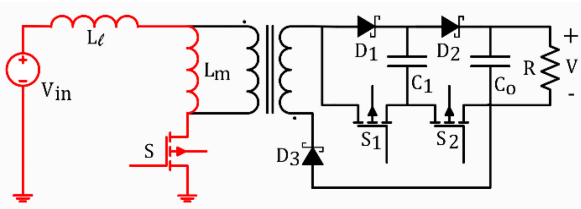

FIGURE 2. States 1 and 3 of FCMFC operation: Charging L_m.

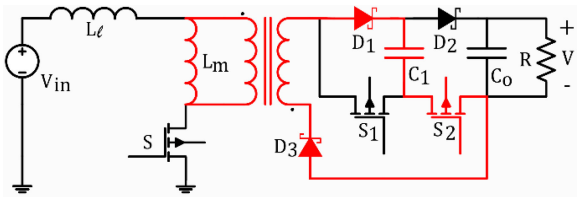

FIGURE 3. State 2 of FCMFC operation: Charging C_1.

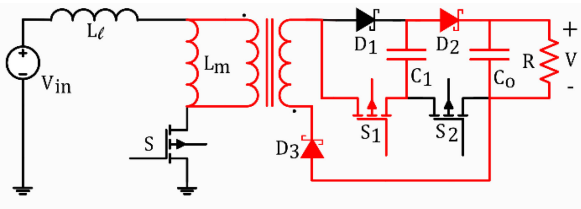

FIGURE 4. State 4 of FCMFC Operation Output Stage: Charging C_o.

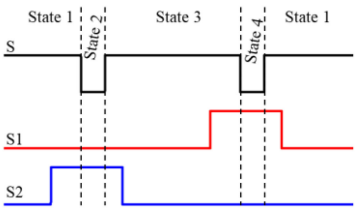

FIGURE 5. Phase shifted pulse width modulation.

the pace of the switching for the FCMFC. The converter is controlled using PSPWM shown in Fig. 5. When the input primary switch is OFF, (N-2) of the secondary switches will conduct to charge a flying capacitor stage.

With S ON, the magnetizing inductance of the double wound inductor will charge for DT_s shown in Fig. 2, where D is the duty cycle of input switch S, and T_s is the switching period or inverse of the switching frequency f_s. During this stage, secondary conduction through the body diode of the FETs is prevented by the addition of diode D_3. Next, S turns OFF and S_2 turns ON with S_1 OFF, shown in Fig. 3. In this stage, the inductor solely charges the flying capacitor C_1 through D_1, S_2, and D_3. The next state is the same as the first and is shown in Fig. 2, where the inductor charges again. Finally, the output stage happens in Fig. 4 where S and S_2 are OFF and S_1 is ON. In this state, notice the current flowing up through the negative end of C_1 and through D_2 into the output capacitance and then back through D_3. The

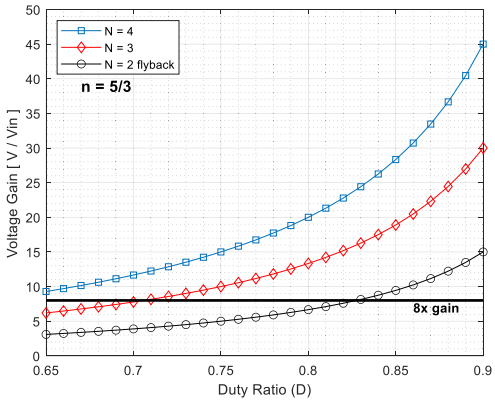

FIGURE 6. Ideal voltage gain vs duty cycle for flyback and FCMFC.

energy of the output capacitor is boosted by the inductor and flying capacitor. This is the energy multiplication effect that leads to higher gains as shown in (1), the voltage conversion ratio derived using inductor volt-second balance. Note that the flyback converter is the simplest FCMFC (the N2 case) and this equation becomes the same as the conversion ratio for a flyback converter. For a higher N level structure, this process would happen with each flying capacitor charging the next until the output capacitor is charged as shown in Fig. 4.

$$\mathrm{M(D)} = \frac{\mathrm{V}}{\mathrm{V_{in}}} = \frac{\mathrm{n\,(N-1)\,D}}{1-\mathrm{D}} \tag{1}$$

Plotted in Fig. 6 is the ideal gain shown in (1) with a transformer turns ratio of $n = 5/3$ for all converters. FCMFC has a higher gain for any given duty cycle. Mathematically, each flying capacitor has a multiplicative effect on the voltage conversion ratio, *"(N-1)"* term in (1). One flying capacitor doubles the gain of a flyback converter, two flying capacitors will triple the gain, and so on for higher level converters. This relationship is apparent in Fig. 6, where voltage gain is shown for the flyback and two FCMFC converters. Hardware conditions are not ideal, however, and thus this ideal gain curve gives insight into absolute capabilities.

Upon constructing a hardware version of the flyback and FCMFC, the losses reduce the achievable gain. A more accurate predictor of voltage gain is shown in Fig. 7. These curves account for the major loss elements of an FCMFC with analysis from [24]. The flat line at eight times gain is included to show what duty is required for the application of this work. Notice that in Fig. 6 the required duty cycles are much lower in the ideal case than in the loaded case shown in Fig. 7. Near 90% duty cycle there is a crossover point where the N3 converter exhibits a higher gain than the N4 converter due to conduction losses, which illustrates the eventual tradeoff with a multilevel structure. Higher *N-level* structures are not necessarily less efficient, but this work is based around proof of operation and not optimization. Higher-order multilevel converters, ten levels or more, can be very efficient [25] for similar principles explained in this work. The FCMFC secondary FETs have a reduced blocking voltage

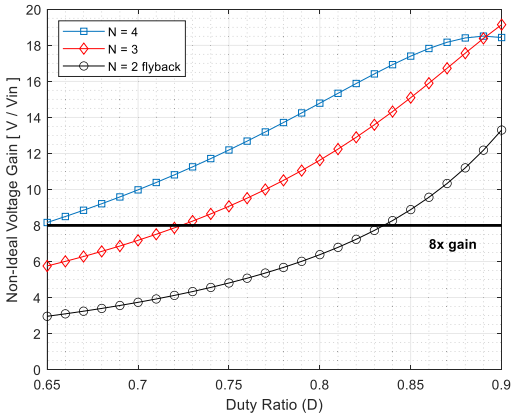

FIGURE 7. Non-Ideal voltage gain for flyback and FCMFC for 160Ω load.

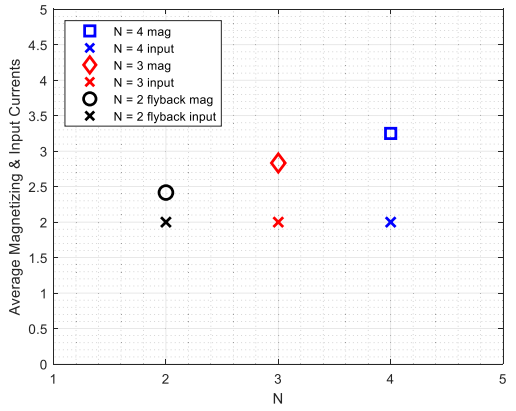

FIGURE 8. Magnetizing and input currents.

rating of V/(N-1), which facilitates the use of lower-rated FETs that have a lower on-resistance, as seen in [25]. In the case of this paper, all switches were chosen at the same 100V rating to account for the significant gain increase that FCMFC experiences. Note that even under load, the FCMFCs both have significantly higher gain than the flyback converter.

B. CURRENT ANALYSIS

The average magnetizing inductor current is shown in (2) and was derived using capacitor-charge balance. The resultant equation is the same as a flyback converter with an added (*N*-1) term in the numerator to account for flying capacitors. Magnetizing current does not directly double or triple because a lower duty cycle can be used for higher *N* level converters, due to the gain increase discussed in the previous subsection. In Fig. 8 the average magnetizing current is calculated as expected for the three converters designed in this paper. The average magnetizing currents for N2,34 level devices are 2.42A, 2.83A, 3.25A respectively. The duty cycle of the input switch decreased from 82.76%, 70.59%, to 61.54% respectively due to the gain increase shown in (1). Because of this decrease in primary side conduction, the average input current of each

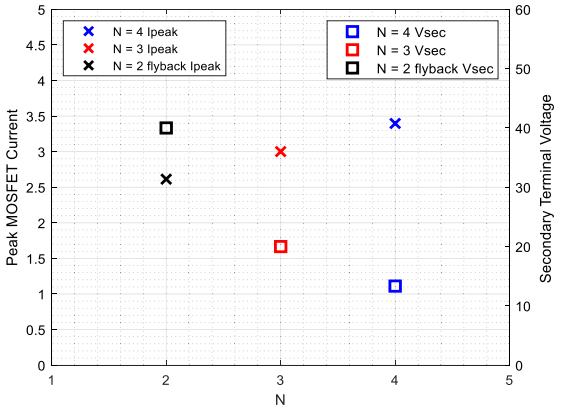

FIGURE 9. Peak MOSFET currents and secondary terminal voltage.

converter is the same at 2A, shown in Fig. 8.

$$I_L = \frac{n\,(N-1)\,V}{R\,(1-D)} \qquad (2) \qquad \Delta i_{L_m} = \frac{V_{in} D}{2 f_s L_m} \qquad (3)$$

Ripple current, (3), varies for magnetizing inductance L_m, the input voltage V_{in}, duty cycle D, and switching frequency f_s. The only variance shown in this equation for multilevel structures is in the operating duty cycle for the desired conversion ratio. A higher-level converter can use a lower duty cycle for a given gain, resulting in a lower ripple current value on the primary inductor. The average magnetizing current is higher for higher-level devices and shown in Fig. 9 is the calculated peak current that occurs through the MOSFET before turning OFF.

C. ZENER SNUBBER POWER CONSUMPTION

Leakage inductance on the primary winding will cause large voltage spikes at turn OFF of the primary FET. This is one drawback of the flyback converter that is solved with various types of snubber circuits. The most robust of which is the Zener snubber which is suitable for this exercise and shown in Fig. 1. A Schottky and Zener diode are placed in series from the switching node of the FET to the positive input voltage node. When the FET turns off the peak current flowing is now stored in the leakage inductance of the "transformer" and this results in a very large voltage spike across the FET. When this happens the Zener diode will conduct at its Zener voltage and regulate the voltage at the switching node, passing the leakage current back to the source. The derived power consumption for this snubber circuit is shown in (4), [26]. There is one modification made to account for the FCMFC, the *(N-1)* term. This represents the fact that only a fraction of the converter output voltage is reflected through the transformer during the OFF state of the primary FET, due to the voltage distribution across the flying capacitors on the secondary side of the circuit. This relationship is shown in Fig. 9, where the secondary terminal voltage is shown, *V/(N-1)*, for N 2, 3, 4. Although the peak FET current will be higher for higher-level converters, the reflected voltage will be significantly reduced: 50% for

an N3 converter and 33% for an N4. The predicted loss in the voltage clamp snubber for these converters is significantly reduced, calculated using (4). Going from the flyback (N2) converter to an N3 FCMFC, the reduction in power loss is significant, 67%, because of the reduced blocking voltage, 1.20W for the flyback down to 0.39W for the N3 FCMFC. However, notice that for an N4 device there is a slight increase in power loss, 0.39W (for N3) to 0.40W (N4), because of the output voltage fraction of one-half compared to one-third and also the peak current increase, shown in Fig. 9. The 0.4W loss for the N4 device is still 66% less than the 1.2W loss of the flyback converter. There is a rise in power loss through the Zener clamp snubber circuit for higher-level devices, but it would take a 12-level device or higher to see the 1.2W snubber loss seen by the flyback. While a higher turns ratio could be utilized for a flyback converter, and thus power loss in this snubber decreased, this work is showing how FCMFC can increase utilization of existing, off-the-shelf flyback transformers, making this a fair comparison. The snubber could also be tuned to a higher voltage resulting in less power loss but also less protection for the primary FET, sacrificing reliability.

$$P_{clamp} = \frac{1}{2} L_{lk} {I_{max,S}}^2 \frac{V_{clamp}}{V_{clamp} - \frac{1}{n(\mathrm{N}-1)} V_{out}} f_S \qquad (4)$$

III. HARDWARE DESIGN

The goal of this section is to showcase a robust prototype testbed. Components were selected to account for a wide range of operations to ensure safe and reliable testing above the specified 40V output. The lower voltage ratings permitted by the flying capacitor structure are not taken advantage of in this work for two reasons: (1) to allow for higher voltage testing and (2) to show how FCMFC can operate more efficiently using the same components as the flyback converter. This shows that future iterations will achieve even higher efficiencies when taking advantage of lower-rated semiconductors. To validate the theory of operation previously discussed, three hardware prototypes were developed using the same components, listed in Table 1. The flyback converter will serve as a basis for comparison for the two FCMFCs. The flyback design is considered an N2 FCMFC. The N3 and N4 converters designed have 2 and 3 capacitor stages on the secondary, respectively.

A. CONTROL SENSING

A Texas Instruments C2000 F28335 Delfino control development board was used to provide the PSPWM control signals for the primary FET and floating FETs for the flying capacitors on the converter secondary. PLECs coder was used to program the board. A soft start function was used for the primary FET to slowly energize the double wound inductor and avoid a high inrush current that results because of the uncharged output capacitance. This scheme prevents magnetic saturation and protects future iterations which will utilize FETs with lower voltage ratings. *Open-loop control was used to run the FETs at a fixed duty cycle for each testing trial.*

TABLE 1 Component List

Component	Brand	Part number
Planar Transformer	Coilcraft	NA5871-AL 42μH, 3:5
Flying Capacitors	TDK AVX	CGA6M2X7R2A105K200AA – 1uF 22201C106MAT2A – 10uF X7R, 100V
MOSFETs	Infineon	IPD30N10S3L-34 100V, 30A
Diodes	Diodes Inc.	PDS5100 100V, 5A
Bootstrap Diode	Nexperia	PMEG10010ELR 100V, 1A, 50Apk, 3.7ns
Gate Driver	Texas Instruments	UCC27512
Isolated Gate Driver	Texas Instruments	UCC21220A
Isolated Power	Analog Devices	LTM8067
Controller	Texas Instruments	C2000 F28335

B. ISOLATED AUXILIARY POWER, FLOATING GATE DRIVE, BOOTSTRAPS

One challenge in multilevel structures is floating voltages at the source node of the transistors. In the case of FCMFC, this challenge is met with the additional challenge of maintaining primary to secondary electrical isolation; but fortunately, FCMFC does not require advanced bootstrap techniques.

An Analog Devices LTM8067 isolated power chip was chosen to provide auxiliary power for bootstrap circuitry. This chip was set to boost the input 5V supply up to 8V and drive the MOSFETs on the secondary side. This chip, being a flyback converter itself, retains primary to secondary isolation for the main converter with a 2kV rating. It provides a selectable voltage output, tuned with a resistor, to allow FETs to be driven at higher voltages if necessary. For this work 8V and 12V can be used on the Infineon FETs which are limited to 20V gate drive. Input and output capacitances are 2μF and 30μF respectively for adequate voltage regulation. A 20 mΩ resistor was placed in series with the input of the auxiliary converter to dampen a potential resonant tank circuit that can arise between the inductance of the supply and the input capacitance.

Texas instruments UCC21220A isolated gate driver chips were chosen to reference the floating voltage nodes as a virtual ground. They also provide 4kV isolation from their logic level controller input side to the secondary high voltage side that drives the flying capacitor MOSFETs.

Bootstraps are required to drive each floating voltage node that corresponds to the flying capacitors. In the *N3* FCMFC, there is one bootstrap circuit and there are two in the N4 converter. Each bootstrap circuit consists of a resistor (R_B) diode (D_B) and capacitor (C_B). Isolated 8V DC supply feeds the resistor is in series with the diode and then the capacitor which finally connects to the floating source node of which, is the negative side of a flying capacitor, indicated in Fig. 1on $C_{1,}$ by a red dot and re-emphasized by the red dot in the bootstrap circuit diagram shown in Fig. 10. The positive polarity of C_B

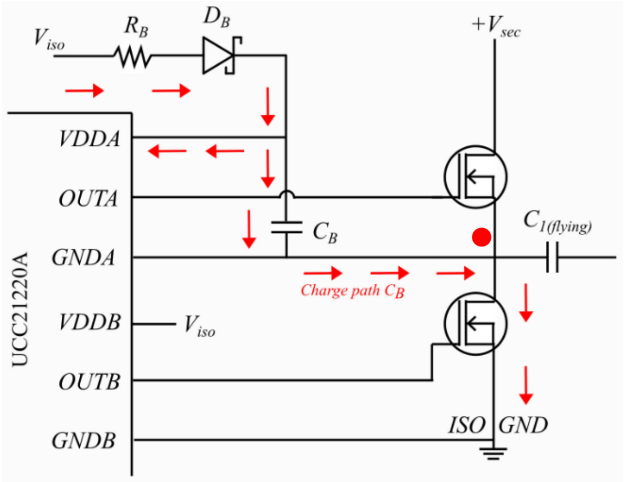

FIGURE 10. Bootstrap circuit for N3.

is connected to the input voltage node of the isolated driver chip. In this configuration the bootstrap circuit charges to the secondary ground of the transformer using the isolated power supply with all latter switch(es) in the FC network ON. When the latter switch(es) turn(s) OFF the voltage across C_B is now $V_{iso} - VD_B + V_{C1}$. This allows the effective floating FET gate-to-source voltage to be equal to the isolated power supply voltage minus the voltage drop that occurs across the bootstrap diode. The bootstrap capacitor is sized so that it can charge fast enough and have enough stored energy to bias the FET for its required ON-time per cycle. For higher-level converters, like the N4 in this work, the first bootstrap capacitor (closest to the coil) will have to charge through multiple FETs. The PSPWM must be set such that there is adequate charge time for the bootstrap capacitor. The balance between charging and discharging time must be met and considered for the bootstrap circuit when varying the switching frequency, as done in this work.

The chosen bootstrap diode has a reverse recovery time of 3.7ns which is less than the effective turn-on time of the FET. This is done to prevent excessive current from damaging the auxiliary power supply. The FETs effective-turn on time includes the time it takes the drain-to-source voltage to drop once the gate has been charged plus the time it takes the drain-to-source voltage to start dropping when the gate voltage begins to rise. The bootstrap diode was chosen to handle the maximum average current of charging the capacitor which occurs when the primary duty cycle is at its lowest point, 50%. The diode can handle peak current during startup conditions which is the supply voltage minus the diode voltage drop divided by the bootstrap resistance, approximately 2A.

C. PRINTED CIRCUIT BOARD LAYOUT AND CAPACITOR DESIGN

Fig. 11 is a picture of the three converters with input on the left and output on the right. The three converters are included on one 4-layer PCB. From top to bottom - N4, N3, and N2

FIGURE 11. Printed circuit board N2 (bottom), N3 (middle), N4 (top).

(flyback) are provided. The yellow wires are 14AWG current jumpers for a current transformer testing probe to measure primary and secondary current. There is no electrical connection between any of the three converters. RC pads were added for snubber circuitry on each active device. The flying and output capacitors were chosen to be 20-30μF, to yield 2.5% ripple as per analysis done in [27]. Extra pads (1μF, 10μF) were added to fine-tune capacitance based on device performance and experimentation.

D. SNUBBER CIRCUITS

The primary FET has two snubber circuits. The Zener snubber circuit clamps the voltage overshoot at the switching node that rises because of the leakage inductance energy present at turn OFF. The Zener voltage is set to 27V to protect the FET. Fig. 12 shows the Zener clamp snubbing the voltage to a maximum of 32.03V before leveling off to the regulated voltage, well below the 100V FET rating. The voltage scale is 5V/div and the time scale is 2μs/div. The primary FET and other active devices have series RC snubbers to reduce voltage ringing. These are designed to work for all cases in the wide frequency operating range. For example, Fig. 12 at 500kHz has little visible ringing.

IV. EXPERIMENTAL RESULTS

Each converter was tested at 100kHz, 250kHz, 452kHz and 500kHz for an increasing constant current load with a 5V input fixed duty cycle and 1μs blanking time. Starting from a very small load (<10mA) and increasing in 50mA increments up to a maximum load. Input and output voltage and current

FIGURE 12. Primary FET switching node voltage with zener snubber clamp.

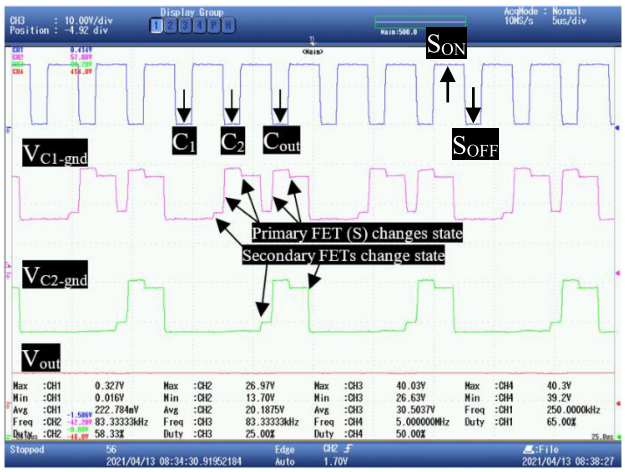

FIGURE 13. N4 flying capacitor charging action.

were measured at each point along with the flying capacitor voltages.

A. OPERATION AND VOLTAGE BALANCE

The oscilloscope used was a 50Mhz Yokogawa DL850E with probes: Yokogawa 700929 and Rigol PVP2150. The 5V to 40V, 250kHz case was recorded for the N4 converter and shown in Fig. 13. The primary FET gate drive signal is shown on top in blue with the two flying capacitor voltages shown in pink (C_1) and green (C_2) with the output voltage in red. Note that *these are not differential measurements* but are measured from the flying capacitor positive node to the isolated secondary side ground. The time scale is 5μs/div and the voltage scale is 10V/div for the flying capacitors. When the blue gate signal drive goes low, the secondary side flying capacitor charging action will take place. The magnetizing inductor will first charge C_1 which is illustrated by a black arrow on the blue gate drive signal. Because the voltage ripple is ~1V the charging of C_1 is not visible but does take place as

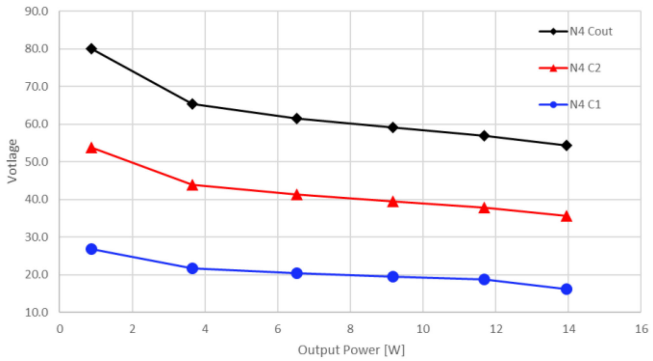

FIGURE 14. Experimental N4 flying capacitor charging action and natural voltage balance.

indicated. The next cycle is the inductor in series with C_1 to charge C_2. This is apparent on the C_1 (pink) voltage waveform because the measured voltage is pulled up to that of C_2. Next is the output stage where the inductor with C_2 charges the output capacitor. Now the green measurement matches the output voltage of 40V seen in red, with a 2.5% ripple. Again, the *actual ripple voltage of each capacitor is 1V* and what is shown in the figure is measurements to ground so the changes shown are changes in switching states. There is a change in voltage when the secondary switches change state and then a change when the primary FET switches ON or OFF as indicated in Fig. 13.

The flying capacitor voltages were measured at each state to verify the charging action and voltage balance. Fig. 14 is a voltage plot for the N4 converter which has two flying capacitors (C_1 & C_2) and the output capacitor (C_{out}). The voltages were measured at each 50mA increment up to a 14W power output. At each point, the voltage across the flying capacitors holds at one-third and two-thirds of the output voltage. For example, at the 9W point, the voltages for C_1, C_2, and C_{out} are 20V, 40V, and 60V, respectively. C_1 is closest to the secondary coil and in this case maintains the primary reflected voltage that is cut to one-third of the output voltage when compared to the flyback converter. Load step-response is not shown as steady-state performance is under evaluation compared to dynamic performance but is expected to be similar to other multilevel converters.

B. VOLTAGE GAIN

To check the gain potential of each converter, a duty cycle sweep was performed from 50% to 90% under no-load with 5V input, shown in Fig. 15. The theoretical prediction of (1) and Fig. 6 are correct. The N3 converter holds at about double the voltage gain of the flyback converter and the N4 is about triple. Take duty of 85% for example, the flyback has a gain of 10 and the N2 is 20 while the N4 is 32. Also of note here is that the typical switching limit of the flyback converter is around 90%. The flyback voltage gain drops off after 85%, going from 10 down to 8 at 90%. Both FCMFC converters maintain a gain increase from 85% to 90% with the N4 device being

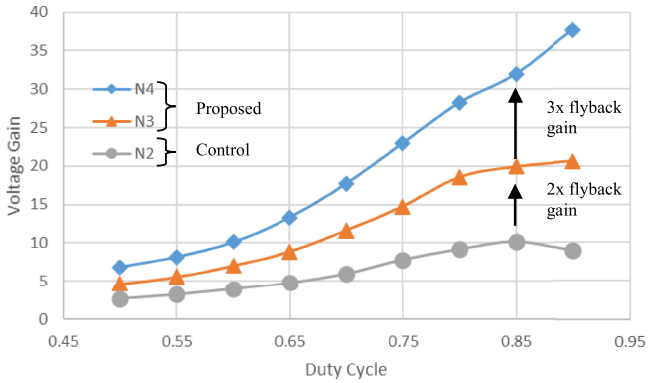

FIGURE 15. Experimental Unloaded Voltage Gain to be compared to Fig. 6.

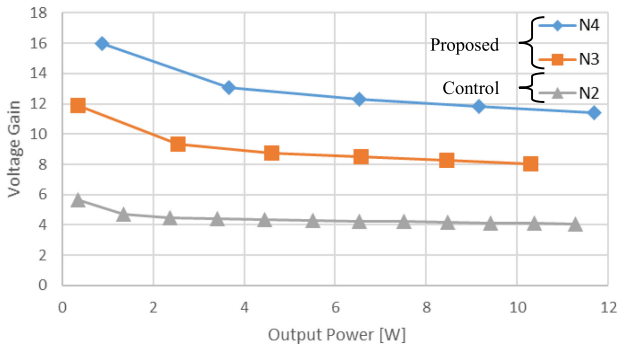

FIGURE 16. Experimental loaded voltage gain. Fig. 7 should be used to validate this plot but with *D* fixed to 72.5%.

more significant. The N2 increases from 20 to 21 while the N4 increases from 32 to 37. *Note that even with a higher turns ratio the FCMFCs would still double and triple the voltage gain that a flyback can achieve.*

To show the effects of loading on voltage gain, Fig. 16 shows a plot of output power versus voltage gain. The switching frequency is held fixed at 250kHz and the effective duty cycle is 72.5% for each converter with an input voltage of 5V. The flyback gain holds at 4 while the N3 is double at 8 and the N4 is tripled to 12, as expected. The FCMFC voltage gain is always double, triple, etc. that of the flyback converter.

C. ZENER SNUBBER LOSS

As predicted in Section II C, the FCMFC converters will have about one-third of the Zener snubber loss as the flyback converter. To illustrate this point, the N2 and N3 converters were run at an 8W load until a stable temperature was reached and thermal images are shown in Fig. 17. In both images, the Zener diode is the hottest (white) area. For the flyback converter, the temperature rises to 156F while the N3 only reaches 86F. This result is similar for the N4 converter. The flying capacitor connected directly to the secondary coil has a voltage that is half of the steady-state voltage across the output capacitor on the flyback converter. This voltage is reflected to the primary during the OFF state of the FET and increases the loss of the Zener.

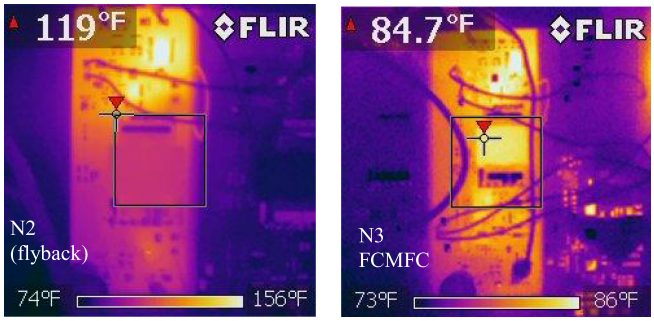

FIGURE 17. Thermal images of N2 and N3 at 8W load.

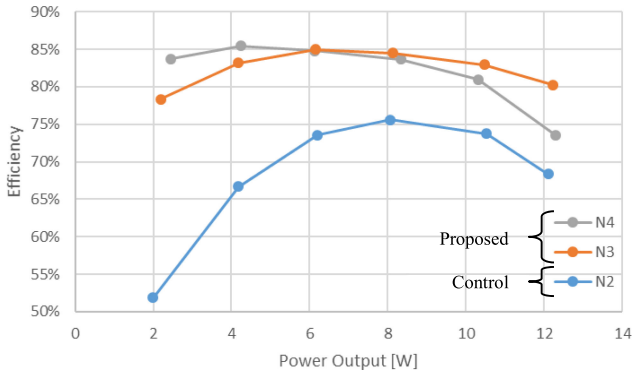

FIGURE 18. Efficiency vs Output Power N2, N3, N4.

D. EFFICIENCY

Fig. 18 shows the converter efficiencies when operating with 5V to 40V at 250kHz. The efficiency calculation includes all onboard circuitry: auxiliary power, primary gate driver, isolated gate drivers, etc.

The only power consumption unaccounted for is that of the microcontroller, which is similar for each of the three converters. Over the load range, FCFMC converters are more efficient than the flyback converter. The flyback efficiency peaks at 75.6% and the N3 peaks at 85.0% and the N4 peaks at 85.5%. The FCMFC converters are achieving higher efficiencies while having more switching devices and supporting circuitry. Overall, these efficiencies are not high compared to other works referenced herein. An approach was taken to prove circuit functionality and directly compare a flyback converter to the proposed FCMFCs and prove the relative efficiency increase. Careful consideration can now be taken to design an FCMFC around an existing flyback design to achieve higher efficiency than presented. FCMFC converters (N3 and N4) can also maintain a higher gain range with the lower duty cycle of operation. For the 100kHz, 452kHz, and 500kHz operation, similar efficiency behavior was observed. Higher frequency operation results in higher switching losses and thus a slight degradation in efficiency.

To compare application capability, the duty cycles were tuned so that the converters achieve 40V, 10W output at 250kHz, and the results are shown in Table 2. The flyback efficiency is 77.72% and the N3 converter reaches 84.74%.

TABLE 2 Efficiency At 5V to 40V, 10W Load, 250kHz

N	Duty Cycle	Efficiency
2	82.5%	77.72%
3	72.5%	84.74%
4	66.0%	81.57%

TABLE 3 Comparative Analysis of the High Voltage Gain Converters

Converter	Voltage Gain	Voltage Stress on MOSFET(s)	# of MOSFETs	# of Diodes
Converter in [28]	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{V(1-D)}{3+2n-D(3+n-D)}$	2	5
Converter in [29]	$\frac{n(3D+2)-(2-D)}{2(1-D)^2}$	$\frac{V(2+D(n-1))}{n(3D+2)-(2-D)}$	1	6
Converter in [30]	$\frac{1+n}{(1-D)^2}$	$\frac{V}{1+n}$	1	5
Converter in [31]	$\frac{1+nD}{(1-D)^2}$	$\frac{V}{1+nD}$	1	5
Converter in [32]	$\frac{1+n-D}{(1-D)^2}$	$\frac{V(1+n)(1-D)}{1+n-D}$	1	5
Converter in [33]	$\frac{1+n}{(1-D)^2}$	$\frac{V}{1+n}$	1	5
Converter in [34]	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{V(1\pm D)}{1+D+2n(1-D)}$	2	4
Converter in [35]	$\frac{2+(1+n)D}{(1-D)^2}$	$\frac{V(1-D)}{2+(1+n)D}; \frac{V}{2+(1+n)D}$	2	5
Converter in [36]	$\frac{2(1+n)}{1-D}$	$\frac{V}{2(1+n)}$	2	6
Proposed Converter	$\frac{n(N-1)D}{1-D}$	$(1-D)(V_{in}+\frac{V}{n(N-1)}); \frac{V}{N-2+D}$	3-4	3-4

The Zener snubber loss reduction predicted in Section II C, and shown thermally in Fig. 17 makes the FCMFC more efficient because of the reduction in the secondary coil voltage caused by the flying capacitor. The same benefit is found for the N4 converter, but the efficiency is lower at 81.57% because of the added conduction and switching losses associated with the extra flying capacitor stage. Further iterations of this converter can take advantage of lower-rated FETs and further reduce conduction losses, which will significantly increase their efficiency.

VI. DISCUSSION

This work is not an attempt to create a highly efficient prototype for one application; it is an effort to prove the *hardware* viability of using flying capacitors on an isolated, DC/DC flyback design, which is not reported in the literature other than by the authors of this work. The converter herein also poses many benefits over other designs in the space of voltage boosting, which will be discussed further.

A. STATE-OF-THE-ART COMPARISON

The proposed can achieve very high voltage gain inherently without relying on the transformer turns ratio. It can always scale the voltage gain of a flyback converter because of the capacitor stages. Other converters attempt to achieve high gain with complex combinations of boost converters and coupled inductors. Table 3. compares the most recent and capable high voltage gain converters to the proposed in terms of gain, component stress, and semiconductor count. All gain functions rely solely on duty cycle (D) and turns ratio (n) while the proposed has a third component (N). N, the capacitor stages, is the scaling effect and the critical parameter for higher gain. Of course, the turns ratio can double and triple but FMCFC allows for an alternative option, which also has the stress distribution benefit as seen in the stress function column. The proposed has two stress functions shown: one for the primary FET and another for secondary FETs and diodes. The other converters block some portion of the output voltage which can be very high while the proposed converter distributes this stress across multiple stages while maintaining a similar component count to the other converters from the literature. [19], [28]–[42].

TABLE 4 Comparative Analysis of the Boost Component of Microinverters

Converter Type	Voltage Gain	Voltage Stress on MOSFET(s)	Voltage Stress on Secondary MOSFET(s) & Diode(s)	# of FETs; Diodes
Flyback with bidirectional switches [37]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	3; -
Interleaved Flyback with active-clamping [38]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	4; 2
Interleaved Flyback with adaptive-snubber [39]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	4; 2
Flyback with dissipative-snubber [40]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	1; 2
Flyback converter with voltage multiplier [41]	$\frac{1+2n-nD}{1-D}$	$\frac{V}{1+2n-nD}$	$\frac{nV}{1+2n-nD}$	2; 3
Boost-Flyback/Flyback converter [42]	$\frac{1+nD}{1-D}$	$\frac{V}{1+nD}$	$\frac{nV}{1+nD}$	3; 1
Flyback converter with Voltage-Doubler [19]	$\frac{n}{1-D}$	$V_{PV}+\frac{V}{n}$ V_{PV} is nominal PV voltage (Vin)	$\frac{nV_{PV}+V}{2}$	2; 2
Proposed Converter	$\frac{n(N-1)D}{1-D}$	$(1-D)(V_{in}+\frac{V}{n(N-1)})$ *	$\frac{V}{(N-1)D}$ * $=\frac{V}{N-2+D}$	3-4; 3-4*

Another comparison is made to a set of converters that were designed to be used as the *voltage-boosting portion* of a microinverter shown in Table 4. The proposed again has a significant gain benefit over the others while also distributing stress across the SDC stages and maintaining a semiconductor count that is average for all entries in the table.

B. TRADEOFFS

While FCMFC does achieve higher gain and efficiencies, it does come with tradeoffs. Cost of more components due to the increased SDC stages and auxiliary components to support them like the bootstrap circuits. Added components would seem to decrease power density but that is not necessarily the case because of the reduced size of each component as converter stages increase. Fig. 19 compares the required inductance for FCMFC converters (N=*3-8*) normalized to the required inductance for a flyback converter to achieve a given current ripple. Equation (3) is the basis for the chart and is plotted with respect to converter gain. As the number of stages increases the required inductance decreases. The reduction is very significant at gains lower than 10 and approaches

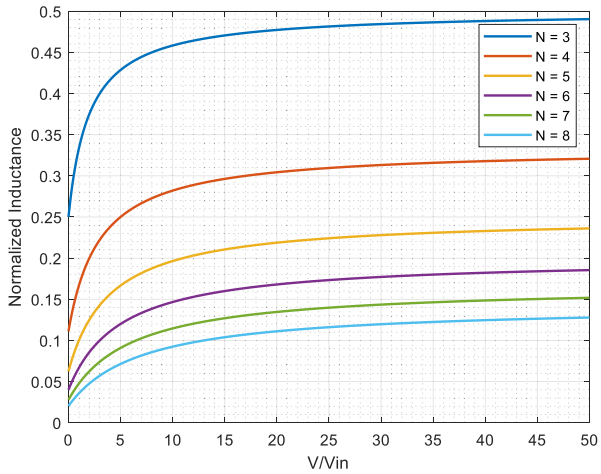

FIGURE 19. Required inductance normalized to flyback converter.

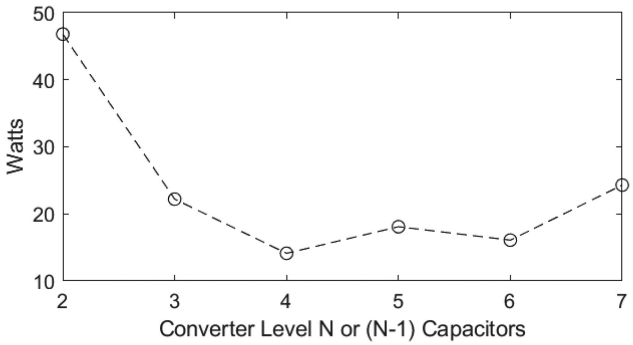

FIGURE 20. Power Loss vs Flying Capacitors for 40V to 400V, 200W.

asymptotes for each converter that are one half, one third, etc. This advantage was not realized in the current work for design reasons state herein. Future designs will use this relationship to achieve higher power densities. The comparison is made for converters up to *N=8* and not further because the size reduction benefit is minimal beyond this level.

C. STAGE SELECTION IMPACTS ON SYSTEM EFFICIENCY

Higher-level multilevel boost converters have been developed, such as in [25] for example, but do not achieve isolation and do not have an inherent voltage gain benefit. Increasing the stages will always decrease the individual component stress but there is a diminishing return with this relationship. More stages would distribute stress and allow for lower-rated semiconductors to be used, which can reduce conduction and switching losses, but each stage adds more resistance in the conduction path which eventually counteracts the reduction in individual component resistance. This is like the inductance relationship shown in Fig. 19 where the required inductance is cut by 1/2, 1/3, etc. Eventually, the size benefit is not significant enough to justify the increase in circuit complexity. Fig. 20 shows how this relationship works for converter power loss using the flyback and FCMFC converters for a 40V to 400V application at 200W power output. This plot considers component stress and utilizes lower-rated components for the higher-level FCMFCs. The *N=4* converter is the most efficient with 14W of power loss while the flyback loses 47W. For FCMFCs higher than *N=4* the power loss trends upwards because the component stress reduction is counteracted by the sheer increase in component count, making the overall converter less efficient.

Operating parameters and available semiconductors impact the optimal stage level. This work was not focused on optimizing the level or layout and components of the proposed converter but to prove inherent gain benefits with FCMFC over the flyback converter. FCMFC can now be used to optimize converter operation for specific applications, where efficiency will be a primary driver, and number of stages can be modified to achieve the desired outcome. Future FCMFC iterations can utilize many advanced design techniques to achieve even higher efficiency such as zero-voltage switching [11], [12], advanced bootstrap design [43], and time-optimal control [44].

VI. CONCLUSION

This work has derived and demonstrated the operation of the FCMFC for two cases, N3 and N4, and an N2 or flyback design. Using the same transformer and semiconductor components to remove bias in comparison, a flyback converter as compared to the multilevel alternative, the FCMFC. Although all converter designs in this effort could be optimized for peak converter efficiency the point of this effort was to showcase topological benefits without additional auxiliary circuitry that could enhance circuit performance. Because the FCMFCs outperform the flyback as shown experimentally, it is apparent that any optimization would yield FCMFCs that are more efficient than any flyback counterpart.

This work has also shown the effective use of flying capacitors to reduce component stress of the flyback converter while using an off-the-shelf flyback transformer. The latter statement has two important takeaways. First, FCMFC converters are more efficient using the same componentry as the flyback converter even with added circuitry due to their inherent stress distribution. Second, designers can utilize existing transformers to achieve higher gain and minimize custom magnetic designs.

It is important to understand that a flyback transformer can have a higher turns ratio but the FCMFC will always provide a significant gain increase *on top* of the flyback's performance. The flyback converter is limited in power that it can handle because of component stress and other factors. This work shows that utilizing FCMFC can increase the power processing of an existing flyback design. In addition, this work extends the benefits of FCML converters to an isolated topology while minimizing the losses from transformer leakage inductance, which have historically limited the power levels of flyback converters.

The voltage stress across the semiconductors is reduced because of the fractioning of the output voltage across multiple output stages. Future iterations will utilize lower voltage rated

semiconductors, due to the stress distribution, and achieve much higher efficiencies.

ACKNOWLEDGMENT

Thanks to Coilcraft for providing the planar transformers for this work. A special thanks to the University of Pittsburgh Central Research Development Fund for funding the hardware associated with the prototypes developed.

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