IEEE Open Journal of
Power Electronics

Received 30 December 2021; revised 7 February 2022; accepted 23 February 2022. Date of publication 25 February 2022; date of current version 25 March 2022. The review of this article was arranged by Associate Editor Navid Reza Zargari.

Digital Object Identifier 10.1109/OJPEL.2022.3154726

MMC Based Hybrid Switched Capacitor DC-DC Converter

MARCUS VIEIRA SOARES AND YALES RÔMULO DE NOVAES (Member, IEEE)

Department of Electrical Engineering, Santa Catarina State University - UDESC, 89219-710 Joinville, Brazil

CORRESPONDING AUTHOR: MARCUS VIEIRA SOARES (e-mail: marcus.sov@gmail.com)

This work was supported by the Programa Nacional de Cooperação Acadêmica da Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - CAPES/Brazil - Finance Code 001, PROAP/AUXPE/CAPES and FAPESC.

ABSTRACT Aiming to address the growth and the integration of renewable sources and electronic loads, different types of dc-dc topologies with specific features have been proposed, going from medium frequency isolated Modular Multilevel Converter to Switched Capacitor and Hybrid Switched Capacitor topologies. In this paper, a bidirectional Modular Multilevel Converter based Hybrid Switched Capacitor dc-dc converter is presented, featuring transformerless structure, automatic total arm voltages clamping/balancing, voltage static gain independent of the submodules quantity and efficiency with reduced duty cycle influence. The topology operates with a Quasi-Two-Level modulation, which provides passive components volume/weight reduction, a degree of freedom regarding the dv/dt applied on the magnetic windings and basis to perform the submodule capacitor voltages equalization within each arm. The topology operating principles are approached by an average value static analysis, while an instant value static analysis is used to estimate the operating current spike worst case. A 1.17 kW, 350/200 V laboratory scale prototype using IGBTs is implemented to experimentally confirm the theoretical approaches.

INDEX TERMS Switched Capacitor, Modular Multilevel Converter, MMC, Hybrid Switched Capacitor, Non-Isolated DC-DC Converters.

I. INTRODUCTION

Intending to reliably interface medium/high voltage dc grids (MVDC/HVDC) and low/medium voltage dc power loads, such as electrical vehicles, electrified transport, data centers, etc, dc-dc converters based on multilevel topologies have been intensively studied in recent years, with the Modular Multilevel Converter (MMC) playing an important role in this scenario, mainly because of the modularity and capability of using well known electronic technologies provided by this topology.

In this context, medium frequency isolated MMC based dc-dc topologies have been proposed [1]–[3]. The galvanic isolation enhances the fault protection capability and the transformer turns ratio can be used to better interface the inverter and the rectifier stages. Moreover, the medium frequency operation leads to the converter volume/weight reduction. On the other hand, all the power processed by the converter must flow through the transformer and the higher frequency tends to increase the dv/dt applied on the windings, which can limit the medium transformer volume/weight reduction and make its design quite challenging [4].

In order to reduce the power processed by the transformer, the dc auto-transformer converter is proposed in [5]. Also based on MMC with Half-Bridge (HB) submodules (SM), this topology has a direct electrical connection between the inverter and the rectifier stages, allowing part of the power to flow straight from the input dc voltage source to the load and, then, reducing the transformer power rating. However, this arrangement comes at the cost of loosing the galvanic isolation between the dc terminals, as well as part of the converter fault blocking capability, unless more complex SM configurations are used, instead of HB. Furthermore, the transformer can still be bulky, specially when the difference between the input and the output voltages is significant.

Due to the medium frequency transformer issues, some transformerless MMC based dc-dc converters have been studied [6]–[13]. In general, these topologies use either a capacitive path or the MMC arm inductors to perform the

voltage balancing between the upper and lower arms. However, when the difference between the input and output voltages is significant, a high ac current and/or bulky arm passive components are needed to achieve this balance, leading to low efficiency and bad use of the components capacity in these cases. This drawback is addressed in [14], [15], where different current source modules are used to intermediate the energy transfer between the dc terminals. Since the increase of the SMs quantity takes to a decrease of the maximum output voltage, these topologies covers applications that demand high voltage ratio between dc input and output.

Another category of transformerless dc-dc converters is composed by the Switched Capacitor (SC), Switched Inductor (SL) and Hybrid Switched Capacitor (HSC) topologies [16]–[22]. The operating principle of these converters consists in parallel/series connecting groups of capacitors/inductors to process the energy, which results in high voltage ratio capability and converters with high power density. Moreover, self-voltage clamping and balancing of some components is achieved on SC and HSC converters. On the other hand, the efficiency dependence on the operating duty cycle, the large components count, the voltage ratio variation with the number of cells and the current/voltage spikes concern can impose some limitations or add complexity to these topologies.

This paper is aimed to present a bidirectional MMC based Hybrid Switched Capacitor (MMC-HSC-DC) dc-dc topology. It is a transformerless converter, that structurally differs from those in [6], [11] and [12] by the absence of the arms inductors. It provides a new strategy to balance the arms total voltages, which become automatically clamped by the flying capacitor C_f. Consequently, it is not necessary to generate an ac power flux through the arms to achieve the voltage balance, unlike the mentioned topologies. Additionally, the converter acquires a switched capacitor operational behavior, demanding a new approach regarding the topology design, since issues like current spikes and equivalent output resistance must be addressed.

On the other hand, when compared to other HSC converters, the number of SMs in the MCC-HSC-DC arms can be changed without leading to output voltage range restrictions. Furthermore, due to the topology operational symmetry, it can be designed to reduce the duty cycle influence on the converter conduction losses. Hence, better efficiency behavior can be achieved in closed-loop operation.

The Quasi-Two-Level (Q2L) modulation [23] is used to reduce the passive components size, to create a degree of freedom regarding the dv/dt applied on the magnetic, by limiting the voltage steps on the windings [24], and to provide a voltage equalization method to balance the SM capacitors within each arm.

The step-down unidirectional variant of the proposed converter is introduced in [25], where more superficial and general topology analyses are developed. The current paper is conceived to provide a broader and more detailed mathematical approach regarding the topology operation, covering: two operation modes; an equivalent output resistance thorough analysis; a peak current estimation method that takes into account the Q2L transitions and the SM capacitance effects; and experimental results to compare with the analytical data.

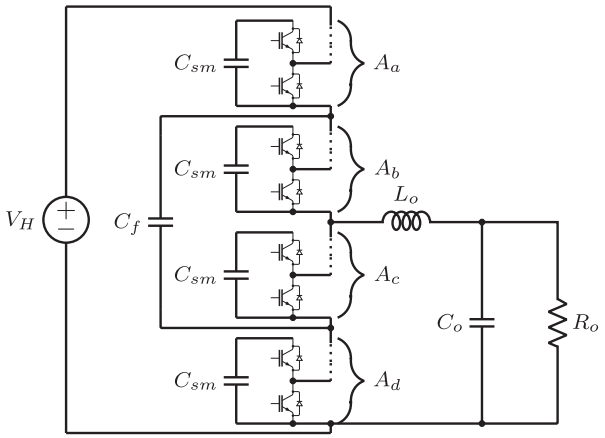


FIGURE 1. DC-DC converter.

This text is divided in a general topology overview, approaching the topological states and the applied modulation technique; an average value static analysis, to define the converter equivalent output resistance characteristic and the voltage static gain; an instant value static analysis, to address the SC current spikes; and the laboratory scale prototype experimental results along with discussion. Variables defined with small and capital initial letters represent ac plus dc signals and signal average or RMS value, respectively. Matrices are defined by bold and initial capital letter variables.

II. PROPOSED DC-DC TOPOLOGY

The topology presented in this paper is a transformerless bidirectional dc-dc converter based on the integration of the Three-Level Buck converter (or dc-dc Flying Capacitor converter) and the MMC. The representative diagram of the topology is presented in Fig. 1, which is composed by four series connected sets of N SMs, here defined as arms (A_a, A_b, A_c and A_d), a flying capacitor (C_f) and an output LC filter composed by L_o and C_o. The LC filter input voltage is defined as $v_{LC} = v_{Lo} + v_o$. All the analysis presented in this paper considers the topology operating in Buck mode, but can be similarly applied to obtain the Boost mode equations.

The SM configuration can be chosen according to some desired features. For example, HB SMs will provide a low account of semiconductors, reducing the converter complexity and losses. On the other hand, the use of Full-Bridge (FB) SMs in the upper arms (A_a and A_b) provides bidirectional short-circuit interruption capability to the topology, improving safety and robustness. All the analysis presented in this paper considers equal HB SMs composing the proposed converter.

A. TOPOLOGICAL STATES

Initially, it is considered that all the SMs within an arm operate equally, always changing to the same requested state

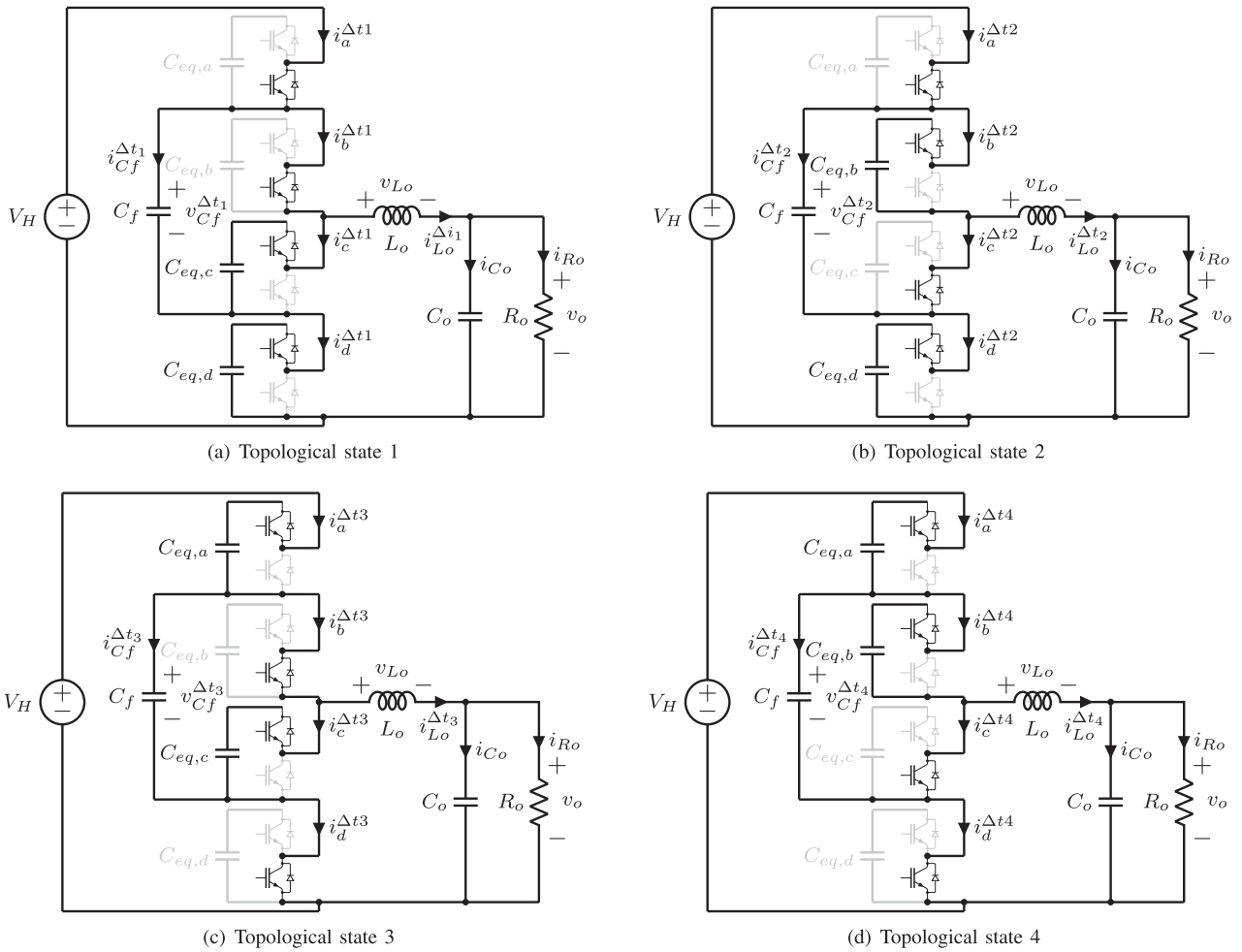


FIGURE 2. **Proposed converter topological states. (a) Topological state 1. (b) Topological state 2. (c) Topological state 3. (d) Topological state 4.**

at the same time. Therefore, the N SMs of each arm can be represented by an equivalent SM, where $C_{eq,i} = C_{sm}/N$ and $i \in \{a, b, c, d\}$ identifies the arms. Additionally, it is defined that an arbitrary arm assumes the state $A_i = 1$ when the corresponding equivalent SM upper switch is off and the lower is on, bypassing $C_{eq,i}$. On the other hand, $A_i = 0$ when the upper switch is on and the lower is off, connecting $C_{eq,i}$ to the SM output.

Considering that $A_a = \overline{A_d}$ and $A_b = \overline{A_c}$, in order to avoid short circuits and high voltage differences when the switched capacitor parallel connections are performed, four fundamental topological states, depicted in Fig. 2, can be obtained from the arms configuration.

The converter behavior during each topological state can be described as follows:

- **State 1** ($A_a = \overline{A_d} = 1; A_b = \overline{A_c} = 1$)**:** V_H transfers energy through L_o to the output, increasing i_{Lo}. C_f exchanges charges with $C_{eq,c}$. V_H, C_f and $C_{eq,d}$ also exchange charges among themselves;
- **State 2** ($A_a = \overline{A_d} = 1; A_b = \overline{A_c} = 0$)**:** V_H transfers energy through C_f and L_o to the output, increasing v_{Cf}. The current i_{Lo} decreases if $V_o > V_H/2$ and increases if $V_o < V_H/2$. C_f exchanges charges with $C_{eq,b}$. V_H, C_f and $C_{eq,d}$ also exchange charges among themselves;
- **State 3** ($A_a = \overline{A_d} = 0; A_b = \overline{A_c} = 1$)**:** C_f transfers energy through L_o to the output, decreasing v_{Cf}. The current i_{Lo} decreases if $V_o > V_H/2$ and increases if $V_o < V_H/2$. C_f exchanges charges with $C_{eq,c}$. V_H, C_f and $C_{eq,a}$ also exchange charges among themselves;
- **State 4** ($A_a = \overline{A_d} = 0; A_b = \overline{A_c} = 0$)**:** only L_o transfers energy to the output on a free-wheeling behavior, decreasing i_{Lo}. C_f exchanges charges with $C_{eq,b}$. V_H, C_f and $C_{eq,a}$ also exchange charges among themselves.

B. MODULATION

To operate the converter, the Q2L PWM modulation is chosen. Basically, it is composed by one triangular carrier with peak value V_p and by $4N$ modulation signals, one for each SM. Since $A_a = \overline{A_d}$, there is always one modulation signal of A_a equivalent to another of A_d. The same can be applied to the pair A_b and A_c. These definitions are represented by the modulation signals $v_m^{a,d}$ and $v_m^{b,c}$, respectively, where $v_m^{b,c} = V_p - v_m^{a,d}$. The implemented comparison logic between the

TABLE 1 Topological States Used on Each Operation Mode Along a Switching Period ($T_s = 4t_{tr} + \sum_{i=1}^{4} \Delta t_i$)

	Δt_1	Δt_2	Δt_3	Δt_4
BM1 ($D \leq 0.5$)	$0 \leq t \leq DT_s - t_{tr}$	$DT_s \leq t \leq \frac{T_s}{2} - t_{tr}$	$\frac{T_s}{2} \leq t \leq \frac{(1+2D)T_s}{2} - t_{tr}$	$\frac{(1+2D)T_s}{2} \leq t \leq T_s - t_{tr}$
$v_m^{a,d}(t) < v_m^{b,c}(t)$	State 2	State 4	State 3	State 4
BM2 ($D \geq 0.5$)	$0 \leq t \leq \frac{(1-2D)T_s}{2} - t_{tr}$	$\frac{(1-2D)T_s}{2} \leq t \leq \frac{T_s}{2} - t_{tr}$	$\frac{T_s}{2} \leq t \leq DT_s - t_{tr}$	$DT_s \leq t \leq T_s - t_{tr}$
$v_m^{a,d}(t) > v_m^{b,c}(t)$	State 1	State 2	State 1	State 3

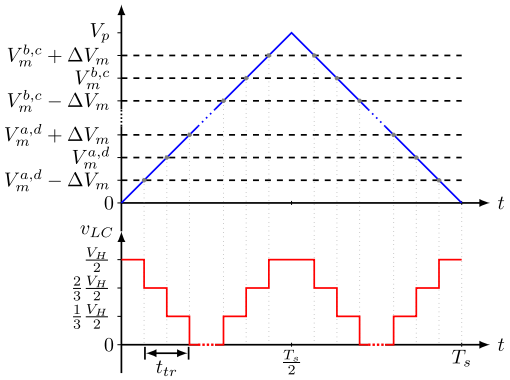


FIGURE 3. Q2L modulation (upper waveforms) and the resulting v_{LC} (lower waveform) for $N = 3$.

modulators and the carrier is

$$\begin{cases} A_a = 1;\ A_d = 0, & \text{if } v_m^{a,d}(t) \geq v_{tri}(t) \\ A_a = 0;\ A_d = 1, & \text{if } v_m^{a,d}(t) < v_{tri}(t) \\ A_b = 0;\ A_c = 1, & \text{if } v_m^{b,c}(t) \geq v_{tri}(t) \\ A_b = 1;\ A_c = 0, & \text{if } v_m^{b,c}(t) < v_{tri}(t) \end{cases} \tag{1}$$

The analysis of (1) leads to two different topology operating modes, where each one uses a distinct set of topological states. These modes are defined as Buck Mode 1 (BM1) and Buck Mode 2 (BM2), being implemented according to the amplitude of $v_m^{a,d}$ and $v_m^{b,c}$.

The converter can change from one mode to another without discontinuities, basically varying $v_m^{a,d}$ and, consequently, $v_m^{b,c}$. It results in only one static and one dynamic model for both modes, simplifying the topology analysis and the controller design.

The Q2L modulation is achieved by adding/subtracting a constant value ΔV_m to/from each modulation signal. Consequently, the SM capacitors will be connected/disconnected to/from the circuit in a sequential order, adding a transition state between every subsequent topological states, as represented in Fig. 3.

The modulation signals condition, the set of states that defines each mode (BM1 or BM2) and the respective duration times are summarized in Table 1., where $0 \leq D \leq 1$ is the duty cycle regarding the time interval that $A_a = \overline{A_d} = 1$. Each transition duration time is defined as $\Delta t_{12} = \Delta t_{23} = \Delta t_{34} = \Delta t_{41} = t_{tr}$.

C. AVERAGE VALUE STATIC ANALYSIS

The objective of this analysis is to achieve a mathematical understanding about the topology currents and voltages average values, when it operates in steady state. From this, the voltage static gain and the equivalent output resistance behavior, which is related to the converter conduction losses and inherent resistive voltage drops, can be obtained.

Some considerations are made in order to simplify the analysis:

- the switches and diodes have the same on-resistance R;
- the switches saturation voltage is V_{sat} and the diodes forward voltage drop is V_f, unless otherwise specified;
- each arm is composed by N SMs, represented by an equivalent SM with capacitance $C_{eq,i}$;
- $t_{tr} << T_s$, making the transition effects negligible;
- the converter operates in BM1, unless otherwise specified.

The state-space representation of each topological state is created from the Kirchoff's Voltage and Current Laws, being defined by

$$\dot{\boldsymbol{x}} = \boldsymbol{A_{st}} \cdot \boldsymbol{x} + \boldsymbol{B_{st}} \cdot \boldsymbol{u}. \tag{2}$$

The state-space inputs are V_H, V_f and V_{sat}; and the state variables are v_{Cf}, $v_{Ceq,a}$, $v_{Ceq,b}$, $v_{Ceq,c}$, $v_{Ceq,d}$, i_{Lo} and v_{Co}. $\boldsymbol{A_{st}}$ and $\boldsymbol{B_{st}}$ are 7-by-7 and 7-by-3 matrices, respectively, where $st \in \{1, 2, 3, 4\}$ represents the respective topological state.

At first, the topology equivalent output resistor characteristic is approached. To achieve this mathematical model, the voltage ripple over $C_{eq,i}$ is considered negligible regarding the respective average value $V_{Ceq,i}$. Moreover, $V_{sat} = V_f = 0$. The inductor current is also considered constant and equal I_{Lo}. Thus, defining $\alpha \in \{\Delta t_1, \Delta t_2, \Delta t_3, \Delta t_4\}$ as the currently analyzed time interval and T_ϕ^α as its respective initial time (e.g. $T_\phi^{\Delta t_2} = DT_s$, for BM1), the solution of (2) for v_{Cf} is

$$v_{Cf}^\alpha = K_{Cf}^\alpha \left[1 - e^{-k_1\left(t - T_\phi^\alpha\right)}\right] + v_{Cf0}^\alpha e^{-k_1\left(t - T_\phi^\alpha\right)}, \tag{3}$$

where

$$\begin{cases} k_1 = \frac{1}{NRC_f} = \frac{f_s}{NRC_f f_s} = \frac{f_s}{h_{Cf}} \\ K_{Cf}^{\Delta t_1} = \frac{V_{Ceq,b} - V_{Ceq,d} + V_H}{2};\ K_{Cf}^{\Delta t_2} = \frac{V_H}{2} \\ K_{Cf}^{\Delta t_3} = \frac{V_{Ceq,c} - V_{Ceq,a} + V_H}{2};\ K_{Cf}^{\Delta t_4} = \frac{V_H}{2} \end{cases} \tag{4}$$

The initial values in (3) can be obtained by recursively equaling each v_{Cf0}^α to the respective previous state final value. The variable $h_{Cf} = NRC_f f_s$ is a dimensionless parameter that

relates the time constant of the RC meshes composed by NR and C_f to the switching frequency f_s (or switching period T_s). The longer is NRC_f regarding T_s, the lower are the current spikes.

Obtaining $i_a^{\Delta t_1}$, $i_a^{\Delta t_2}$ and $i_a^{\Delta t_4}$ from the circuit analysis and knowing that $I_a^{\Delta t_1} = I_{Lo}$, the following relation is achieved

$$\frac{1}{DT_s}\int_0^{DT_s} i_a^{\Delta t_1}(t)\,\mathrm{d}t = I_{Lo}. \tag{5}$$

Solving (5) leads to

$$V_{Ceq,a} = V_{Ceq,c} + \frac{D\left(-V_H + 2V_{Ceq,c} + 2NRI_{Lo}\right)k_{r2}}{h_{Cf}k_{r1} - Dk_{r2}}, \tag{6}$$

where

$$k_{r1} = e^{\frac{1+4D}{2h_{Cf}}} - 2e^{\frac{1+2D}{2h_{Cf}}} + e^{\frac{1}{2h_{Cf}}} + e^{\frac{1+D}{h_{Cf}}} - e^{\frac{2D}{h_{Cf}}} + e^{\frac{D}{h_{Cf}}} - e^{\frac{1}{h_{Cf}}} \tag{7}$$

and

$$k_{r2} = \left(e^{\frac{1}{h_{Cf}}} - 1\right)e^{\frac{D}{h_{Cf}}}. \tag{8}$$

On the other hand, $i_b^{\alpha} = i_a^{\alpha} - i_{Cf}^{\alpha}$ average value is zero within the interval from the beginning of Δt_4 until the end of Δt_2 and the following relation is achieved

$$\frac{1}{(1-D)T_s}\int_{-(1-D)T_s}^{\frac{T_s}{2}} i_b^{\alpha}(t)\,\mathrm{d}t = 0. \tag{9}$$

Solving (9) leads to

$$V_{Ceq,c} = \frac{V_H}{2} - NRI_{Lo}\left[1 - (1-D)\,k_{r3}\right] \tag{10}$$

and, replacing (10) in (6), takes to

$$V_{Ceq,a} = \frac{V_H}{2} + NRI_{Lo}\left(1 - Dk_{r3}\right), \tag{11}$$

where

$$k_{r3} = \frac{2\left(h_{Cf}k_{r1} + Dk_{r2}\right)}{h_{Cf}k_{r1} - D\left(1-2D\right)k_{r2}}. \tag{12}$$

The LC filter input voltage during Δt_1 and Δt_2 can be described by

$$v_{LC}^{\Delta t_1} = V_H - V_{Ceq,b} - NR\left(i_a^{\Delta t_1} + i_b^{\Delta t_1}\right) \tag{13}$$

and

$$v_{LC}^{\Delta t_2} = V_H - V_{Ceq,a} - V_{Ceq,b} - NR\left(i_a^{\Delta t2} + i_b^{\Delta t_2}\right), \tag{14}$$

which results in

$$V_o = V_{LC} = \frac{V_H}{2} - V_{Ceq,a}(1-D) + V_{Ceq,d}D - NRI_{Lo}. \tag{15}$$

It is shown in the subsequent analysis that $V_{Ceq,a} = V_{Ceq,b}$ and $V_{Ceq,c} = V_{Ceq,d}$. Therefore, replacing (10) and (11) in (15) leads to

$$V_o = DV_H - \underbrace{2NR\left[1 - D\left(1-D\right)k_{r3}\right]}_{R_{eqo}}I_{Lo}, \tag{16}$$

where R_{eqo} is a function of h_{Cf} and D that represents the topology equivalent output resistance. Since $R_{eqo}(h_{Cf}, D)$ is a quite large exponential equation, that do not provide a clear idea of the responses caused by varying h_{Cf} and D, it is decided to present an abacus to illustrate R_{eqo}.

The lowest $R_{eqo}(h_{Cf}, D)$ value is $2NR$, which is obtained when $h_{Cf} \to \infty$. This value can be used to normalize R_{eqo}, as follows

$$\overline{R_{eqo}}(h_{Cf}, D) = \frac{R_{eqo}}{\lim\limits_{h_{Cf}\to\infty} R_{eqo}} = \frac{R_{eqo}}{2NR}. \tag{17}$$

Sweeping (17) for different values of h_{Cf} and D results in the abacus presented in Fig. 4(a), which is intended to be used as a design guideline to find C_f or the switching frequency f_s. As typical for SC converters, the increase of h_{Cf} leads the converter to operate in Partial Charge (PC) and No Charge (NC) modes [26], where $\overline{R_{eqo}}$ and, consequently, the conduction losses are both reduced, because of the lower current spikes caused by the capacitors parallel connections. However, it also makes $\overline{R_{eqo}}$ to be more independent of D, which is an interesting characteristic in terms of the converter efficiency when it is operated in closed-loop, since duty cycle variations will not significantly increase the conduction losses.

In order to reduce the conduction power losses and its duty cycle dependence, it is considered, from now on, that the converter operates with $h_{Cf} \geq 0.5$. Within this region, the maximum value that $\overline{R_{eqo}}$ can assume is 1.04, approximately, which leads to an acceptable conduction loss penalty. Moreover, the $\overline{R_{eqo}}$ variation with D is not significant. However, it must be considered that the reduction rate of $\overline{R_{eqo}}$ decreases for higher h_{Cf} values. In other words, the reduction in conduction losses tends to not worth regarding the switching frequency and/or C_f increase, which is necessary to achieve such high h_{Cf}. In this case, the switching losses and/or capacitor volume/weight tend to be the converter limitation.

Taking into account that additional resistances and inductances will be part of the converter, due to the actual components and PCB characteristics, a better damp of the current spikes tends to be achieved in real operation. Therefore, to simplify the converter design, it is assumed that this additional impedance sufficiently increases the total loop resistance, so that the definition of R as the highest conduction resistance between the used switch and diode results in a good trade-off between current spikes and component design.

Continuing the average value analysis, from (2) is also possible to obtain the following average value matrix

$$\boldsymbol{A} = \boldsymbol{A_2}\cdot D + \boldsymbol{A_4}\cdot\frac{(1-2D)}{2} + \boldsymbol{A_3}\cdot D + \boldsymbol{A_4}\cdot\frac{(1-2D)}{2}. \tag{18}$$

The matrix $\boldsymbol{B}$ is similarly obtained.

In steady state, $\dot{\boldsymbol{x}} = 0$. Therefore, the state-space variables average values are calculated by

$$\boldsymbol{X} = -\boldsymbol{A}^{-1}\cdot\boldsymbol{B}\cdot\left[V_H\; V_f\; V_{sat}\right]^T, \tag{19}$$

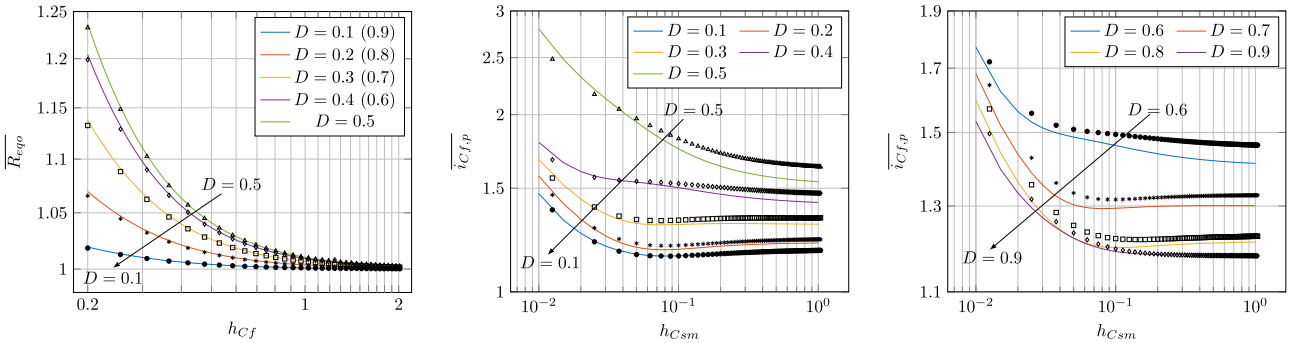


FIGURE 4. Abacus relating (a) $\overline{R_{eqo}}$, h_{Cf} and D (b) $\overline{i_{Cf,p}}$, h_{Csm} and D for BM1 (c) $\overline{i_{Cf,p}}$, h_{Csm} and D for BM2. Abacus of $\overline{i_{Cf,p}}$ obtained considering $N = 3$, $h_{Cf} = 0.5$, $t_{tr} = 0.02T_s$ and $p = 0.25$.

that results in

$$\boldsymbol{X} = \begin{bmatrix} V_{Cf} \\ V_{Ceq,a} \\ V_{Ceq,b} \\ V_{Ceq,c} \\ V_{Ceq,d} \\ I_{Lo} \\ V_{Co} \end{bmatrix} = \begin{bmatrix} \frac{V_H}{2} \\ \frac{V_H}{2} + NRI_{Lo} + NV_f \\ \frac{V_H}{2} + NRI_{Lo} + NV_f \\ \frac{V_H}{2} - NRI_{Lo} - NV_s \\ \frac{V_H}{2} - NRI_{Lo} - NV_s \\ \frac{V_H D}{2NR+R_o} - k_{dr}^{out} \\ \frac{V_H DR_o}{2NR+R_o} - k_{dr}^{out} R_o \end{bmatrix}, \tag{20}$$

where R_o is the load equivalent resistance and

$$k_{dr}^{out} = \frac{2N\left[(1-D)V_f + DV_{sat}\right]}{2NR + R_o}. \tag{21}$$

It is verified in (20) that the total voltage average value on each upper arm is slightly higher than on each lower arm. It is due to the output current circulation through the semiconductors conduction resistances, which generates voltage drops that increase the upper arms and decrease the lower arms voltages.

Since $V_{Co} = V_o$, the topology voltage static gain ($\overline{M_{VDC}}$) is defined by

$$\overline{M_{VDC}} = \frac{V_{Co} + k_{dr}^{out}}{V_H} = \frac{DR_o}{2NR + R_o}. \tag{22}$$

Replacing (20) in (2) for the used set of topological states, average value representations of C_f and $C_{eq,i}$ currents (I_{Cf}^{α} and $I_{Ceq,i}^{\alpha}$, respectively) are achieved for each time interval α. Therefore, applying the RMS mathematical definition to I_{Cf}^{α} along T_s, the RMS values of C_f currents for BM1 and BM2 are respectively defined as

$$I_{Cf,BM1}^{rms} = I_{Lo}\sqrt{2D} \tag{23}$$

and

$$I_{Cf,BM2}^{rms} = I_{Lo}\sqrt{2\,(1-D)} \tag{24}$$

Similarly, the average and RMS values of the equivalent SM lower switches ($S_{i,L}$) currents, shown in Table 2., can be obtained. These equations are valid for BM1 and BM2.

TABLE 2 Switches Average and RMS Currents

	AVG	RMS
$S_{a,L} = S_{b,L}$	$I_{Lo}D$	$I_{Lo}\sqrt{D}$
$S_{c,L} = S_{d,L}$	$I_{Lo}(D-1)$	$I_{Lo}\sqrt{1-D}$

It is important to mention that (20) is only valid when the converter operates in PC or NC, which are the charge modes aimed by the topology operation to minimize the conduction losses.

Despite of the method usefulness, the consideration of only average values results in zero voltage ripple on $C_{eq,i}$ and no current spikes. However, this is not a practical condition and non-linear currents will flow through $C_{eq,i}$ and C_f. By estimating the current spikes values, it is possible to better calculate the converter switching losses and to prevent possible EMI issues. Furthermore, high power semiconductors with significant on resistances, such as SiC and silicon IGBT, may be used to build the converter, demanding a detailed conduction losses calculation. For this reason, an instant value analysis is developed to allow an estimation of C_f peak current ($i_{Cf,p}$) and of the SM capacitors currents RMS ($I_{Csm,i}^{rms}$) values.

D. INSTANT VALUE STATIC ANALYSIS

This analysis basically consists in obtaining $C_{eq,i}$ voltages and currents equations as functions of time by solving (2). Once the analyzed system is composed by seven state variables, it is considered that, for simplification purposes, $V_{sat} = V_f = 0$ and v_{Cf} is defined by (3). Additionally, i_{Lo} time equations can be defined using (20) to find v_{Lo} for the used topological states, since $h_{Cf} \geq 0.5$.

At first, considering only BM1, the transition states influence on this analysis has to be addressed. During t_{tr}, an equivalent SM capacitor per arm is defined as follows

$$C_{eq,i}^{tr} = \frac{C_{sm} + \frac{C_{sm}}{N-1}}{2} = \frac{NC_{sm}}{2\,(N-1)}. \tag{25}$$

Analyzing the interval from the beginning of Δt_{41} until the end of Δt_{12}, it can be stated that $I_d = 0$ and the L_o current

TABLE 3 Values of the Constants Used in $v_{Ceq,a}^{\{\alpha,\beta\}}$ and $v_{Ceq,d}^{\{\alpha,\beta\}}$

$\{\alpha,\beta\}$	K_{q1}	K_{q2}
Δt_2	$\frac{2\left(\Delta v_{Cf}^{\Delta t_4} - NR\Delta i_{Lo}^{\Delta t_4}\right)}{k_2[(1-2D)T_s - 2t_{tr}]}$	$v_{Cf0}^{\Delta t_4} + NRi_{Lo0}^{\Delta t_4} - K_{q1}$
Δt_{23}	0	$V_H - v_{Cf0}^{\Delta t_{23}} + NRi_{Lo0}^{\Delta t_{23}}$
Δt_3	$\frac{2\left(\Delta v_{Cf}^{\Delta t_1} + NR\Delta i_{Lo}^{\Delta t_1}\right)}{k_2(DT_s - t_{tr})}$	$v_{Cf0}^{\Delta t_1} + NRi_{Lo0}^{\Delta t_1} - K_{q1}$
Δt_{34}	0	$V_H - v_{Cf0}^{\Delta t_{34}} + NRi_{Lo0}^{\Delta t_{34}}$
Δt_4	$-\frac{2\left(NR\Delta i_{Lo}^{\Delta t_2} + \Delta v_{Cf}^{\Delta t_2}\right)}{k_2[(1-2D)T_s - 2t_{tr}]}$	$v_{Cf0}^{\Delta t_2} + NRi_{Lo0}^{\Delta t_2} - K_{q1}$
α	K_{q3}	K_{q4}
Δt_1	$-\frac{2\left(NR\Delta i_{Lo}^{\Delta t_3} + \Delta v_{Cf}^{\Delta t_3}\right)}{k_2(DT_s - t_{tr})}$	$v_{Cf0}^{\Delta t_3} - NRi_{Lo0}^{\Delta t_3} - K_{q3}$

average value is I_{Lo}. Furthermore, according to the Table 2, $I_a = I_{Sa,L} = I_{Lo}D$ during Δt_1. With some mathematical manipulation, it results in

$$I_{Ceq,a}^{\Delta t_{12}} + I_{Ceq,a}^{\Delta t_{41}} = I_{Lo}, \tag{26}$$

where $I_{Ceq,a}^{\Delta t_{12}}$ and $I_{Ceq,a}^{\Delta t_{41}}$ are the $C_{eq,a}^{tr}$ currents average values during the respective transition intervals.

The currents that flows through C_{eq}^{tr} have a stepped waveform, due to the SMs voltages sorting algorithm. As an approximation, this current is considered to be a ramp that varies $|I_{Lo}|$ during t_{tr}. Thus, $C_{eq,i}^{tr}$ voltages can be defined as

$$v_{Ceq,i}^{\beta}(t) = \frac{I_{Lo}(t - T_{\phi}^{\beta})^2}{C_{eq}^{tr} t_{tr}} + v_{Ceq0,i}^{\beta}, \tag{27}$$

where $\beta \in \{\Delta t_{12}, \Delta t_{23}, \Delta t_{34}, \Delta t_{41}\}$ defines the considered transition interval and T_{ϕ}^{β} its respective initial time (e.g. $T_{\phi}^{\Delta t_{12}} = DT_s - t_{tr}$).

The same method used to obtain (3) can be applied to define $v_{Ceq,i}^{\{\alpha,\beta\}}$, which results in

$$v_{Ceq,a}^{\{\alpha,\beta\}} = R_a + v_{Ceq0,a}^{\{\alpha,\beta\}} e^{-k_2\left(t - T_{\phi}^{\{\alpha,\beta\}}\right)} \tag{28}$$

and

$$v_{Ceq,d}^{\Delta t_1} = K_{q3}k_2 t + K_{q4}\left(1 - e^{-k_2 t}\right) + v_{Ceq0,d}^{\Delta t_1} e^{-k_2 t}, \tag{29}$$

where

$$R_a = K_{q1}k_2\left(t - T_{\phi}^{\{\alpha,\beta\}}\right) + K_{q2}\left[1 - e^{-k_2\left(t - T_{\phi}^{\{\alpha,\beta\}}\right)}\right]. \tag{30}$$

The voltages $v_{Ceq,b}$ and $v_{Ceq,c}$ are defined as $v_{Ceq,a}(t - \pi)$ and $v_{Ceq,d}(t - \pi)$, respectively. The constants of (29) and (30) are shown in Table 3., where $k_2 = 1/2RC_{sm}$, Δi_{Lo}^{α} is the variation of i_{Lo} in the interval α and Δv_{Cf}^{α} is the variation of v_{Cf} in the interval α.

Taking $C_{eq,a}$ and $C_{eq,d}$ currents from (28) and (29), respectively, $i_{Cf,p}$ can be obtained. For BM1, the peak value happens at the beginning of Δt_1 and can be normalized regarding I_{Lo}, resulting in

$$\overline{i_{Cf,p}} = \frac{i_{Cf,p}}{I_{Lo}} = i_{Lo0}^{\Delta t_1} + i_{Ceq0,d}^{\Delta t_1} - i_{Ceq0,a}^{\Delta t_1}. \tag{31}$$

The normalized current $\overline{i_{Cf,p}}$ is a quite large equation, function of h_{Csm}, D, N, h_{Cf}, t_{tr} and $p = \Delta I_{Lo}/I_{Lo}$, where ΔI_{Lo} is the L_o peak-to-peak current ripple and $h_{Csm} = RC_{sm}f_s$. A similar process can be done to achieve $\overline{i_{Cf,p}}$ for BM2.

To provide a better understanding of $\overline{i_{Cf,p}}$, the abacus of Figs. 4(b) and 4(c) are generated, where $\overline{i_{Cf,p}}$ is plotted for different values of h_{Cf} (changing C_{sm}) and D, adopting $N = 3$, $t_{tr} = 0.02T_s$ and $p = 0.25$. Since $\overline{i_{Cf,p}}$ tends to increase for lower values of h_{Cf}, it is defined $h_{Cf} = 0.5$, in order to have a worst case analysis.

The normalized peak current tends to be lower and to have less sensibility, regarding h_{Csm} variations, when h_{Csm} increases. It is because a higher C_{sm} reduces the ripple of $v_{Ceq,i}$, which becomes more negligible regarding $V_{Ceq,i}$. Therefore, the latter ends up predominating on $i_{Cf,p}$ behavior.

It is noticed that $\overline{i_{Cf,p}}$ increases when $D \to 0.5$. This is because a pair of complementary arms tends to perform the SC connections on the same instant, the more D approaches to 0.5. It means that both arms peak currents will occur with a short time difference between each other. Since part of i_{Cf} is composed by these currents overlap, it results in a higher $i_{Cf,p}$.

Despite the assumed simplifications, the errors are within an acceptable tolerance (maximum of 5.7% for $D = 0.5$). Therefore, the presented methodology can be used as a $\overline{i_{Cf,p}}$ related design guideline for C_{sm}.

The equations (28) and (29) can be used to calculate the respective RMS values of the capacitors currents. To achieve a better precision, the sorting algorithm effect can be taken into account. These currents acquire a stepped waveform during the transitions, where the amount of steps, with $t_{tr}/(N-1)$ duration time, increases/decreases every time the arm is transitioned. It means that the current of each SM capacitor changes in amplitude and duration, cycling in a frequency of f_s/N due to the sorting logic.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A laboratory scale prototype is used to proceed with the experimental verification of the topology operation. The prototype picture is presented in Fig. 5, whereas the parameters and components specification is described in Table 4.. For C_f and C_{sm} film capacitors are used, due to their low ESR. The former capacitance is chosen to respect $h_{Cf} \geq 0.5$, whilst the laboratory component availability defined the latter. The inductance L_o is chosen in order that $\Delta i_{Lo} \leq 0.25I_{Lo}$ and the capacitance C_o is designed so that the output filter resonance frequency is $f_s/20$, at least. The output power is defined according to the available load bank.

Generally, SC converters are implemented with MOSFETs, due to their resistive conduction characteristic. However, IGBTs with ultrafast soft recovery diodes are used in this case,

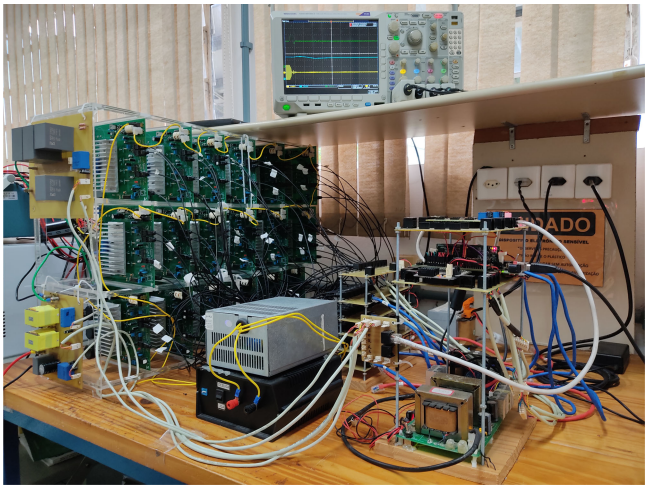


FIGURE 5. Converter prototype.

TABLE 4 Converter Specification

Parameter	Value
Output power (P_o)	1.17 kW
Input voltage (V_H)	350 V
Output voltage (V_o)	200 V
Number of SMs per arm (N)	3
Switching frequency (f_s)	12.5 kHz
Flying capacitor (C_f)	2x MKPC4AQ - 22 μF/1500 V 2x MKPC4AQ - 15 μF/1500 V
SM capacitor (C_{sm})	1x MKP1848 - 8 μF/700 V
Output capacitor capacitance (C_o)	125 μF
Inductor inductance (L_o)	853.23 μH
Semiconductors	IGBT IRGP50b60PD

due to the laboratory components availability. Despite of being an oversized IGBT regarding the prototype parameters, there is the interest to verify the operational viability of using this technology in a HSC topology. Since IGBTs tend to have a higher conduction current capability than MOSFETs, the use of the former would increase the topology power processing level.

The first order model of an conducting IGBT is composed by a resistance plus V_{sat}. As V_{sat} is not considered in the instant value analysis, the converter can be designed by adopting an equivalent conduction resistance composed by the sum of (V_{CE}, I_C) curve slope and V_{sat}/I_C, for $I_C = I_o$, resulting in $R = 0.2\,\Omega$.

The converter operation is analyzed for the two different buck modes. Since the specified parameters of Table 4 result in $D = 0.6$, the rated converter operation occurs in BM2. For BM1, it is defined $D = 0.35$. Furthermore, all the experimental waveforms presented are obtained with the prototype working in closed-loop for $V_{Cf} = 175$ V to assure a balanced operation.

A. STEADY STATE RESULTS

As expected, v_{LC} acquires different amplitude levels, depending on the topology operation mode, which results in different V_o and ΔI_{Lo}. These behaviors are presented in Figs. 6 and 7. The voltage v_o assumed 118.3 V, 166.7 V and 201.67 V against the theoretical values 114 V, 164 V and 199 V for $D < 0.5$, $D = 0.5$ and $D > 0.5$, respectively. Moreover, when $D = 0.5$, only the topological states 2 and 4 are used, leading to $v_{LC} = 175$ V during almost whole T_s. Consequently, ΔI_{Lo} is significantly minimized in this operation condition.

Focusing on the rated operation waveforms (BM2), $\Delta I_{Lo} = 1.3$ A, which corresponds to 21.7% of $I_{Lo} = 5.83$ A, and $i_{Cf,p} = 7.17$ A, resulting in an experimental $\overline{i_{Cf,p}} = 1.23$. The defined topology parameters lead to $h_{Cf} = 0.56$ and $h_{Csm} = 0.02$. Relating the latter value with Fig. 4(c) results in a theoretical $\overline{i_{Cf,p}} = 1.56$. The difference regarding the experimental value is explained by the presence of the circuit stray resistances and inductances. Since the prototype is not designed to minimize these elements, the lower experimental $\overline{i_{Cf,p}}$ is expected. Moreover, the considered abacus is implemented to a defined worst case, where $h_{Cf} = 0.5$, also contributing for the obtained difference.

There is a predominance of i_{Lo} over the switched capacitor exponential currents in i_{Cf} composition. It is indicated by the nearly trapezoidal shaped v_{Cf} ac component presented in the detailed waveform of Fig. 8(a). This behavior is consequence of choosing $h_{Cf} \geq 0.5$, since it places the SC converter stage in PC or NC operation.

The effects of the transition between topological states on v_{LC} and i_{Cf}, generated by the Q2L modulation, are presented in Fig. 8(b) for BM2. Despite of the high frequency oscillations, caused by the interaction of the circuit stray inductances and the semiconductors output capacitors, the voltage steps are clearly defined on v_{LC}, as expected. It can also be noticed that, between every two steps, i_{Cf} pattern changes during a short period. This behavior is caused by the SMs dead time and the stray inductances in series with each arm. When in dead time state, the SMs upper diodes become forward biased because of the stray inductances voltages, generated to keep the flowing direction of the arms currents. Considering $D > 0.5$, this behavior does not change the voltage levels applied on the filter input. On the other hand, when $D = 0.5$, the two pairs of complementary arms are transitioned at the same time, clamping the stray inductances voltages in a value that increases v_{LC} during the dead time periods, as shown in Fig. 8(c). It does not change the topology basic operation when $D = 0.5$, however, it may influence on L_o physical design, due to the variation of v_{Lo}.

The voltages on the upper arms SM capacitors are slightly higher than on the lower arms, stabilizing in 61 V and 57 V, respectively, as depicted in Fig. 9(a). The calculated theoretical values are 59.6 V and 57.1 V, respectively. The high frequency distortions in both waveforms are switching noises circulating through the switches stray capacitances.

B. LOAD STEP RESPONSES

The SM sorting algorithm, implemented with the Q2L modulation, achieves the expected voltage equalization within the arms. To evaluate this functionality, a load step is performed,

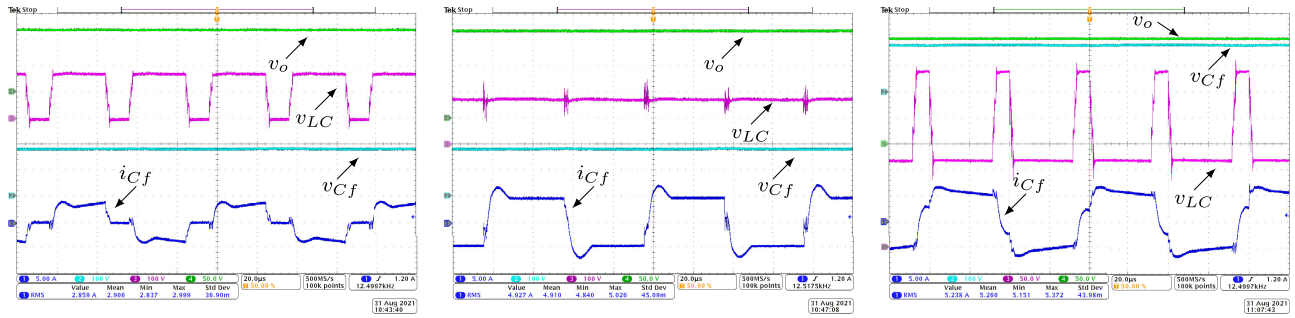


FIGURE 6. i_{Cf} (Ch 1 - 5 A/div), v_{Cf} (Ch 2 - 100 V/div), v_{LC} (Ch 3 - 100 V/div) and v_o (Ch 4 - 50 V/div) steady state waveforms (20 μs/div) with: (a) $D < 0.5$ (b) $D = 0.5$ and (c) $D > 0.5$.

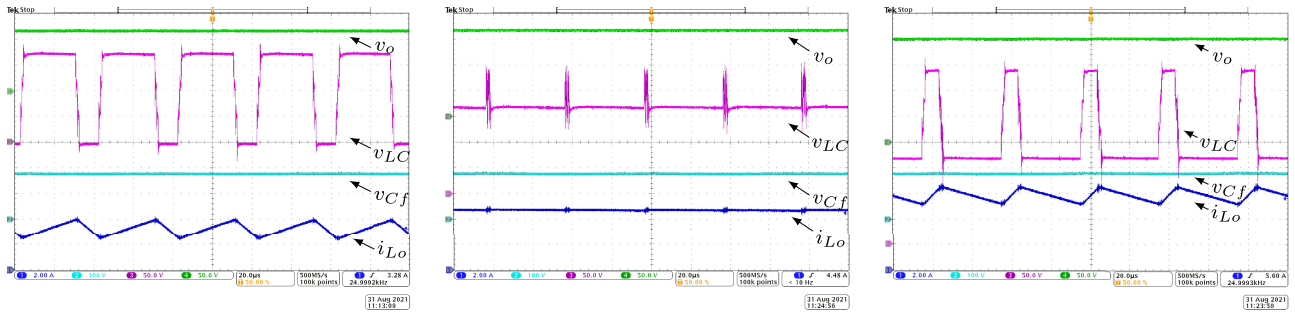


FIGURE 7. i_{Lo} (Ch 1 - 2 A/div), v_{Cf} (Ch 2 - 100 V/div), v_{LC} (Ch 3 - 50 V/div) and v_o (Ch 4 - 50 V/div) steady state waveforms (20 μs/div) with: (a) $D < 0.5$ (b) $D = 0.5$ and (c) $D > 0.5$.

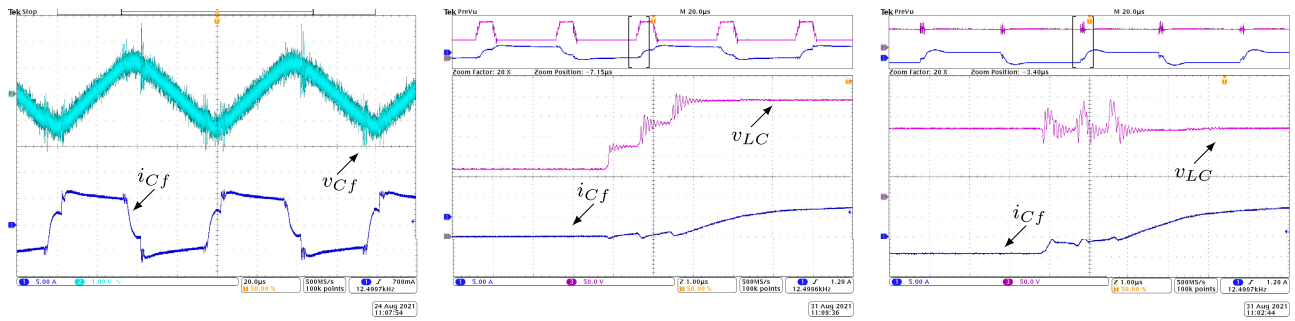
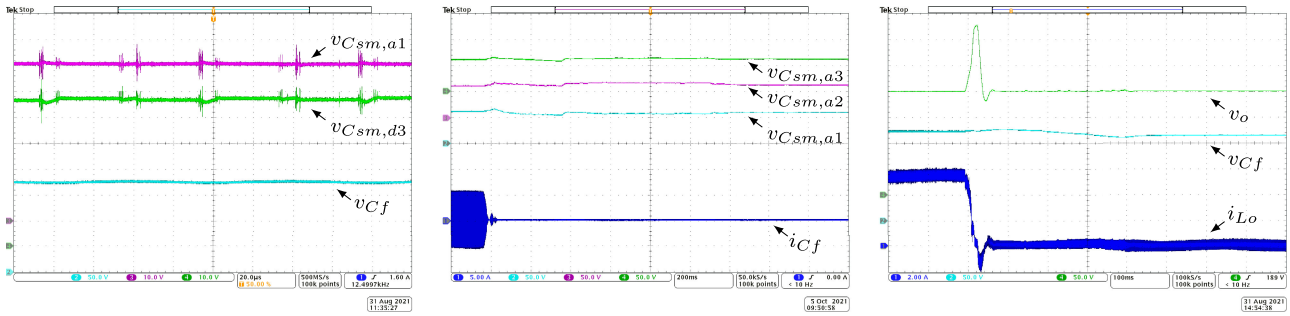


FIGURE 8. Detailed waveforms of: (a) i_{Cf} (Ch 1 - 5 A/div) and v_{Cf} (Ch 2 - AC coupling - 1 V/div) for $D > 0.5$ (20 μs/div) (b) i_{Cf} (Ch 1 - 5 A/div) and v_{LC} (Ch 3 - 50 V/div) for $D > 0.5$ (1 μs/div) and (c) i_{Cf} (Ch 1 - 5 A/div) and v_{LC} (Ch 3 - 50 V/div) for $D = 0.5$ (1 μs/div).

decreasing from 100% to 0% of the rated output power. The disturbance behavior of the A_a SM capacitors voltages is presented in Fig. 9(b), where the proper equalization process can be noticed, with small deviation during the transient period.

With the converter operating in closed-loop for V_o, V_{Cf} and I_{Lo}, the zero load operation stability and the topology bidirectional characteristic are verified. The prototype is designed with a low C_o value, in order to assess the converter performance during considerable v_o undershoot and overshoot conditions.

Applying the same mentioned load step, V_o converges and stabilizes to the rated value after the transition period, as depicted in Fig. 9(c). This behavior also indicates the power flux reversion. When the load is removed, v_o increases. Consequently, the inductor voltage assumes a negative average value and I_{Lo} starts to decrease. When the direction of I_{Lo} is changed, i.e. $I_{Lo} < 0$, the topology boost operation begins and energy starts to be processed from the low to the high voltage dc bus. Therefore, the output capacitor surplus charge is sent back to the converter input source after the load step. If the bidirectional feature was not available, the output voltage



(a) (b) (c)

FIGURE 9. Steady state waveforms of (a) v_{Cf} (Ch 2 - 50 V/div), $v_{Csm,a1}$ (Ch 3 - 10 V/div) and $v_{Csm,d3}$ (Ch 4 - 10 V/div) for $D > 0.5$ (20 μs/div). The 100% to 0% load step transient waveforms of: (b) i_{Cf} (Ch1 - 5 A/div), $v_{Csm,a1}$ (Ch 2 - 50 V/div), $v_{Csm,a2}$ (Ch 3 - 50 V/div) and $v_{Csm,a3}$ (Ch 4 - 50 V/div) during a 100% to 0% load step (200 ms/div) and (c) i_{Lo} (Ch 1 - 2 A/div), v_{Cf} (Ch 2 - 50 V/div) and v_o (Ch 4 - 50 V/div) (100 ms/div).

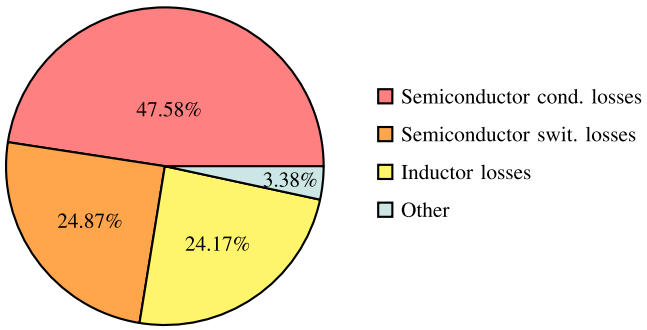


FIGURE 10. Converter losses distribution.

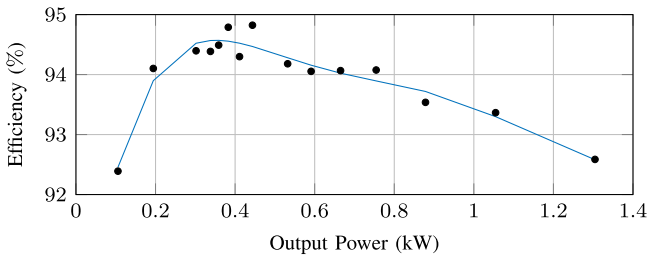


FIGURE 11. Experimental efficiency data and trend curve.

would settle in a higher amplitude level, because the remaining inductor energy would be transferred to C_o and there would be no path to send this energy back to V_H.

It can also be noticed that V_{Cf} converges to a slightly different value after the disturb. This is because the variation of V_{Cf} is physically performed by I_{Lo}, that becomes too low to compensate the small static error in no load operating condition. Additionally, it is verified that the converter operation mode can be naturally changed from BM2 to BM1.

C. POWER LOSSES ANALYSIS

The achieved converter efficiency is 93.3% on the rated P_o and the estimated losses distribution for this condition is shown in Fig. 10, where it is noticeable the semiconductors conduction losses prevalence on the overall converter losses. The other losses percentage covers capacitors, wires and connections.

The obtained efficiency curve presents a typical buck-type behavior, indicating the negligible duty cycle influence on R_{eqo}. The experimental data points and the respective trend curve are presented in Fig. 11 and are obtained with the converter operating in closed-loop, with $V_o = 200$ V being applied on different load values. The efficiency reduction for $P_o < 360$ W is due to the switching losses predominance over the conduction losses. However, this scenario is reverted when $P_o > 360$ W. In this case, the higher P_o, the lower is the difference between R_o and R_{eqo}, causing the efficiency decrease, influenced by the conduction losses, mostly.

IV. CONCLUSION

A bidirectional MMC based HSC dc-dc topology is proposed. It can be composed by different SM configurations (HB, FB, NPC, etc), according to the application requirements, and the number of SMs per arm is defined in order to attend the semiconductors blocking voltage limit. The Q2L modulation allows the equalization of the SMs capacitors voltages within each arm.

The absence of arm inductors allows the total arms voltages automatic clamping on half the input voltage, eliminating the need for a voltage balancing control among the arms. On the other hand, the acquired SC converter characteristics demand a low, duty cycle independent, output equivalent resistance and low current spikes oriented design, in order to increase the topology efficiency and to avoid harmful EMI issues.

Based on the achieved theoretical and experimental results, it can be inferred that the proposed topology can be suitable to attend low to medium voltage dc-dc applications, in the range of tens to hundreds of kW, such as medium/low voltage dc grids interconnection, electrical vehicles, data centers, UPS, vessels and railway systems. The main bottlenecks that limit the use for higher voltages and powers are: the voltage applied to the flying capacitor, that, depending on the required capacitance, may lead to an expensive and bulky capacitor bank;

the semiconductors switching speed attached to the number of SMs, since the transition time must be reasonable to cover all the steps and, at the same time, considerably lower than f_s; and the hard switching characteristic, that limits the increase of f_s.

Some future works suggestions are: converter implementation with GaN and SiC technologies, since some of the mentioned issues tend to be naturally addressed by them; flying capacitor replacement by MMC SMs, in order to overcome the bulky capacitor bank for high power and voltage applications; an interleaved topology variation can be evaluated, where two or more parallel connected converters divide the total power processing, allowing the increase of f_s and, consequently, the use of faster semiconductors and smaller passive components; and the study of MMC based HSC dc-ac topologies.

REFERENCES

[1] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated DC/DC structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015.

[2] G. Lambert, M. V. Soares, P. Wheeler, M. L. Heldwein, and Y. R. de Novaes, "Current-fed multipulse rectifier approach for unidirectional HVDC and MVDC applications," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3081–3090, Apr. 2019.

[3] X. Xiang, X. Zhang, T. Lüth, M. M. C. Merlin, and T. Green, "A compact modular multilevel DC-DC converter for high step-ratio MV and HV use," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7060–7071, Sep. 2018.

[4] S. Milovanovic and D. Dujic, "High-power DC–DC converter utilising scott transformer connection," *IET Electric Power Appl.*, vol. 13, no. 10, pp. 1441–1452, Apr. 2019. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/iet-epa.2018.5746

[5] A. Schön and M.-M. Bakran, "A new HVDC-DC converter for the efficient connection of HVDC networks," in *Proc. Europe Int. Exhib. Conf. Power Electron. Intell. Motion Renewable Energy Manage*. Nürnberg: VDE Verlag GmbH, 2013, pp. 525–532.

[6] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A novel medium-voltage modular multilevel DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7939–7949, Dec. 2016.

[7] S. Du, B. Wu, D. Xu, and N. R. Zargari, "A transformerless bipolar multistring DC/DC converter based on series-connected modules," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1006–1017, Feb. 2017.

[8] S. Du and B. Wu, "A transformerless bipolar modular multilevel DC-DC converter with wide voltage ratios," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8312–8321, Nov. 2017.

[9] S. Du, B. Wu, and N. R. Zargari, "A transformerless high-voltage DC–DC converter for DC grid interconnection," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 282–290, Feb. 2018.

[10] S. H. Kung and G. J. Kish, "A modular multilevel HVDC buck-boost converter derived from its switched-mode counterpart," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 82–92, Feb. 2018.

[11] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel DC/DC converter with fault blocking capability for HVDC interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 148–162, Jan. 2015.

[12] H. You and X. Cai, "A three-level modular DC/DC converter applied in high voltage DC grid," *IEEE Access*, vol. 6, pp. 25448–25462, 2018.

[13] H. You and X. Cai, "Stepped 2-level operation of non-isolated modular DC/DC converter applied in high voltage DC grid," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1540–1552, Sep. 2018, doi: 10.1109/JESTPE.2017.2784426.

[14] P. Gray, P. W. Lehn, and N. Yakop, "A modular multilevel DC–DC converter with flying capacitor converter like properties," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6774–6783, Jul. 2022.

[15] P. A. Gray and P. W. Lehn, "The current shaping modular multilevel DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10050–10063, Oct. 2020.

[16] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[17] T. B. Lazzarin, R. L. Andersen, and I. Barbi, "A switched-capacitor three-phase AC–AC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 735–745, Feb. 2015.

[18] M. D. Vecchia, M. A. Salvador, and T. B. Lazzarin, "Hybrid nonisolated DC–DC converters derived from a passive switched-capacitor cell," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3157–3168, Apr. 2018.

[19] C. Schaef, J. Rentmeister, and J. T. Stauth, "Multimode operation of resonant and hybrid switched-capacitor topologies," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10512–10523, Dec. 2018.

[20] M. A. Salvador, T. B. Lazzarin, and R. F. Coelho, "High step-up DC–DC converter with active switched-inductor and passive switched-capacitor networks," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5644–5654, Jul. 2018.

[21] Y. Zhang, H. Liu, J. Li, M. Sumner, and C. Xia, "DC–DC boost converter with a wide input range and high voltage gain for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4100–4111, May 2019.

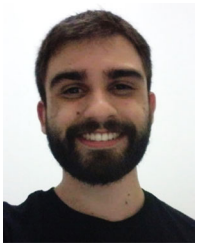
[22] X. Zhu, K. Ye, K. Liu, and B. Zhang, "Non-isolated high step-up DC–DC converter with passive switched-inductor-capacitor network," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, early access, doi: 10.1109/JESTPE.2021.3125403.

[23] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.

[24] P. Czyz, P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "New 40kv–300kva quasi-2-level operated 5-level flying capacitor sic "super-switch" IPM," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 813–820.

[25] M. V. Soares, G. Lambert, and Y. R. de Novaes, "Hybrid switched capacitor DC–DC converter based on MMC," in *Proc. IEEE 15th Braz. Power Electron. Conf. 5th Southern Power Electron. Conf.*, 2019, pp. 1–6.

[26] S. Ben-Yaakov, "Behavioral average modeling and equivalent circuit simulation of switched capacitors converters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 632–636, Feb. 2012.



MARCUS VIEIRA SOARES was born in Tubarão, Santa Catarina, Brazil, in 1990. He received the B.S. degree in electrical engineering from Santa Catarina State University (UDESC), Joinville, Brazil, in 2015, and the M.S. and Ph.D. degrees from the Electrical Energy Processing Group (nPEE), UDESC, in 2017 and 2022, respectively.

YALES RÔMULO DE NOVAES (Member, IEEE) was born in Indaial, Santa Catarina, Brazil, in 1974. He received the B.S. degree in electrical engineering from Regional University of Blumenau (FURB), Blumenau, Brazil, in 1999, and the M.Eng. and Dr. degrees from the Power Electronics Institute (INEP), Federal University of Santa Catarina, Florianópolis, Brazil, in 2000 and 2006, respectively. In 2001, he was a Researcher Engineer with the same institute. From 2006 to 2008, he was a Postdoctoral Fellow with the Industrial Electronics Laboratory, École Polytechnique Fédéral de Lausanne, Lausanne, Switzerland. From 2008 to 2010, he was a Scientist with the Power Electronics Systems Group, ABB Corporate Research Center, Daetwill, Switzerland. He is currently an Associate Professor with UDESC - Santa Catarina State University, Joinville, Brazil, and a Coordinator of CMEAR (Research Cell on Microgrids of Alternative and Renewable Energies).