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1 kW MHz Wideband Class E Power Amplifier

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ABSTRACT Class E power amplifiers are widely used in high-frequency applications due to their simplicity and use of only one ground-referenced switch. However, Class E power amplifiers are usually tuned to operate at a fixed frequency due to their resonant nature. Extending the bandwidth of these switch-mode power amplifiers is beneficial in many applications, such as plasma generators and wireless power transfer systems. In this paper, we present a 1 kW wideband Class E power amplifier using Silicon Carbide (SiC) MOSFETs that achieves 93% efficiency at 13.56 MHz with a bandwidth of ±1 MHz. We incorporate a reactance compensation network in the output loading stage to achieve wideband operation; design a custom gate drive circuit to reduce the gate power loss and improve thermal performance compared to using a gate driver IC. The total gate power of one SiC MOSFET is measured to be 1.55 W at 13.56 MHz.

INDEX TERMS Power amplifiers, wideband, wide band gap semiconductors.

I. INTRODUCTION

Nowadays, many applications use high-frequency power amplifiers, including plasma generators, wireless power transfer systems, and medical devices [1]–[4]. In many of these applications, the load that the power amplifier needs to drive does not have a fixed value. Using plasma generators as an example, the plasma load varies with temperature, gas pressure, gas types, frequency of operation, and the power delivered [5]. Commercial radio-frequency (RF) systems for plasma generation often use a tunable matching network to match the variable plasma load to a fixed value (for example, 50 Ω) to allow the use of standard coaxial cables and RF testing equipment [6], [7]. In some specialized applications requiring plasma pulsing, the mechanically tunable matching network is not fast enough to quickly match to the desired load. Therefore, the matching network also requires a frequency tuning feature for faster matching and a wider matching load range [1], [8].

Conventionally, RF system manufacturers use linear power amplifiers to drive these loads because of their simplicity and linearity. These features allow them to operate over a wide range of frequencies and input voltages but with low efficiency. As the need for higher efficiency arises, switch-mode power amplifiers such as Class D, Class E, and Class Φ_2 are becoming more popular since they can achieve much higher efficiency when operating under zero voltage switching (ZVS) conditions [9]–[11]. However, these switch-mode power amplifiers can only maintain efficient operation within a narrow frequency band due to their resonant nature. When shifting away from the designed frequency, both the efficiency and the output power of the switch-mode power amplifiers degrade significantly.

The literature offers various methods to drive a variable load, including applying impedance compression networks [12]–[14], load independent power amplifiers [15], and phase-switched impedance modulation [1]. The literature also has references describing various techniques to extend the power amplifier's operational bandwidth to address the need for frequency tuning in many applications [2], [16]–[18]. These include using switched-capacitors, dual-band multistage converters, manually changing components in the output network, and applying reactance compensation [19]–[23]. Among all of these options, reactance compensation provides the benefits of simple circuit design, component count reduction, and elimination of manual tuning during operation.

Wide bandgap (WBG) power devices are favorable for kW power converters at MHz switching frequencies because of their high critical fields and high thermal conductivity [24], [25]. As an example of WBG power devices, commercial Silicon Carbide (SiC) devices have higher voltage ratings than Gallium Nitride (GaN) devices due to their vertical structures,

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making them more suitable in high-power converters. However, even with the same device ratings, SiC devices have larger gate charges than GaN devices, resulting in higher gate losses and limiting their operation at high frequencies. Commercially-available gate driver ICs for SiC devices are usually designed for lower frequencies, and they tend to have higher losses, larger parasitics, and poor thermal handling capability. [26]–[28] proposed different methods to drive SiC devices at high frequencies, such as using resonant gate drivers and cascode GaN/SiC devices. However, these gate drive circuits either require precise tuning at a fixed frequency or have limitations on device choices. To solve these issues, we design a custom resonant gate drive circuit suitable for driving SiC MOSFETs in a MHz wideband power amplifier.

In switch-mode power amplifiers, the resonant nodes, including the drain node of the switch, can have very high voltages. In a Class E power amplifier, the maximum voltage of its drain node is approximately 3.6× the input DC voltage [10], which can exceed 1 kV in a kW design. Besides selecting the power device with the appropriate ratings, choosing stable capacitors in the resonant circuits is also important. As part of the Class I ceramic family, C0G capacitors have low losses, and they are stable over temperature and voltage variations with the trade-off of lower energy density compared to the Class II ceramic capacitors [29]. The market offers C0G capacitors from a few pF to tens of nF with voltage ratings of a few kV, which are suitable for MHz and kW resonant converters. Voltage measurements at these high-frequency and high-voltage nodes often require capacitor dividers due to derating of the voltage probes over frequency.

In this paper, we present a 1 kW wideband Class E power amplifier using reactance compensation and a custom gate drive circuit, which achieves 93% efficiency across the frequency band of 12.56 MHz to 14.56 MHz. The paper expands from our earlier conference publication [30] and includes more theoretical analysis and experimental results, especially on the custom gate drive design. Section II describes the detailed design of the wideband Class E power amplifier and the resonant gate drive circuit for SiC MOSFETs; Section III shows the experimental results; and Section IV concludes the paper.

II. DETAILED DESIGN OF THE WIDEBAND CLASS E POWER AMPLIFIER

A. WIDEBAND CLASS E POWER AMPLIFIER

Among different topologies of switch-mode power amplifiers, the Class E power amplifier has the most straightforward design that only requires a single ground-referenced switch and two sets of LC resonant tanks. Compared to the Class D topology, using only a ground-referenced switch makes the Class E power amplifier more suitable for high-frequency applications. While comparing to the Class Φ_2 topology, the Class E power amplifier has one less pair of LC resonant tanks with the trade-off of having higher voltage stress on the device. The relatively high voltage stress can limit the use of

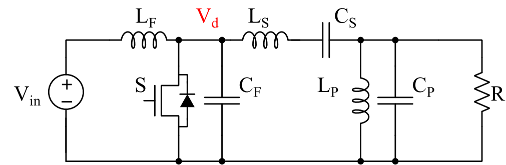


FIGURE 1. Wideband Class E power amplifier with the reactance compensation network.

GaN HEMTs, whereas SiC MOSFETs are more suitable in these cases because of their higher device ratings (1.2 kV to 1.7 kV).

In a regular Class E power amplifier with finite DC-feed inductance, the $L_F C_F$ network helps to meet ZVS conditions, while the $L_S C_S$ resonant tank filters out higher harmonics. The design of a Class E power amplifier follows the equations for the maximum output power [31]:

$$lR = \frac{1.365 V_{in}^2}{P},$$
$$C_F = \frac{0.685}{\omega R}, L_F = \frac{0.732R}{\omega},$$
$$L_S = \frac{Q_S R}{\omega}, C_S = \frac{1}{\omega Q_S R}, \tag{1}$$

where P is the output power, ω is the angular frequency, and Q_S is the quality factor of the L_S C_S series filter.

In the wideband Class E power amplifier, we add an additional $L_P C_P$ resonant tank at the output (shown in Fig. 1) to include the reactance compensation feature. The goal is to maintain high efficiency and deliver the same output power across a wide band, which requires the power amplifier to operate under ZVS and have a constant drain impedance in the entire bandwidth.

Achieving a flat drain impedance requires us to design the loading network such that the total reactance/susceptance seen at the node V_d is constant. The susceptance of the $L_F C_F$ network ($B_{L_F C_F}$) is $\omega C_F - \frac{1}{\omega L_F}$, which has a positive slope of $C_F + \frac{1}{\omega^2 L_F}$. To compensate for this slope, we choose the $L_P C_P$ values based on the equations below:

$$\frac{1}{\sqrt{L_P C_P}} = \omega,$$
$$\frac{dB_{L_F C_F}}{d\omega} = -\frac{dIm(Y_L)}{d\omega}$$
$$C_F + \frac{1}{\omega^2 L_F} = -\frac{d}{d\omega} Im\left(\frac{1}{Z_P + jX_S}\right), \tag{2}$$
$$\text{where } B_{L_F C_F} = \omega C_F - \frac{1}{\omega L_F},$$
$$Y_L = \frac{1}{Z_P + jX_S},$$
$$Z_P = \frac{1}{\frac{1}{R} + j\omega C_P + \frac{1}{j\omega L_P}},$$

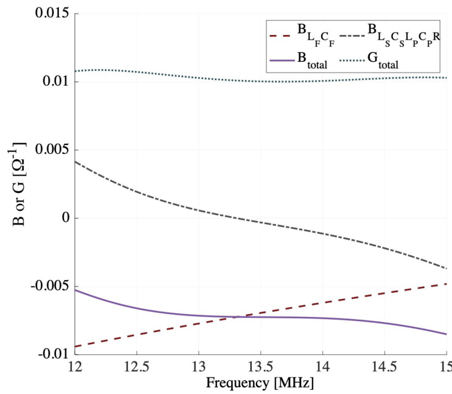


FIGURE 2. Simulated susceptance and conductance plot. The design parameters are listed in Table 1.

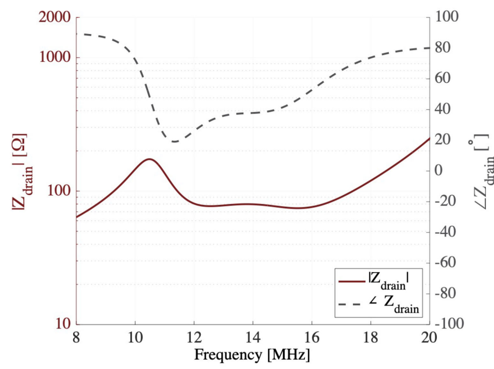


FIGURE 3. Simulated drain impedance at the node V_d in the wideband power amplifier. The design parameters are listed in Table 1.

$$X_S = \omega L_S - \frac{1}{\omega C_S},$$

which simplifies to

$$C_F + \frac{1}{\omega^2 L_F} = \frac{2}{\omega R}(Q_S - Q_P), \quad (3)$$

where Q_S is the quality factor of the series tank $L_S C_S R$, and Q_P is the quality factor of the parallel tank $L_P C_P R$. We select Q_S based on the output filtering requirement and then calculate Q_P from Equation 3 to achieve wideband operation. Finally we calculate L_P and C_P from Equation 4.

$$\frac{1}{\sqrt{L_P C_P}} = \omega,$$

$$Q_P = \omega R C_P \quad (4)$$

Fig. 2 shows the simulated susceptance and conductance plots of $L_F C_F$, $L_S C_S L_P C_P R$, and the total drain impedance of both networks. After adding the designed output network, both the total susceptance (B_{total}) and total conductance (G_{total}) at the drain node (V_d) show approximately flat slopes around the center frequency of 13.56 MHz. Fig. 3 shows the drain impedance at the node V_d, and Table 1 lists the simulation parameters in this design. Within the bandwidth of 12.56 MHz to 14.56 MHz, the drain impedance is relatively flat with an inductive angle to achieve ZVS.

TABLE 1 Design Parameters of the Wideband Class E Power Amplifier

Component	Value
V_{in}	180 V
L_F	859 nH
C_F	80 pF
L_S	3.6 μH
C_S	39 pF
L_P	594 nH
C_P	230 pF
R	100 Ω

The presented design demonstrates a wideband power amplifier with a bandwidth of 2 MHz for the specific plasma etching application; however, it is possible to make the bandwidth wider with the trade-off of allowing more harmonics in the output. If necessary, we can also transform the $L_F L_S C_S L_P C_P$ network to match a different load value [23], [32].

B. GATE DRIVE CIRCUIT FOR SIC MOSFETS

Most commercially-available gate driver ICs use a hard-gating half-bridge topology, which results in a gate loss of $Q_g V_g f$ in the power device. Besides the power lost to charge and discharge the gate capacitor of the power device, the gate driver also dissipates power in terms of internal switching and conduction losses. Depending on the gate charge, the total gate power to drive a SiC MOSFET using a gate driver IC ranges from a few watts to a few tens of watts at MHz switching frequencies [26], [33]. Because of such large gate losses, it is important to select gate driver ICs with good thermal handling packages. Additionally, at MHz switching frequencies, even a few nH of inductance can result in ringing on a device's gate. Large ringing can trigger false turn-on or turn-off, and gate overshoot may also damage the device. Therefore, carefully laying out the gate drive path is essential to reduce the parasitics and minimize ringing. Considering the requirements of good thermal handling capability, low parasitics, and short rising/falling time, the options of gate driver ICs for SiC MOSFETs at MHz frequencies are very limited. Previous papers have demonstrated ways to drive SiC devices at high frequencies, including using resonant gate drivers [26], [27], [34] and cascoding a GaN HEMT to drive a SiC JFET [28]. The multi-resonant gate drivers require precise tuning of the components and only works at a fixed frequency. Other resonant gate drive circuits require precise timing control of the switches, which can be challenging at MHz frequencies. The cascode GaN/SiC device uses a GaN HEMT to drive a SiC JFET. However, there are very limited SiC JFETs available on the market, and they usually have large gate resistance and capacitance, making them unsuitable for high-frequency operations. We present a custom gate drive circuit (shown in Fig. 4) to meet the goal of driving SiC MOSFETs efficiently across a wide band. Similar to the wideband Class E power amplifier shown in Section II-A,

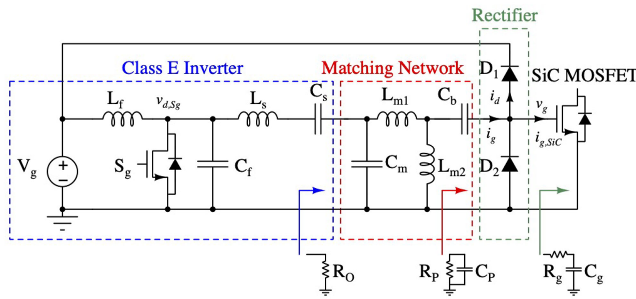


FIGURE 4. **Proposed gate drive circuit for SiC MOSFETs.**

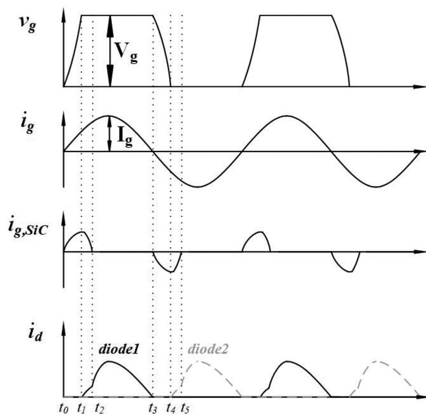


FIGURE 5. **Ideal waveforms of the custom gate drive circuit.**

we use the same idea of reactance compensation in the gate drive design to achieve wideband operation. The gate drive circuit consists of three sections, namely the Class E inverter, matching network, and rectifier. This gate drive circuit should meet the following requirements to achieve efficient wideband operation:

- The power amplifier's output load is matched to the gate impedance of the SiC MOSFET over the desired bandwidth,
- ZVS operation over the desired bandwidth,
- Maintaining a sinusoidal gate current (i_g).

Fig. 5 shows the ideal waveforms of this gate drive circuit. From t_0 to t_1, as the current i_g rises from zero, it charges the gate capacitance of the SiC MOSFET until the gate voltage v_g reaches the DC input voltage V_g. Then diode D_1 turns on, and the energy will get recycled to the DC input source. Similarly, the negative current i_g discharges the gate capacitance at turn-off, and the source recycles the rest of the energy. Fig. 6 shows the design flow of the gate drive circuit. We use first order approximation in the design steps to simplify the analysis.

1) Calculate the amplitude of gate current (I_g) given the desired rising and falling time:

$$I_g = \frac{\omega C_g V_g}{1 - \cos(\omega t_r)}, \tag{5}$$

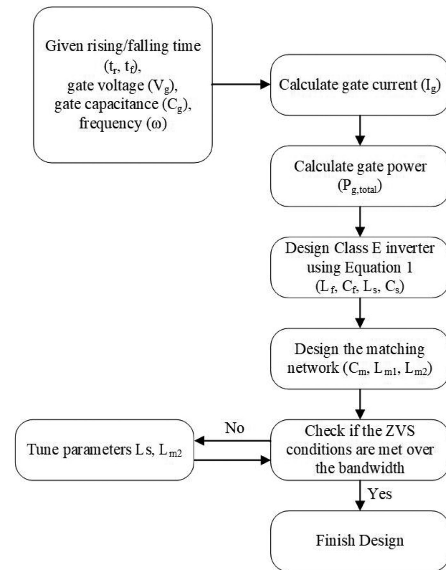


FIGURE 6. **Design flow of the gate drive circuit.**

where C_g is the gate capacitance, V_g is the gate voltage, t_r is the rising time, and ω is the angular frequency.

2) Calculate the total gate power, including the power losses in the gate resistor and two diodes, and the recycled power to the DC voltage source.

$$\begin{aligned} P_{g,total} &= P_{R_g} + 2P_D + P_{DC}, \\ \text{and } P_{R_g} &= \frac{I_g^2 R_g}{T}\left(t_r - \frac{1}{2\omega}\sin(2\omega t_r)\right), \\ P_D &= \frac{V_D I_g}{2\pi}(1 + \cos(\omega t_r)), \\ P_{DC} &= \frac{V_g I_g}{2\pi}(1 + \cos(\omega t_r)), \end{aligned} \tag{6}$$

where T is the switching period and V_D is the forward voltage of the diodes.

3) Design the Class E inverter based on the input gate voltage and the gate power using Equation 1 in Section II-A.

4) Design and tune the matching network to provide efficient wideband matching. Depending on the quality factor of the load, the circuit can include a one or two-stage matching network. Fig. 7 shows the step-by-step impedance waveforms of the circuits shown in Fig. 8. First, we select the initial value of L_{m2} to compensate for the equivalent capacitance in the SiC MOSFET's gate and the rectifier (C_P in Fig. 4). As labeled in Fig. 7(a), L_{m2} determines the impedance below the resonant frequency of L_{m2}-C_P, and C_P determines the impedance above the resonant frequency. Next, we design the L_{m1}-C_m matching network for impedance matching and enforcing a sinusoidal output current at the center frequency.

$$lR_O = \frac{L_{m1}}{C_m R_P},$$

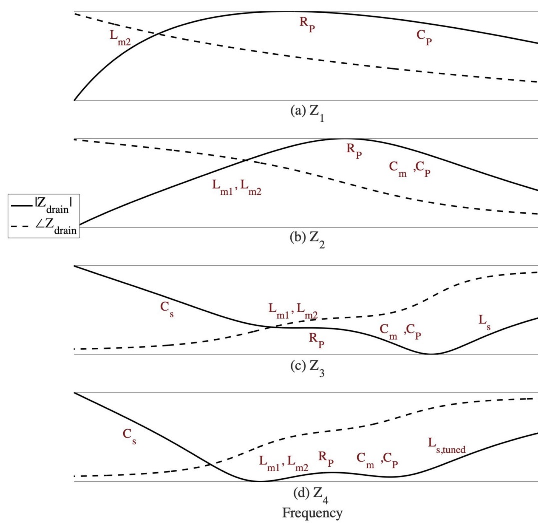


FIGURE 7. Step-by-step impedance waveforms of the gate drive circuits shown in Fig. 8. The red labels on the graphs indicate the determining parameters of the impedance at these locations.

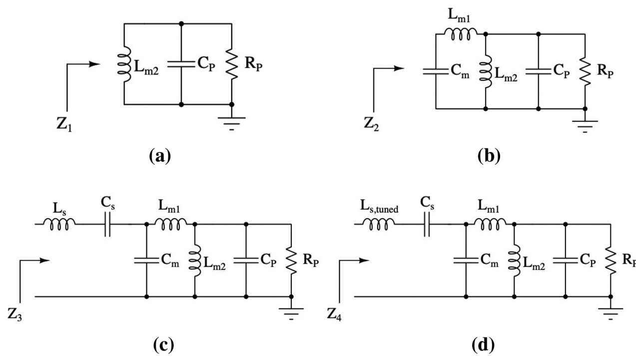


FIGURE 8. Equivalent circuits of the impedance waveforms shown in Fig. 7.

$$\frac{1}{\sqrt{L_{m1}C_m}} = \omega, \tag{7}$$

where R_O is the output resistance of the Class E inverter, and R_P is the equivalent parallel resistance seen into the rectifier and the SiC MOSFET's gate as shown in Fig. 4. Fig. 7(b) shows the impedance waveform after adding L_{m1} and C_m, and Fig. 7(c) shows the impedance including L_s-C_s designed in the previous step. The resulting impedance is not flat over the bandwidth, especially the part determined by C_m, C_P, and L_s. C_P and C_m are hard to change since C_P is the equivalent capacitance of the device and diodes, and C_m determines the matching ratio. Therefore, we choose to tune L_s with the trade-off of slightly higher circulating power due to larger inductive angle. In this example, increasing L_s leads to a more flat impedance waveform in Fig. 4(d). Similarly, tuning L_{m2} or C_s helps make the impedance below the center frequency more constant. C_b in Fig. 4 is the DC blocking capacitor, which does not affect the drain impedance.

TABLE 2 Design Parameters of the Custom Gate Drive Circuit

Component	Value
V_{in}	15 V
L_f	220 nH
C_f	364 pF
L_s	519 nH
$L_{s,tuned}$	650 nH
C_s	265 pF
L_{m1}	90 nH
C_m	1.53 nF
L_{m2}	90 nH
C_P	1.6 nF
R_P	3.3 Ω

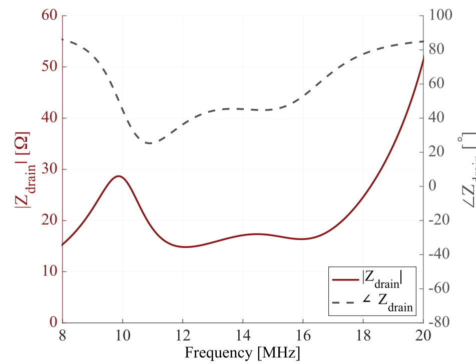


FIGURE 9. Simulated gate drive circuit's drain impedance. Table 2 lists the design parameters.

Table 2 lists the design parameters used to generate the impedance plots in Fig. 7. The overall drain impedance shown in Fig. 9, including L_f and C_f, confirms a relatively constant magnitude with an inductive angle to achieve ZVS over the bandwidth of 12.56 MHz to 14.56 MHz.

III. EXPERIMENTAL RESULTS

Following the design steps presented, we build a 1 kW Class E power amplifier, operating at the center frequency of 13.56 MHz with a bandwidth of ±1 MHz. Designing a kW power amplifier often requires more than one power stage due to the switching devices' thermal limit, the magnetic cores' saturation constraints, and other component ratings. In this work, we connect two identical wideband Class E power amplifiers in parallel with each outputting 500 W. Fig. 10 and Fig. 11 show the schematic and PCB of the design.

The SiC MOSFET used in the design (G3R350MT12 J) has low gate charge (10 nC) and low gate resistance (2.5 Ω), making it suitable to switch at 13.56 MHz. In the power amplifier, L_F is a hand-wound air-core inductor; L_S and L_P use material 67 from Fair-Rite because of its highest performance factor around 10 MHz [35]. In the gate drive circuit, we use the air-core inductors from Coilcraft for L_f, L_{m1}, and L_{m2}, and hand wind L_s. Table 3 lists the component values and part numbers of the devices used in the design.

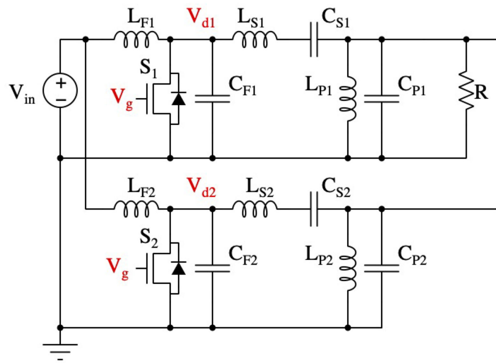


FIGURE 10. Schematic of the parallel-connected wideband Class E power amplifier.

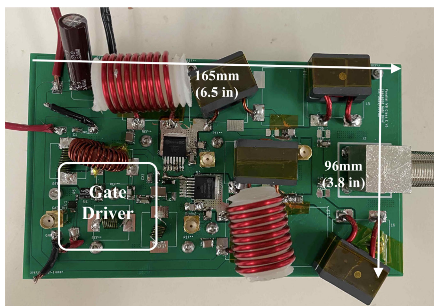


FIGURE 11. PCB of the wideband Class E power amplifier.

TABLE 3 Component List of the Wideband Class e Power Amplifier

Circuit	Component	Value
Gate Drive	S_g	GS61004B
	L_f	220 nH
	C_f	220 pF
	L_s	650 nH
	C_s	265 pF
	L_{m1}	90 nH
	C_m	1.5 nF
	L_{m2}	110 nH
	C_b	100 nF
	D_1, D_2	DFLS230
Power Amplifier	S_1, S_2	G3R350MT12J
	L_{F1}, L_{F2}	880 nH
	C_{F1}, C_{F2}	39 pF
	L_{S1}, L_{S2}	3.5 μH
	C_{S1}, C_{S2}	39 pF
	L_{P1}, L_{P2}	594 nH
	C_{P1}, C_{P2}	232 pF

Fig. 12 shows the measured drain impedances at nodes V$_{d1}$ and V$_{d2}$ in Fig. 10 after tuning. The parallel-connected power amplifiers have matched and relatively flat drain impedances within the bandwidth of 12.56 MHz to 14.56 MHz. Fig. 13 shows the measured drain voltages (V_{d1}, V_{d2}) and gate voltages (V_g) in the power amplifier (Fig. 10), and the drain voltages of the switching device in the gate drive circuit ($V_{d,Sg}$ in Fig. 4) at 12.56 MHz, 13.56 MHz and 14.56 MHz. At all frequencies, the drain voltages in the parallel-connected Class E power amplifiers reach zero before the gates of the SiC MOSFETs turn on, demonstrating ZVS behaviors. Due to probes' derating at high frequencies, we use a capacitor divider to measure V_{d1} and V_{d2} by connecting a 1 pF C0G capacitor between the drain node and the probe. The actual maximum drain voltages are around 800 V in all cases. We use a GaN HEMT as the switching device in the gate drive circuit since its low gate charge makes it easy to drive at MHz frequencies. The drain voltage waveforms of the GaN HEMT at all three frequencies also demonstrate operations under or close-to ZVS. Fig. 14 shows the measured gate power at 12.56 MHz, 13.56 MHz, and 14.56 MHz. The red bars show the gate power in driving the GaN HEMT at three frequencies, which ranges from 0.35 W to 0.4 W. The gray bars show the power dissipated in the rest of the gate drive circuit from the DC input source. With a rising time of 10 ns, the total gate power to drive both SiC MOSFETs (shown in the blue line) is between 2.95 W to 3.1 W across the 2 MHz bandwidth.

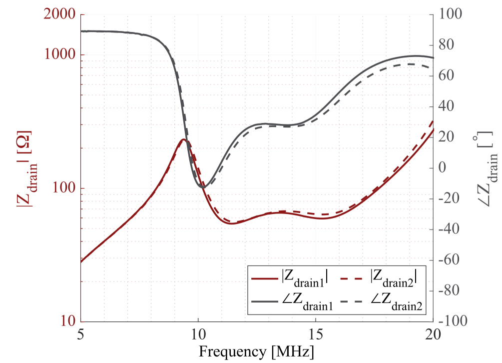


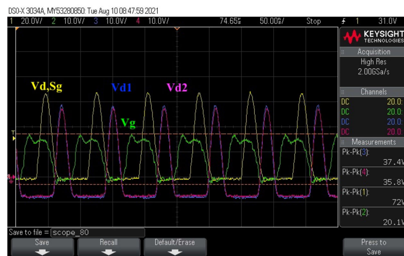
FIGURE 12. Measured drain impedances of two parallel-connected wideband Class E power amplifiers.

Fig. 15 shows the total output power and efficiency of the design presented. The wideband Class E power amplifier achieves a total efficiency of 93% to 94% and maintains the output power with less than 10% variation within the bandwidth of 12.56 MHz to 14.56 MHz. Fig. 16 shows the loss breakdown of the design. 70% of the power losses come from the two SiC MOSFETs, mainly consisting of MOSFETs' conduction losses and C_{oss} losses [36]. Core and winding losses from all inductors add to a total of 17%, and the custom gate drive circuit consumes another 5%. Other losses include the losses in the capacitors, parasitics on the PCB, and estimation errors.

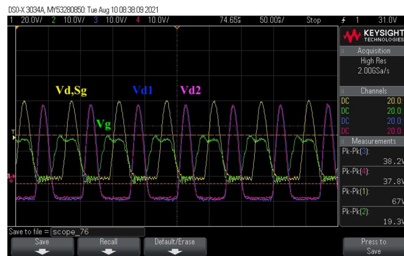
Table 4 compares the wideband power amplifier in this work with other high-frequency power amplifiers in the literature. The design presented achieves both the highest efficiency and highest output power compared to the other wideband power amplifiers in [23], [37], [38]. The target application of this work is for the specific plasma etching

TABLE 4 Performance Comparison of This Work With State-of-Art High-Frequency Power Amplifiers in the Literature

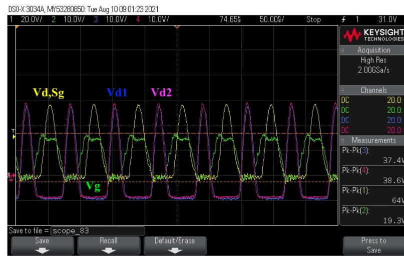
	This Work	[23]	[37]	[38]	[28]	[33]	[39]
Topology	Class E	PPT Class Φ_2	Push-Pull Class E	Class E	Class E	Class Φ_2	Class $E/F_{2,odd}$
Operating Frequency [MHz]	12.56-14.56	12.56-18.06	8-12	5.4-10.2	13.56	6.78	7
Output Power [W]	1000	300	2.9	55	640	2200	1100
Efficiency	93-94%	85-93%	80-88%	55-90%	91%	93%	85%



(a) 12.56 MHz



(b) 13.56 MHz



(c) 14.56 MHz

FIGURE 13. **Measured drain voltages (V_{d1} and V_{d2} in Fig. 10), gate voltages of the SiC MOSFETs (V_g in Fig. 10, and the drain voltages of the switching device in the gate drive circuit ($V_{d,Sg}$ in Fig. 4) at (a) 12.56 MHz, (b) 13.56 MHz, and (c) 14.56 MHz. We use a capacitor divider to measure V_{d1} and V_{d2} by connecting a 1 pF C0G capacitor between the drain node and the probe.**

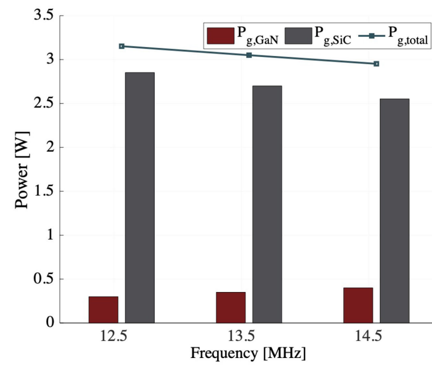


FIGURE 14. **Measured gate power of the custom gate drive circuit at 12.56 MHz, 13.56 MHz, and 14.56 MHz. The red bars show the measured gate power in driving the GaN HEMT, the gray bars show the measured power in the rest of the gate drive circuit, and the blue line shows the total gate power.**

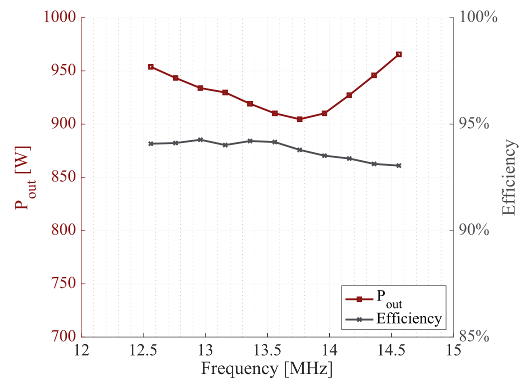


FIGURE 15. **Measured output power and efficiency of the wideband Class E power amplifier across the 2 MHz bandwidth centered at 13.56 MHz.**

system with a bandwidth of 12.56-14.56 MHz. It is possible to extend the bandwidth of this design with the trade-off of having larger output harmonics. This design also shows high efficiency compared with high-frequency power amplifiers with similar output power operating at a fixed frequency [28], [33], [39].

Besides device and component selection, careful layout design is also essential to achieve high efficiency and balanced current sharing at MHz frequencies. Making the high-frequency and high-current traces short and wide reduces the losses and ringing on the board. Eliminating the ground plane under the high-frequency and high-voltage nodes also reduces the losses through the PCB capacitors. In addition, using an aluminum heat sink with an insulating thermal pad reduces the thermal resistance of the device, increasing the total power delivery and decreasing the device's conduction losses. Matched layout and component design, both on the gate signal paths and the power stages, are essential to have equal power delivery in a parallel-connected system. In particular, tuning the inductors and capacitors to attain matched drain impedances before powering on the system helps to achieve equal current sharing.

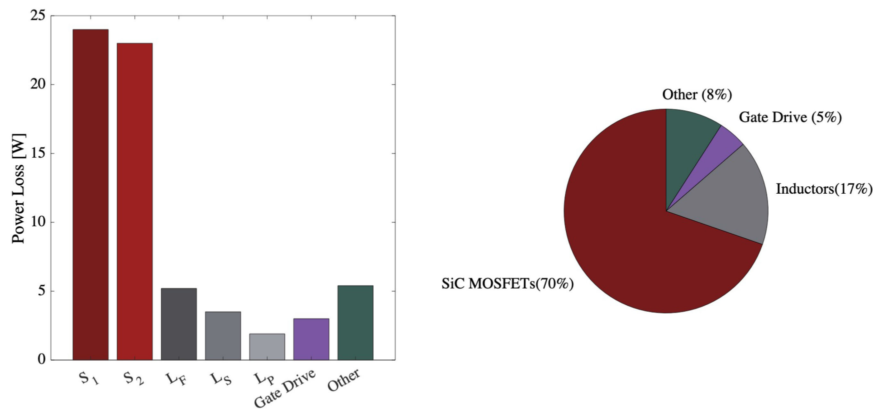


FIGURE 16. Power loss breakdown of the design presented.

IV. CONCLUSION

This paper demonstrates a wideband Class E power amplifier that operates efficiently across a 2 MHz bandwidth centered at 13.56 MHz. The addition of only one pair of LC resonant network to achieve reactance compensation is a simple technique to extend the Class E power amplifier's bandwidth without manual tuning or extra switches. Using the same idea of reactance compensation, we design a custom gate drive circuit for SiC MOSFETs, which consumes 1.55 W per device at 13.56 MHz. The experimental results demonstrate that the 1 kW Class E power amplifier maintains around 93% efficiency from 12.56 MHz to 14.56 MHz.

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