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Miniaturization and Thermal Design of a 170 W AC/DC Battery Charger Utilizing GaN Power Devices

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ABSTRACT This paper presents the design and analysis of a high-density two-stage battery charger for mid-power applications like small electric vehicles and high-performance laptops utilizing gallium nitride (GaN) power devices. In addition to adherence of maximum junction temperatures, a thermal analysis is carried out for in-housing operation, which is particularly critical for fanless wall chargers. Design measures include calorimetric semiconductor selection, half-bridge miniaturization, thermally conductive epoxy resin and reference-based convection modeling for thermally optimized component placement using 3D-stacking. Furthermore, the remaining optimization potential of the charger is estimated by virtual prototyping. A 170 W hardware prototype is developed and tested, achieving a two-stage power section efficiency of 95.4% with a maximum switching frequency of 550 kHz. This results in a power density in open-housing operation of 1.6 kW/dm^3. Using epoxy resin, copper and graphite heat spreaders, an in-housing operation power density of 1.1 kW/dm^3 is achieved with minor reduction of output power due to surface temperature constraints.

INDEX TERMS AC-DC power conversion, battery chargers, epoxy resins, gallium nitride, graphite.

I. INTRODUCTION

With the increasing acceptance and use of electric vehicles, the demand for compact, resource-saving battery chargers is growing [1], [2]. Small electric vehicles, like eScooters and eBikes, require portable fanless chargers in the medium power range of 100-250 W. With modern wide bandgap semiconductors and the high frequency operation of one or two-stage topologies, battery chargers can achieve very high efficiency with low component volume [3]–[8]. In addition to switching frequency and efficiency, the thermal design of the charger is also a critical aspect for high power density, especially in this power class which typically only relies on passive cooling. Of course, the reliable operation of all electrical components must be ensured, which primarily includes sufficient cooling of the power semiconductors. Prior research has demonstrated new concepts for optimizing component placement to reduce electrical pathways and device temperatures [9]–[11]. In addition to the maximum junction temperature of all semiconductor devices, the housing surface must also be kept below a maximum temperature specified by standards to allow safe handling [12], [13]. Individual components can thus quickly limit the output power due to hotspots on the surface. However, the influence of housing and component placement on the surface temperature is generally not considered when optimizing chargers in terms of power density [3]–[8]. It is therefore not clear how much high-density charger designs are affected by these standards and to what extend packing density can be increased by measures such as potting and optimized component positioning.

This work proposes the design and analysis of a high-density two-stage GaN battery charger for mid-power applications like small electric vehicles and high-performance laptops. The two-stage architecture consists of a totem-pole power factor correction (PFC) stage and an isolated

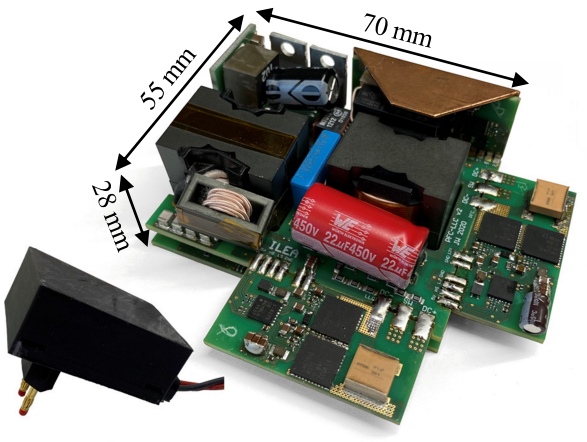

FIGURE 1. 170 W battery charger prototype inside the plastic wall charger housing (left) and open with folded down half-bridges (right).

TABLE 1. Prototype Battery Charger Performance Summary

Parameter	Symbol	Value
Output power	P_{out}	170 W
AC input voltage	V_{ac}	230 V (50 Hz)
System volume	V_{sys}	0.11 dm^3
System mass	m_{sys}	0.3 kg
Peak efficiency power section	η	95.4 %
Peak efficiency system	η_{sys}	94.2 %
Power factor	$cos(\varphi)$	0.969
GaN HEMT (S_1, S_2)		LMG3410R150
GaN HEMT (S_3, S_4, S_5, S_6)		LMG3410R070
Si MOSFET (S_7, S_8)		IPP076N15N5
Maximum switching frequency LLC	f_{LLC}	550 kHz
Switching frequency PFC	f_{PFC}	60 kHz
Junction-to-ambient thermal resistance	$Z_{\mathrm{th,j-A}}$	10.5 K/W
DC-link voltage	V_{lk}	360 V $\pm$ 45 V
Output voltage	V_{dc}	28 V $-$ 42 V
Maximum output current	I_{dc}	4 A $\pm$ 0.5 A

resonant half-bridge LLC converter with synchronous rectification (SR). To enable high switching frequencies for small passive components, this well-established topology [14]–[19] is combined with a semiconductor selection based on new calorimetric measurements of zero-voltage switching (ZVS) losses [20], [21]. Miniaturized half-bridges and a 3D-stacked design of the AC/DC converter allow the compact connection of both stages while maintaining necessary isolation distances. The influence of the thermal design with respect to surface area, metal and graphite heat spreader, potting material and component distribution on the power density of the overall system is investigated. In contrast to prior research, this work demonstrates the charger operation in a plastic housing and points out the influence of surface temperature standards. Measures required to develop high-density chargers with acceptable surface contact temperatures are presented.

The 170 W hardware prototype with a volume of 0.11 dm^3 achieves a volumetric power density of 1.6 kW/dm^3 in open-housing operation with a maximum switching frequency of 550 kHz (see Fig. 1). The drivers and measurement sensors are controlled and supplied outside the prototype via a rapid prototyping system. Due to the high power section efficiency of 95.4%, the maximum component temperature on the surface remains below 100 °C without active cooling. Taking auxiliary supply for drivers and sensors into account the system efficiency is 95.2%. In the housing, while maintaining a maximum surface temperature of 65 °C, operation can be ensured with a power density of 1.1 kW/dm^3 with minimal reduction of output power, utilizing copper, graphite and epoxy resin as heat spreaders. Furthermore, with a thermal 3D finite element method (FEM) simulation based on prototype measurements, the remaining optimization potential of the converter is estimated in a virtual prototyping process. Monte Carlo simulations are used to optimize component positions and metal heat spreader dimensions for a high-density design. Compared to optimization approaches of prior research [9]–[11], the temperature of the housing is identified as the limiting factor.

II. ELECTRICAL CONCEPT

A. TOPOLOGY AND CONTROL

The proposed two-stage battery charger combines a totem-pole PFC rectifier and an isolated resonant half-bridge LLC converter with synchronous rectification. Fig. 2 shows the corresponding circuit schematic with the performance summary in Table 1. In addition to the converter stages, an input filter integrated into the power plug, a DC-link capacitor and an output π-filter are also part of the charger. The development of both stages was carried out individually in separate hardware prototypes, with a focus on functionality and efficiency [22], [23]. This includes electrical modeling and analysis of losses in the various components of both stages, supported by electrical and calorimetric measurements. In addition to the efficiency and component volume optimization, the corresponding component losses are used in the thermal simulation of the charger.

Due to the European regulatory threshold of 75 W regarding power factor and total harmonic distortion (THD) limits, active rectification is difficult to avoid [24]. To mitigate the effects of this stage on overall system efficiency, GaN high-electron-mobility transistors (HEMTs) were used to decrease switching losses compared to conventional Si metal–oxide–semiconductor fieldeffect transistors (MOSFETs) [15]. Pulse width modulation (PWM) and triangular current mode (TCM) were investigated experimentally as possible modulation techniques [22]. Although TCM achieves 99% efficiency, it fails to provide the necessary power factor correction, has higher THD and introduces challenges regarding miniaturization of the required high bandwidth current sensor. Therefore the PWM scheme was implemented to meet the PF and THD requirements. Furthermore, the high current load at TCM resulted in a large litz wire cross-section and thus an enlarged inductor. Implementing PWM results in a front-end converter peak efficiency of 98% and a 30% volumetrically smaller inductor compared to TCM.

For the DC/DC stage, resonant LLC converters show many advantages [17], [18]. In particular ZVS can be achieved

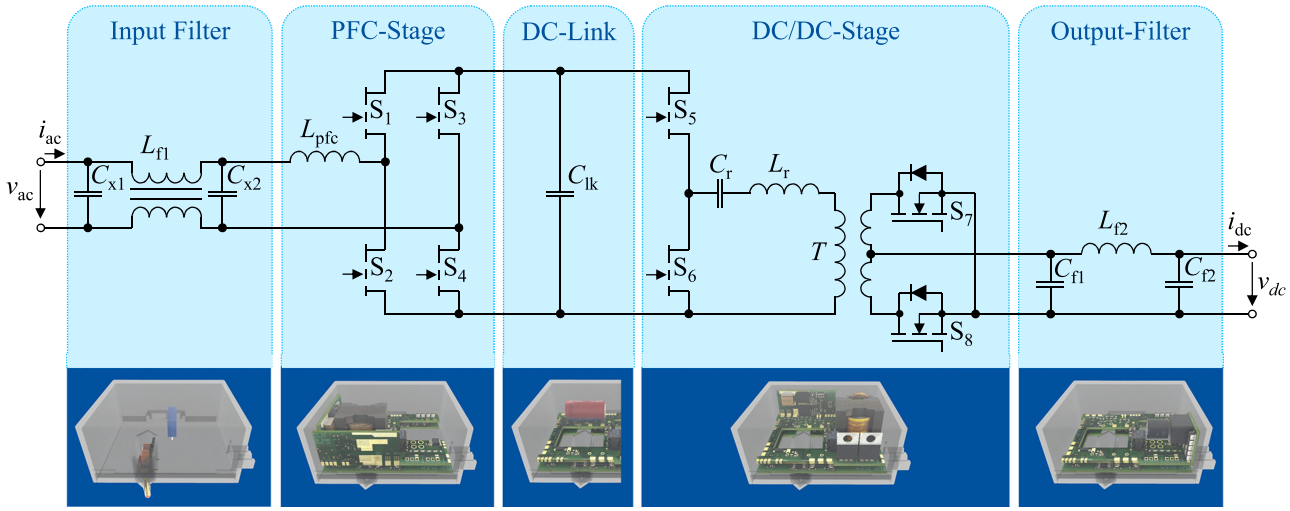

FIGURE 2. Proposed two-stage battery charger topology consisting of the AC/DC PFC-stage and the DC/DC LLC stage with additional input, DC-link and output filters (top). Position of the corresponding components within the housing (bottom).

over the entire operating range. This allows high switching frequencies, resulting in small passive components and high power density. However, the wide output voltage range requirements for a battery charger make optimization difficult compared to applications with a narrow output voltage range. Loss and electrical models are therefore used to optimize the converter in order to meet the loss requirements while minimizing volume and maintaining ZVS over the wide operating range [22]. The limitation to 550 kHz switching frequency represents a compromise between loss and volume optimization. In addition, the implementation of SR significantly reduces secondary-side losses. With the Si MOSFETs S_7 and S_8 additional parasitic capacitance and influences by the SR control are introduced, thereby increasing the voltage gain in step-down operation at high switching frequency [25], [26]. In order to still cover the entire constant-current and constant-voltage charging profile, burst mode operation is implemented for low output current operation [27]. The LLC is operated with a proportional-integral controller with a constant duty cycle of 50%.

The analog-to-digital conversion and control of the modulation is implemented on a rapid prototyping system outside the battery charger. This allows real-time monitoring of the operation and easy optimization of the control parameters. However, the electrical ground connection prevents conclusive electromagnetic interference (EMI) measurements. A transfer to an integrated microcontroller or a dedicated application-specific integrated circuit (ASIC) within the charger housing is possible. In addition, the battery is modeled using an electrolytic capacitor (10 mF), a series resistor (235 mΩ), a voltage source and an active load. For the reliability and thermal load of the battery, the current ripple is limited by the output filter to ±0.5 A. Lower requirements would allow for volume savings. However, especially with very small currents, the output filter is also necessary to suppress oscillations.

B. SEMICONDUCTOR SELECTION

Current research based on analytical models and experimental comparison shows, that wide bandgap semiconductors, in particular GaN devices, lead to a major efficiency increase in soft-switching applications [18]. In order to select the most suitable semiconductor for the LLC stage, GaN and silicon carbide (SiC) power transistors were characterized with new calorimetric measurements and compared for use in the planned topology [20], [21]. In contrast to conventional characterization using the double-pulse test (DPT) method, the transient Z_{th}-calibrated calorimetric measurement can be used to accurately determine even very small switching loss energy in ZVS operation. The switching current and voltage dependent results are integrated into the converter simulation to improve the efficiency prediction. The GaN power stage with integrated driver shows in average 37% percent lower switching loss energy than the SiC MOSFET under the same switching conditions. Furthermore, implemented over-temperature and over-current safety features in the power stage prevent failures during the development process and improve safety in the final prototype. Due to dominant hard-switching losses in the PFC stage [15], the same GaN power stage with smaller chip area is used. In comparative measurement, the 150 mΩ semiconductors show 0.4 percentage points better efficiency than the 70 mΩ variant at 170 W output power. In addition, the 50 Hz PFC half-bridge is realized with the 70 mΩ GaN HEMTs to reduce conduction losses and to avoid EMI-critical current spikes at AC zero-crossing [28]. GaN semiconductors for SR were considered, but fail to improve the resonant behavior to avoid burst-mode compared to the more cost-effective Si MOSFETs.

C. 3D-STACKING OF PCBS AND COMPONENTS

The final position of the components is a compromise between electrical and thermal requirements (see Fig. 3). For

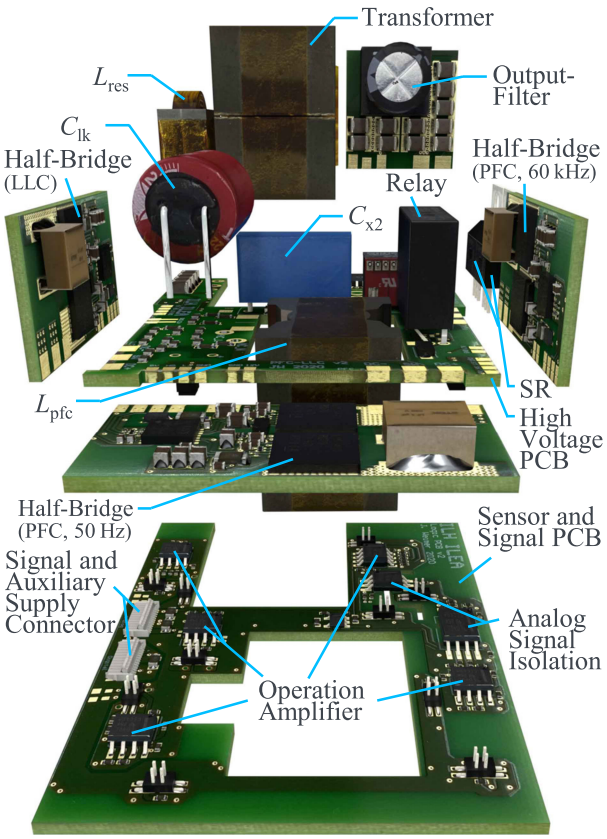

FIGURE 3. **Exploded view of the inner charger assembly consisting of passive components on the high voltage PCB, half-bridges soldered to the edges and stacked on the sensor and signal PCB.**

electrically short paths, galvanic isolation of the output side and low EMI between the converter stages, the individual building blocks such as resonance tank or output stage are positioned with narrow distances in between, supported by thermal and electrical simulations. The basic concept used here is the separation of sensors and signals from the high voltage components by two stacked main PCBs. At the same time, the miniaturized half-bridges are soldered vertically to the high-voltage PCB via edge plating whereas large components are positioned in the center within PCB cutouts. The metal heat spreaders of the half-bridges thus located in the housing edges ensure optimum thermal performance with few hotspots. Generally, only commercially available components are used. Magnetics are optimized for low losses and small volume with regard to core, air gap and litz wire. The half-bridges are reduced to 20 × 40 mm PCB modules by a four-layer structure, minimal footprint components (SMD-0201 to 0805, imperial) and the use of bootstrapping. The connection between high voltage and signal board is made via pin headers with 1 mm pitch. Flexible printed circuit (FPC) cables connect the charger to the rapid prototyping system. The sensor and signal PCB is only populated on one side and offers further space for a possible integration of the closed loop control unit. Isolated hall sensor integrated circuits (ICs) are used for output and PFC inductance current measurement. Differential amplifiers are used for AC-input, DC-link and DC-output voltage measurement. The output voltage signal is isolated.

In this section the electrical concept of the hardware prototype and its performance characteristics were introduced. The direct comparison of modulation schemes of the PFC stage results in the decision for PWM modulation to meet power factor standards and to reduce the volume of the PFC coil. The focus on wide output range ZVS for the high-efficiency LLC design and the challenges posed by SR are presented. The selection process for semiconductors based on new calorimetric measurements is outlined, showing advantages of GaN devices for ZVS in this power class. Finally, the 3D-stacking of the miniaturized components optimized by thermal and electrical simulations is presented.

III. THERMAL CONCEPT

A. SYSTEM POWER DENSITY

The thermal design of the battery charger has two main objectives:

1) Sufficient heat dissipation for components, especially power semiconductors, to ensure functionality and reliability.
2) Compliance with surface temperature standards to prevent fires and burns from handling.

At the same time, parasitic influences of the thermal design on the losses must be kept as small as possible. This primarily includes the temperature-dependent losses of semiconductors and magnetic components, but also increased eddy currents and capacitive coupling through metal heat spreaders and heat sinks. If a potting material is used, its electrical properties such as the dielectric constant become an additional factor [29].

Often, the focus is only on functionality in open-housing operation and challenges from in-housing operation, especially in fanless battery chargers, are neglected [3]–[8]. Compact housings have a power dissipation budget limited to a few watts, which is further reduced by hotspots [30]. Assuming sufficiently low thermal resistance between semiconductor and heat sink, the system power density ρ_{sys} is not determined by the maximum semiconductor, but by the maximum uniform housing surface temperature delta $\Delta T_{s,max}$ [13]. For given system efficiency η_{sys} and system volume V_{sys}, the power density of the converter is defined as

$$\rho_{sys} = \frac{P_{out}}{V_{sys}} = \frac{\eta_{sys}}{1-\eta_{sys}} \frac{\Delta T_{s,max}/R_{th,s-amb}}{V_{sys}}. \quad (1)$$

With natural convection, which is common for battery chargers of this power class, the thermal resistance $R_{th,s-amb}$ between housing surface and ambient results in

$$R_{th,s-amb} = (\alpha A_s)^{-1} \quad (2)$$

with surface temperature-dependent heat transfer coefficient $\alpha(T_s)$ and the housing surface area A_s. For touch protection, maximum housing surface temperatures are defined in standards such as the European standard EN 60335-1, depending

on the material [12]. In general, stricter limits apply to metal surfaces than to plastics. Therefore, for the battery charger of this work, a plastic housing is used and a maximum surface temperature limit of $T_{s,max} = 65°C$ is selected. This ensures a sufficient margin compared to the limit of the standard of 75°C. In addition, the charger is designed for an ambient temperature of 20 °C. Higher temperatures require a reduction of the output power. Based on (1) and (2) the maximum power density using the temperature limit follows as

$$\rho_{sys,max} = \frac{\eta_{sys}}{1-\eta_{sys}} \frac{A_s}{V_{sys}} \left(T_{s,max} - T_{amb}\right) \alpha. \tag{3}$$

From a thermal design point of view, an increase in power density can thus be achieved by bringing the average surface temperature $T_{s,avg}$ closer to the temperature limit $T_{s,max}$ and by maximizing the surface-to-volume ratio A_s/V_{sys} and the heat transfer coefficient α. A match of the mean surface temperature $T_{s,avg}$ and $T_{s,max}$ by avoiding hotspots thereby also increases the temperature dependent heat transfer coefficient.

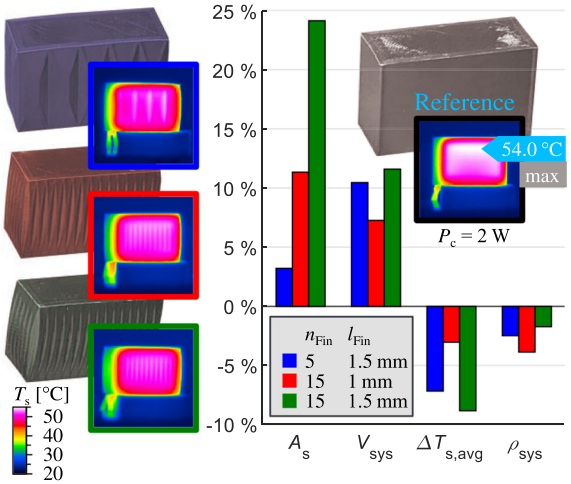

FIGURE 4. Acrylonitrile butadiene styrene (ABS) plastic housing with differently structured surfaces. The reference housing with smooth surface is 50 × 20 × 30 mm³ in size. All convection tests are performed using a ceramic resistor and 1 mm thick copper heat spreader on the inner housing wall with 2 W of conduction losses P_c. The enclosures differ in their number of fins n_{Fin} and fin length l_{Fin}.

B. NATURAL SURFACE CONVECTION

The amount of losses that can be dissipated by means of natural convection depends on the temperature-dependent air flow. For the thermal simulation of the battery charger in the miniaturization stage and for estimating the optimization potential in virtual prototyping, natural convection is analyzed and modeled. For this purpose, the air flow can be simulated directly with 3D-FEM fluid dynamics or taken into account using a temperature-dependent heat transfer coefficient α. The heat transfer coefficient is determined with analytical equations under simplified boundary conditions or via thermal measurements. For high accuracy but low computing effort, the heat transfer coefficient in this work is determined thermographically on a reference housing with similar dimensions [30]. The measured data is approximated as a function of temperature and location for the various housing sides. This includes further cooling due to thermal radiation. The spatial housing orientation showed only a minor influence for the reference and thus is not taken into account. With respect to the final dimensions of the battery charger and based on the convection model, a maximum power dissipation budget of $P_{dis} = 11$ W can be estimated for uniform surface temperature distribution. This corresponds to an average heat transfer coefficient over all surfaces of $\alpha = 13.5$ W m^{-2} K^{-1}. For a worse temperature distribution with up to 15 K delta between average and maximum surface temperature, the budget for final dimensions is reduced to $P_{dis} = 7.6$ W.

In addition to better utilization of the housing surface with uniform temperature distribution, the surface-to-volume ratio can be improved. A flat design is advantageous here [13], but cannot be realized with the magnetic components of the converter. However, in order to improve the ratio A_s/V_{sys}, different fin structures are investigated. Fig. 4 shows three different test housings and a reference housing with a smooth surface. To avoid larger gaps and the buildup of particles in normal use, the fin length is limited to 1.5 mm. With the measured thermal convection resistance $R_{th,s-amb} = \Delta T_{s,avg}/P_c$, equal system efficiency η_{sys}, and equal surface temperature limit $\Delta T_{s,max}$, the power density achieved by the fin structure with respect to the reference design ($\rho_{sys,0}$) is given by (1) as

$$\frac{\rho_{sys,1}}{\rho_{sys,0}} = \frac{R_{th,s-amb,0} V_{sys,0}}{R_{th,s-amb,1} V_{sys,1}} = \frac{\Delta T_{s,avg,0} V_{sys,0}}{\Delta T_{s,avg,1} V_{sys,1}}. \tag{4}$$

The 3D-printed fin structures show an increased surface area, but also a larger volume. With all housings, the maximum and average surface temperature is reduced. However, the average temperature differs only within a 2 K range and is subject to limited measurement accuracy due to temperature transitions to ambient at the edges. The unexpectedly higher temperature change by design 1 (blue) suggests too little impact on convection and results within the error range of the setup and measurement. None of the fin structures could increase the power density, which is why a housing with a smooth surface is implemented for the battery charger.

C. HALF-BRIDGE COOLING

a) Cooling Approach and Measuring Method: The half-bridges positioned vertically in the housing sides are attached to metal heat spreaders via double-sided adhesive, isolating, elastomer thermal interface material (TIM) sheets. Fig. 5 shows the cross-section through the 60 kHz PFC half-bridge in the potted configuration. The junction-to-ambient thermal impedance for symmetrical high-side and low-side losses measured from the prototype are shown in Fig. 6. For thermal simulation, a model of the half-bridge is used according to the setup in Fig. 7.

The 100 μm thick stainless steel sheet is in first concept utilized as a folded heat spreader to connect to all half-bridges in order to distribute the heat over a large area below the housing

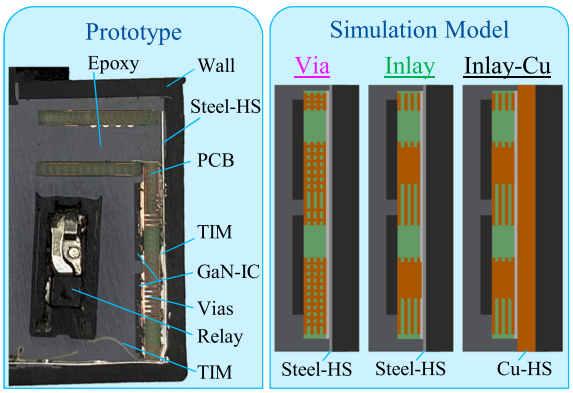

FIGURE 5. Cross section of thermal prototype (left) and comparison of thermal half-bridge models including via structures (right, Via) and thermally equivalent inlay structures (right, Inlay). Heat spreading is achieved by means of stainless steel (100 μm) or copper (Inlay-Cu, 1 mm) sheet.

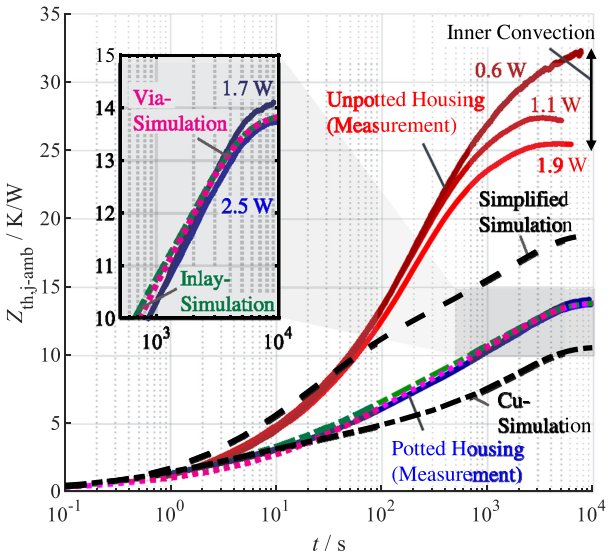

FIGURE 6. Thermal impedance junction-to-ambient of the thermal prototype half-bridge with losses applied to both GaN HEMTs simultaneously for potted and unpotted housing. Measured $Z_{th,j-amb}$ is equal to $Z_{th,j-amb,S1} || Z_{th,j-amb,S2}$ to account for thermal coupling. Dashed curves show corresponding thermal simulations from different models.

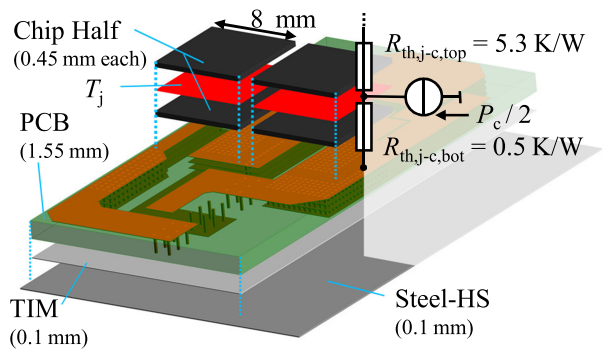

FIGURE 7. Thermal model of the four-layer half-bridge considering GaN power stage package data-sheet values for top to case and bottom to case cooling.

wall. Due to the capacitive coupling of the half-bridges and the insufficient hotspot suppression on the surface, a copper heat spreader with a thickness of 1 mm is implemented for each half-bridge separately in the final prototype. The thermal impedance is measured by the on-resistance R_{on} as a thermo-sensitive electrical parameter (TSEP). Heating is performed by means of conduction losses P_c across both semiconductors S_1 and S_2. Calibration of the temperature dependence of R_{on} via measurements at low sense-current in the thermal chamber over a temperature range of 10 to 70 °C shows very good agreement with the data-sheet values. Impedance measurement and TSEP calibration are implemented as a four-port measurement.

b) Thermal Impedance: The thermal resistance for an unpotted housing ($R_{th,j-amb} = 25$ K/W; see Fig. 6) and the maximum half-bridge losses of 2.1 W determined via simulation and measurement result in a steady state junction temperature of 72.5 °C at an ambient temperature of 20 °C. Neglecting thermal coupling of other loss sources, the converter can be operated in first approximation without limitation by the maximum junction temperature of 125 °C. By using potting material to reduce the thermal resistance to less than 15 K/W, the semiconductor temperature does not limit the power density anymore. In this case the junction temperature is reduced to 49 °C. For the copper heat spreader the junction temperature results in 42 °C. Furthermore, a simulation of the unpotted converter requires complex fluid 3D-FEM simulations of the internal convection, which significantly impacts virtual prototyping optimization. This can be seen in the loss dependence of the thermal impedance, which is caused by the temperature dependence of the internal convection. The outer convection takes place at significantly lower temperature differences and thus shows less dependence on the power loss.

c) Modeling: Since no exact geometry information about the internal power stage chip structure is available from the manufacturer, the chip is modeled according to the data-sheet thermal junction-to-case top $R_{th,j-c,top}$ and junction-to-case bottom $R_{th,j-c,bot}$ resistance. Unfortunately, a simplified model consisting of a Si block on FR-4 does not produce accurate enough results (see Fig. 6, simplified simulation). By dividing the semiconductor into two halves, the high conductivity towards PCB and the low conductivity towards epoxy can be modeled. The thermal conductivity of the bottom side $\lambda_{Chip,bot}$ and that of the top side $\lambda_{Chip,top}$ are calculated with the chip package area A_{Chip} and half of the chip package height l_{Chip} according to

$$\lambda_{Chip} = \frac{l_{Chip}}{2R_{th,j-c}A_{Chip}} \tag{5}$$

In addition to modeling the chip and its thermal connection to the housing, the copper layers and vias in which initial heat spreading takes place must also be modeled. Although the geometries are known exactly, the model structure must not become too complex in order to limit the computing effort for virtual prototyping. Instead of simulating each of the 360 vias per half-bridge in the optimization process, the structure

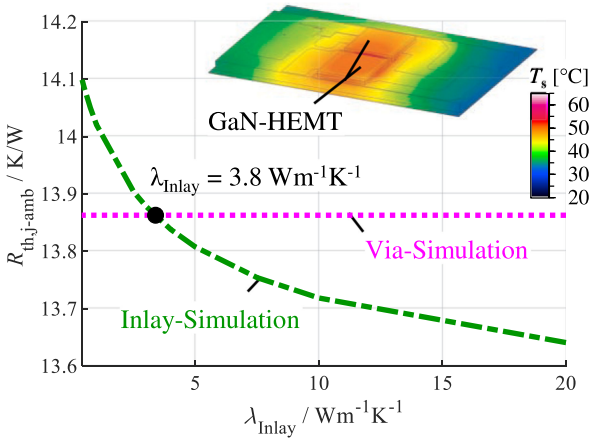

FIGURE 8. Dependence of the junction to ambient resistance $R_{th,j-amb}$ on the thermal conductivity λ_{Inlay} of the inlay used for modeling the via structure.

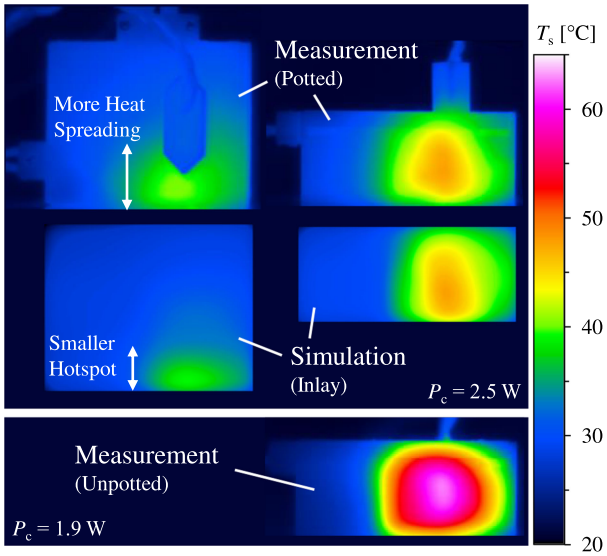

FIGURE 9. Thermographic measurement of package surface temperature for losses applied to the 60 kHz PFC half-bridge.

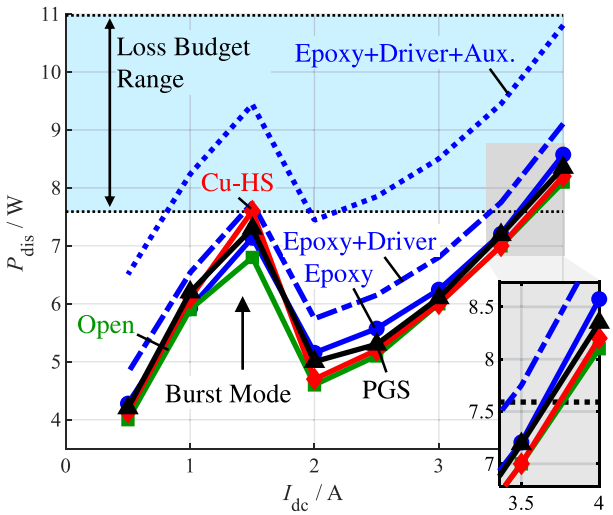

FIGURE 10. System losses at an output voltage of 40 V for different build-up stages of the system. Losses of the power section in open (green), open with copper heat spreaders (red), open with copper and graphite heat spreaders (black) and potted system (blue) configuration. The dotted lines include system driver and auxiliary losses of the signal amplification and isolation.

can be simplified to an inlay (see Fig. 5). The system simulation with one via-half-bridge and two inlay-half-bridges has 949000 mesh nodes. The same system simulation with three half-bridges simplified with inlays has 388000 mesh nodes. The thermal conductivity of the inlay does not correspond to either copper or FR-4, but represents an effective thermal conductivity of the via structure. By matching the thermal junction-to-ambient resistance of the conductivity-dependent inlay simulation to the via simulation, λ_{Inlay} is determined to be 3.8 W m^{-1} K^{-1} (see Fig. 8). Solder layers between chip package and PCB are neglected. Both via-simulation and inlay-simulation show high agreement with the thermal impedance measurement (see Fig. 6). For the setup with a copper heat spreader, the 3D-FEM simulation results in a reduced thermal junction-to-ambient resistance of 10.5 K/W.

D. POTTING WITH EPOXY RESIN

An unpotted structure is sufficient to comply with junction temperature limits by first approximation. If this approximation is not accurate, the larger copper heat spreader used in the final prototype ensures compliance. However, maintaining the maximum surface temperature is only enabled by the thermally conductive potting material. Fig. 9 shows the surface temperature distribution for the thermal impedance measurements from Fig. 6. Even with higher power dissipation, the potted structure shows a significantly reduced maximum surface temperature. The thermal resistance $R_{th,s-amb} = \Delta T_{s,avg}/P_c$ is reduced by 39%. Furthermore, the 3D-FEM simulation also shows good agreement for the surface temperature distribution (see Fig. 9). Only the hotspot on the bottom and top of the housing demonstrates slightly less heat spread in the simulation. This indicates a deviating convection or underestimated thermal conductivity of the epoxy resin. The high confidence in the thermal conductivity characterization by several measuring methods indicates a mismatch due to the nonlinear natural convection model. Since this model is approximated based on a reference design with slightly different dimensions and for losses distributed over the entire housing, minor deviations are possible. For complete system simulations with temperature distributions closer to the reference measurement, a better agreement is expected. In addition to epoxy resin, thermal silicone with a thermal conductivity of 1.55 W m^{-1} K^{-1} was tested, but proved too difficult to distribute without air pockets in our manual dispensing process. The epoxy resin with a thermal conductivity of 1.54 W m^{-1} K^{-1}, in contrast, shows no visible air inclusions (see Fig. 5). The influence of the epoxy resin on the electrical properties of

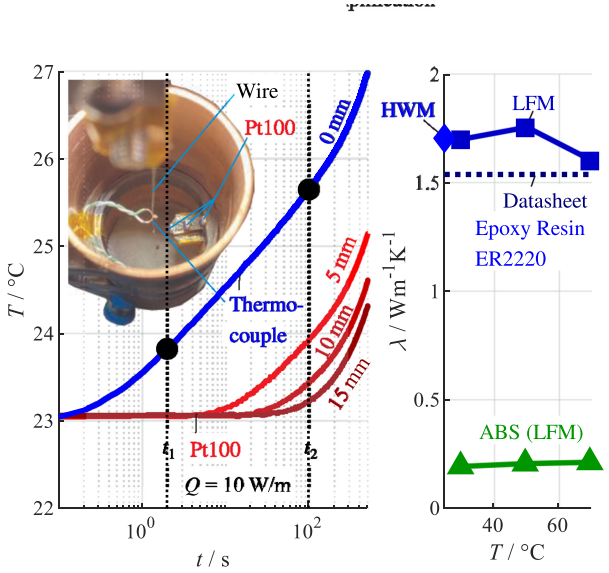

FIGURE 11. Temperature step responses of the HWM measurement for a power step with $Q = 10$ W/m power per unit length (left). Temperature dependent thermal conductivity of ABS and Eposy Resin ER2220 determined via HWM and LFM (right).

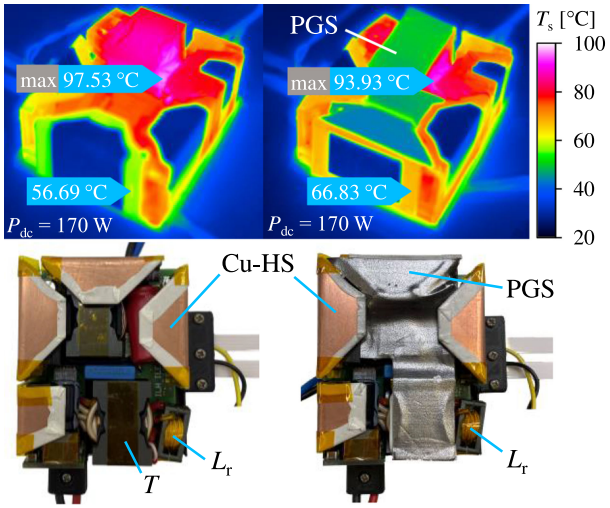

FIGURE 12. Thermographic analysis of the battery charger in open and fanless operation without (left) and with PGS (right) as an additional heat spreader for magnetic components.

the design were also investigated [29]. Fig. 10 shows the measured system losses of the charger for different build-up levels. In direct comparison, the losses increase with the use of epoxy compared to the unpotted structure by 3% at maximum output current of 4 A. The reason for this is a frequency-dependent increase in parasitic electrical capacitances due to the elevated dielectric constant ϵ_r, which ultimately leads to a shift in the resonance behavior of the LLC stage. This results in higher losses in the core material of the transformer compared to the optimized behavior in the open system. A redesign of the resonant tank could compensate those losses.

E. MATERIAL PROPERTIES

Where available, data-sheet parameters of the different materials in the system are used for the thermal simulation. Where this is not the case, typical literature values such as a thermal conductivity of 400 W m^{-1} K^{-1} and a specific heat of 385 J kg^{-1} K^{-1} for copper are assumed. Due to the slight deviations between simulation and measurement in the surface temperature (see Fig. 9), the conductivity of the thermally conductive epoxy resin ER2220 in particular is characterized by different measuring methods. Fig. 11 (left) shows the unpotted measurement setup and the results for the implemented hot wire method (HWM) for ER2220 conductivity measurement. Based on the one-dimensional radial heat flow model, the thermal conductivity is determined with dynamic temperature changes of a hot wire within the material [31]. Therefore, a nickel-chromium (NiCr) resistance wire is heated with known losses and the temperature step response is measured with temperature sensors at a known radial distance. The measurement setup is equipped with three Pt-100 sensors at different distances and a K-type thermocouple with direct contact. From the measured temperature change, according to

$$\lambda = \frac{Q}{4\pi\left(T(t_2) - T(t_1)\right)} \ln\left(\frac{t_2}{t_1}\right), \tag{6}$$

the thermal conductivity can be derived. The measurement with 0 mm distance shows the characteristic curve in logarithmic time scale and results in 1.7 W m^{-1} K^{-1} according to (6). The results at 5 mm show a much smaller range in which the behavior corresponds to the ideal radial model, but gives a similar thermal conductivity with greater uncertainty. A distance greater than 5 mm does not give clear results.

As a second characterization method, a laser flash method (LFM) measurement is performed according to the standard DIN EN 821-2 [32]. The method determines the conductivity based on the temperature rise through a thin test sample triggered by a short energy pulse. Fig. 11 (right) shows the thermal conductivity derived from the known density (2.22 g/mL) as a function of temperature. The results confirm the HWM and are higher than the data-sheet value within the relevant temperature range. In addition, the specific heat is derived from the measurement ranging from 1.15 to 1.37 J g^{-1} K^{-1} as a function of temperature. Furthermore, the material parameters of the ABS material for the 3D-printed housing are determined. The simulation results presented in this work utilize the temperature-dependent results of the laser flash measurement for ABS and ER2220.

F. GRAPHITE HEAT SPREADING

Fig. 12 (left) shows the miniaturized setup in unpotted operation outside the housing. Thermographic measurements show a surface temperature below 100 °C for nominal operation at 170 W. To avoid higher temperatures an unpotted operation inside the housing is avoided. By separating the different converter stages, a temperature gradient is introduced between the PFC and the less efficient LLC stage. A difference of 41

K can be observed between the transformer windings and the copper heat spreader (Cu-HS) of the 50 Hz PFC half-bridge. The measurement is carried out on non-reflecting surfaces at the Cu-HS edge with TIM on top. To prevent this imbalance, both converter stages must be better thermally coupled to each other. However, due to eddy currents, no metal heat spreaders or heat pipes can be placed close to the transformer. The additional losses would lead to a low efficiency and an exceeding of the power loss budget.

As an alternative approach for heat spreading, pyrolytic graphite sheets (PGS) are investigated. The 100 μm thin sheets have a very high thermal conductivity of 700 W m^{-1} K^{-1} in plane and 26 W m^{-1} K^{-1} through plane. This makes them very well suited for temperature balancing. The transformer and Cu-HS of the PFC stage are therefore connected via two PGS on both the top and bottom sides of the housing. Double-sided adhesive TIM ensures electrical isolation and good thermal connection of the ferrite and copper surfaces to the graphite. Fig. 12 (right) shows the temperature difference reduced by 34% to 27 K in the thermal steady state. Like copper, the graphite also reflects thermal radiation and cannot directly be measured thermographically. According to the data-sheet, the graphite material has a very high electrical conductivity of $1\times$ 10^4 S/cm, but showed poor conductivity when actually measured with a multimeter. Contrary to initial expectations, the losses with PGS increase relatively little by 2.6% at an output current of 4 A (see Fig. 10). The reason for this behavior could be the different electrical conductivity in-plane and through-plane of graphite [33] as well as the magnetoresistance ($\Delta\rho/\rho$) of 6.2 $\times$ 10^{-2} (at 0.4 T) of the used PGS [34]. Whether eddy currents can in principle be avoided with graphite heat spreaders requires further investigation. To significantly reduce the transformer hotspot, the additional losses are accepted and the PGS is included in the final potted prototype. As an alternative approach to further reduce the hotspot, newly developed methods of topology optimization with targeted heat flow control also show promising results [35].

In this section, the analytical description of power density limits by surface temperature standards were addressed and natural convection as dominant cooling mechanism was investigated. Short fins on the surface of the evaluated housing increase convection only minimally and do not result in power density benefits. To avoid limiting hotspots, heat spreading measures were analyzed for the charger application. Thermally conductive potting material and heat spreaders made of metal and PGS can be used to effectively compensate for temperature gradients on the surface. In addition, natural convection, material parameters and model structures were evaluated for model-based optimization.

IV. EXPERIMENTAL RESULTS

The experimental hardware prototype shown in Fig. 1 was built and tested. Fig. 13 shows the voltage and current waveforms of the AC input and DC output of the battery charger. A power factor $cos(\varphi)$ of 0.969 is achieved. However, a conclusive EMI measurement is prevented with the ground connection to the external rapid prototyping system. The efficiency measurements are conducted using a ZES Zimmer LMG670 power analyzer with a 10 kHz AC and 10 MHz DC bandwidth. Fig. 14 shows the efficiency of the charger power section and the overall system. At maximum output power, the power section achieves 95.4% efficiency, which drops by 1.2 percentage points without SR. Taking the driver and auxiliary supply into account, the efficiency is reduced to 95.2%. Here, the main potential for electrical optimization is found in avoiding inefficient measurement amplification to high voltages ($\pm$12 V) and additional DC/DC converters to isolate supply voltages on the output side. Corresponding ASIC controllers do not allow the optimization of the control system implemented in this work, but are significantly lower in loss overall. In Fig. 15 (left) the thermographic measurements at 170 W output power and 20 °C ambient are visible. With an average steady-state surface temperature of 59.8 °C,

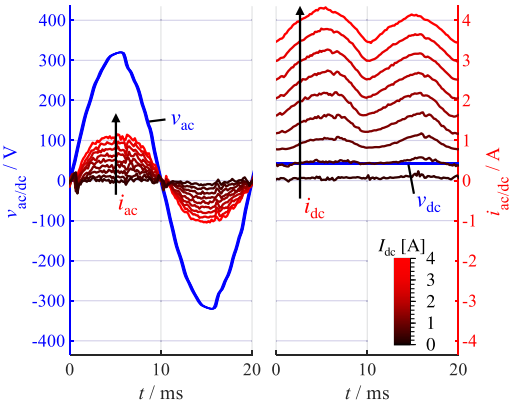

FIGURE 13. Voltage and current characteristics of the grid input and the battery charger output for different battery load currents I_{dc} between 0 and 4 A at an output voltage of V_{dc} = 42 V.

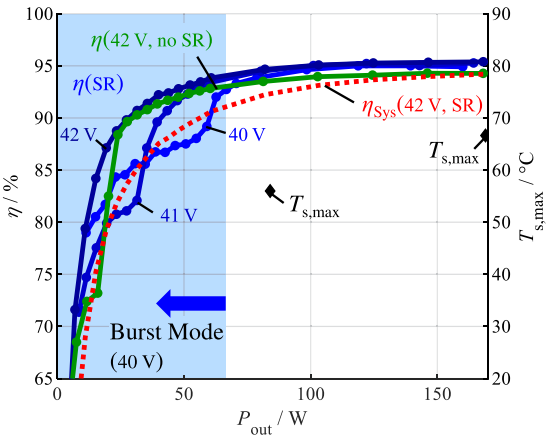

FIGURE 14. Efficiency of the potted battery charger power section for output voltages between 40 and 42 V (blue) and of the power section without synchronous rectification at 42 V (green). Efficiency of the total system including driver and auxiliary losses for an output voltage of 42 V (red). Diamond markings show the maximum surface temperature in steady state for ambient temperature T_{amb} = 20°C.

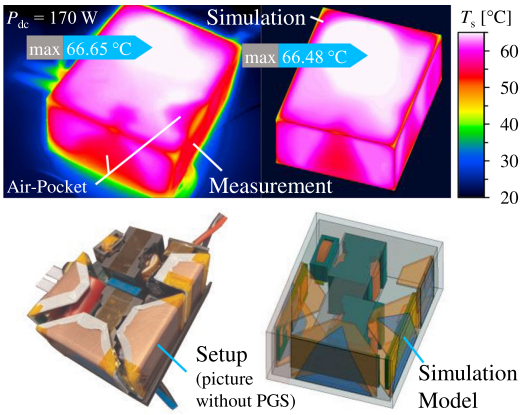

FIGURE 15. **Thermographic measurements of the battery charger housing surface of the potted assembly at 170 W output power (left). Temperature is corrected by 5 K for the specified ambient temperature of $T_{amb} = 20°C$. Results of 3D-FEM thermal simulation for surface temperature at 170 W output power (right).**

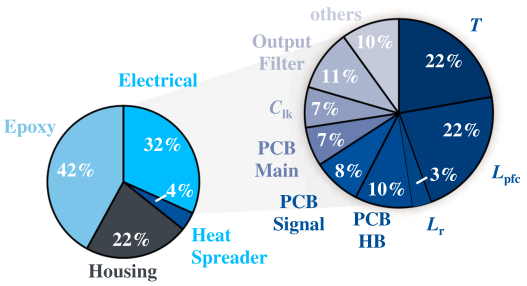

FIGURE 16. **Breakdown of system components and their share in the total volume of 0.11 dm³.**

a very good temperature distribution close to the maximum temperature of 66.7 °C is achieved, especially due to epoxy resin and PGS heat spreading. However, this lies slightly above the selected limit of 65 °C. Assuming no change in thermal resistance $R_{th,s-amb}$ for minor loss adjustments results in 95% of nominal output power at 65 °C maximum surface temperature, taking power dependent efficiency into account.

A closer look at the surface temperature distribution shows colder areas at the copper heat spreaders. The potting did not reach all areas due to higher contact pressure between heat spreaders and plastic wall compared to the thermal prototype from Fig. 5. Prior epoxy application directly to the copper surfaces or larger clearances can prevent this. The thermal 3D-FEM simulation of the experimental prototype including air-pockets, visible in Fig. 15 (right), shows a high agreement with the measured results. The simulation without air pockets for a defect-free potting results in a maximum surface temperature of 65.6 °C and thus 98% of the nominal output power. No power reduction is required for the temperature limit of the EN 60335-1 standard [12]. In addition, Fig. 16 shows the distribution of the system volume between housing, epoxy resin, heat spreader and electrical components.

The results presented in this section show that with additional measures such as thermally conductive epoxy resin and PGS, the critical temperature limits of the standards can be met. In the following section, the remaining optimization potential is determined within a virtual prototyping process.

V. THERMAL POWER DENSITY OPTIMIZATION WITH VIRTUAL PROTOTYPING

In order to make predictions with high accuracy, a highly accurate thermal model is required. However, additional losses due to parasitic influences occur only in the miniaturized hardware structure and are difficult to estimate using simulations alone. This is especially relevant for effects that have not been investigated in detail, such as the interaction with specific epoxy resins [29] or eddy current losses in graphite heat spreaders with magnetoresistance [34]. Therefore, the thermal model is improved with the hardware prototype measurement results and then used to estimate the further optimization potential in terms of power density by varying the thermal design in a virtual prototyping process. The model improvements include the adjustment of component losses to the efficiency measured in the hardware prototype of the entire system from Fig. 14. Besides an increase in the loss share of the transformer due to the epoxy resin, the remaining loss distribution is retained. A more precise characterization is challenging due to the miniaturized structure and encapsulation with epoxy resin. However, the high agreement of the surface temperature distribution and thermal half-bridge impedances confirms the high accuracy of this approach.

The developed virtual prototyping system utilizes the thermal 3D-FEM tool Ansys, the numerical tool Matlab and the computer aided design (CAD) tool FreeCAD. With the CAD tool, variable 3D-models of the system are generated (see Fig. 15 bottom, right) and transferred to the 3D-FEM tool. Within a simulation loop, the maximum surface temperature is adjusted to the limit of 65 °C by iteratively changing the output power according to the efficiency characteristics. The maximum deviation of all performed simulations is 90 mK. The virtual prototype systems thus make full use of the surface temperature limit for maximum power density. The numerical tool controls the automated process and sets component losses and geometry parameters. The position of the components, the housing dimensions, the housing wall thickness as well as the material, thickness and spacing of the metal heat spreaders are varied. In Monte Carlo simulations, parameter selection is done randomly based on predefined value ranges and piecewise-uniform probability distributions. More extreme component edge positions or a particularly thick housing wall are thus less likely. The value range changes depending on other variable parameters such as the housing dimensions.

Fig. 17 shows the achieved volume and the output power of the different virtual system configurations, limited by the housing temperature. This results in a pareto-front, which shows the maximum optimization potential through the system changes of the prototyping approach. This front is very close to the housing power density limit, especially around 150 W. This housing limit is calculated using the maximum

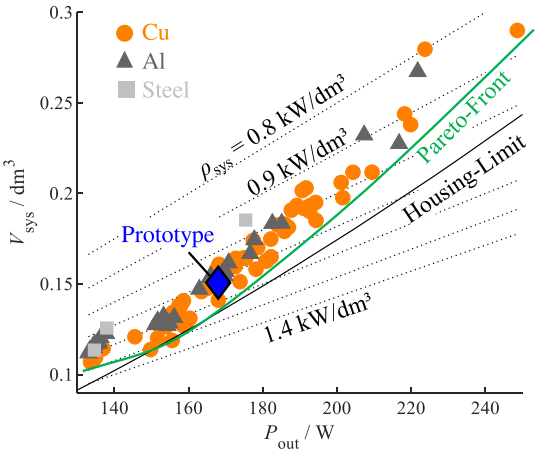

FIGURE 17. Thermal virtual prototyping results of different volume and output power at a fixed maximum surface temperature of 65°C ± 90*mK* for various heat spreader materials.

system efficiency $\eta_{sys} = 95.2\%$, the hardware prototype aspect ratio and the average heat transfer coefficient for the maximum power dissipation budget $\alpha = 13.5$ W m^{-2} K^{-1} according to (3). Thus, the limit applies to a uniform temperature distribution. However, better aspect ratios allow the limit to be exceeded. Prototypes with copper heat spreaders show a higher power density than those with aluminum heat spreaders. Due to the higher thermal conductivity they can avoid surface hotspots more effectively. The few prototypes with stainless steel heat spreaders similar to the thermal hardware prototype (see Fig. 5) show the lowest power density due to small thermal conductivity. The Pareto front reaches the housing limit for an output power of 150 W. For higher power, especially the hotspot at the transformer increases. Since no metal heat spreaders are an option here, the temperature distribution can only be improved to a limited extent with additional volume and the power density decreases. For systems with higher output power than the hardware prototype, a constant efficiency is assumed. With the expected drop in efficiency due to additional losses, especially in magnetic components, an even sharper rise of the Pareto front is expected for losses greater than 170 W. For powers smaller than 150 W, the pareto front deviates from the housing limit due to reduced system efficiency. In addition, housings with a volume smaller than the hardware prototype require a higher degree of 3D-integration. According to the volume distribution in Fig. 16 with 42% potting material, there is still potential for optimization. In particular, custom form factors of magnetic and electrical components could be used for this purpose. Furthermore, the higher dielectric strength of the epoxy resin (10 kV/mm) may allow isolation distances to be reduced. The virtual prototyping thus shows that a power density of 1.3 kW/dm^3 is possible for an output power of 150 W with higher 3D-integration levels and optimized thermal design.

In this section, the results indicate that the charger power density in-housing can be further increased to the convection limit of the plastic housing by an automated process of component placement. However, since the optimization does not yet take all design restrictions into account, the improvements could not be directly implemented in a further prototype. Despite not fully utilizing the housing convection limit, to the authors' best knowledge, the presented hardware charger achieves the highest reported in-housing power density in its power class. This represents an improvement of over 50% compared to current technology for laptop and small electric vehicle charging. Table 2 shows the battery charger performance metrics in comparison.

TABLE 2. Battery Charger Performance Metrics

Parameter	[3]	[4]	[36]	Prototype
Type	pub.	pub.	com.	pub.
Output Power	150 W	150 W	180 W	170 W
Volume (Open)	0.06 dm^3	0.11 dm^3	-	0.11 dm^3
Volume (Housing)	-	-	0.26 dm^3	0.15 dm^3
Efficiency	95 %	95.5 %	-	94.2 %
Power Density (kW/dm^3)				
Open	2.4	1.3	-	1.6
Housing	-	-	0.7	1.1 (1.3)

VI. CONCLUSION

In this work, a high-density GaN-based battery charger for mid-power applications such as small electric vehicles and high-performance laptops is presented. The thermal limit of power density, which is critical in this application context due to the maximum housing surface temperature, is introduced. Additional investigations results on the influence of PGS as a heat spreader for magnetic components and epoxy resin as a thermally conductive potting material are discussed. The hardware prototype achieves a power density of 1.6 kW/dm^3 for open and 1.1 kW/dm^3 for in-housing operation, which is an improvement of over 50% compared to current technology in laptop and small electric vehicle charging. However, EMI cannot not be reliably determined due to the use of a rapid prototyping system and might reduce the achieved power density with additional filtering effort. Furthermore, the remaining thermal optimization potential is estimated up to 1.3 kW/dm^3 based on virtual prototyping simulations. These results indicate the potential improvement in power density that can be achieved with GaN devices and by addressing surface temperature standards with advanced heat spreading using graphite sheets and epoxy resin along with optimized component placement.

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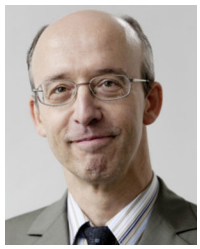

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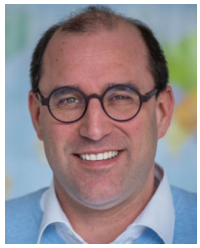

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