IEEE Open Journal of
Power Electronics

Received 24 November 2021; accepted 8 December 2021. Date of publication 13 December 2021;
date of current version 27 December 2021. The review of this article was arranged by Associate Editor Cong Li.

Digital Object Identifier 10.1109/OJPEL.2021.3134640

A Review of Thyristor Based DC Solid-State Circuit Breakers

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ABSTRACT Characterized by ultra-fast and arc-free fault clearing, solid state circuit breakers (SSCBs) are getting increasing popularity with the latest development of advanced power semiconductor devices, like the silicon carbide (SiC) MOSFETs. On the other hand, the mature and cost-effective thyristor technology exhibits the beneficial features of low conduction losses, high surge current capability, bidirectional voltage blocking capability, etc., making it a very attractive candidate for SSCB development. However, the conventional thyristors (silicon controlled rectifiers) have no current turn-off capability and need some auxiliary circuits (e.g., LC resonant circuit) or special topology (e.g., Z-source breakers) to be applied in SSCBs. Meanwhile, some active turn-off thyristors (like integrated gate-commutated thyristors, emitter turn-off thyristors, etc.) are specially modified to have current turn off capability, and better suitable for SSCBs. This paper reviews and studies the SSCBs based on the conventional or active turn-off thyristors. The design challenges and performance comparison of SSCBs with different thyristor technologies are also discussed.

INDEX TERMS Thyristor, solid state circuit breaker, integrated gate-commutated thyristor, Z-source breaker, silicon carbide.

I. INTRODUCTION

The popularity of solid state circuit breakers (SSCBs) is increasing during recent years due to the advantages of ultra-fast fault clearing speed, arc-free current interruption and low peak fault current compared to conventional mechanical breakers. The power semiconductor devices in SSCBs can switch off within 100 ns to 10 μs depending on the selection of semiconductor technology, which is 2$\sim$4 orders of magnitude faster than any switch based on mechanical contact or any semiconductor-mechanical hybrid solutions [1]. In addition, the higher safety without risks of arc energy exposure, long lifetime (millions of operations with near-zero servicing requirement) make the SSCB a promising candidate for the next generation of power system protection, especially for the emerging direct current (DC) power systems. Because of the absence of natural zero current crossing in DC system, mechanical circuit breakers require additional arc extinguishing mechanisms to force the fault current to zero, which leads to a bulky and complicated design. Taking advantage of power semiconductor device's fast and arc-less current turn-off capability, SSCBs are finding more and more applications from low voltage DC (48 – 1500 V) to lower range of medium voltage (MV) DC (5 – 10 kV). The potential applications of SSCBs in low voltage DC include commercial and naval vessels [1], data centers [56], aviation power distribution [57], battery protection [58], Photo-Voltaic (PV) systems [59], power converter protection [60], Electric Vehicle (EV) charging infrastructure [61], etc. Applicable MVDC power systems include railway power systems [62], electric shipboard requiring high voltage and high power.

One major challenge with the SSCB is the high conduction losses due to the much higher voltage drops across the power semiconductor devices compared to the traditional electromechanical contacts. Then the selection of the right semiconductor technology and devices for a SSCB is of essential importance.

Developed as early as 1960s, thyristors are still the main workhorse in high power applications such as HVDC, FACTS, etc., thanks to their large power handling capability [2], [3]. Fig. 1 shows a survey of the state-of-art commercial

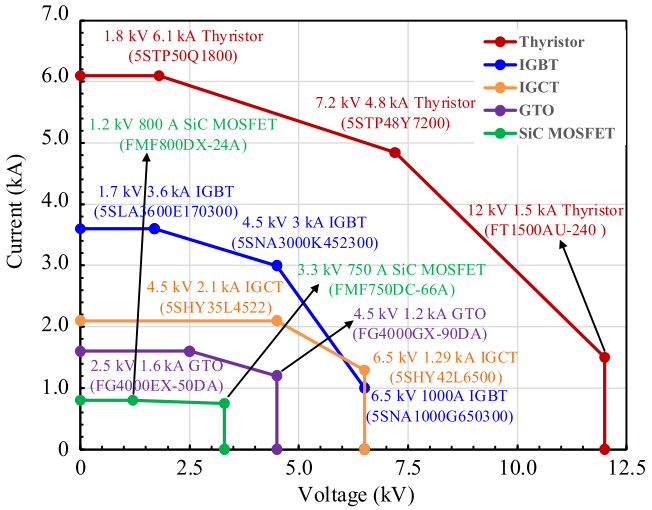

FIG. 1. **State-of-the-art commercial 3-terminal controllable power devices in terms of the upper boundary of the voltage and current ratings achieved in a single-packaged device [2].**

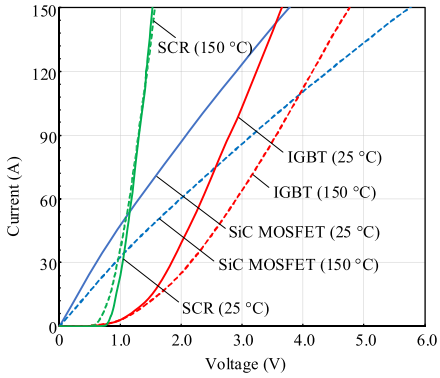

FIG. 2. **I-V curves of the SiC MOSFET [4], IGBT [5] and thyristor [6] at room temperature (25 °C) and high temperature (150 °C).**

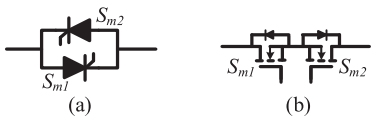

FIG. 3. **(a) SSCB topology based on anti-parallel connected symmetric thyristors; (b) SSCB topology based on anti-series connected SiC MOSFETs.**

TABLE I. **SiC MOSFET, IGBT and Thyristor Comparison**

Features		Device Type		
		SiC MOSFET	IGBT	Thyristor
Device		C3M0021120K	IXYR100N120C3	CS60-12io1
Voltage Rating		1200 V	1200 V	1200 V
Current Rating	Continuous (110 °C)	70 A	56 A	60 A
	Pulsed (1 ms)	200 A	450 A	>1500 A*
Price		5x	1.7x	1x

*8.3ms, 60 Hz sinusoidal current

controllable power devices in terms of the upper boundary of the voltage and current ratings achieved in a single-packaged device [2]. The Si thyristor have achieved the highest voltage and current ratings (up to 12 kV, 1.5 kA) among the 3-terminal controllable power devices due to the excellent bipolar conduction mechanism, indicating a high commercial readiness and great potential for high voltage high power applications.

Wide bandgap (WBG) power devices, like SiC MOSFETs, demonstrate promising prospects in power converter as well as SSCB applications, thanks to the much lower specific on-state resistance, the high switching speed and blocking voltage capability compared to the Si counterpart device [3]. From a semiconductor current conduction mechanism point of view, the thyristor technology has the lowest forward conduction losses at high current due to its strong conductivity modulation. For example, three different types of power semiconductor devices [4]–[6] with the same voltage rating (1.2 kV), device package (TO-247) and similar continuous current ratings (~60 A) are selected and compared in Table I.

Fig. 2 compares the I-V curves of the three selected power devices, and shows that the SiC MOSFET has better conduction characteristics at low current level (<30 A) due to its unipolar device characteristics. At high current level (>50 A), the thyristor demonstrates the lowest conduction voltage drop, thanks to the double-sided carrier injection and strong conductivity modulation. The thyristor's advantage of better conduction characteristics is more obvious at higher temperatures. Another important advantage of the thyristor is its high pulse current (surge current) capability, ~7 times better than the SiC MOSFET, according to Table I. The surge current capability is one of the most important requirements for the power semiconductor devices in the SSCB application, as the power devices need to withstand the short circuit fault current which could rise to several times (e.g., 5 times) of the normal current.

Besides the advantages of low conduction voltage drop at high current level and the high surge current capability, the thyristors with symmetrical structure have bidirectional (forward and reverse) voltage blocking capability, which means no second device connected in anti-series is needed to block the reverse voltage in bidirectional SSCBs, as shown in Fig. 3. This further reduces the SSCB conduction losses with half number of devices in the conduction path.

Table I also list the high volume price information of the three types of power devices from the distribution website [7]. The thyristor appears a more cost-effective solution due to the mature device fabrication technology and the relatively lower material (Si compared to SiC) cost.

In summary, the beneficial features including the low conduction losses, high surge current capability, bidirectional voltage blocking capability, high technology readiness

level and low prices, all make the thyristor technology a very attractive candidate for SSCB application. Another essential requirement for the power semiconductor devices in the SSCB is the current interruption/turn-off capability. However, it's well known that the conventional thyristors (Silicon-Controlled Rectifiers or SCRs) are semi-controlled power devices, having no current interruption capability. To empower the thyristor with turn off current capability, two technologies are developed: i) thyristor forced commutation technique [8]; and ii) modified thyristor structure with current turn-off capability.

The thyristor forced commutation technique usually needs some auxiliary circuit (LC resonant circuit) connected in parallel with the thyristor. Although the thyristor forced commutation technique is not new [8], only a few papers studies and applies this technique in SSCB. Ref [9], [10] investigate the forced commutation thyristors based AC SSCBs, and this paper further investigates and evaluates the different topologies in DC system which requires faster current interruption speed. In addition, the design guidelines and circuit limitations with the forced commutation thyristor based SSCBs are elucidated in the paper.

For the technology ii) (modified thyristor structure), one good example is the gate turn-off thyristor (GTO) [11] or gate commuted thyristor (GCT) technology [12], [13]. To further increase the device's controllability and facilitate the gate driver design, the technologies like the integrated gate-commutated thyristor (IGCT) [14], [15], and emitter turn-off thyristor (ETO) [16], [17], etc. are invented and called active turn-off thyristors. The active turn-off thyristor based SSCBs have been investigated extensively in the past decade [1], [18]–[24] and the paper reviews the technology status in the SSCB application and summarizes the advantages and disadvantages with these technologies.

The Z-source breaker [25]–[29] is also one type of thyristor based SSCB and can be categorized into the forced commutation thyristor based SSCBs. However, due to its particularity in topologies and wide research interests, it was discussed and summarized in one single section. This paper systematically summarizes and compares the different types of Z-source breakers. Specially, the technical challenges limiting the wide application of the Z-source breaker are explained and summarized.

The paper is organized as follows: In section II, the SSCBs based on conventional thyristor topology (SCR) are studied and compared, and in Section III, the different types of Z-source breakers are compared, and their design challenges and limitations are elucidated. Section IV reviews SSCBs based on the active turn-off thyristors including IGCT, ETO, etc. Section V provides a performance comparison of the thyristor based SSCBs in literature and discusses their strengths and weaknesses. Section VI concludes the paper.

II. FORCED COMMUTATION THYRISTOR BASED SSCBS

The conventional thyristors (SCRs) are known as a semi-controlled power device, which can be fired to turn on the current by gate signals but does not have current interruption capability. To switch off the SCR, there are two techniques: natural commutation and forced commutation. The natural commutation is usually used in AC systems, where the SCR is turned off after the current zero-crossing point and a reverse biased voltage is applied to the anode of the SCR. The natural commutation technique does not need external circuits or components to assist the SCR turn-off but requires current zero crossing or AC voltages. In opposite, the forced commutation technique requires some auxiliary circuits to force the SCR current commutate to zero. To ensure the reliable turn-off of the SCR, a reverse biased voltage is applied to the anode of the SCR and must last long enough for the SCR to complete the reverse recovery and excess carriers recombination process. This time period is usually called the thyristor turn-off time in the device datasheet [6]. If a forward biased voltage is applied to the SCR within the turn-off time, the SCR would be self-triggered and turned on again by the remaining charge carriers left unrecombined in the PN junction.

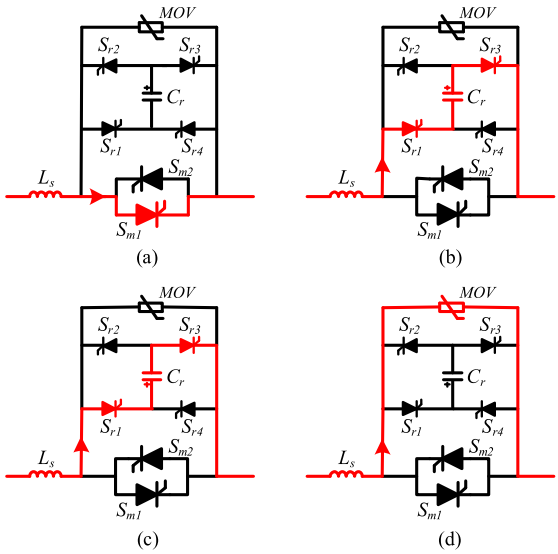

FIG. 4. Operation modes of Topology #1 which uses SCRs as auixiliary switches. (a) Normal conduction mode (t_1-t_2); (b) Main SCR S_{m1} turn-off mode (t_2-t_3); (c) Pre-charge capacitor C_r reverse charging mode (t_3-t_4); (d) MOV clamping mode (t_4-t_5).

The thyristor natural commutation technique cannot be applied in DC power systems due to the lack of current zero crossing point, while the forced commutation thyristor could be used. With very few papers [40], [41] investigating the thyristor forced commutation techniques in DC solid state circuit breaker applications, the next part of the section will present and discuss some feasible forced commutation thyristor based SSCB topologies, providing some key design guidelines and topology limitations.

A. TOPOLOGY #1

Fig. 4 shows one SSCB topology (Topology #1) based on thyristor forced commutation technique [9]. The main SCRs

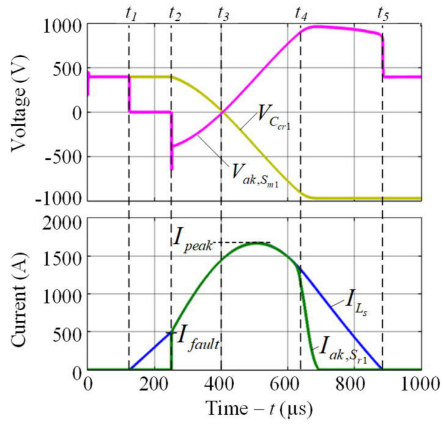

FIG. 5. Current interruption waveforms of the thyristor based SSCB Topology #1 with 500 A as fault tripping current level.

(S_{m1} and S_{m2}) are connected in anti-parallel for bidirectional current conduction, and an auxiliary SCR and pre-charged capacitor (C_r) based auxiliary circuit is connected in parallel with the main SCRs (S_{m1} and S_{m2}). The four auxiliary SCRs ($S_{r1} \sim S_{r4}$) are forming a bridge for bidirectional current interruption. Fig. 5 shows the simulated current interruption waveforms of Topology #1, where the system voltage is 400 V, system parasitic inductance $L_s = 100\ \mu$H, the capacitor $C_r = 0.4$ mF with 380 V pre-charged voltage (V_{Cr}), and the MOV clamping voltage is ~1000 V.

The different operation modes of Topology #1 during current interruption process is illustrated in Fig. 4. By turning on the auxiliary SCRs (S_{r1}, S_{r3}), the main SCR (S_{m1}) current is forced to commutate to the auxiliary SCR branch and a reverse biased voltage from the pre-charge capacitor is applied to the anode of the main SCR (S_{m1}) as shown in Figs. 4(b) and 5 from t_2 to t_3. At t_3, the capacitor C_r is fully discharged and then reversely charged, starting to apply a forward biased voltage to the main thyristor S_{m1}, as shown in Figs. 4(c) and 5 from t_3 to t_4. The main SCR turn-off time abovementioned should be shorter than the capacitor discharge time from t_2 to t_3 as shown in Fig. 5, otherwise, the main SCR will be falsely turned on again at t_3. Once the capacitor C_r is reversely charged to the MOV clamping voltage (~1000 V), the current will commutate to the MOV branch and eventually decreases to zero, as shown in Figs. 4(d) and 5 from t_4 to t_5.

From Fig. 5, it can be seen that one main disadvantage of Topology #1 is the relatively long current interruption time (~600 μs) due to the thyristor turn-off time (from t_2 to t_3) and the capacitor reverse charge time (from t_3 to t_4). Another disadvantage is the high fault current peak value (~3 times of the fault current trip level) because the fault current keeps rising until the capacitor C_r is reversely charged to the system voltage (400 V).

B. TOPOLOGY #2

To address the high fault current peak level and long current interruption time, an improved topology (Topology #2)

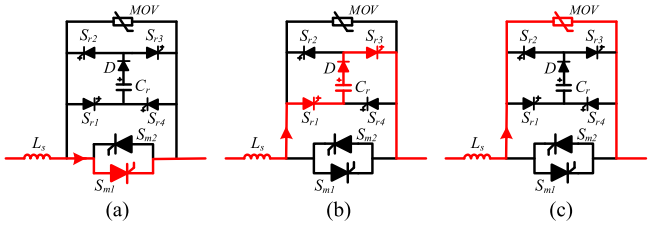

FIG. 6. Operation modes of Topology #2 which uses fully controlled switches like GTOs as auixiliary switches. (a) Normal conduction mode (t_1- t_2); (b) Main thyristor S_{m1} turn-off mode (t_2- t_3); (c) MOV clamping mode (t_3- t_4).

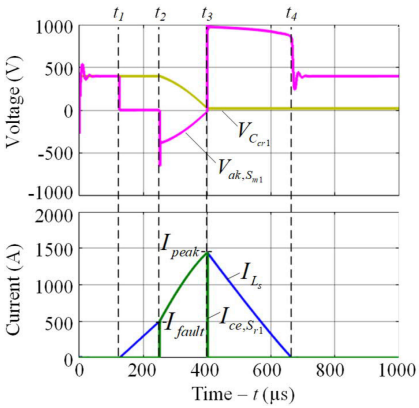

FIG. 7. Current interruption waveforms of the thyristor based SSCB Topology #2 with 500 A as fault tripping current level.

[45] is proposed by replacing the auxiliary SCRs with fully controlled switches (like GTOs or transistors) as shown in Fig. 6. Compared to SCRs, the GTOs or other transistors have higher conduction voltage drop, but the conduction losses in the auxiliary circuits are not relevant due to very short conduction time. With current interruption capability from the auxiliary switches (GTOs), the current is immediately commutated from the auxiliary switch branch to the MOV branch after the auxiliary GTOs (S_{r1}, S_{r3}) are turned off as shown in Fig. 6. (no capacitor reverse charging mode).

Fig. 7 shows the waveforms of Topology #2 during current interruption process under the same test conditions of Fig. 5. Compared with waveforms of Topology #1 (in Fig. 5), the resonant capacitor C_r reverse charging mode is omitted, thanks to the current interruption capability of the fully controlled switches, which as enable a lower fault current peak value (I_{peak}) and shorter current interruption time.

Fig. 8 compares the current interruption time and the peak value of the two topologies when their fault tripping current levels are set from 250 A to 1000 A. It can be seen clearly that Topology #2 has about 30% (~200 μs) shorter current interruption time and 200 A lower peak current value compared to Topology #1.

Another benefit of Topology #2 is that the capacitor voltage becomes unipolar (capacitor is not reversely charged), making it possible to use the polarized capacitors like the electrolytic

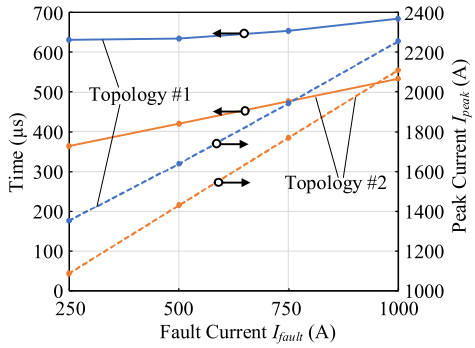

FIG. 8. Current interruption time and peak current level comparion bewteen Topology #1 and Topology #2 when the fault tripping current level (I_{fault}) is set from 250 A to 1000 A.

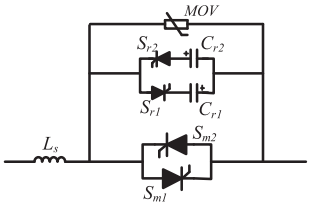

FIG. 9. Topology #3 (alternative circuit for Topology #1 by reducing the auxiliary SCR number and increase one more resonant capacitor).

TABLE II. Comparison of the Forced Commutation Thyristor Based SSCB Topologies

Features	Topologies		
	#1	#2	#3
Number of capacitors	One	One	Two
Number of resonant switches	Four SCRs	Four GTOs +one diode	Two SCRs
Capacitor voltage polarity	Bipolar	Unipolar	Bipolar
Current interruption speed	Slow	Medium	Slow
Peak fault current	High	Low	High
Cost	$$	$$$	$$$$
Volume	Medium	Small	Large

capacitors, which usually have higher capacitance/volume ratio to save the size of the auxiliary circuits and lower cost compared to the non-polar capacitors like the film capacitors.

C. COMPARISON AND DISCUSSIONS

There are some circuit variances compared to Topology #1 and #2. For example, Fig. 9 depicts an alternative topology [9] to Topology #1, by reducing the number of auxiliary switches from 4 to 2 and adding another pre-charge capacitor (C_{r2}). Topology #1 and #3 show similar current interruption waveforms and breaker performances like current interruption speed, peak current level, etc.

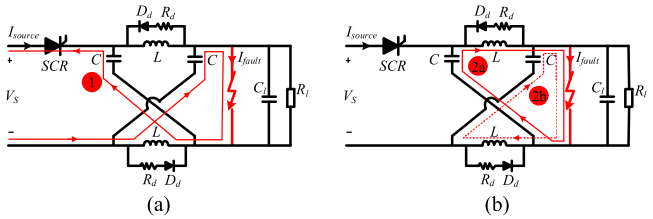

FIG. 10. Crossed Z-source breaker topology; (a) Current path to achieve SCR current zero crossing; (b) LC resonant current paths after SCR current commutates to zero, where the power source current $I_{source} = 0$.

Table II compares and summarizes the different topologies in terms of electronic components needed, current interruption speed, peak fault current level, etc. As discussed above, the capacitor voltage in Topology #2 is unipolar (voltage not reversed), creating the possibility to use the polarized capacitors (e.g., the electrolytic capacitors), which are usually less bulky and cheaper than the non-polar capacitors (e.g., film capacitors). Topology #3 needs two non-polar capacitors, resulting in the largest volume while Topology #2 has smallest volume with only one polarized capacitor needed. Also, the two non-polarized capacitors greatly increase the cost of Topology #3 although it needs only two auxiliary thyristors, which are relatively cheap as compared in Table I. Topology #2 costs higher than Topology #1 due to the more expensive fully controlled switches (like GTOs) used.

The major drawback of the forced commutation thyristor based SSCBs is the long SSCB current interruption time (∼0.4 ms, even for the improved Topology #2), due to the main thyristor turn-off time (usually varying from 100 μs to 250 μs). In this sense, the fast turn-off thyristors with shorter turn-off time are preferred for the main thyristors in the SSCB topology. To be mentioned that, during the main thyristor turn-off time, the fault current in the system keeps increasing, and the forced commutation thyristor based SSCBs are not quite suitable for power systems with high fault (short circuit) current rising rate (di/dt). Another drawback of the forced commutation thyristor based SSCBs is the bulky capacitors needed. Take the Topology #1 as example, to interrupt 500 A current within 0.6 ms, 0.4 mF with 1000 V DC voltage rating non-polar capacitors (e.g., film capacitors) are needed, which take ∼ 1 L volume [64].

III. Z-SOURCE DC CIRCUIT BREAKERS

A. Z-SOURCE BREAKER INTRODUCTION AND OPERATION PRINCIPLES

The Z-source breaker is also developed based on SCRs and has the advantage of autonomous current interruption (no current sensor needed), which eliminates the fault current sensing time, enabling a fast fault clearing speed during a critical short circuit fault. The Z-source breaker is first proposed by Dr. Corzine [25] in 2010, which is named after the Z-source inverter [30], due to the similar impedance components, as

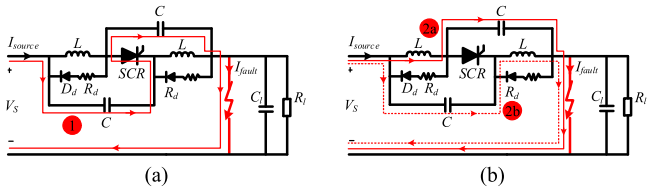

FIG. 11. Parallel-connected Z-source breaker topology; (a) Current path to achieve SCR current zero crossing; (b) LC resonant current paths after SCR current commutates to zero, where the power source current $I_{source} = I_{fault}$.

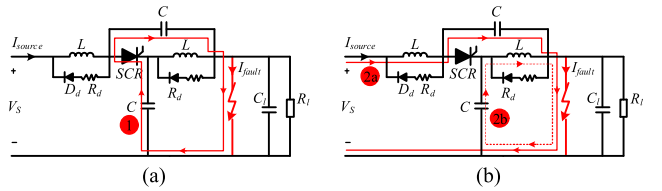

FIG. 12. Series-connected Z-source breaker topology; (a) Current path to achieve SCR current zero crossing; (b) LC resonant current paths after SCR current commutates to zero, where the power source current $I_{source} < I_{fault}$.

shown in Figs. 10–12. The Z-source breaker usually has certain fault current limiting function due to the relatively large inductors (L) adopted in the circuits. When there is a critical short circuit fault, the inductor current is assumed constant for short time period, and the capacitors provide transient current path (red lines as depicted in Figs. 10(a), 11(a) and 12(a)), creating a current zero-crossing in the SCR. The SCR commutates off after current reaches zero and the short circuit fault is isolated from the power source. The commutation of the SCR does not need the OFF command from the control circuits, enabling a fast fault clearance speed.

Based on the locations of the LC resonant circuit, the Z-source breakers can be classified into three categories: crossed Z-source breaker, parallel-connected Z-source breaker and the series connected Z-source breaker [26].

The crossed Z-source breaker (as depicted in Fig. 10), named according to the crossed LC circuit configuration, requires an inductor to be placed in the return path of the power source, which can be seen as a disadvantage in systems needing a common ground connection. The paralleled connected Z-source breaker (as depicted in Fig. 11) is proposed with a common ground connection between the power source and load [27], which is named because the LC circuit is in parallel with the SCR after the SCR is commutated off. One major issue with the paralleled connected Z-source breaker is the large source current reflected from the fault current after the SCR current commutates to zero, as shown in Fig. 11(b). To further improve the circuit, the series connected Z-source breaker (in Fig. 12) is proposed in [26]. The new topology is termed as series connected Z-source breaker because the LC circuit are connected in series with the SCR after it commutates off. The series connected Z-source breaker provides part of the fault current from the capacitors (current path 2b as shown in Fig. 12(b)) instead of all from the power source. Hence, the

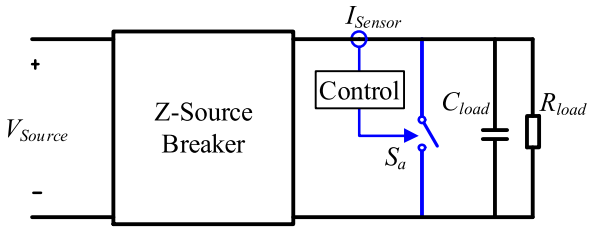

FIG. 13. Method to realize overload fault proction for Z-source breakers by adding a switch S_a to introduce artifical fault.

reflected current to the source during current interruption is greatly reduced. A detailed comparison of the three Z-source breaker topologies are presented in the next section, and some major issues or limitations with the Z-source breakers are also discussed.

B. COMPARISON AND DISCUSSIONS

While the Z-source breakers demonstrate some inherent advantages like autonomously short circuit protection, there are also some limitations with the Z-source breakers.

The first limitation is incompetence of overload protections and high impedance short circuit faults with low di/dt. The crossed Z-Source breaker and the parallel-connected Z-source breaker can only protect the most critical fault with high fault current ramp rates (e.g., the low impedance short circuit fault), which is only a subset of faults in practical power system. Moreover, it is difficult to adjust the tripping current threshold because the fault current rising di/dt also depends on the L and C in the Z-source breaker. Although the series-connected Z-source breaker can protect the overload faults in theory, the overload current tripping level is extremely high (>10 times of the rated current) [26], making the overload protection not so practical and meaningful.

To realize overload protection, an auxiliary switch S_a can be added at the load side, as shown in Fig. 13. The switch S_a could be solid state switches, like thyristors, IGBT, etc. and could also be mechanical contactors or even manual switches for the manual tripping function. To protect the overload current fault, the load current is sensed, and once the load current reaches the pre-set overload tripping level, a signal is sent out to close the switch S_a [26]. Then the Z-source breaker sees an instantaneous high *di/dt* current surge, and autonomously interrupts the fault current. In this way, the Z-source breakers can protect both high di/dt fault like the short circuit fault and the low *di/dt* overcurrent fault.

The second limitation of the abovementioned three types of Z-source breakers is only suitable for unidirectional current conduction. Some topologies [28], [29] are proposed to realize bidirectional current conduction and interruption, however, the components (SCRs, capacitors, inductors) needed are almost doubled, making the circuit a little costly, bulky and complicated.

Another limitation is from the necessity of the output capacitors (C_{load}) in all the three types of Z-source breakers [27]. In

TABLE III. Comparison Between Different Z-Source Breaker Topologies

Features	Z-Source Breaker		
	Crossed	Parallel	Series
Breaker current direction	Unidirectional	Unidirectional	Unidirectional
Common ground	No	Yes	Yes
I_{source} during SCR turn-off	0	I_{fault}	$<I_{fault}$
Z-Source transfer function	Resonator	Notch filter	Low pass filter
Overload protection	No	No	Yes
Output capacitor needed	Yes	Yes	Yes
Isolation from power source	SCR	Series LC	Series LC

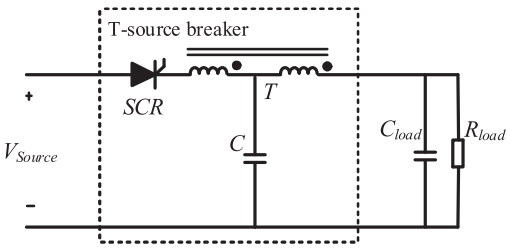

FIG. 14. T-source breaker consisting of a two-winding transformer (*T*) and a capacitor (*C*) formed in a T-shape.

absence of the load capacitors, the load step increase could also introduce a high *di/dt*, and the Z-source breakers could misinterpret load change as a short circuit fault, mistakenly turning off the load current.

Table III compares and summarizes the features of the three types of Z-source breakers in terms of common ground, source current I_{source} needed during the SCR turn-off time, overload protection function, etc. One feature to be mentioned is the way of isolation between the power source and load after the SCR is off. The parallel connected and series connected Z-source breakers always have a LC circuit connected between the source and the load even if the SCR is turned off, which may cause high leakage current and some safety concerns.

To address the limitations and further improve the breaker performances, ongoing efforts are made by researchers [42]–[44]. For example, a T-source breaker is reported in [42], [43], which employs a two-winding coupled transformer and a capacitor in T-shape, as shown in Fig. 14. The T-breaker can also achieve the similar objectives of autonomous fast fault current isolation and simple control with the Z-source breakers. Meanwhile, the detectable fault current level and ramp rate could be adjusted by the transformer's turns ratio in the T-source breaker, and it can also distinguish the load step change and the short-circuit fault.

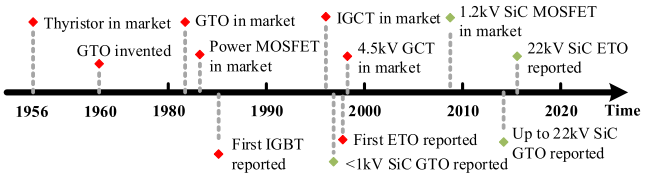

FIG. 15. Thyristors and other key power semiconductor devices development history.

IV. ACTIVE TURN-OFF THYRISTOR BASED SSCBS

Understanding the difficulties and challenges for conventional thyristors (SCRs) to interrupt the current, the ideas come naturally to modify the physical structure of the thyristor to enable its current interruption capability. The modified thyristors (active turn-off thyristors) like Gate Turn Off thyristors (GTO), Gate-Commutated Thyristors (GCT), etc., become fully controlled devices. Fig. 15 summarizes and shows the thyristors and some other key power devices' development progress, which may help readers have a better understanding of the technologies.

The first thyristor devices were released commercially in 1956 by General Electric (GE), as a replacement for the thyratron, a vacuum tube used for power applications [32]. Due to the significant demand for the control of motors in DC power system, the GTO, as a fully controlled device, was invented in 1960s and commercialized in 1980s [31], [32]. The GTOs usually need a dv/dt snubber during turn-off to limit the voltage rising rate, otherwise, the high turn-off voltage and current focus on a small portion of the device, leading to a device failure. Until 20 years ago, the GTO was one of the mainstream devices for high power electronics, but since the late 1990s, they have been replaced by the GCT, due to the bulky turn-off *dv/dt* snubber needed [13]. The Integrated Gate-Commutated Thyristor (IGCT) concept is further developed by integrating the gate unit with the GCT wafer and introduced to the market in 1996 by ABB, characterized by fast and snubberless turn-off and convenient ON/OFF control for users [14], [15]. Similar to the IGCT concept, the GTO based Emitter Turn Off Thyristor (ETO) concept was invented by Dr. Huang in 1998 [33], which can realize the snubberless and unity gain turn-off of the GTO. From early 1990, SiC based power devices like the SiC SBD and MOSFET started to increase in popularity due to the superior material performances such as 10x higher breakdown field and 3x better thermal conductivity compared to Si material [32], [34]. The SiC thyristor like the SiC GTO with less than 1 kV blocking voltage was first reported by Northrop Grumman in 1997 [35], and its blocking voltage was gradually increased in the last two decades and now reaches as high as 22 kV reported by Cree [36]. The ETO concept was also applied to the SiC area, based on the SiC GTO. In 2014, the 15 kV SiC ETO was reported by NCSU and Cree [21], and later in 2015, up to 22 kV SiC ETO was developed and validated in SSCB applications [3].

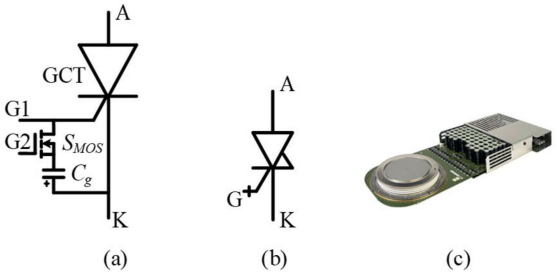

FIG. 16. **(a) Simplified IGCT schematics [32]; (b) IGCT symbol; (c) 2.5 kV reverse-blocking IGCT prototype with integrated gate unit [19].**

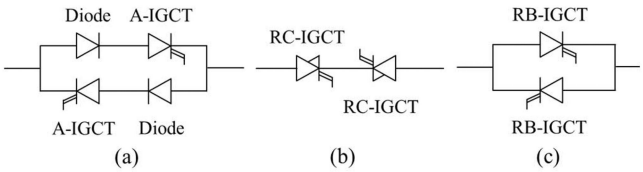

FIG. 17. **The arrangement of different types of IGCTs for bidirectional SSCB. (a) An additional diode connected in series with the A-IGCT to realize reverse voltage blocking and two set of the diode and A-IGCT connected in anti-parallel; (b) Two RC-IGCT connected anti-series; (c) Two RB-IGCT connected in anti-parallel.**

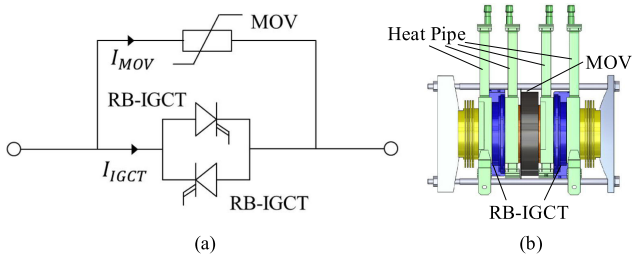

FIG. 18. **(a) Circuit topology of the 91 mm, 2.5 kV RB-IGCT based bidirectional SSCB; (b) Mechanical layout of the assembly of the power stack with two RB-IGCTs and one MOV [37].**

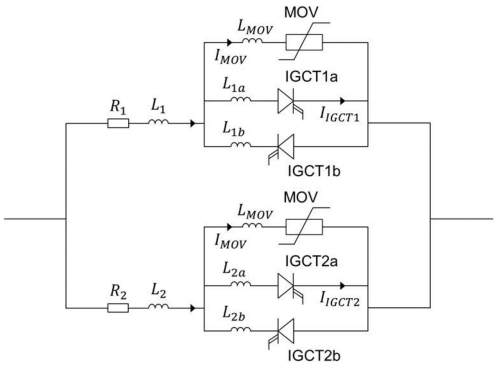

FIG. 19. **High current DC SSCB based on parallel connection of RB-IGCTs [46].**

A. IGCT BASED SSCBS

Since its invention, the IGCT technology has found wide applications in medium voltage drives, wind power conversion, STACOMs, etc., thanks to its low conduction losses and convenient ON/OFF control with the integrated gate unit. Recently, the IGCT devices become an attractive option also for SSCB application with the further optimization of the device structure to drive down the conduction losses. In 2014, ABB developed a new variant of the IGCT. The 2.5 kV reverse blocking IGCT (RB-IGCT) is optimized for low conduction losses rather than switching losses and is also able to block both forward and reverse biased voltages [15].

Fig. 16 shows the simplified asymmetrical IGCT schematics, its symbol and the 2.5 kV RB-IGCT prototype based on 91 mm GCT wafer. A pre-charged capacitor C_g and low voltage MOSFET (S_{MOS}) are applied in the integrated gate driver unit. In the conduction state, S_{MOS} is maintained OFF and to turn-off the IGCT, S_{MOS} is turned on. The current is forced commutated from the cathode of the GCT to the S_{MOS} branch by the pre-charged capacitor, realizing the unit gain turn-off of the GCT.

In the past 10 years, the IGCT technology has experienced continuous optimization and customization to better suit different applications. The asymmetrical IGCT (A-IGCT) can block high voltages in only forward direction and needs a diode in series connection to block the reverse voltage in a bidirectional SSCB (Fig. 17(a)). The reverse conduction IGCT (RC-IGCT), which can only block forward biased voltage, needs to be connected in anti-series with another RC-IGCT (Fig. 17(b)). Instead, the optimized reverse-blocking IGCT (RB-IGCT) [18], [19], [37] can block high voltages in both forward and reverse directions. To realize a bidirectional SSCB, the two RB-IGCTs can be connected in anti-parallel (Fig. 17(c)), enabling a higher efficiency with a single device in the conduction path.

The 2.5 kV RB-IGCT in Fig. 17(c) demonstrates on-state voltage drop as low as 0.9 V at 1 kA, 125 °C and a maximum controllable turn-off current capability up to 6.8 kA at 1.6 kV, 125 °C, making it an attractive switch for high current SSCBs. Based on the 2.5 kV RB-IGCT, a 1 kV, 1 kA bidirectional SSCB prototype was successfully developed as shown in Fig. 18. The experimental results show that the developed SSCB prototype can interrupt 2.6 kA fault current within 200 μs at 1 kV system voltage [37], validating the suitableness of the RB-IGBT technology for the SSCB application.

RB-IGCT have also been proven to be able to be connected in parallel in order to develop SSCBs with high nominal current ratings. Fig. 19 illustrates the circuit topology of a DC SSCB with nominal current ratings up to 5000 A, and short circuit current interruption up to 13.5 kA [46]. Both static and dynamic current sharing between two RB-IGCTs connected in parallel has been experimentally validated and shows acceptable current deviation for the SSCB application.

B. ETO BASED SSCBS

GTO devices add current interruption capability to the thyristor's typical advantages, like low conduction voltage

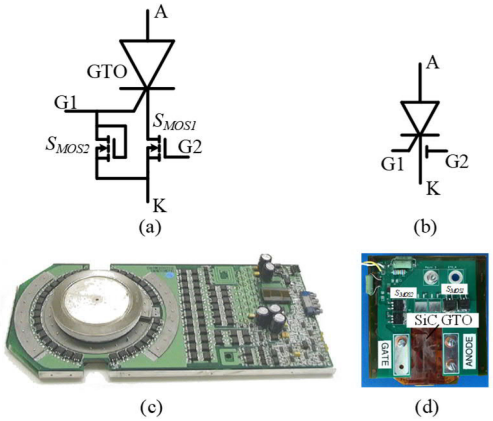

FIG. 20. (a) Simplified ETO schematics; (b) ETO symbol; (c) Picture of the 4.5 kV, 4 kA ETO prototype with integrated gate unit [17]; (d) Picture of the 22 kV SiC ETO prototype based on a p-type SiC GTO device [47].

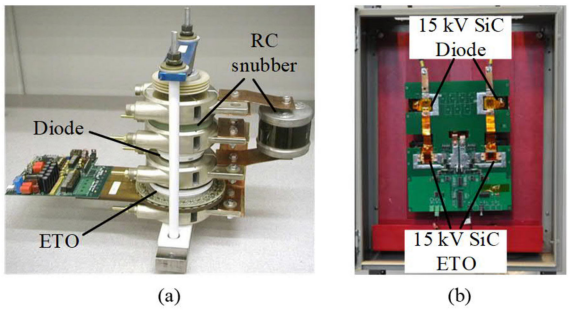

FIG. 21. (a) 4.5 kV, 1.5 kA unidirectional circuit breaker based on 4.5 kV, 4 kA ETO4045TA and A 4.5 kV, 2 kA freewheeling diode 5SDF10H4502 and 1Ω, 1.0 μF RC snubber to limit the dv/dt [20]; (b) A bidirectional SSCB based on two anti-series connected 15 kV SiC ETOs and two 15 kV PiN diodes [21].

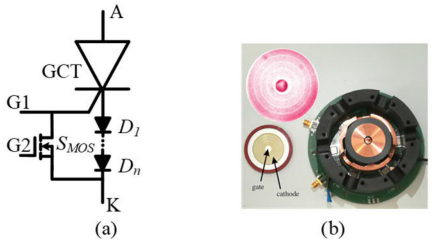

FIG. 22. (a) Simplified schematic of the DAGCT, which have stacked diodes to increase the total voltage drop across the diodes to facilitate the current commutation from the cathode to the gate of the GCT; (b) Picture of the assembled 2.8 kV DAGCT prototype based on 51 mm reverse conducting GCT wafer [23].

drop, high surge-current capability, and bidirectional voltage-blocking capability with symmetrical device structure. However, one drawback of the GTO device is the complicated and slow transient-response gate driver circuit, resulting in a very long turn-off time. Besides IGCT technology, the ETO technology is another major effort made to overcome this drawback and improve the GTO concept.

As shown in Fig. 20(a), the ETO technology is developed from mature GTO and power-MOSFET technologies, and combines the advantages of both, in particular, GTOs' high voltage/current ratings and low forward-voltage drop, and power-MOSFET's simple interface for gate driving, similar to IGBT's. In addition, ETOs also exhibit wide reverse-biased safe operation area (RBSOA), and relatively high switching speed, making them good candidates for SSCBs.

The ETO is in conduction state when the MOSFET S_{MOS1} and the GTO are in on state. To turn off the ETO, the turn-on gate signal for the GTO and S_{MOS1} are removed and S_{MOS2} is turned on simultaneously. The rising voltage across the drain and source terminal of S_{MOS1} forces the current commutate from the GTO cathode to the gate, extracting the charge carriers out from the gate PN junction of the GTO, which prompts the turn-off of the GTO.

Fig. 20(b) shows the symbol of ETO device, and Fig. 20(c) shows the picture of a 4.5 kV, 4 kA ETO prototype with integrated gate unit [17]. Fig. 20(d) shows a world-record 22 kV SiC ETO prototype which is developed based on a 2 cm^2 chip size p-type SiC GTO device [47]. Applying the ETO concept to the SiC, the SiC ETO presents a unique opportunity for MV SSCB applications: the ultra-high blocking voltages, large RBSOA, and potential for high-temperature operation.

Fig. 21(a) is the picture of a unidirectional 1.5 kA DC SSCB prototype based on the 4.5 kV, 4 kA ETO4045TA [20]. A 4.5 kV, 2 kA freewheeling diode 5SDF10H4502 [48] is paralleled with the ETO to provide the reverse conduction path. A 1 Ω and 1 μF RC snubber is applied to improve the reliability and increase the ETO current turn-off capability. Fig. 21(b) shows the picture of a bidirectional SSCB based on two anti-series connected 15 kV SiC ETOs and two 15 kV PiN diodes. Thanks to the SiC devices' high blocking voltage capability, no devices series connection is needed to reach ~7 kV operation voltage, which greatly simplified the circuit and increases the power density as well as the circuit reliability.

C. DAGCT BASED SSCBS

The diode-assisted gate commutated thyristor (DAGCT) concept was proposed by Dr. Rik W. De Doncker [23], [24], which is similar to the IGCT, by replacing the pre-charged capacitor bank in the IGCT with multiple diodes connected in series forming a diode-stack in the GCT cathode terminal, as shown in Fig. 22(a). During the turn-off process, the S_{MOS} is turned on, and the current is forced commutated from GCT cathode to the S_{MOS} branch by the forward voltage of the diode-stack. Compared to IGCT concept, there is no need for an extra voltage source in the DAGCT to charge the capacitor bank.

To facilitate the fast and successful current commutation in the DAGCT, there are two key design parameters according to (1): i) Small parasitic loop inductances (L_s) between the gate, cathode of the GCT and the S_{MOS}, D_1~D_n circuit loop. Smaller loop inductances L_s leads to fast current commutation (higher di/dt) from the cathode to the gate of the GCT. To

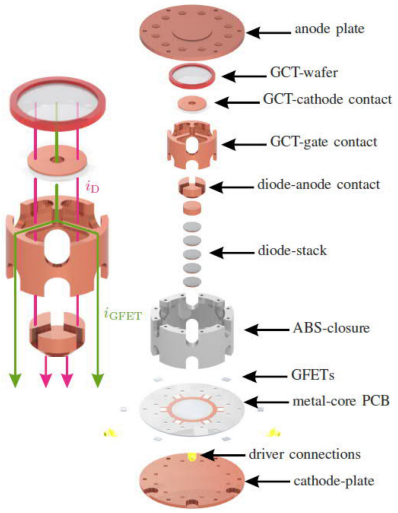

FIG. 23. **DAGCT press-pack package design. A metal-core PCB is used in the package to minimize the thermal resistance. Moreover, the metal core is used to conduct current in the package and is connected to the cathode potential. This reduces the package size and decreases the stray inductance. Only the MOSFETs at the gate terminal (GFETs in the pictures) are soldered on the PCB. All other electrical and mechanical components are connected by means of mechanical pressure [23].**

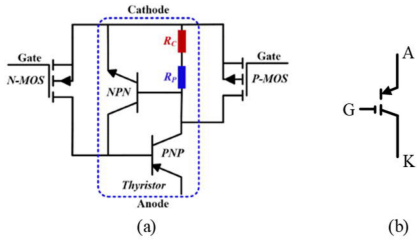

FIG. 24. **(a) Equivalent circuit of MCT [21]; (b) Symbol of MCT.**

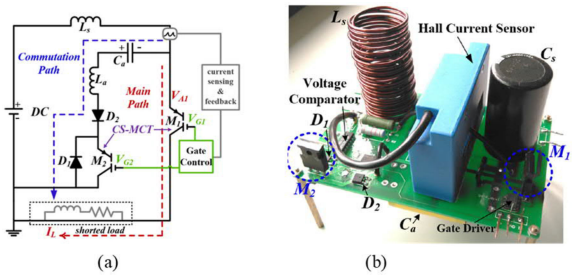

FIG. 25. **(a) Schematics of the MCT based SSCB, where C_a is pre-charged capacitor similar to the one in forced commutation thyristor to assist the MCT turn-off; (b) Picture of the 400 V MCT based SSCB prototype [22].**

realize a small loop inductance, a press-pack package design as shown in Fig. 23 are adopted. ii) Sufficient forward voltage drops (V_{D1}~V_{Dn}) across the stacked diode. One way to increase the total voltage drops across the stacked diodes is to increase the number of diodes in series. However, larger number of diodes in series leads to complicated package assembly and could increase the loop inductance, which could harm the current commutation. To address this issue, rectifier diodes with high blocking voltage and consequently high forward voltage are selected. Here some tradeoff needs to be considered: the high forward voltage drop also causes high conduction losses and high thermal stress in the device.

$$-L_s\frac{di_D}{dt} = V_{D1} + \ldots + V_{Dn} + V_{GK} - V_{MOS} \qquad (1)$$

Fig. 22(b) show the picture of the 2.8 kV DAGCT prototype which is developed based on a 51 mm reverse conducting GCT wafer, successfully demonstrated 550 A current interruption test.

At 550 A conduction current, the diode-stack contributes to ~ 65% conduction losses of the DAGCT, with ~ 4.1 V forward voltage drop [23]. However, to achieve higher interruption current, higher diode forward voltage drop is required. The DAGCT seems an interesting option for MVDC circuit breaker application, but the high conduction losses are a significant drawback and needs to be addressed carefully. It could find a better application in hybrid circuit breakers, working as the solid state current interruption device, which does not require long conduction time.

D. MOS-CONTROLLED THYRISTOR (MCT) BASED SSCBS

The MOS-controlled thyristor (MCT), invented by V.A.K. Temple in 1984 [38], was another type of fully controllable thyristor device, which is similar to GTO in operation, but has voltage controlled insulated gates like IGBTs. Two MOSFETs of opposite conductivity types are integrated with the thyristor on the same chip in MCT as shown in Fig. 24(a). One MOSFET (N-MOS) is responsible for turn-on and the other (P-MOS) is for turn-off.

Fig. 25(a) shows the schematic of a SSCB developed based on the MCT, which has two current paths: the main path for normal current conduction and the commutation path for current interruption. The commutation path has a pre-charge capacitor C_a same with the one in forced commutation thyristor to assist the MCT turn-off, due to the limited current turn-off capability of the MCT under hard switching condition [22]. After the fault current commutates from the main path (M_1) to the commutation path (M_2), it will decrease to zero in sequent resonant process. Fig. 25(b) show the picture of the 400 V MCT based SSCB, experimentally verified at 100 A interruption current.

V. DISCUSSION

Table IV shows a comparison of a few selected thyristor based SSCBs with experimental validation. In this table, the polarity (unidirectional vs. bidirectional), nominal voltage and current are listed. The experimentally tested maximum turn-off current, and the current turn-off/interruption time of the semiconductor switches and the SSCBs are also compared.

TABLE IV. Comparison of Selected Thyristor Based SSCBs in Literature with Experimental Validation

Current Turn-off Technique	Thyristor Type	Polarity	Nominal Voltage	Nominal Current	Max turn-off Current Tested	Semiconductor Current Turn-off time	SSCB Current Interruption time
Forced commutation thyristor	SCR [10][49]	Unidirectional	380 V	13 A	160 A	<280 µs	N/A
	SCR [9]	Bidirectional	7000 V	N/A	2000 A*	N/A	2 ms
Z-source Breaker	SCR [25][26]	Unidirectional	120 V	3 A	5.25 A	<200 µs	1~3 ms
	SCR [28]	Bidirectional	120 V	3 A	3 A	<300 µs	N/A
T-source Breaker	SCR [42]	Unidirectional	15 V	0.5 A	0.5 A	N/A	15 ms
	SCR [50][51]	Bidirectional	300 V	10 A	10 A	N/A	2 ms
Active turn-off Thyristor	Si ETO [20]	Unidirectional	2500 V	1500 A	750 A	<15 µs	N/A
	SiC ETO [21][52]	Unidirectional	4500 V	200 A	200 A	2.5 µs	N/A
	RB-IGCT [53][54]	Bidirectional	1000 V	5000 A**	13500 A**	<10 µs	0.5 ms
	DAGCT [23]	Unidirectional	N/A	N/A	550 A	<4 µs	N/A
	CS-MCT [22][55]	Unidirectional	600 V	25 A	100 A	<10 µs	0.5 ms

*Simulation based study only
**2 RB-IGCTs in parallel

The forced commutation thyristor based SSCBs have the advantages of low conduction losses, high surge current capability and easiness to realize bidirectional voltage blocking. One drawback of the forced commutation SCR based SSCBs (including the Z-source and the T-source breakers) is the relatively long fault current interruption time (a few milliseconds), as shown in Table IV. The reasons for the long current interruption include: 1) SCR's slow turn-off due to the reverse recovery process, usually 200 μs to 500 μs long, depending on the SCR's structure and voltage/current level. During the reverse recovery time, the minority carriers inside the SCR recombine to be able to block the forward voltage again; 2) after the SCR is turned off, the current is still conducting in the auxiliary LC circuit, which may take a few more milliseconds to drop to zero. The long fault current interruption time also leads to a high peak fault current level. Because of that, the forced commutation SCR based SSCBs are more suitable for low fault current rising di/dt (large system parasitic inductance) power systems or ac power system protection, which usually has limited fault current rising rate.

Moreover, the forced commutation thyristor based SSCBs (including the Z-source and the T-source breakers) are experimentally validated only at relatively low current and voltage levels (tens of amperes and hundreds of volts), which do not match with the high voltage and current handling capability of the available SCRs. One possible reason could be the relatively bulky and complicate auxiliary circuits (capacitors in forced commutation thyristor or LC resonant circuits in Z-source breakers), especially for high current and high voltage interruption.

The Z-source breakers not only have the advantages of SCR based SSCBs (e.g., low conduction losses), but also some unique features like autonomously short circuit protection and fast critical short circuit fault response speed. Meanwhile, limitations, like incompetence of overload protection, necessity of the output capacitors, etc., still need a lot of efforts to address and further improve the topologies.

Thanks to the semiconductor switch's fast current turn-off speed (usually a few microseconds), active turn-off thyristor based SSCBs demonstrate fast fault current interruption speed, which usually takes less than 1 ms, even including the residual energy dissipation time by the MOV or other energy absorbing components, as shown in Table IV.

Both the Si ETOs and RB-IGCTs demonstrate high turn-off current capability (thousands Amperes), especially RB-IGCT based SSCBs successfully interrupted a current as high as 13.5 kA. The reverse blocking characteristics of the RB-IGCT make it very suitable for bidirectional SSCBs by avoiding the two devices anti-series connection, which reduce the SSCB's conduction losses. The possible issue with the RB-IGCT may be the limited available voltage and current options, which may restrain their widespread implementation in various voltage and power levels.

The SiC ETO based SSCB shows a high operational voltage (4.5 kV), thanks to their intrinsic high blocking voltage capability (15 kV, and up to 22 kV reported). The high blocking voltage of SiC ETO could significantly simplify the SSCB's circuit design by reducing the number of power devices needed for series connection, promising great potentials in MV power system protection. One drawback of the SiC ETO is the relatively high conduction voltage drops (>3 V) even at low current levels, due to the intrinsic higher SiC PN junction voltage drop. This could lead to large power losses in SSCBs. To dissipate the conduction power losses, carefully

TABLE V. Summary of the Pros and Cons of Thyristor Based SSCBs

	Pros	Cons
Forced commutation thyristor based SSCB	+ Low conduction losses + High surge current capability + Bidirectional blocking voltage capability	− Large capacitors needed for high current and high voltage interruption − Relatively long (a few milliseconds) fault current interruption time − High peak fault current level
Z-source Breaker	+ Low conduction losses + Autonomous short circuit protection + Fast short circuit fault response speed	− Large auxiliary LC circuits needed for current interruption − Relatively long (a few milliseconds) fault current interruption time − Not suitable for protection against overload and low di/dt faults
Si ETO based SSCB	+ Simple ON/OFF gate control of the ETO + Low conduction losses + Fast current interruption speed	− Si ETO still in academic research stage
SiC ETO based SSCB	+ High blocking voltage capability + Simple ON/OFF gate control of the ETO + Fast current interruption speed	− Relatively high conduction losses − SiC ETO still in early academic research stage
RB-IGCT based SSCB	+ Low conduction losses + Bidirectional blocking voltage capability + Fast current interruption speed + High technology readiness level	− Limited RB-IGCT voltage/current options available
DAGCT based SSCB	+ Simple ON/OFF gate control of the DAGCT + Fast current interruption speed	− Relatively high conduction losses − DAGCT still in academic research stage
MCT based SSCB	+ Low conduction losses + Simple ON/OFF gate control of the MCT	− Auxiliary LC circuits needed for high current interruption − Relatively long fault current interruption time − Only low current level MCT available

designed cooling systems are needed. Moreover, the ETO, especially the SiC ETO are still in early academic research stage, and there are no commercial devices available.

The DAGCT has the advantages of easy ON/OFF control through gate signals and fast current interruption speed. As shown in Table IV, Ref [23] developed a 2.8 kV DAGCT prototype which successfully demonstrated 550 A current interruption within 4 μs. However, to interrupt higher current, higher diode forward voltage drop is required to force the current to commutate from the GCT cathode to the gate. The high diode forward voltage drop causes high losses during nominal current conduction in the SSCBs, which may require large cooling system to dissipate the heat.

The MCTs have the advantage of low conduction losses and simple ON/OFF control of the device. However, the MCT based SSCB is experimentally validated at relatively low current level (tens of amperes). Although the MCT could actively interrupt the current, its maximum interruption current is not only a function of internal parameters, but also depends on external supply voltage [22], [39], which indicates not feasible to achieve snubberless operations. In addition, the unavailability of MCT devices [39] in the market also limits the application of this concept.

To help readers have a better understanding and select the right type of thyristor based SSCBs, Table V. provides a comprehensive comparison and full summary of their strengths and weaknesses.

VI. CONCLUSION

The mature and cost-effective thyristor technologies exhibit some beneficial features: low conduction losses, high surge current capability, bidirectional voltage blocking possibility, etc. All these features make them a very attractive candidate for SSCB application. This paper reviews and studies the SSCBs based on the conventional or active turn-off thyristors. The performance comparison and the design challenges of SSCBs with different thyristor technologies are also presented and summarized in the paper.

By comparison, the RB-IGCT is today's most promising solution for high power SSCBs, thanks to the advantages of low conduction losses, fast current interruption speed, reverse voltage blocking characteristics and easy implementation. SiC ETOs are also interesting with the high voltage blocking capability, in particular for MVDC applications, but the device is still in early academic research stage and there is no information about its release on the market.

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