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An Interleaved Quadratic High Step-Up DC-DC Converter With Coupled Inductor

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ABSTRACT A new high step-up DC-DC converter for renewable energy applications is proposed in this paper. Employing an interleaved quadratic structure, two two-winding coupled inductors (CIs), and voltage multiplier cells (VMCs), the proposed converter can provide high-voltage gains, continuous input current with low ripple, reduced voltage stresses on semiconductors, common ground between input and output sides, and low numbers of components. In addition, diode-capacitor lossless clamp circuits are utilized to limit the voltage stresses of the power switches and further extend the voltage gain. The operating and steady-state analyses, design considerations, and a comparison with other previously published high step-up converters are presented. Lastly, experimental results of a 400 W prototype with 400 V output voltage are illustrated to verify the theoretical analysis and the functionality of the proposed converter.

INDEX TERMS Interleaved DC-DC converter, quadratic DC-DC converter, high step-up, renewable energy, photovoltaic (PV), fuel cell (FC), coupled inductor (CI), voltage multiplier cell (VMC).

I. INTRODUCTION

IN recent decades, renewable energy sources (RESs), such as solar photovoltaic (PV) panel and fuel cell (FC), were the focal points for electricity production because they do not deplete finite fossil fuel resources and are non-polluting. However, the RESs generate a low voltage ranging from 12 to 48 V [1]; thus, they require a high step-up DC-DC converter, which provides high-voltage gains [2], [3]. Fig. 1 shows how a high step-up DC-DC converter interfaces a low-voltage RES to a high-voltage DC bus (200-800 V) in a DC micro-grid. Boosting the output voltage of RESs to the voltage of DC bus can be a challenge because at high-voltage gains, conventional boost converter suffers from extreme duty cycle, high voltage stresses on the switches, and diode reverse-recovery problems [3], [4]. Thus, the development of high step-up DC-DC converters to provide high output voltages from the low voltage of RESs is an essential step toward the integration of RESs into DC micro-grids. To this point, literature presented techniques to derive high step-up topologies [5].

In general, high step-up converters are based on classical DC-DC topologies in which voltage-boosting techniques are applied to increase the voltage gain under low or medium duty cycles, reduce the voltage and current stresses on components, and achieve high efficiency [6]. Voltage-boosting techniques are based on voltage multiplier cell (VMC)—including switched inductor (SL) and switched capacitor (SC)—multilevel, cascade, quadratic, interleaved structures, coupled inductor (CI), and built-in transformer (BIT), in addition to combinations of the aforementioned. The SC technique was applied to converters in [7]–[9]—the main drawback of these converters was that they suffered from high surge current in the capacitors and increased conduction losses. The SL technique was adopted to obtain high-voltage gain in converters proposed in [10], [11]. The converters in [12]–[14] combined the interleaved and BIT techniques to further increase the voltage gain. For converters in [15]–[18], the voltage gain had quadratic dependency on the duty cycle, resulting in large gains. The CI technique was integrated with the quadratic converters in [19]–[23]. Using either CI or BIT, there were two degrees of freedom to adjust the voltage gains: one is the duty cycle of the power switch; another is the turn-ratio of the CI or BIT. Accordingly, the design of such converters is more flexible. Additionally, in the converters adopting the CI or BIT, a clamped circuit is required to dissipate the

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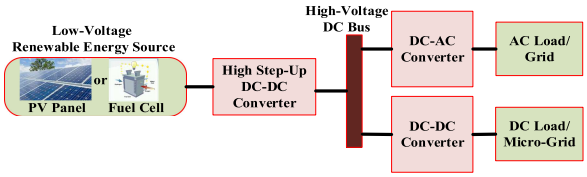

FIGURE 1. High step-up DC-DC converter in a DC micro-grid.

energy of the leakage inductance. Furthermore, the leakage inductance energy is effectively recycled to further extend the voltage gain in the high step-up converters. A clamped circuit can be either active or passive; in comparison with an active clamped circuit, the passive clamped circuit is lossless and simple without impacting the control system. Thereby, the passive lossless clamped circuit was widely employed in the high step-up converters, with either BIT or CI, to recycle the energy stored in the leakage inductance [23]. The combination of CI and interleaved techniques were adopted in the high step-up converters in [24]–[31]. Thanks to the interleaved structure, the input current ripple was reduced, which helped to increase the lifetime of RESs. In addition, an interleaved structure is useful for high-power applications because the current stresses on the components are decreased significantly compared to the non-interleaved topologies. Converters in [32]–[34] had interleaved structure with quadratic voltage gain, while the converter proposed in [35] combined the CI, interleaved, and quadratic techniques to extend the voltage gain significantly. To summarize, all high step-up converters have VMCs composed of capacitors and diodes, along with other voltage boosting techniques.

In this paper, a new DC-DC converter is proposed to boost the voltage of the RESs. The proposed converter incorporates the interleaved, quadratic, CI, and VMC techniques to reach a high voltage gain with low voltage stresses on the semiconductor devices; thus, switches with low voltage-rating and low ON-state resistance, which reduce the conduction losses and costs, are selected. The voltage gain of the proposed converter depends on the duty cycle and turns-ratio of CI, which helps to avoid operating at extreme duty cycle to achieve a high voltage gain; the two degrees of freedom—duty cycle and turns-ratio—make the converter design more flexible. Lossless clamped circuits are used to absorb the energy of the CIs' leakage inductances, limit the voltage stress on the power switches, and further extend the voltage gain. In addition, the proposed converter has continuous input current with low ripple and low current stresses on the switches and CIs due to the use of interleaved structure, and the proposed converter has a simple structure with a common ground between the input source and output load and a low number of components. The low input current ripple of the proposed converter prolongs the lifetime of the input RES.

This paper is organized as follows: the circuit configuration of the proposed converter and its operating analysis are presented in Section II. The steady-state circuit performance

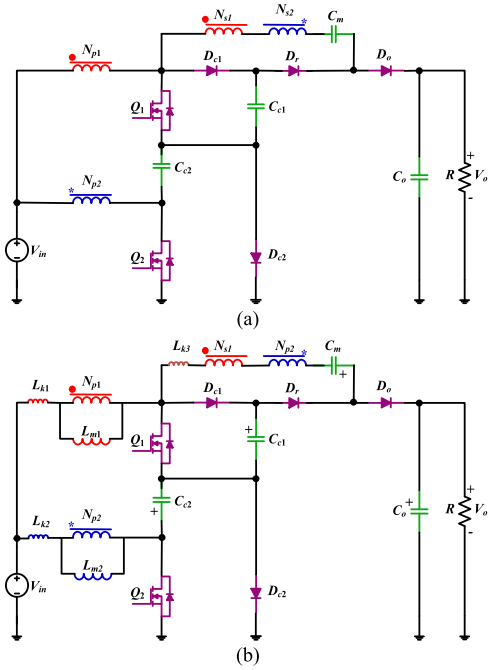

FIGURE 2. Proposed converter and its equivalent circuit: (a) proposed converter, (b) equivalent circuit.

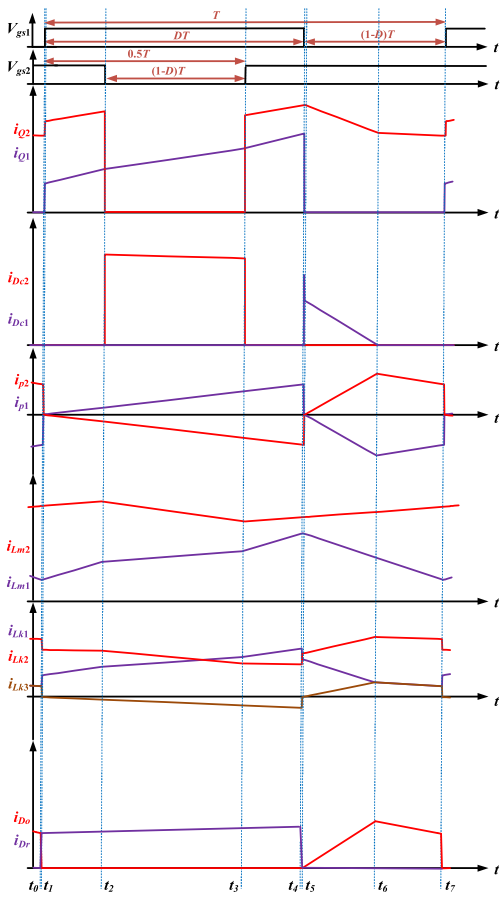

FIGURE 3. Key waveforms of the proposed converter.

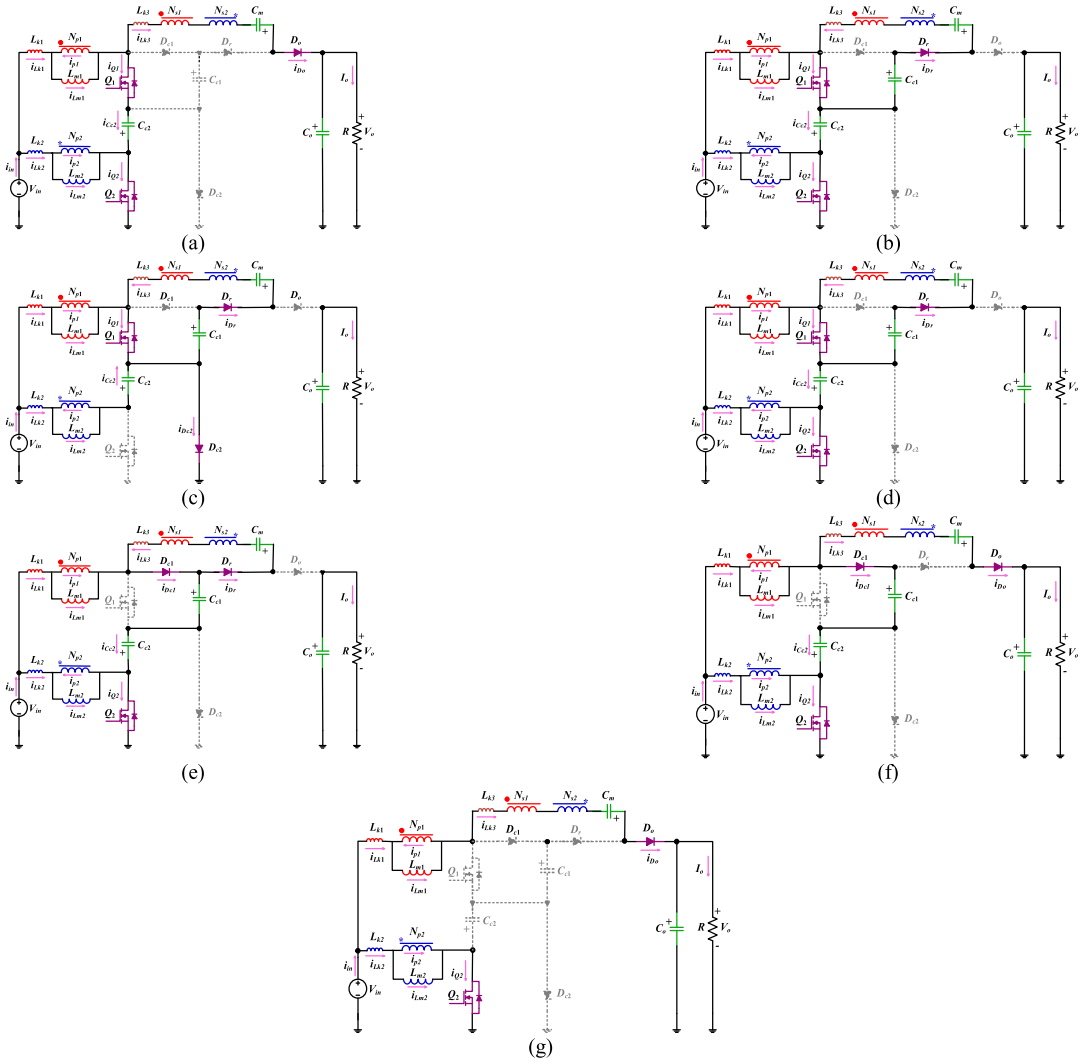

FIGURE 4. Operation stages in one switching period: (a) Stage 1 [t_0-t_1]; (b) Stage 2 [t_1-t_2]; (c) Stage 3 [t_2-t_3]; (d) Stage 4 [t_3-t_4]; (e) Stage 5 [t_4-t_5]; (f) Stage 6 [t_5-t_6]; (g) Stage 7 [t_6-t_7].

analysis is illustrated in Section III. The design guidelines of the proposed converter are explained in Section IV. A comprehensive comparison with other similar topologies is given in Section V. Experimental verification of the proposed converter is outlined in Section VI, and finally, the study is concluded in Section VII.

II. CONFIGURATION AND OPERATING ANALYSIS OF THE PROPOSED CONVERTER

A. CONFIGURATION OF THE PROPOSED CONVERTER

Fig. 2 shows the configuration of the proposed converter and its equivalent circuit. Switches Q_1 and Q_2 are commanded in an interleaved manner with the phase shift of 180°; that is, the proposed converter has a two-phase interleaved structure. There is a CI in each phase. The CIs have primary turns of N_{p1} and N_{p2} and secondary turns of N_{s1} and N_{s2}. Each CI is modeled with an ideal transformer, a magnetizing inductance placed in the primary side, and leakage inductances placed on the primary and secondary sides. The coupling references of the CIs are represented by "•" and "∗". Parameters L_{m1} and L_{m2} denote the magnetizing inductances for the couple inductors; L_{k1} and L_{k2} represent the primary leakage inductances; L_{k3} denotes the summation leakage inductance of two CIs in the secondary sides. The secondary windings of the CIs are connected in series with the leakage inductance L_{k3} and an intermediate energy storage capacitor C_m to extend the voltage gain of the proposed converter. The diode-capacitor pairs (D_{c1}, C_{c1}) and (D_{c2}, C_{c2}) provide the clamp circuits for the power switches to recycle the leakage energy caused by the leakage inductances. Diode D_r is the regenerative diode; the output diode and capacitor are D_o and C_o, respectively; V_{in} and V_o are the input and output voltages, respectively; R is the load; $N_1 = N_{s1}/N_{p1}$ and $N_2 = N_{s2}/N_{p2}$ are the turns-ratios of the CIs.

B. OPERATING ANALYSIS OF THE PROPOSED CONVERTER

Two gate signals with the same frequencies f_{sw} and the same duty cycles D are applied to the power switches, where there

is a phase shift of 180° between the gate signals. Using the steady-state analysis, 7 operation stages exist during one switching period T. Fig. 3 illustrates the key current waveforms of the proposed converter. The equivalent circuits for the different operation stages are shown in Fig. 4, which are:

Stage 1 [$t_0 \sim t_1$]: During this stage, both switches Q_1 and Q_2 and output diode D_o are in ON state; other diodes are reverse-biased; both CIs are energized, and their secondary windings and intermediate capacitor C_m release the energy to output capacitor C_o and load R. The key circuit relationships of this stage are as (1). The current of D_o decreases during this stage. Ignoring the current ripples of magnetizing inductances of the CIs, the output diode's current variation rate (di_{Do}/dt) is obtained; as obvious, the output diode's current-falling rate is controlled by the leakage inductances.

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -N_1 V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k3}} = V_o + V_{C_{c2}} - V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = i_{D_o}(t) \\ V_{L_{kj}} = L_{kj} \frac{di_{L_j}}{dt} \quad (for\ j = 1,\ 2,\ 3) \\ \frac{di_{D_o}(t)}{dt} = -\frac{V_o + (N_1 - N_2)V_{in} + (N_1 - 1)V_{C_{c2}} - V_{C_m}}{N_1^2 L_{k1} + N_2^2 L_{k2} + L_{k3}} \end{cases} \tag{1}$$

Stage 2 [$t_1 \sim t_2$]: At $t = t_1$, regenerative diode D_r turns on and output diode D_o turns off; both switches Q_1 and Q_2 remain in ON states, resulting in linear increases of the current for magnetizing inductances L_{m1} and L_{m2}; capacitor C_m begins to charge, and the primary winding's current direction is reversed for both CIs; the energy to the load is provided by output capacitor C_o. For this stage, the key relationships as (2).

Stage 3 [$t_2 \sim t_3$]: At $t = t_2$, switch Q_2 turns off and clamp diode D_{c2} is forward-biased; accordingly, the voltage across switch Q_2 is clamped to the V_{Cc2}. The relationships for this stage are as (3).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \end{cases} \tag{2}$$

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c2}}(t) = i_{L_{k1}}(t) + i_{L_{k2}}(t) - i_{L_{k3}}(t) - i_{D_r}(t) \\ \qquad = i_{L_{m1}}(t) + i_{L_{m2}}(t) + (N_1 - N_2) i_{D_r}(t) \end{cases} \tag{3}$$

Stage 4 [$t_3 \sim t_4$]: At the beginning of this operation stage, switch Q_2 turns on and clamp diode D_{c2} turns off, resulting in the relationships as (4).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} - V_{C_{c2}} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c2}}(t) = i_{L_{k1}}(t) + i_{L_{k2}}(t) - i_{L_{k3}}(t) - i_{D_r}(t) \\ \qquad = i_{L_{m1}}(t) + i_{L_{m2}}(t) + (N_1 - N_2) i_{D_r}(t) \end{cases} \tag{4}$$

Stage 5 [$t_4 \sim t_5$]: This stage begins when switch Q_1 turns off clamp diode D_{c1} turns on at $t = t_4$; thus, the voltage of switch Q_1 is clamped to V_{Cc1}. The current of D_r starts to decrease linearly in this stage, and the relationships are yielded as (5).

Stage 6 [$t_5 \sim t_6$]: At $t = t_5$, the regenerative diode D_r turns off; simultaneously, output diode D_o turns on and its current increases linearly, while the current of clamp diode D_{c1} decreases linearly. The power of the load and output capacitor C_o is provided by the input source through the secondary windings of the CIs and intermediate capacitor C_m. The relationships of this stages are as (6).

Stage 7 [$t_6 \sim t_7$]: At $t = t_6$, the current through clamp diode D_{c1} decreases to zero, and it turns off. The current of output diode D_o starts to decrease, and its decreasing rate is controlled by the leakage inductances. Like previous stage, the input energy is continuously transferred to output capacitor C_o and the load R. The relationships of this stage are as (7).

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ N_1 V_{L_{m1}} - N_2 V_{L_{m2}} + V_{L_{k3}} = V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) + N_1 i_{D_r}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) - N_2 i_{D_r}(t) \\ i_{L_{k3}}(t) = -i_{D_r}(t) \\ i_{D_{c1}}(t) = i_{L_{k1}}(t) - i_{L_{k3}}(t) = i_{L_{m1}}(t) + (N_1 + 1) i_{D_r}(t) \end{cases} \tag{5}$$

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -N_1 V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k3}} = V_o + V_{C_{c2}} - V_{C_m} - V_{C_{c1}} \\ i_{L_{k1}}(t) = i_{L_{m1}}(t) + i_{p1}(t) = i_{L_{m1}}(t) - N_1 i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \\ i_{L_{k3}}(t) = i_{D_o}(t) \\ i_{D_{c1}}(t) = i_{L_{k1}}(t) - i_{L_{k3}}(t) = i_{L_{m1}}(t) - (N_1 + 1) i_{D_o}(t) \end{cases} \tag{6}$$

$$\begin{cases} V_{L_{m1}} + V_{L_{k1}} = V_{in} + V_{C_{c2}} - V_{C_{c1}} \\ V_{L_{m2}} + V_{L_{k2}} = V_{in} \\ -(N_1 + 1)V_{L_{m1}} + N_2 V_{L_{m2}} - V_{L_{k1}} - V_{L_{k3}} = V_o - V_{in} - V_{C_m} \\ i_{L_{k1}}(t) = i_{L_{k3}}(t) = i_{D_o}(t);\ \ i_{L_{m1}}(t) = (N_1 + 1)\, i_{D_o}(t) \\ i_{L_{k2}}(t) = i_{L_{m2}}(t) + i_{p2}(t) = i_{L_{m2}}(t) + N_2 i_{D_o}(t) \end{cases} \tag{7}$$

III. STEADY-STATE CIRCUIT PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

To simplify the steady-state analysis of the proposed converter, the following assumptions are made:

1. The equivalent series resistance (ESR) of all passive components is neglected.
2. The voltages of all capacitors are constant throughout the whole switching period because they are assumed to be large enough.
3. The voltage drops and internal resistances of all semiconductor devices are ignored.
4. The turns-ratios of both the CIs are equal to N; that is $N_1 = N_2 = N$.
5. Stages 1 and 5 are neglected because they are transitional modes with very short times.
6. The converter operates in continuous conduction mode (CCM).

A. VOLTAGE GAIN DERIVATION

By ignoring the voltage drops on the leakage inductances and applying the volt–second balance principle to the magnetizing inductances L_{m1} and L_{m2}, the voltages across capacitors C_{c1} and C_{c2} are:

$$\begin{cases} V_{C_{c1}} = \frac{1}{(1-D)^2} V_{in} \\ V_{C_{c2}} = \frac{1}{1-D} V_{in} \end{cases} \tag{8}$$

Having the voltages of the clamp capacitors, from Stage 2, the voltage of C_m is given by:

$$V_{C_m} = V_{C_{c1}} + N V_{C_{c2}} = \frac{(1-D)N + 1}{(1-D)^2} V_{in} \tag{9}$$

From Stage 6, the voltage of C_o and the voltage gain (M) of the converter can be given by:

$$\begin{cases} V_{C_o} = V_o = V_{C_m} + (N+1)(V_{C_{c1}} - V_{C_{c2}}) = \frac{1+N+D}{(1-D)^2} V_{in} \\ M = \frac{V_o}{V_{in}} = \frac{1+N+D}{(1-D)^2} \end{cases} \tag{10}$$

Fig. 5 shows the plot of the voltage gain of the proposed converter. It is clear that when either duty cycle or turns-ratio increases, the voltage gain increases. Additionally, the voltage gain has a quadratic dependency on the duty cycle, providing a large gain.

In what follows, considering the leakage inductances of CIs, the voltage gain is obtained.

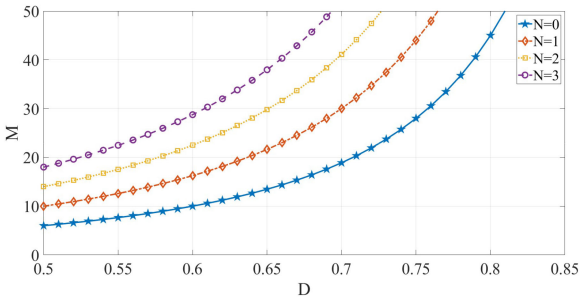

FIGURE 5. The voltage gain of the proposed converter versus turns-ratio N and duty cycle D.

Neglecting transitional Stage 5 and considering Stage 6, the following voltage relationship is obtained:

$$\begin{cases} V_o = (1+N)V_{C_{c1}} - (1+N)V_{C_{c2}} \\ \quad + V_{C_m} + N V_{L_{k1}} - N V_{L_{k2}} - V_{L_{k3}} \end{cases} \tag{11}$$

Ignoring the current ripples of the CIs' magnetizing inductances and voltage ripples of capacitors, (12) can be written.

$$\begin{cases} \Delta i_{D_o} = I_{D_{o\_\max}} = \frac{(N+2)I_o}{(N+1)(1-D)} = \frac{(N+2)V_o}{(N+1)(1-D)R} \\ V_{L_{k1}} = L_{k1}\frac{di_{L_{k1}}}{dt} = L_{k1}\frac{d(i_{Lm} - N i_{D_o})}{dt} = -N L_{k1}\frac{\Delta i_{D_o}}{\Delta t} \\ \quad = -N L_{k1}\frac{I_{D_o,\max}}{kT} = -\frac{N(N+2)f_{sw}L_{k1}V_o}{k(N+1)(1-D)R} \\ V_{L_{k2}} = L_{k2}\frac{di_{L_{k2}}}{dt} = L_{k2}\frac{d(i_{Lm} + N i_{D_o})}{dt} = N L_{k2}\frac{\Delta i_{D_o}}{\Delta t} \\ \quad = N L_{k2}\frac{I_{D_o,\max}}{kT} = \frac{N(N+2)f_{sw}L_{k2}V_o}{k(N+1)(1-D)R} \\ V_{L_{k3}} = L_{k3}\frac{di_{L_{k3}}}{dt} = L_{k3}\frac{di_{D_o}}{dt} = L_{k3}\frac{\Delta i_{D_o}}{\Delta t} \\ \quad = L_{k3}\frac{I_{D_o,\max}}{kT} = \frac{(N+2)f_{sw}L_{k3}V_o}{k(N+1)(1-D)R} \end{cases} \tag{12}$$

where kT is the time duration of Stage 6. Substituting (8), (9), and (12) in (11), in the presence of leakage inductances, the voltage gain is derived as:

$$M = \frac{V_o}{V_{in}} = \frac{1+N+D}{(1-D)^2 + \frac{f_{sw}(N+2)(1-D)\left(N^2(L_{k1}+L_{k2})+L_{k3}\right)}{k(N+1)R}} \tag{13}$$

It is observed that the leakage inductances of the circuit lead to a slight decrease in the voltage gain; thus, the higher the leakage inductances, the lower the voltage gain.

B. VOLTAGE STRESS ON SEMICONDUCTOR DEVICES

The maximum voltage stresses of the semiconductor devices are obtained from (14).

$$\begin{cases} V_{Q_1} = V_{D_{c1}} = V_{C_{c1}} = \frac{1}{(1-D)^2} V_{in} = \frac{1}{1+N+D} V_o \\ V_{Q_2} = V_{D_{c2}} = V_{C_{c2}} = \frac{1}{1-D} V_{in} = \frac{1-D}{1+N+D} V_o \\ V_{D_r} = V_{D_o} = V_o + V_{C_{c2}} - V_{C_{c1}} = \frac{1+N}{(1-D)^2} V_{in} = \frac{1+N}{1+N+D} V_o \end{cases} \tag{14}$$

Fig. 6 shows the normalized voltage stresses of the semiconductor devices for the sample duty cycle of 0.65; the voltages are normalized to the output voltage. It is observed that as N increases, the voltage stresses on the switches and clamp diodes decrease and voltage stresses on the regenerative

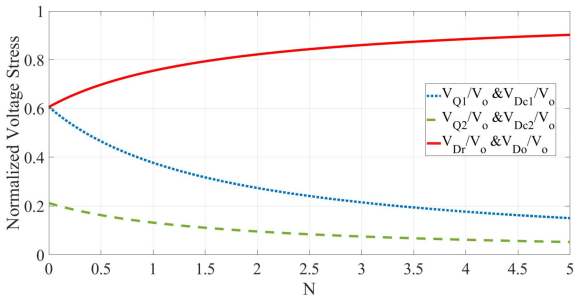

FIGURE 6. The Normalized voltage stresses of switches and diodes versus turns-ratio *N* for *D* = 0.65.

and output diodes increase, but they are always lower than the output voltage.

C. CURRENT STRESS OF SEMICONDUCTOR DEVICES

By applying the amp–second balance principle to the capacitors, the average currents of the capacitors for the main operating Stages 2, 3, 4, 6, and 7 are obtained. It is worth noting that the average currents of the capacitors for the entire switching cycle are zero; however, for an individual stage, they may not be zero. Then, using the average currents of the capacitors for stages, the average currents of the CIs' magnetizing inductances as well as the maximum currents of the semiconductors are extracted. It must be noted that the equivalent average currents of the semiconductors during their ON states (not entire switching period) are considered as the maximum current stresses of the semiconductors in this paper. The current relationships are as:

$$\begin{cases} I_{Lm1} = \frac{2+N}{1-D} I_o \\ I_{Lm2} = \frac{(3+N)D-1}{(1-D)^2} I_o \end{cases} \tag{15}$$

$$\begin{cases} I_{D_{c1\_avg}} = I_{D_{r\_avg}} = I_{D_{co\_avg}} = I_o \\ I_{D_{c2\_avg}} = \frac{1+N+D}{1-D} I_o \\ I_{Q1\_avg} = I_{Lm1} = \frac{2+N}{1-D} I_o \\ I_{Q2\_avg} = I_{Lm2} = \frac{(3+N)D-1}{(1-D)^2} I_o \end{cases} \tag{16}$$

$$\begin{cases} I_{D_{c1\_max}} = \frac{1}{k} I_o; \quad I_{D_{c2\_max}} = \frac{1+N+D}{(1-D)^2} I_o \\ I_{D_{r\_max}} = \frac{2N}{(1+N)(1-D)} I_o \\ I_{D_{o\_max}} = \frac{2+N}{(1+N)(1-D)} I_o \\ I_{Q1\_max} = \frac{2+3N}{1-D} I_o; \quad I_{Q2\_max} = \frac{1+N+D}{(1-D)^2} I_o \end{cases} \tag{17}$$

The root-mean-squared (RMS) current stresses of the switches are as (18).

$$\begin{cases} I_{Q1\_RMS} = \frac{N+1}{(1-D)\sqrt{D}} I_o \\ I_{Q2\_RMS} = \frac{(3+N)D-1}{(1-D)^2\sqrt{D}} I_o \end{cases} \tag{18}$$

IV. DESIGN CONSIDERATIONS

A. COUPLED INDUCTOR DESIGN

If the required voltage gain and the duty cycle are provided, the turns-ratio of the CIs is:

$$N = M(1 - D)^2 - (1 + D) \tag{19}$$

Assuming the maximum current ripple of $x\%$, the magnetizing inductances are determined. Considering Stages 6 and 7 in which switch Q_1 is in OFF state and the current of the magnetizing inductance L_{m1} is falling from the maximum to the minimum value, L_{m1} is obtained by using:

$$\begin{cases} \Delta i_{Lm1\_max} = x\% I_{Lm1} \\ I_{Lm1} = \frac{2+N}{1-D} I_o \\ V_{Lm1} = V_{in} + V_{C_{c2}} - V_{C_{c1}} = \frac{(1-D)(2-D)-1}{(1-D)^2} V_{in} \\ L_{m1} \geq \frac{|V_{Lm1}|(1-D)}{f_{sw}\Delta i_{Lm1\_max}} = \frac{(1-(1-D)(2-D))V_{in}}{(2+N)x\% I_o f_{sw}} \end{cases} \tag{20}$$

For the design of magnetizing inductance L_{m2}, Stage 2 is considered and L_{m2} is calculated as:

$$\begin{cases} \Delta i_{Lm2\_max} = x\% I_{Lm2} \\ I_{Lm2} = \frac{(3+N)D-1}{(1-D)^2} I_o \\ V_{Lm2} = V_{in} - V_{C_{c2}} = \frac{-D}{1-D} V_{in} \\ L_{m2} \geq \frac{|V_{Lm2}|(1-D)}{f_{sw}\Delta i_{Lm2\_max}} = \frac{D(1-D)^2 V_{in}}{((3+N)D-1)x\% I_o f_{sw}} \end{cases} \tag{21}$$

As for the leakage inductance of the CIs, it must not be too large because it decreases the voltage gain of the converter.

B. CAPACITORS DESIGN

The rated voltages of the capacitors were determined from (8)–(10). By applying the amp-balance law to the capacitors, their average currents could be determined for all the operation stages. For Stage 3, the average currents of the capacitors are given by (22). Then, by considering the maximum voltage ripple of $y\%$, the capacitances can be calculated from (23).

$$\begin{cases} I_{C_{c1}} = -\frac{N}{(N+1)(1-D)} I_o \\ I_{C_{c2}} = \frac{(N^2+5N+3)D-(2N+1)}{(N+1)(1-D)^2} I_o \\ I_{C_m} = \frac{N}{(N+1)(1-D)} I_o \\ I_{C_o} = -I_o \end{cases} \tag{22}$$

$$\begin{cases} C_{c1} \geq \frac{(1-D)|I_{C_{c1}}|}{y\% V_{C_{c1}} f_{sw}} = \frac{N(1+N+D)}{y\%(N+1) f_{sw} R} \\ C_{c2} \geq \frac{(1-D)I_{C_{c2}}}{y\% V_{C_{c2}} f_{sw}} = \frac{(1+N+D)\left((N^2+5N+3)D-(2N+1)\right)}{y\%(N+1)(1-D)^2 f_{sw} R} \\ C_m \geq \frac{(1-D)I_{C_m}}{y\% V_{C_m} f_{sw}} = \frac{N(1+N+D)}{y\%(N+1)(2+(1-D)N) f_{sw} R} \\ C_o \geq \frac{(1-D)|I_{C_O}|}{y\% V_{C_O} f_{sw}} = \frac{1-D}{y\% f_{sw} R} \end{cases} \tag{23}$$

C. SEMICONDUCTORS SELECTION

From (14) and (16)-(18), the voltage and current stresses of semiconductors were calculated, which provided an estimation for the voltage and current ratings of the switches and diodes. To consider the effect of the parasitic elements and to make sure that the semiconductors always operate within

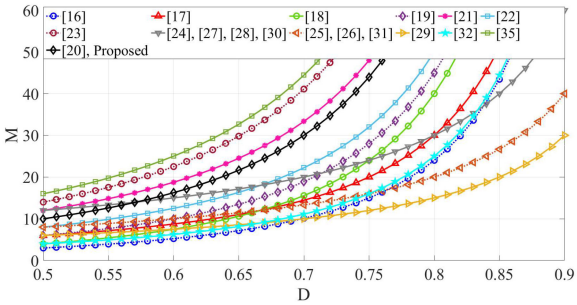

FIGURE 7. The voltage gain comparison for N = 1.

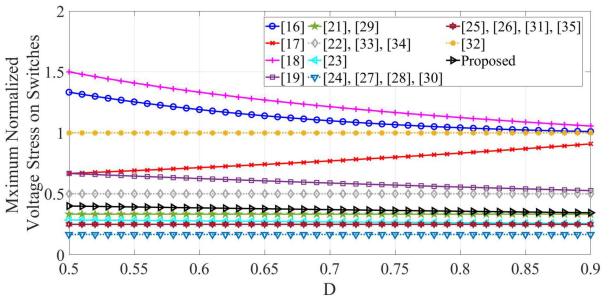

FIGURE 8. Comparison of the maximum normalized voltage stress of switches for N = 1.

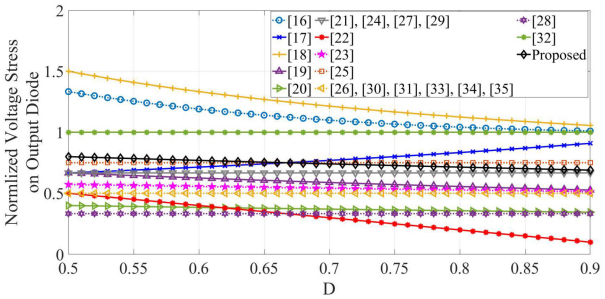

FIGURE 9. Comparison of the normalized voltage stress of output diode for N = 1.

the safe operating area, the voltage and current ratings of the selected semiconductors must be higher than the calculated values.

V. CIRCUIT PERFORMANCE COMPARISON

As established from (10), the voltage gain of the proposed converter is a quadratic function of the duty cycle, leading to extended significant voltage gains. The voltage gain is adjustable with two parameters: duty cycle (D) of the switches and turns-ratio (N) of the CIs; these two degrees of freedom make the design of the converter more flexible. In addition, the proposed converter has an interleaved structure that leads to a low input current ripple and low current stresses of the components. Thus, it was helpful to compare the proposed converter with two categories of existing high step-up converters: 1) non-interleaved quadratic converters, including both non-CI-based topologies in [16]–[18] and CI-based structures in [19]–[23]; 2) interleaved converters, including both non-quadratic converters in [24]–[31] and quadratic topologies in [32]–[35]. Thus, the proposed converter is compared to 20 existing converters in the literature to cover all aspects of comparison; 12 of them are quadratic high step-up converters and the rest is non-quadratic. Such a comparison is made in Table 1. The curves of the voltage gain using the same turns-ratio (if applicable) are sketched in Fig. 7, where $N = 1$ is used as the comparative reference. Furthermore, the voltage gain values of all converters are calculated for the example case of $N = 1$ and $D = 0.7$, listed in the second column from the last of Table 1. The voltage gains of the quadratic converters in [16]–[18] are adjusted only by duty cycle, which are not high enough compared to the proposed converter. In addition, the converters in [16]–[18] lack the interleaved configuration that is useful for renewable energy applications where a low input current ripple is required. Considering the CI-based quadratic converters in [19]–[23], the voltage gain of the converter in [23] is higher than the proposed converter, but it has two additional components. The voltage gain of the converter in [21] is slightly higher than the proposed converter, but the difference is not significant, and it does not have the interleaved configuration that is essential to reduce the input current ripple. Although the converter in [20] has the same voltage gain as the proposed converter, it has two more components and is lack of the interleaved structure. Other non-interleaved CI-based quadratic converters have lower voltage gains than the proposed converter. Among the interleaved converters in [24]–[35], only the CI-based interleaved converter in [35] has higher voltage gain than the proposed converter; however, it has six more components with the three-winding CIs. The proposed converter has the best voltage-boosting capability with highest voltage gain compared to the other quadratic or non-quadratic interleaved converters in [24]–[34]. In addition, Fig. 8 shows the comparison of the maximum normalized voltage stress on the switches for $N = 1$. It is obvious that the proposed converter has lower maximum voltage stress on the switches compared to the converters in [16]–[19], [22], [32]–[34]. Moreover, Fig. 9 depicts the comparison of the normalized voltage stress on the output diode for $N = 1$; as seen, like many other high step-up DC-DC converters, the voltage stress of the output diode is lower than the output voltage. Thus, the proposed converter has a low number of the components with low voltage stresses on the semiconductors, resulting in selecting low-voltage-rated switches and diodes with low ON-state resistances that causes the reduction in the conduction losses. Furthermore, according to the last column of Table 1, unlike some converters in the literature, the input and output sides of the proposed converter share the common ground that increases the reliability. Overall, the proposed converter stands out from the prior works as a suitable candidate for RE applications because it has a high voltage gain, an interleaved structure with low input current ripple, high reliability, low voltage stresses on the semiconductors, and simple structure with a low number of components.

TABLE 1 Comparison of the Presented DC–DC Converter with Several Other Similar Topologies

Topology		Number of Components						Normalized voltage stresses on switches ($\frac{V_Q}{V_o}$)	Normalized voltage stress on output diode ($\frac{V_{D_o}}{V_o}$)	Voltage gain ($M=\frac{V_o}{V_{in}}$)	Voltage gain for D=0.7 and N=1 (if applicable)	Common ground for input and output
		S	D	C	CI	L	Total					
Non-Interleaved Quadratic Converters	[16]	2	2	2	0	2	8	$\frac{1}{D(2-D)}$ $\frac{1-D}{D(2-D)}$	$\frac{1}{D(2-D)}$	$\frac{D(2-D)}{(1-D)^2}$	10.10	NO
	[17]	1	4	3	0	2	10	$\frac{1}{2-D}$	$\frac{1}{2-D}$	$\frac{2-D}{(1-D)^2}$	14.44	YES
	[18]	2	3	3	0	2	10	$\frac{1+D}{2D}$ $\frac{1-D}{2D}$	$\frac{1+D}{2D}$	$\frac{2D}{(1-D)^2}$	15.55	NO
	[19]	1	4	3	1	1	10	$\frac{1}{DN+1}$	$\frac{N}{DN+1}$	$\frac{DN+1}{(1-D)^2}$	18.88	YES
	[20]	1	6	5	1	1	14	$\frac{2+D(N-1)}{N(3D+2)+(2-D)}$	$\frac{2N}{N(3D+2)+(2-D)}$	$\frac{N(3D+2)+(2-D)}{2(1-D)^2}$	30	YES
	[21]	1	5	4	1	1	12	$\frac{1}{N+2}$	$\frac{N+1}{N+2}$	$\frac{N+2}{(1-D)^2}$	33.33	YES
	[22]	1	5	4	1	1	12	$\frac{1}{N+1}$	$\frac{2N-2ND}{N+1}$	$\frac{N+1}{(1-D)^2}$	22.22	YES
	[23]	1	6	5	1	1	14	$\frac{1}{N+ND+2}$	$\frac{N+1}{N+ND+2}$	$\frac{N+ND+2}{(1-D)^2}$	41.11	YES
Interleaved Non-Quadratic and Quadratic Converters	[24]	2	4	4	2	0	12	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	$\frac{2N+4}{1-D}$	20	YES
	[25]	4	2	3	2	0	11	$\frac{1}{2N+2}$	$\frac{2N+1}{2N+2}$	$\frac{2N+2}{1-D}$	13.33	YES
	[26]	2	7	7	2	0	18	$\frac{1}{2N+2}$	$\frac{2}{2N+2}$	$\frac{2N+2}{1-D}$	13.33	NO
	[27]	2	4	4	2	0	12	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	$\frac{2N+4}{1-D}$	20	YES
	[28]	2	6	6	2	0	16	$\frac{1}{2N+4}$	$\frac{2N}{2N+4}$	$\frac{2N+4}{1-D}$	20	NO
	[29]	2	4	3	2	0	11	$\frac{1}{2N+1}$	$\frac{2N}{2N+1}$	$\frac{2N+1}{1-D}$	10	YES
	[30]	4	4	5	2	0	15	$\frac{1}{4N+2}$	$\frac{1}{2}$	$\frac{4N+2}{1-D}$	20	NO
	[31]	2	5	4	2	0	13	$\frac{1}{3N+1}$	$\frac{2N}{3N+1}$	$\frac{3N+1}{1-D}$	13.33	YES
	[32]	2	6	3	0	4	15	1	1	$\frac{1}{(1-D)^2}$	11.11	YES
	[33]	2	6	4	0	4	16	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{2}{(1-D)^2}$	22.22	YES
	[34]	2	6	4	2	0	14	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{2}{(1-D)^2}$	22.22	YES
	[35]	2	8	6	2	0	18	$\frac{1}{2N+2}$	$\frac{2}{2N+2}$	$\frac{2N+2}{(1-D)^2}$	44.44	YES
Proposed converter		2	4	4	2	0	12	$\frac{1}{1+N+D}$ $\frac{1-D}{1+N+D}$	$\frac{1+N}{1+N+D}$	$\frac{1+N+D}{(1-D)^2}$	30	YES

(S = switch, D = diode, C = capacitor, CI = coupled inductor, L = simple inductor, T = total number of components)

VI. EXPERIMENTAL RESULTS

Considering the design of Section IV, a 400 W laboratory prototype, as shown in Fig. 10, is implemented to verify the theoretical analysis and the effectiveness of the proposed converter. Assuming the maximum current ripple of 25 % for the CIs' magnetizing inductances and maximum voltage ripple of 2 % for the capacitors for N = 1, V_{in} = 25 V, and V_o = 400 V, the required inductances and capacitances are as: $L_{m1}\geq$293.6 μH, $L_{m2}\geq$136 μH, $C_{c1}\geq$1.3 μF, $C_{c2}\geq$49 μF, $C_m\geq$20 μF, and $C_o\geq$1 μF. The selected components and specifications of the experimental setup are listed in Table 2.

Figs. 11–18 illustrate the experimental voltage and current waveforms of the proposed converter for the input voltage of 25 V. To achieve the output voltage of 400 V, the switches operate at the equal duty cycle of 0.597 but 180° out of phase; the gate pulses of the MOSFETs are generated by the TMS320F28335 microcontroller. Fig. 11 illustrates the voltages across the capacitors; the experimental

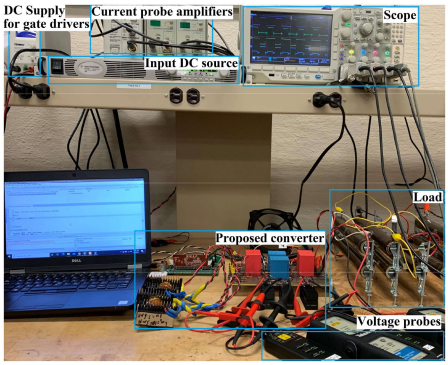

FIGURE 10. Experimental setup.

TABLE 2 Specifications of the Experimental Setup

Parameters	Values/Part number
Rated Power	400 W
f_{sw}	50 kHz
Capacitors C_m, C_o	DCP4L052007GD4KSSD (20 µF, R_{Cm}= R_{Co}=6.25 mΩ)
Capacitor C_{c1}	B32678G4206K000 (20 µF, R_{Cc1}=3.3 mΩ)
Capacitor C_{c2}	B32776G4506K000 (50 µF, R_{Cc2}=4 mΩ)
Switch Q_1	FDH44N50 ($R_{DS(on)}$=110 mΩ, C_{oss}=645 pF, t_{on}=100 ns, t_{off}=124 ns)
Switch Q_2	IRFP4668PBF ($R_{DS(on)}$=8 mΩ, C_{oss}=810 pF, t_{on}=146 ns, t_{off}=138 ns)
Diodes D_{c1}, D_r, D_o	VS-ETL1506-M3 ($V_{F0,\ Dc1}$=$V_{F0,\ Dr}$=$V_{F0,\ Do}$=0.6 V, $R_{on,\ Dc1}$=$R_{on,\ Dr}$=$R_{on,\ Do}$=17 mΩ)
Diode D_{c2}	APT60S20BG ($V_{F0,\ Dc2}$ =0.3 V, $R_{on,\ Dc2}$=7 mΩ)
CIs	Core: ETD59/31/22-3C97 (N=1, L_{m1}=314, L_{m2}=191 µH, L_{k1}=1.5, L_{k2}=1, L_{k3}=3.5 µH, R_{p1}=R_{s1}=30 mΩ, R_{p2}=R_{s2}=20 mΩ)

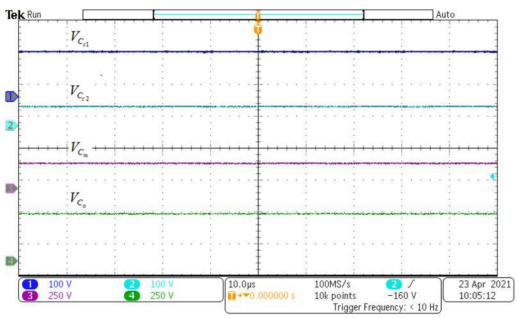

FIGURE 11. Voltages of capacitors C_{c1} (CH1), C_{c2} (CH2), C_m (CH3), and C_o (CH4).

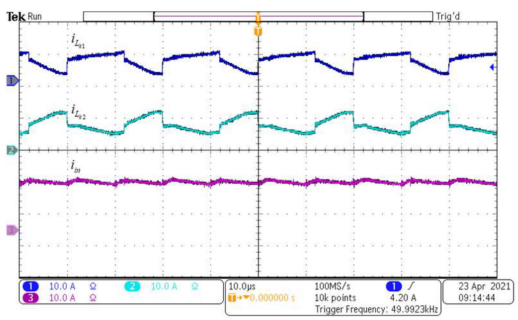

FIGURE 12. Currents i_{Lk1} (CH1) and i_{Lk2} (CH2) along with input current (CH3).

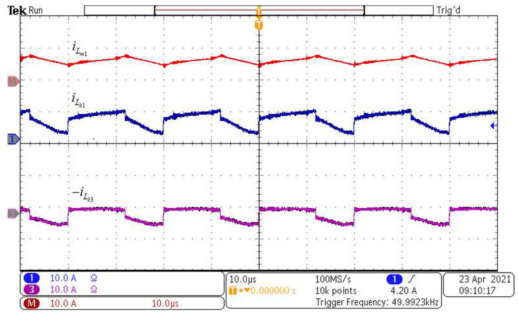

FIGURE 13. Currents i_{Lk1} (CH1) and -i_{Lk3} (CH3) along with current i_{Lm1} (Math).

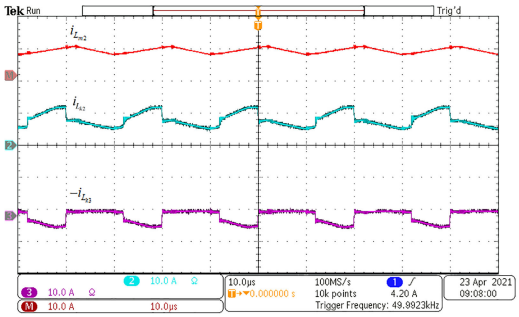

FIGURE 14. Currents i_{Lk2} (CH2) and -i_{Lk3} (CH3) along with current i_{Lm2} (Math).

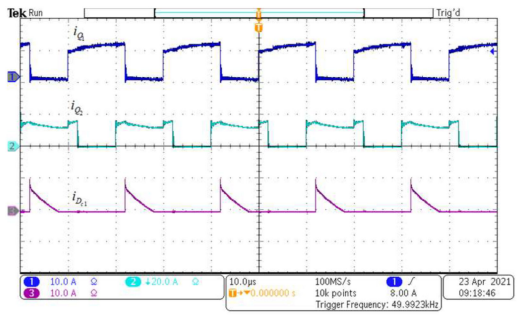

FIGURE 15. Currents of switches Q_1 (CH1) and Q_2 (CH2) and diode D_{c1} (CH3).

results of $V_{Cc1} = 145$ V, $V_{Cc2} = 60$ V, $V_{Cm} = 206$ V, and $V_o = V_{Co} = 381$ V are close enough to the theoretical results that are as: $V_{Cc1} = 154$ V, $V_{Cc2} = 62$ V, $V_{Cm} = 216$ V, and $V_o = V_{Co} = 400$ V. Figs. 12–14 demonstrate the input current and the currents of magnetizing and leakage inductances of the CIs. As observed, currents i_{Lk1} and i_{Lk2} (similarly currents i_{Lm1} and i_{Lm2}) are 180° out of phase from each other, which verifies the interleaved operation of the proposed converter. Also, due to the interleaved operation of the proposed converter, the input current has a small ripple, which helps for the long lifetime of the input RES. Note that it is not possible to directly measure the magnetizing inductances' currents i_{Lm1} and i_{Lm2}; however, since the turns-ratios of the CIs are unity (i.e., $N = 1$), currents i_{p1} and i_{p2} are equal to $-i_{Lk3}$ and $+i_{Lk3}$, respectively. Accordingly, as shown in Figs. 13 and 14, Math Channel of the oscilloscope is used to extract i_{Lm1} and i_{Lm2}

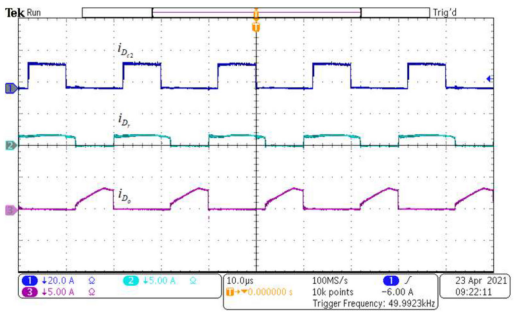

FIGURE 16. Currents of diodes D_{c2} (CH1), D_r (CH2), and D_o (CH3).

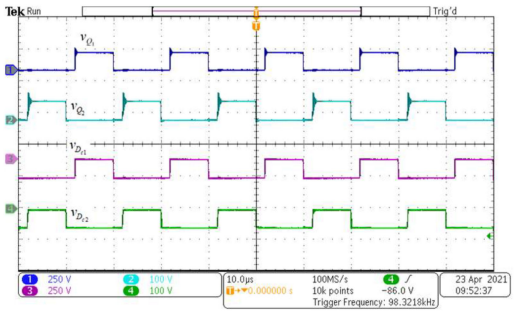

FIGURE 17. Voltages of switches Q_1 (CH1) and Q_2 (CH2) and diodes D_{c1} (CH3) and D_{c2} (CH4).

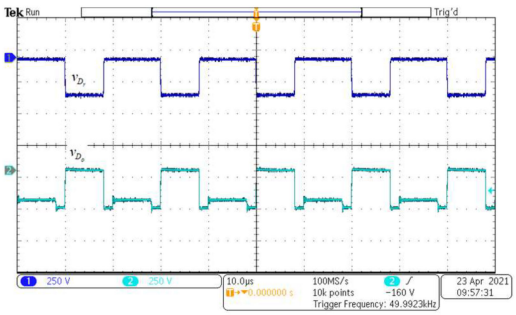

FIGURE 18. Voltages of diodes D_r (CH1) and D_o (CH2).

from $i_{Lm1} = i_{Lk1}+i_{Lk3}$ and $i_{Lm2} = i_{Lk2}$-i_{Lk3}, respectively. The currents of switches Q_1 and Q_2, as well as the currents of diodes D_{c1}, D_{c2}, D_r, and D_o are shown in Figs. 15 and 16. Moreover, as observed in Figs. 13–16, all the currents of inductances and semiconductor devices are consistent with the key waveforms of Fig. 3. The voltages of the switches and diodes are depicted in Figs. 17 and 18, where the approximate voltage stresses of $V_{Q1} = V_{Dc1} = 154$ V, $V_{Q2} = V_{Dc2} = 62$ V, and $V_{Dr} = V_{Do} = 308$ V are observed, validating (14). As seen, the voltage stresses of the power switches are far less than the output voltage that enables the designers to select low-voltage-rating MOSFETs with low ON-state resistance, which contributes to improving the converter's efficiency.

Fig. 19 shows the measured efficiency at input voltage values of 25 V and 40 V for the same output voltage of 400 V; the proposed converter operates at the different duty cycles of 0.597 and 0.5 for input voltages of 25 V and 40 V,

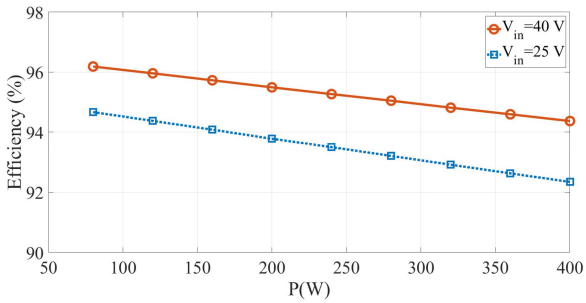

FIGURE 19. The measured efficiency of the proposed converter versus the power for the input voltages of 25 V and 40 V.

TABLE 3 Full-Load Efficiency Comparison of Proposed Converter with Other CI-Based Quadratic Converters

Topology	Parameters	Full-load efficiency
[19]	V_{in}=40 V, V_o=400 V, f_{sw}=40 kHz, P_{rated}=280 W	93.3 %
[20]	V_{in}=24 V, V_o=400 V, f_{sw}=50 kHz, P_{rated}=250 W	93. 96 %
[21]	V_{in}=32 V, V_o=380 V, f_{sw}=40 kHz, P_{rated}=500 W	91.1 %
[22]	V_{in}=20 V, V_o=400 V, f_{sw}=50 kHz, P_{rated}=200 W	89.5 %
[23]	V_{in}=30 V, V_o=400 V, f_{sw}=50 kHz, P_{rated}=300 W	92.2 %
[35]	V_{in}=18 V, V_o=380 V, f_{sw}=50 kHz, P_{rated}=150 W	95 %
Proposed converter	V_{in}=40 V, V_o=400 V, f_{sw}=50 kHz, P_{rated}=400 W	94.4 %

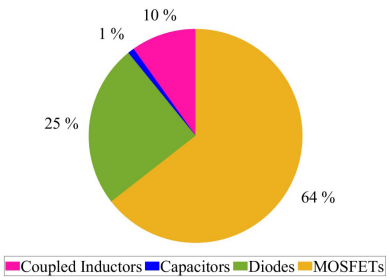

FIGURE 20. The analytical power loss distribution of the proposed converter at full load for V_{in} = 25 V.

respectively. At the full load, the efficiency is 92.3% and 94.4 % for the input voltages of 25 V (with $M = 16$) and 40 V (with $M = 10$), respectively. The full-load efficiency of the proposed converter is compared to other CI-based quadratic converters in Table 3. Furthermore, using the loss analysis presented in [36], the analytical power loss distribution of the proposed is obtained; Fig. 20 shows the analytical loss distribution of the proposed converter at 400 W for the input voltage of 25 V. The MOSFETs, diodes, coupled inductors, and capacitors have the power losses of 19.6 W, 7.5 W, 3 W, and 0.3 W, respectively. Thus, the MOSFETs have dominant power losses with 64 %.

VII. CONCLUSION

In this paper, a new high step-up DC-DC converter was proposed for renewable energy applications. A pair of two-winding CIs and SC-based VMCs were employed in an interleaved quadratic structure. Additionally, diode-capacitor based clamp circuitries were used to limit the switches' voltage stresses, recycle the leakage inductances' energies, and further increase the voltage gain. The high-voltage gain, continuous input current with low ripple, low voltage stresses on the semiconductors, and simple structure are the primary merits of the proposed converter. The operating principles, steady-state analysis, and design considerations were presented. To justify the merits of the proposed converter, its key indicators were compared with other high-voltage gain converters found in the literature. The theoretical operation and analysis of the proposed converter were validated by the experimental results of a 400 W prototype with a voltage gain of 16. The efficiency is found to be 92.3 % and 94.4 % for the voltage gains of 16 and 10 at the full load. The presented results verified that the proposed converter is a promising candidate for renewable energy applications.

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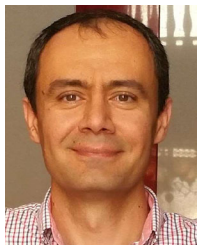

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