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Analysis and Design of a Zero-Current Switching Non-Isolated High Gain Inverter

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ABSTRACT High gain inverters are gaining popularity due to their application in renewable energy sources. Impedance source inverters (ISIs) such as Z-source inverter (ZSI) and its derivatives are favored over the two-stage boost-VSI topology because of their higher gain and better EMI immunity. Another ISI, Current-fed Switched Inverter (CFSI), has a similar gain characteristic as ZSI but with lesser components. The major drawback of high gain inverters is that they draw very high input current. Thus, the switching and conduction losses increase in the front stage converter, resulting in reduced efficiency. This paper proposes a modified CFSI topology to achieve Zero Current Switching (ZCS) of the switch connected in the front-end boost stage. The operating principle and modes of operation of the proposed converter are discussed in detail. A flow chart for designing the resonating components of the modified circuit and the impact of parametric variation on the scheme's performance is reported. The theoretical analysis is verified with the help of a laboratory prototype. The efficiency of the modified converter is found to be increased by 2% (at 450 W load) compared to conventional CFSI.

INDEX TERMS Current-fed switched inverter (CFSI), PWM, inverter, soft switching, ZVS, ZCS, ZCS-CFSI.

I. INTRODUCTION

Over the last few years, the research and development in photovoltaic (PV) systems have improved PV panel's efficiency and manufacturing technology [1]. So, renewable energy systems based on solar PV are getting increased popularity as a feasible alternative. Roof-top PV systems are common in rural areas to utilize solar energy. Low initial capital investment of these makes them a viable power generating solution in rural areas.

A roof-top PV is a standalone system that usually includes only one or two PV panels, as they supply only a few household loads [2]. Therefore, a typical roof-top PV system has lower operating voltage and power. The power converter interface should have a high voltage gain to meet the voltage rating of the utility grid. One popular method of connecting a roof-top solar PV to the utility grid is Boost-VSI, as shown in Fig. 1. First, an active front-end boost stage converts PV output voltage V_{pv} to a high voltage DC voltage V_{dc}. Then, a voltage source inverter (VSI) stage converts this high voltage (V_{dc}) to the required AC grid voltage v_{ac}. This method requires a voltage stiff capacitive link (C_{dc}) and that is operating at high voltage. This may lead to shoot through (ST) of an inverter leg of the VSI stage during high-frequency operation.

A solution for this problem is to use Impedance Source Inverters (ISIs) such as Z-source inverter [2], Quasi-ZSI [3], switched boost inverter (SBI) [4], and CFSI [5]. These are non-isolated inverter topologies with an inherent high voltage gain, as shown in Fig. 2. Moreover, shoot-through protection is not required in these inverters, leading to better EMI immunity and increased reliability. CFSI topology is preferred, as this requires only one LC pair and takes a continuous input current from the low voltage DC source (V_{pv}) [5]. CFSI is also referred to as embedded type q-SBI in [6] and, Active switched capacitor q-ZSI (ASC-qZSI) in [7], as shown in Fig. 3.

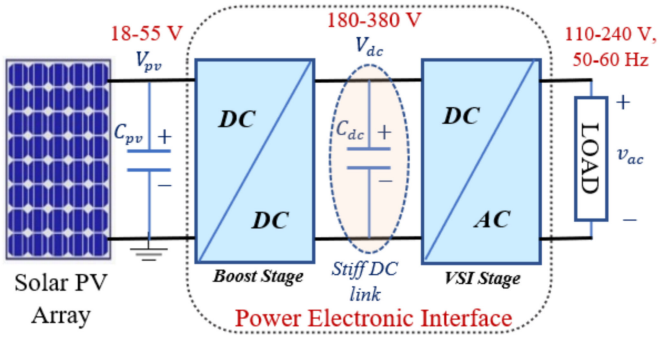

FIGURE 1. Block Diagram of solar PV power supply interface of Boost-VSI.

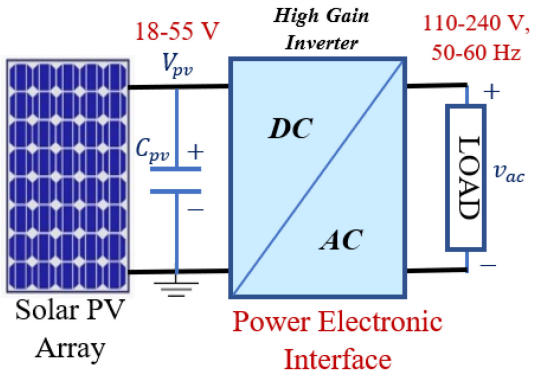

FIGURE 2. Block Diagram of solar PV power supply interface.

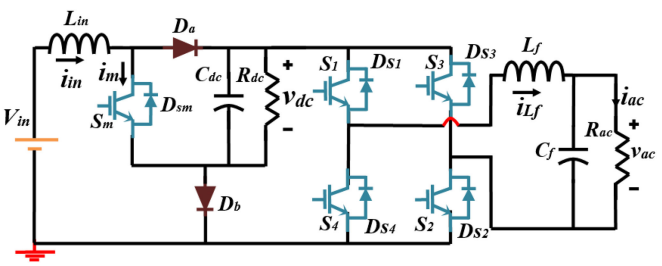

FIGURE 3. Schematic of Current-Fed Switched Inverter (CFSI).

The operation under high voltage gain results in higher voltage stress across the switching devices in the CFSI topology compared to Boost-VSI. The voltage stress can be minimized by operating converter in different Pulse Width Modulation (PWM) schemes as discussed in [8]–[10]. However, the converter takes a relatively higher input current, resulting in higher conduction losses in the switching devices [11], [12]. Although, the selection of IGBTs and diodes with lower ON state drops results in reduced conduction losses.

Furthermore, the switching losses are significantly higher in the IGBTs under high gain operation due to tail current during turn-off. High switching loss in the devices restricts the converter to operate at higher switching frequencies. Additionally, hard switching of the devices leads to EMI problems at higher operating frequencies and increased stress in the switches during transitions [2].

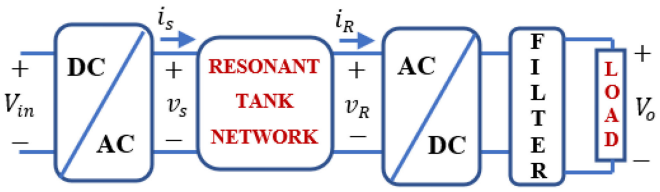

FIGURE 4. Block diagram of a resonant converter.

Different soft-switching techniques have been proposed in the literature to reduce the switching losses [13]–[26]. A soft-switched topology has an LC resonant network integrated with the converter circuit. This resonant network ensures that the voltage across the switching element remains zero during the switching transition, resulting in zero voltage switching (ZVS). Otherwise, the LC network ensures zero current switching (ZCS) by avoiding current flow through the device throughout the switching transition. A load resonant converter, quasi-resonant converter (multi-resonant), and resonant transition converter are typical examples of soft-switched converters [13].

As shown in Fig. 4, a resonant converter has a switching inverter block that converts DC to a high-frequency AC voltage (v_s). This voltage v_s acts as a source to a resonant tank network, resulting in the voltage (v_R) depending on load resistance. Ideally, the resonant tank network is purely reactive, having one or more LC pairs in series/parallel connections. Later, an AC-DC block rectifies the voltage v_R followed by a DC filter to result in the load voltage V_o. The converter's switching frequency is varied to control the voltage gain and achieve soft switching of the converter. Switching frequency higher than the resonant frequency results in the ZVS of the switches in the DC-AC block. However, switching frequency lower than the resonant frequency results in the ZCS of the switches [14]. Typical applications of the load resonant converters are wireless power transfer (WPT), EV chargers, and solid-state transformer [15], [16].

An inductive coil is utilized to resonate with the parasitic capacitance of the switching element to achieve ZVS in Quasi-Resonant Converters (QRCs). The inductive element of the converter topology can also be used to achieve ZVS in some topologies [17]–[20]. However, this leads to increased current ripple and conduction losses [19]. In addition, these topologies also suffer from large voltage stress under high load conditions, as voltage stress is proportional to the loading current for QRCs [20].

A shunt resonating network is connected across the switching element in resonant transition converters. The shunt branch is only activated during switching transitions to achieve soft-switching. The circuit reverts back to its normal operating state after the transition of the switching element is completed [23]–[24]. So, resonant transition converters can be operated at a constant frequency with low switching and conduction losses [25]. Furthermore, these converters can be

operated over a wide range of load variations without affecting soft-switching [26]–[27].

In this paper, the conventional topology of CFSI is modified to achieve ZCS of the boost stage devices. The modified circuit (ZCS-CFSI) contains an auxiliary sub-circuit which includes a resonating inductor, capacitor, and an additional switch. An auxiliary sub-circuit is activated only at switching transitions to achieve soft switching of devices. Other than switching transition, ZCS-CFSI behaves similar to that of conventional CFSI. The gate pulse of the auxiliary switch is synchronized with the PWM scheme of ZCS-CFSI to start the auxiliary branch.

The following section discusses different PWM schemes used for CFSI followed by the proposed ZCS-CFSI circuit and its modified PWM scheme in Section III. Here, different modes associated with the modified PWM scheme, modified gains and loss analysis are also discussed. Section IV discusses the design of the resonant components and their variations on the performance of ZCS-CFSI. The new topology is verified by designing a lab prototype. Based on that, simulation and experimental results are given in Section V. Finally, Section VI concludes this paper.

II. DIFFERENT PWM SCHEMES USED FOR CFSI/Q-SBI

The unipolar PWM scheme of VSI is modified to derive the PWM scheme of CFSI. Here, a shoot-through interval is added in the usual unipolar PWM scheme to achieve a high voltage gain. Shoot-Through (ST) interval is added in one of the inverter legs during the positive half cycle and another leg during the negative half cycle [5]. ST is added in the zero states of the inverter so that no change is needed in the conventional unipolar PWM scheme of VSI. Fig. 6 shows the equivalent circuit of CFSI. This H-bridge is replaced by a shoot-through switch (S_{ST}) and a current source (i_i). Due to the addition of shoot-through interval (D_{ST}) in the inverter legs, the modulation index is limited as,

$$D_{ST} + M \leq 1 \tag{1}$$

As shown in Fig. 5, different PWM schemes are proposed in the literature to improve the modulation index. In this, gate pulse (G_{ST}) represents the shoot-through in inverter legs, and G_{Sm} is the gate pulse of the main switch (S_m).

Scheme-1, in Fig. 5, is the simple boost control (SBC) scheme of CFSI. In this scheme, G_{ST} and G_{Sm} are coupled [5]–[7]. Scheme-2, in Fig. 5, shows the modified PWM scheme of CFSI proposed in [8]. In this, the shoot-through interval is inserted in between the turn-on duration of the main switch. Even though G_{ST} and G_{Sm} are synchronized, their duty cycles are not equal. The main switch and shoot-through switch are turned off together in scheme-3 [9]. However, D_{ST} is made lower than D by varying the G_{ST} turn on the instant. Nguyen *et al.* [10] proposed different PWM schemes named as PWM2, PWM3, and PWM5. These schemes are designated as Scheme-4, Scheme-5, and Scheme-6, respectively. The shoot-through interval decreases as the number of charging periods in a carrier period increases. Therefore, the largest possible value of the modulation index increases for inverter output voltage control.

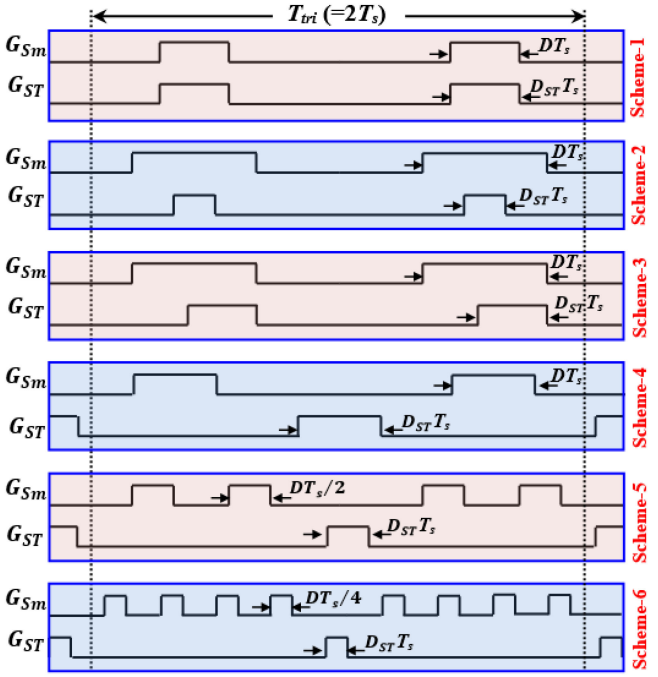

FIGURE 5. Different PWM scheme for CFSI.

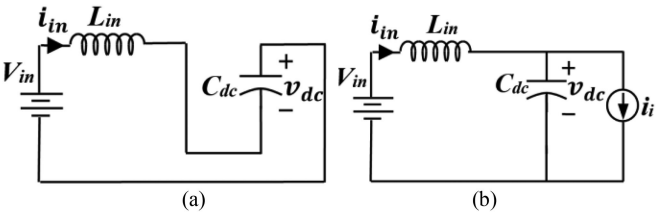

FIGURE 6. Equivalent circuit during (a) Shoot through interval, *D* and (b) Non-shoot through interval, *(1-D)*.

The switching cycle of CFSI is divided into shoot-through (ST) interval and Non-shoot-through (NST) interval to obtain an expression for dc and ac gains of the converter. During ST interval, switches of leg-1 or leg-2 are turned on along with the switch *Sm*, as shown in Fig. 6(a). However, during NST interval, switch *Sm* of the boost stage is turned off, as shown in Fig. 6(b). As a result, *Da* and *Db* are turned on by the inductor current. The voltage across the inductor during ST and NST intervals are given as,

$$\text{During the } D \text{ interval } \left(\text{ST period}\right), \quad L_{in}\frac{di_L}{dt} = V_{in} + v_{dc}$$

$$\text{During } (1-D) \text{ interval } \left(\text{NST period}\right), \quad L_{in}\frac{di_L}{dt} = V_{in} - v_{dc}$$

Using inductor-volt sec balance, DC and AC gain of the CFSI is evaluated as,

$$DC\ Gain: \quad \frac{V_{dc}}{V_{in}} = \frac{1}{1-2D} \tag{2a}$$

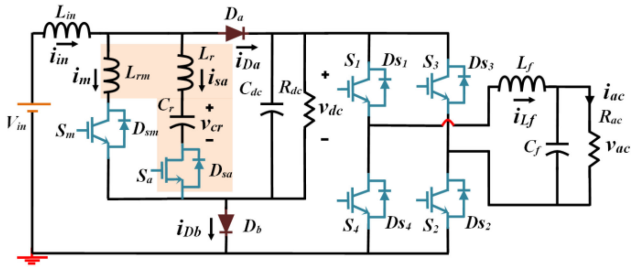

FIGURE 7. Proposed topology of ZCS-CFSI.

$$Ac\ Gain: \quad \frac{\hat{V}_{ac}}{V_{in}} = \frac{M}{1-2D} \tag{2b}$$

Here, the voltage $\hat{V}_{ac}$ is the peak of AC output voltage. Due to the limitation given in (1), CFSI is forced to operate at higher DC-link voltage, which increases the current drawn from the input due to high boost-up operation. But, high DC-link voltage (v_{dc}) lowers the current drawn by the H-bridge inverter. Thus, the switching losses associated with the inverter are lower. However, since the voltage stress and current are higher in the boost stage, switching losses in the switching devices are also significantly higher. Therefore, it is necessary to reduce the losses of the boost stage devices to obtain higher efficiency. Thus, the following section discusses the soft-switching operation of CFSI by adding an auxiliary circuit in the boost stage.

III. PROPOSED TOPOLOGY TO ACHIEVE SOFT SWITCHING IN CFSI

A. PROPOSED TOPOLOGY

As discussed earlier, the proposed topology contains a conventional CFSI converter integrated with a sub-circuit to achieve soft-switching. A conventional CFSI converter has an IGBT switch S_m and two diodes D_a and D_b, in the first DC-DC stage. Other four IGBT switches (S_1-S_4) form a full-bridge inverter configuration. At the load side, a filter containing L_f and C_f is cascaded with the output of the inverter bridge. The sub-circuit containing an auxiliary MOSFET switch S_a, capacitor C_r, inductor L_r, along with a series inductor L_{rm}, is shown as a shaded part in Fig. 7. The inductor L_r and capacitor C_r forms a resonant circuit that operates at a very high frequency compared to the switching frequency. The prominent features of the modified circuit are (a) The main switch S_m is turned off and on with ZCS, (b) The diode D_a turns on with ZVS and turns off with ZCS, and (c) Resonating inductors (L_r and L_{rm}) and capacitor (C_r) are of minimal value (in μH and μF, respectively).

B. SWITCHING SCHEME

The ZCS of the main switch S_m during turn-off is achieved using the auxiliary switch S_a. Here, the basic idea is to turn on the switch S_a before turning switch S_m off. Thus, the auxiliary circuit starts resonating, and the resonating current forces the main switch current to zero. Then the gate pulse of the main switch is removed. Hence, to activate the auxiliary branch, the PWM signal of the auxiliary switch must be synchronized with the main switch.

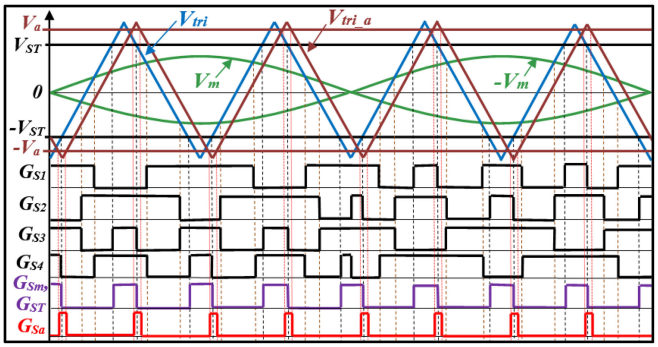

FIGURE 8. PWM control signals of Proposed ZCS-CFSI topology.

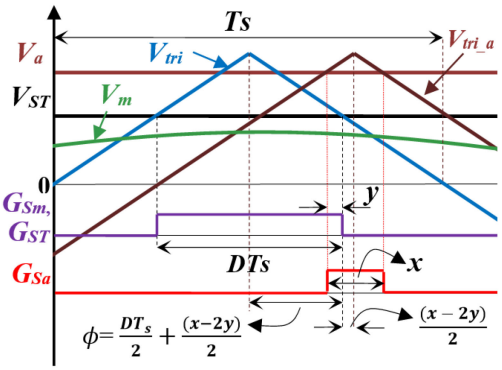

FIGURE 9. Close view of the comparison of triangular signal with V_a and V_{ST} to generate the gate pulses G_{Sa} and G_{ST}, respectively.

Fig. 8 shows the modified SBC scheme of ZCS-CFSI. In this modified PWM scheme, an additional carrier signal V_{tri_a} generates gate pulse for the auxiliary switch. V_{tri_a} must be synchronized with the V_{tri} with a phase shift 'ϕ' to obtain soft switching of the main switch. Gate pulse of the auxiliary switch is produced by comparing DC signal V_a and $-V_a$ with V_{tri_a}. Magnitude, V_a decides the pulse width of the auxiliary switch, and ϕ decides the phase shift between two carrier signals V_{tri} and V_{tri_a}. Thus, ϕ is used to varying the position of gate pulse G_{sa} about the turning off of the main switch. Fig. 9 shows the zoomed picture of the PWM scheme in a switching cycle. It shows that 'x' is the pulse width of the auxiliary switch. 'y' is an overlap period in which both the switches S_m and S_a are in ON-state. This overlap period is required to turn off the main switch safely under ZCS conditions, mathematically,

$$V_a = \hat{V}_{tri_a}\left(1 - \frac{x}{DT_s}\right) \text{ and } \phi = \frac{DT_s}{2} + \frac{x-2y}{2} \tag{3}$$

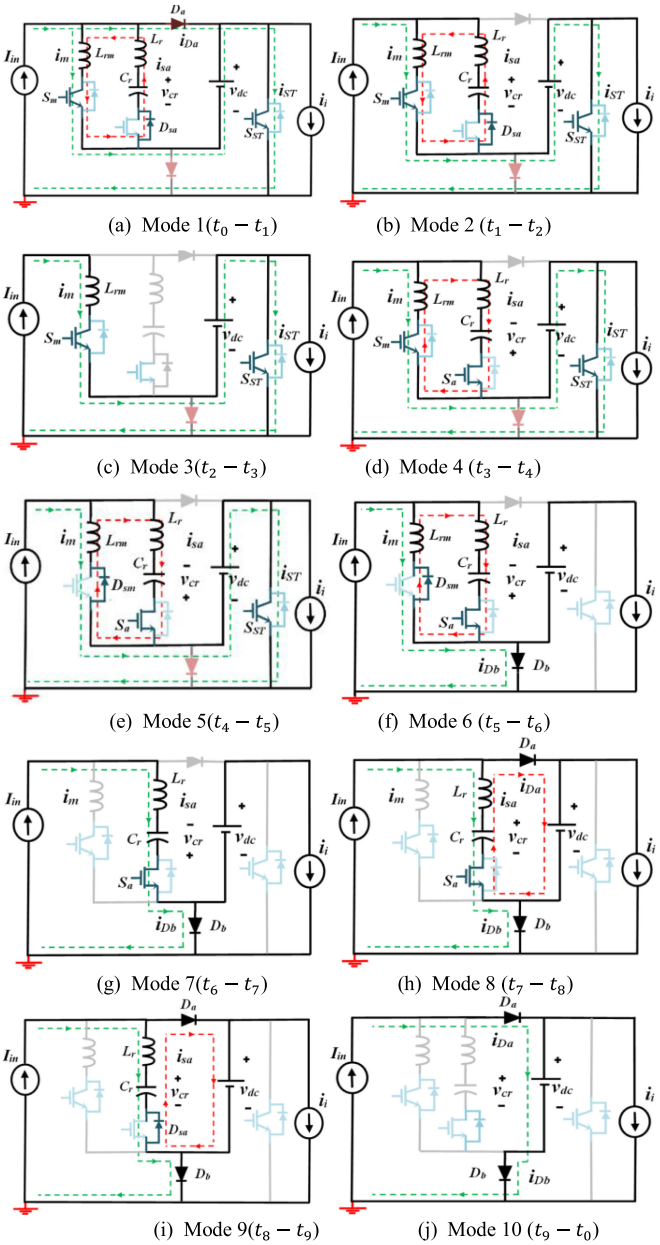

FIGURE 10. Equivalent circuit diagram for each mode of operation.

C. SWITCHING MODES

Some assumptions are considered during the different modes associated with the ZCS-CFSI, which are as follows: (a) circuit is operated in a steady-state, (b) Current through the input inductor (I_{in}), and the voltage across the DC-link capacitor (v_{dc}) is assumed to be constant, (c) resonating components (L_{rm}, L_r and C_r) are much smaller than L_{in} and C_{dc}, and (d) the inverter bridge of ZCS-CSFI is replaced by a combination of shoot-through switch S_{ST} in parallel with an equivalent current source i_i as shown in Fig. 8. Therefore, the operation of the converter is divided into 10 modes and the equivalent circuit under different modes of operation shown in Fig. 10. During this analysis it is assumed that the capacitor C_{dc} and C_r are initially charged with a voltage of V_{dc} and k V_{dc} respectively. Here, the value of k is less than unity and is given by (23) later during this section.

Mode 1 ($t_0 < t < t_1$): This mode starts by turning on both the switches $S_{\rm m}$ and S_{ST}. It is considered that both the diodes are in conduction (NST interval) before turning on the switches. However, turning on S_{ST} in this mode reverses the diode D_b by DC-link voltage (v_{dc}). Turning on of S_m, facilities discharge of C_r while resonating with L_r and L_{rm} , as shown in Fig. 10(a). As S_m turns on, two kinds of current flow through it. (a) Resonating current, which flows through D_{sa}, C_r, L_r, $L_{rm,}$ and S_m. (b) Linear current, which is proportional to V_{dc}/L_{rm}, flows through the switch. Due to the presence of L_{rm} in series with S_m, the current through switch increases, and diode D_a decrease in linear fashion according to (4). Thus, at $t = t_1$, S_m turns on, and D_a turns off at zero current, as shown in Fig. 10. The expressions of $i_m(t)$, $i_{sa}(t)$, and $v_{cr}(t)$, during Mode 1, are as follows:

$$i_{da}(t) = I_{in} - \frac{V_{dc}}{L_{rm}}(t - t_0) \tag{4}$$

$$i_m(t) = \frac{V_{dc}}{L_{rm}}(t - t_0) + \frac{kV_{dc}}{Z_m}\sin\omega_m(t - t_0) \tag{5}$$

$$i_{sa}(t) = -\frac{kV_{dc}}{Z_m}\sin\omega_m(t - t_0) \tag{6}$$

$$v_{cr}(t) = kV_{dc}\cos\omega_m(t - t_0) \tag{7}$$

$$t_{01} = \frac{I_{in} * L_{rm}}{V_{dc}} \tag{8}$$

Here $\omega_m = \frac{1}{\sqrt{(L_{rm}+L_r)C_r}}$, $\omega_r = \frac{1}{\sqrt{L_rC_r}}$, $Z_r = \sqrt{\frac{L_r}{C_r}}$, $Z_m = \sqrt{\frac{(L_{rm}+L_r)}{C_r}}$, and $k = \frac{v_{Cr}(t_9)}{V_{dc}}$. This mode ends at t_1, where $i_{Da}(t_1) = 0$, $v_{cr}(t_1) < kV_{dc}$, and $i_m(t_1) > I_{in}$.

Mode 2($t_1 < t < t_2$): As shown in Fig. 10(b), diodes D_a and D_b remain off during this mode. Therefore, the resonance established between C_r, L_r and L_{rm}, during Mode-1, continues till the current through S_a falls to zero. Voltage (v_{cr}) across the resonating capacitor continues to decrease and is clamped to $-kV_{dc}$ at the end of this mode. The expressions of $i_m(t)$, $i_{sa}(t)$, and $v_{cr}(t)$, during Mode 2, are as follows:

$$i_m(t) = I_{in} + \frac{kV_{dc}}{Z_m}\sin\omega_m(t - t_0) \tag{9}$$

$$i_{sa}(t) = -\frac{kV_{dc}}{Z_m}\sin\omega_m(t - t_0) \tag{10}$$

$$v_{cr}(t) = kV_{dc}\cos\omega_m(t - t_0) \tag{11}$$

At the end of this mode (Ref. to Fig. 10), $i_m(t_2) = I_{in}$, $i_{sa}(t_2) = 0$, $v_{cr}(t_2) = -kV_{dc}$.

Mode 3 ($t_2 < t < t_3$): The auxiliary circuit is inactive during this mode, as shown in Fig. 10(c). So, this interval is similar to the *DTs* interval of conventional CFSI in which S_m and S_{ST} are carrying current I_{in}. Also, diodes D_a and D_b are off. During this interval, $i_m = I_{in}$, $i_{sa} = 0$, and $v_{cr} = -kV_{dc}$.

Mode 4 ($t_3 < t < t_4$): This mode is initiated with turn-on of the auxiliary switch S_a at t=t_3 as shown in Fig. 10(d). As C_r is charged by $-kV_{dc}$, turning on of S_a provides a path to discharge capacitor C_r. C_r along with inductors L_{rm} and L_r starts resonating through the switches S_a and S_m. Therefore, resonating current (i_{sa}) flowing through the auxiliary switch starts increasing sinusoidally. As i_{sa} increases, the main switch current (i_m) decreases following $i_m = I_{in}$ - i_{sa}. At the end of this mode at t=t_4, the auxiliary switch current reaches $I_{in,}$ and i_m reaches zero. The expressions of $i_m(t)$, $i_{sa}(t)$, and $v_{cr}(t)$, are as follows:

$$i_m = I_{in} - \frac{kV_{dc}}{Z_m} \sin \omega_m (t - t_3) \tag{12}$$

$$v_{cr} = -kV_{dc} \cos \omega_m (t - t_3) \tag{13}$$

$$i_{sa} = \frac{kV_{dc}}{Z_m} \sin \omega_m (t - t_3) \tag{14}$$

At the end of this mode $i_m = 0$, and $i_{sa} = I_{in}$

Mode 5 ($t_4 < t < t_5$): In this mode, i_m becomes negative. Thus, the resonance established between C_r, L_r and L_{rm}, during mode 4, continues through the anti-parallel diode (D_{sm}). At t=t_4, the current through S_m reduces to zero. Now, S_m can be turned off softly. At t=t_5, gate pulses of S_m and S_{ST} are removed. This facilitates the zero current turn-off of the main switch (S_m). However, the turning off of switch S_{ST} forces its current to flow through diode D_b and turns D_b on. Expressions of i_m, i_{sa} and v_{cr} are similar as in mode 4. At the end of this mode, $i_{Db} = I_{in}$ *and* C_r charges with some positive voltage.

Mode 6 ($t_5 < t < t_6$): In this mode, S_m and S_{ST} are off and D_b is on. Here also, the resonance established in mode 4 continues through S_a and D_{sm}. This mode ends at t=t_6, when i_{sa} reaches to $I_{in\ ,}$ and i_m(in this mode flowing through D_{sm}) reaches to zero. Thus, the diode D_{sm} turned off with ZCS at t=t_6. Duration of this mode is,

$$t_{56} = \frac{1}{2\omega_m} \left[\pi - 2\sin^{-1} \left(\frac{I_{in}\, Z_m}{k\, V_{dc}} \right) \right] \tag{15}$$

Mode 7 ($t_6 < t < t_7$): In this mode, S_a and D_b are on, while S_m, S_{ST} and D_a are off. D_a is off due to reverse voltage ($V_{dc} - v_{cr}(t)$) across it, as shown in Fig. 10(g). Therefore, I_{in} flows through the path L_r, C_r, S_a and D_b. As constant current I_{in} flows through C_r, v_{cr} Increases linearly following (16). At t= t_7, v_{cr} gets charged to V_{dc} and diode D_a voltage reduces to zero. Now, the diode D_a gets forward biased and turns on with ZVS. Currents flowing in the converter follow $i_m = i_{ST} = 0$, $i_{sa} = I_{in}$, $i_{Db} = I_{in}$ in this mode. The expression of voltage and the duration of this mode t_{67} are as follows:

$$v_{cr} = \frac{I_{in}}{C_r} (t - t_6) \tag{16}$$

$$t_{67} = \frac{V_{dc}}{I_{in}} * C_r \tag{17}$$

At the end of this mode $i_{sa}(t_7) = I_{in}$ and $v_{cr}(t_7) = V_{dc}$.

Mode 8 ($t_7 < t < t_8$): This mode starts with the turning on of diode D_a. As D_a turns on, it provides a path to resonate C_r and L_r, as shown in Fig. 10(h). i_{Da} increases sinusoidally, which helps in the ZCS turn-on of diode D_a. Simultaneously, the net current through S_a start reducing gradually, and this mode ends when i_{sa} reaches to zero. Expressions of i_{sa}, i_{Da} and v_{cr}, in this mode, are as follows

$$i_{Da} = I_{in} - I_{in} \cos \omega_r (t - t_7) \tag{18}$$

$$i_{sa} = I_{in} \cos \omega_r (t - t_7) \tag{19}$$

$$v_{cr} = V_{dc} + I_{in} Z_r \sin \omega_r (t - t_7) \tag{20}$$

Since this mode ends at i_{sa}=0, the duration of this mode is,

$$\omega_r (t_8 - t_7) = \pi/2 \quad \text{or} \quad t_{78} = \pi/2\omega_r \tag{21}$$

Mode 9 ($t_8 < t < t_9$): At t=t_8, current in S_a starts to flow in the reverse direction to maintain the resonance established in mode 8. As soon as i_{sa} becomes negative, the body diode of S_a i.e., D_{Sa} starts conducting. Gate pulse of S_a can be removed any time after i_{sa} becomes negative to achieve soft switching. After turning off S_a, C_r and L_r continues to resonate through D_a and D_{sa} as shown in Fig. 10(i). This mode ends when i_{sa} reaches zero, and diode D_{sa} turns off softly at zero current. i_{sa}, i_{Da} and v_{cr} follow the same equations as in mode 8. Since this mode ends at i_{sa}=0, the duration of this mode is,

$$\omega_r (t_9 - t_8) = \pi \quad \text{or} \quad t_{89} = \pi/\omega_r \tag{22}$$

At the end of this mode, $i_{sa}(t_9) = 0$, $i_{Da}(t_9) = I_{in}$, $i_{Db}(t_9)$=I_{in}, $v_{cr}(t_9)$= $V_{dc} - I_{in}Z_r$.

Mode 10 ($t_9 < t < t_{10}$): In this mode S_m, S_{ST} and S_a are off. Thus, I_{in} flows through the diodes D_a and D_b. This mode is similar to the *(1-D)* interval of the CFSI. At the end of mode 9 (t=t_9), the resonant capacitor is charged with $V_{dc} - I_{in}$. Thus, it remains charged for the whole *(1-D)* interval. Hence, k is, defined as

$$k = \frac{V_{dc} - I_{in}Z_r}{V_{dc}} \tag{23}$$

Fig. 11 shows that t_3-t_5 is the overlap period of gate pulse G_{sa} and G_{sm}. In this period, current (i_{sa}) in the auxiliary branch changes from 0 to $\frac{kV_{dc}}{Z_m}$. Thus, using (7a), the overlap period (y) is calculated as,

$$y = t_{35} = \frac{1}{\omega_m} \sin^{-1} \left(\frac{\pi I_{in} Z_m}{2kV_{dc}} \right) \tag{24}$$

As explained above, the gate pulse of the auxiliary switch is removed after the current through it reaches zero value. Fig. 11 shows that the current through the auxiliary branch is reduced to zero at t_8. Thus pulse width, x is,

$$x = t_{35} + t_{56} + t_{67} + t_{78} \tag{25}$$

Here, t_{35}, t_{56}, $t_{67,}$ and t_{78} intervals are given in (24), (15), (17), and (21), respectively. Values of overlap period (y) and pulse width (x) are used to decide the phase shift ϕ and DC signal V_a, as given in (3).

In the proposed ZCS-CFSI topology, ZCS turn on and turn off of S_a and S_m, respectively, are achieved while moving from ST to NST state and NST to ST state. However, diode D_a is

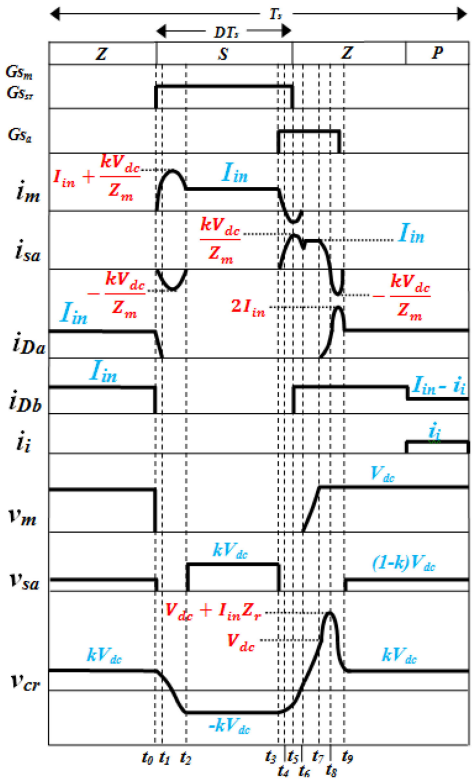

FIGURE 11. Ideal waveform of the proposed converter.

turned on and off with ZVS and ZCS, respectively. Since the soft switching of the devices occurs either at zero current or zero voltage, the switching loss of the boost stage of CFSI reduces, and the efficiency increases.

D. STEADY-STATE GAINS

The addition of an auxiliary circuit for soft switching of switch S_m results in a change of dc gain of the CFSI converter. The dc gain ($\frac{V_{dc}}{V_{in}} = M_{dc}$) of the converter is obtained by applying volt-second balance on the input inductor (L_{in}),

$$V_{in}.t_{01} + (V_{in} + V_{dc})(DT_s - t_{01}) + V_{in}.t_{56} + \left(V_{in} - \frac{I_{in}}{2.C_r}.(t_{67})\right)t_{67} + (V_{in} - V_{dc})t_{79} = 0$$

$$\frac{V_{dc}}{V_{in}} = M_{dc} = \frac{1}{(1-2D) + \frac{\left(t_{01} - \frac{t_{67}}{2} - t_{56}\right)}{T_s}} \tag{26}$$

Here, t_{01}, t_{56} and t_{67} and are duration of mode 1, mode 6 and mode 7 respectively, as discussed earlier. The dc gain of the proposed topology has an additional term compared to the dc gain of CFSI, as given by (2a). This additional $(= (t_{01} - (t_{67}/2) - t_{56})/T_s)$. The value of this term is negative, resulting in slightly higher dc gain compared to CFSI topology, as shown in Fig. 12. The Fig. 12 is plotted for same values components as mentioned in the Table 2.

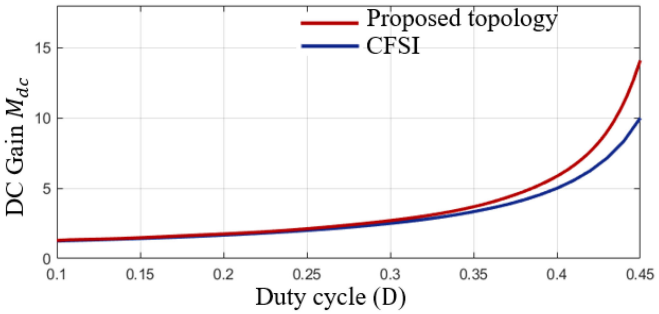

FIGURE 12. Comparison of dc gain between CFSI and proposed topology.

TABLE 1. Device Specifications for Experimental Prototype

Component	Attributes
Switches S_1 to S_4	STGY40NC60VD
Main switch S_m	STGY40NC60VD
Diodes D_a and D_b	C3D10060
Auxiliary switch S_a	C3M0120090D
Gate Driver	FOD3120 (Fairchild)

TABLE 2. Parameters Selected for CFSI

Parameter	Attributes	Parameter	Attributes
Input Inductor (L_{in})	1.2 mH	Resonating inductor (L_r)	8 μH
DC link Capacitor (C_o)	440 μF	Resonating inductor (L_{rm})	1.5 μH
Bleeder Resistor (R_{dc})	20 $k\Omega$	Resonating Capacitor (C_r)	34 nF
Filter inductor (L_f)	700 μH	main switch frequency (f_s)	30 kHz
Filter Capacitor (C_f)	25 uF	Carrier frequency (f_{tri})	15 kHz

The value of the peak ac output voltage ($=\hat{V}_{ac}$) is given by,

$$\frac{\hat{V}_{ac}}{V_{in}} = MM_{dc} = \frac{M}{(1-2D) + \frac{\left(t_{01} - \frac{t_{67}}{2} - t_{56}\right)}{T_s}} \tag{27}$$

Here, M is the modulation index and M_{dc} is dc gain given by (26). The value of peak ac voltage ($=\hat{V}_{ac}$) is proportional to the voltage V_{dc}. Therefore, traditional inverter control schemes can be utilized for the proposed topology.

E. STEADY-STATE LOSS ANALYSIS

The ZCS-CFSI has some additional components compared to a CFSI topology. These components reduce switching losses of the circuit with the introduction of some additional conduction losses. The loss analysis is performed in following discussion. During this analysis, the losses occurring in inverter bridges are neglected as this stage is similar in both CFSI and ZCS-CFSI topologies. A detailed discussion of losses in CFSI topology is available in literature [29]. Here, conduction losses occurring in the input inductor are,

$$W_{c,Lin} = I_{in,r}^2 r_L \tag{28}$$

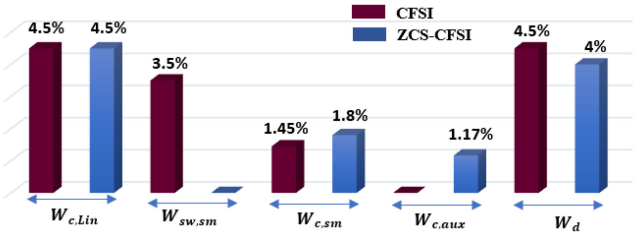

FIGURE 13. Loss breakdown of the CFSI converter and proposed topology.

Where, r_L is resistance of the input inductor and $I_{in,r}$ is root mean squared (rms) current of the input side. This loss remains the same in both CFSI and ZCS-CFSI topologies. However, the switching loss of the main switch is present only in the CFSI converter. The switching losses are given by,

$$W_{sw,sm} = 0 \text{ forZCS} - \text{CFSI} \tag{29a}$$

$$W_{sw,sm} = I_{in}V_{dc}f_s\left(t_{con} + t_{coff}\right), \text{ for CFSI} \tag{29b}$$

Here, t_{con} and t_{coff} are respectively turn on and turn off time of the main switch and are available in datasheet. While, the conduction loss ($W_{c,sm}$) of the main switch is higher in ZCS-CFSI as for a part cycle (during t_{20} and t_{63}) the main switch carries an extra current of auxiliary circuit, as shown in Fig. 11. The conduction loss in main switch is given by,

$$W_{c,sm} = I_{sw,r}^2 r_{dson} \tag{30}$$

Where, $I_{sw,r} = \sqrt{I_{in}^2 D + \left(\frac{kV_{dc}}{2Z_m}\right)^2 (t_{02} + t_{36})f_s}$

Here, the current $I_{sw,r}$ is the rms value of switch current and r_{dson} is the resistance of the main switch during conduction time. The duration t_{02} is time interval between instants t_2 and t_0, as discussed earlier. Similarly, another interval t_{36} is time can be defined. A comparison of different losses is given in Fig. 13 with same components as mentioned in Table 2.

Similarly, the conduction loss ($W_{c,aux}$) of the auxiliary circuit can be calculated. This loss is relatively lesser as the auxiliary switch S_a conducts for a lesser interval in a switching cycle and the inductive coils used in auxiliary circuit have very small resistance. This loss is,

$$W_{c,aux} = I_{aux,r}^2 r_{aux} \tag{31}$$

Where, $I_{aux,r} = \sqrt{\left(\left(\frac{kV_{dc}}{2Z_m}\right)^2 (t_{20} + x - t_{67}) + I_{in}^2 t_{76}\right)f_s}$

The conduction losses occurring in diodes are approximated by,

$$W_d = W_{da} + W_{db} \tag{32}$$

Where, $W_{da} = (1-D)I_{da}V_f + I_{da,r}^2 r_d$ and $W_{db} = (1-D)I_{in}V_f + I_{in}^2 r_d$. The value of I_{da} and $I_{da,r}$ are given by,

$$I_{da} = I_{in}\left(1 - D - t_{93}f_s\right) + \frac{2kV_{dc}}{\pi Z_r}t_{97}f_s \tag{33}$$

$$I_{da,r} = \sqrt{I_{in}^2\left(1 - D - t_{93}f_s\right) + \left(\frac{2kV_{dc}}{2Z_r}\right)^2 t_{97}f_s} \tag{34}$$

In the next section, the design aspects of resonating elements are discussed. Also, the effects of the parametric variation of the resonating components on the converter's performance are discussed in detail.

IV. DESIGN PROCEDURE OF RESONANT ELEMENTS

Design of resonant components is very essential to achieve soft switching of CFSI. According to different modes discussed in Section II, there are three constraints which should always be satisfied to ensure soft switching.

(a) ZCS turn off of the main switch is achieved by reducing i_m to zero or negative. Therefore, components of the auxiliary circuit should be designed so that it injects current higher than the current flowing through the main switch (ref to Mode-3). Therefore, the peak current (i_{sa}^{peak}) through the auxiliary branch, during t_3 to t_6 interval, must be greater than the main switch current, which is given as follows.

$$i_{sa}^{peak} > I_{in}$$

From Fig. 11 and (14), the above relation can be expressed as,

$$\frac{V_{dc} - I_{in}Z_r}{Z_m} > I_{in}$$

Solving for L_r using (8) we obtained,

$$L_r < \frac{C_r}{4}\left(\frac{V_{dc}}{I_{in}}\right)^2 + \frac{1}{4C_r}\left(L_{rm}\frac{I_{in}}{V_{dc}}\right)^2 - \frac{1}{2}L_{rm} \tag{35}$$

(b) As discussed above, to achieve ZCS of the main switch, the auxiliary circuit has to be turned on before the turn-off instant of the main switch. But the auxiliary circuit's turn-on period (t_3-t_9) should be small enough not to affect the converter's regular operation. The sum of linear and resonating intervals is chosen to be less than 10% of the switching period. Thus, using (9), (10), and (11), we get,

$$\frac{C_r V_{dc}}{I_{in}} + \frac{3\prod\sqrt{L_r C_r}}{2} + \sqrt{L_r C_r}\sin^{-1}\frac{I_{in}Z_m}{V_{dc} - I_{in}Z_r} \leq 0.1T_s \tag{36}$$

It is to be observed that t_6-t_7 is the linear interval where the C_r charges linearly with a constant current I_{in}. This occurs after the turn-off of the main switch. Thus, this linear interval should be very low such that the NST interval operation remains unaffected. So, we start by taking a linear interval of 0.5% of the switching period while designing Cr. Then, if (36) is not satisfied, we increase C_r in the step of 10% until (36) is satisfied.

(c) During the turning-off of D_a, L_{rm} comes in series with diode D_a and helps in reducing the reverse recovery losses of diode D_a. Series inductor L_{rm} helps to reduce the di/dt of the diode and hence Q_{rr} (=function of di/dt). However, this also reduces the operating duty cycle and hence the gain of the converter. So, L_{rm} is designed such that the transition of the diode must be less than 5% of the duty cycle during turning

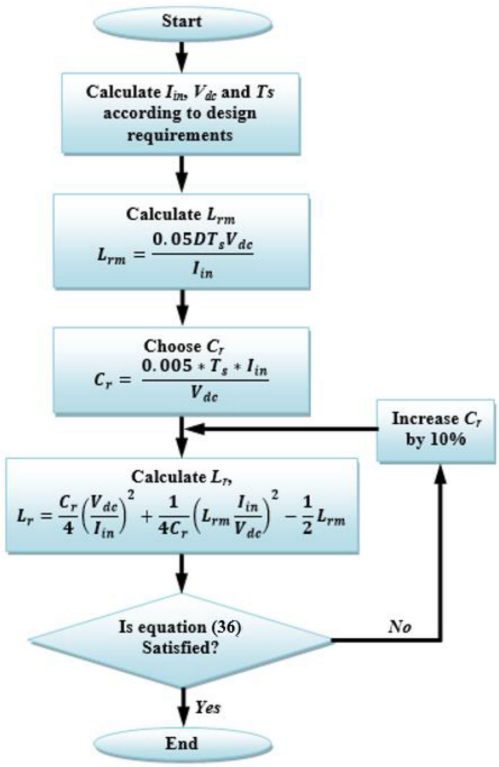

FIGURE 14. Flow Chart to design resonating elements.

off. Thus, we get,

$$L_{rm} \leq \frac{0.05DT_sV_{dc}}{I_{in}} \tag{37}$$

Fig. 14 shows the flow chart for designing the resonant components. L_{rm} is calculated first for the required load and switching frequency using (37). Then, C_r is calculated. Then, considering 0.5% of the calculated value of C_r, L_r is calculated using (35). Finally, these calculated values are checked by putting in (36). If (36) is satisfied, then only the design is finalized.

Based on the design procedure, the resonating components are determined, which are given in Table 2. Since the deterioration in L_r, C_r, and L_{rm} affects the soft switching, a safety margin is considered in the final design.

The current waveform of the main switch is plotted with variations in components to observe ZCS performance. For observation purposes, the circuit parameters are taken as : I_{in}=9A and V_{dc}=290 V. In Fig. 15(a), i_m is plotted during the turn-off transition of S_m with the variation of L_r, $L_{rm,}$ and C_r. The auxiliary circuit provides a turn-off with zero current (ZCS) for a particular set of values of auxiliary circuit components (L_{rm}= 4 μH, L_r= 4 μH, and C_r = 35 nF). However, these values of parameters do not result in the ZVS turn-off of the main switch. As shown in Fig. 15(b), these values of the components results in lesser peak and rms current of main switch, so conduction losses and peak current rating of main switch are also lesser. Moreover, the design of the circuit can be modified to achieve ZVS during turn-off. For example, the auxiliary circuit components with L_{rm} =2 μH, L_r = 5 μH, and C_r = 45nF results in a negative current at the instant of turn-off, so switch can be turned off with ZVS.

The duration for which the main switch current (i_m) is negative is zero current switching's (ZCS) time window. The plot shows that the peak of the main switch current increases due to the increase in C_r and decrease in L_r and L_{rm}

Similarly, Fig. 15(b) shows the plot of i_m during turning on the main switch. In this duration, the resonating capacitor resonates with L_{rm} and L_r through S_m and $D_{sa,}$ as explained in Mode 1 and 2. It is noted that peak current through the main switch increases by choosing a large value of C_r and smaller values of L_{rm} and L_r. The peak in switch current occurs only during the transition and for a concise duration.

Fig. 15(c) shows the voltage stress on C_r due to variation in resonating components. The variation of resonating components does not affect the voltage stress much. But, it can be seen that at higher values of C_r, the diode D_a turns on a little later and reduces the duty cycle effectively. It is also noted that, for every plot, the clamped value of v_{cr} is different due to the different combinations of resonating components.

Thus, from the above observations, it is concluded that much higher and much lower values of resonating components affect the gain relationship and also would not help improve efficiency. Hence, components are designed considering 10% tolerance in the parameters. Such that it doesn't affect the regular operation of ZCS-CFSI. As shown in Fig. 16, the ZCS region follows design rules mentioned earlier and parameter values from Table 2.

V. SIMULATION AND EXPERIMENTAL RESULTS

A laboratory prototype of ZCS-CFSI, as shown in Fig. 17, is developed to verify the soft switching of CFSI and compare their efficiency with different PWM schemes. The experimental setup is also replicated in PSPICE simulating software to verify the results. All the non-idealities and parasitic components such as parasitic capacitance, PCB track inductance, DCR of inductors, ESR of capacitors, and device non-idealities are included. A list of switching devices and their drivers is given in Table 1. The parameters and specifications used in the experiment and simulation are shown in Table 2, respectively. Soft switching of CSFI is tested at V_{in}=56 and v_{ac}= 110 V (RMS).

Fig. 18(a) shows the simulation results and Fig. 18(b) depicts the experimental waveforms of the main switch during ZCS-turn off and turn on. In this, a resistive load of 300 W is connected at the inverter output terminal, and DC-link voltage is kept at 280 V. Turning on of S_a activates the resonating branch to resonate through the main switch. The resonating current forces the main switch current to zero (approximately); afterward, the voltage across the switch starts rising. through the main switch.

The auxiliary switch (S_a) undergoes soft-switching transitions, as shown in Fig. 19(a) and Fig. 19(b). L_r and C_r in series with the S_a, support the auxiliary switch turned on and

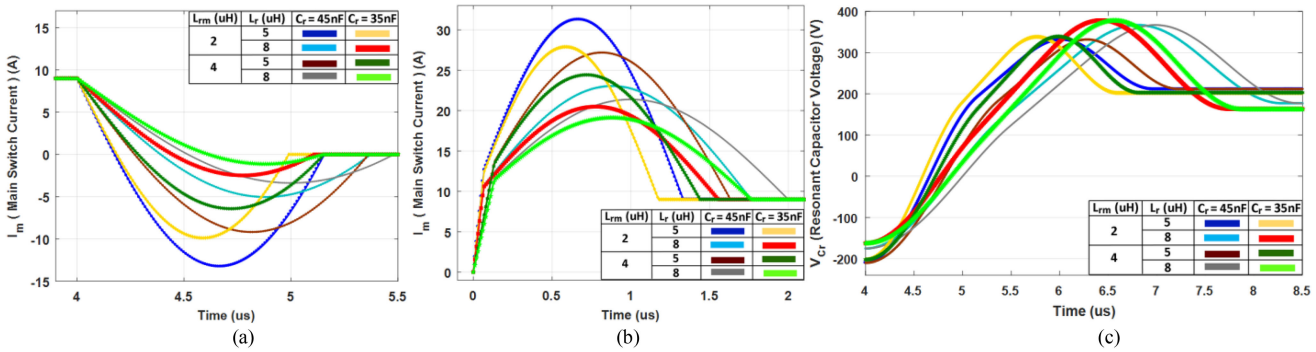

FIGURE 15. Variation of (a) ZCS window available for S_m to get turned off under zero current switching, (b) peak current of main switch S_m and (c) peak voltage of resonating capacitor V_{cr}, with different value of resonating components.

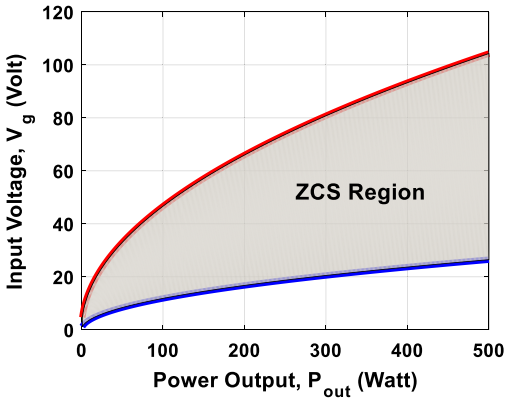

FIGURE 16. Operating region of CFSI with the variation of input voltage and output power to achieve soft switching.

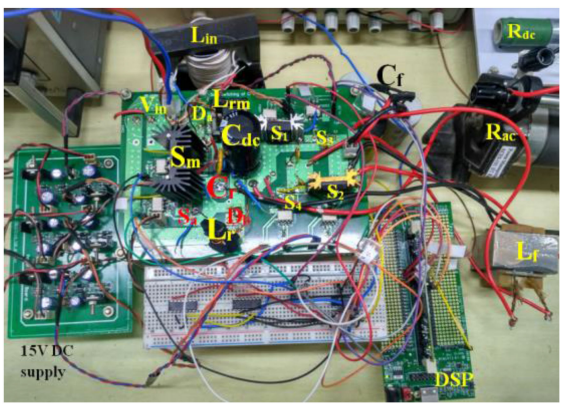

FIGURE 17. Laboratory prototype of ZCS-CFSI.

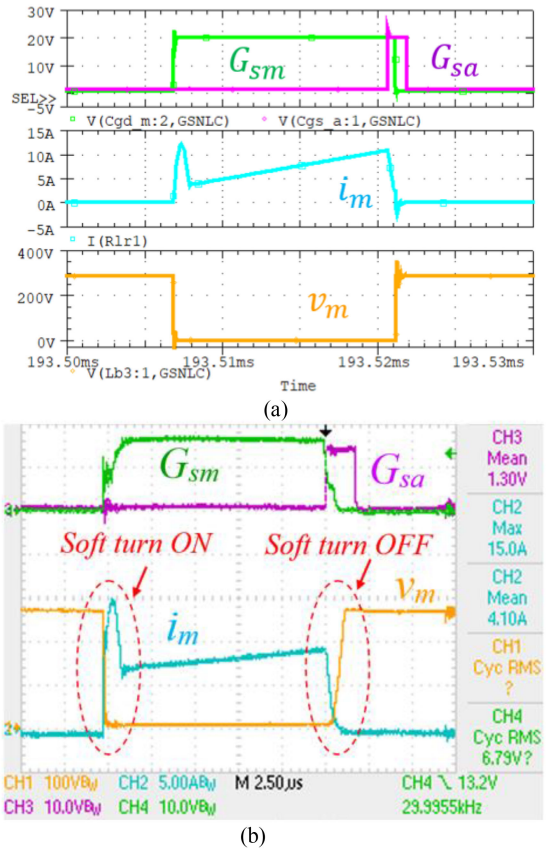

FIGURE 18. Gate pulses of main and auxiliary switches along with current and voltage waveform of S_m during ZCS turn on and turn off. (a) PSPICE simulation Results. (b) Experimental Result.

off softly. S_a is turned on for a very small interval because it is operated only to turn off the main switch, as shown in Fig. 19(b). Thus, the increase in loss (including driver loss), in the auxiliary branch is significantly lower as compared to the reduction in switching loss of the main switch.

Similarly, the operation of the ZCS-CFSI is verified by operating the converter at 450 W. Fig. 20(a) and (b) show that the transition of main switch occurs at zero voltage and current. Also, to reduce overall losses, the auxiliary switch is turned on and off softly, as shown in Fig. 21(a). This verifies the ZCS operation as discussed in theory. Fig. 21(a) also shows the voltage waveform across the resonating capacitor (v_{cr}). It depicts that the magnitude of v_{cr} changes only during transitions.

Fig. 21(b) shows the steady-state current and voltage waveforms at the input and output sides of the ZCS-CFSI. Here, 110 V output voltage is obtained from 56 V input DC source, and a load of 450 W is connected. It shows that

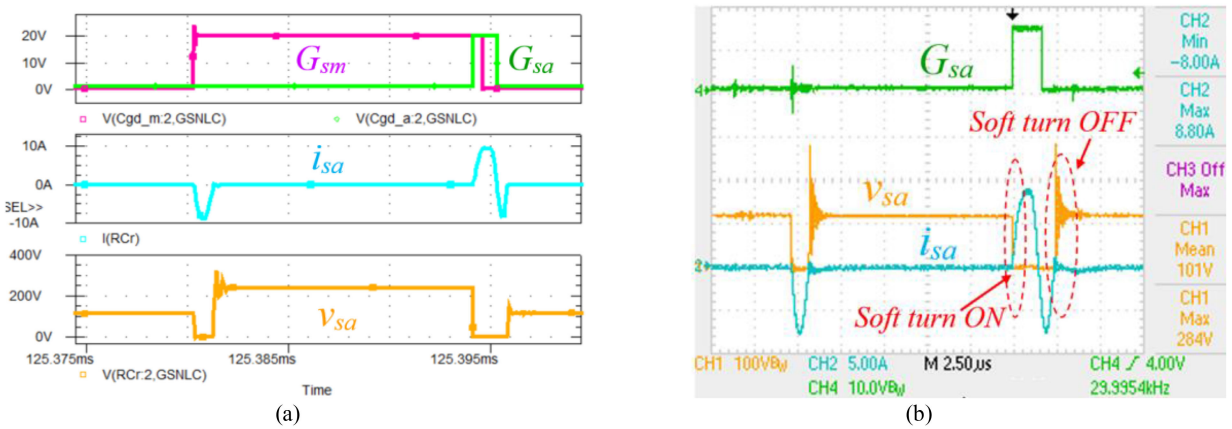

FIGURE 19. Gate pulses of the main and auxiliary switches along with current and voltage waveform of S_a during ZCS turn on and turn off. (a) PSPICE simulation Result, (b) Experimental Result.

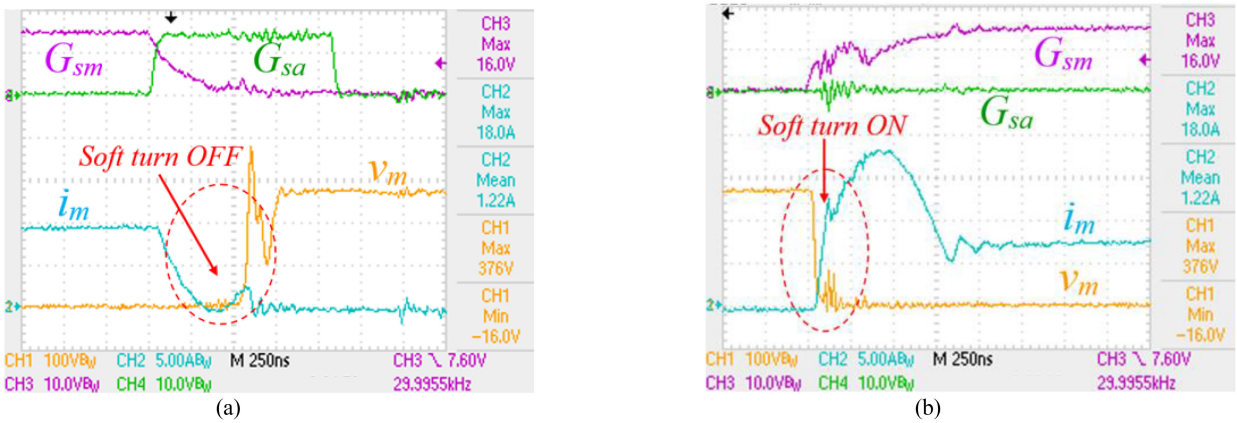

FIGURE 20. Current and Voltage waveform of main switch during (a) turning off and, (b) turning on at the output power of 450 W.

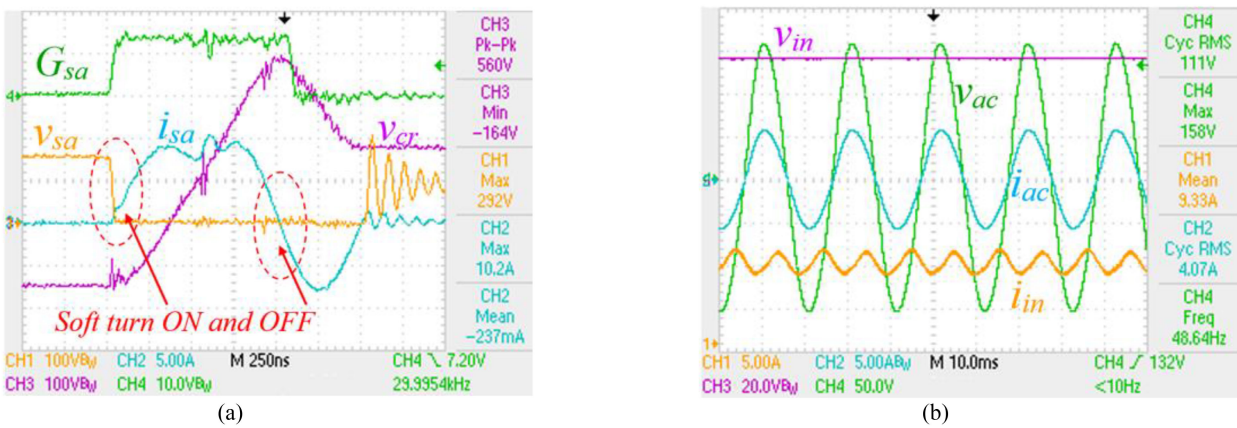

FIGURE 21. (a) Current and Voltage waveform of auxiliary switch during turn on and off, (b) Experimental waveforms of input voltage (V_{in}), input current (I_{in}), output AC voltage (V_{ac}) and output AC current (i_{ac}) of ZCS-CFSI at the output power of 450 W.

the auxiliary circuit is not affecting the regular operation of CFSI.

The efficiency curve of CFSI and ZCS-CFSI with the SBC scheme is verified experimentally and is shown in Fig. 22 for the full range of load. It is observed that the converter's efficiency is increased by 2% at 450 W load. The experimental results are in line with the calculation. The difference in results is attributed to losses in inductor core and parasitic, which are not considered in theory. The measured THD of the load current shows a marginal improvement from

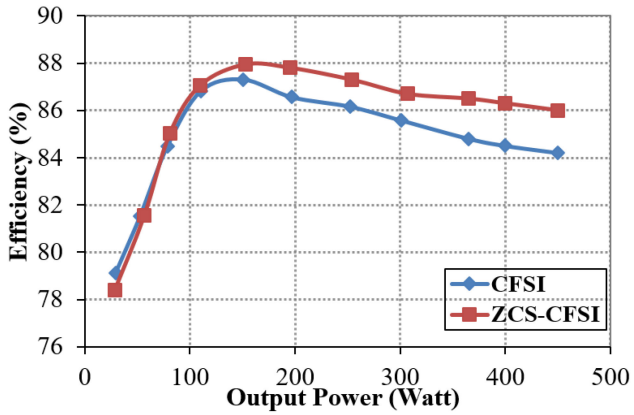

FIGURE 22. Measured Efficiency of CFSI and ZCS-CFSI with Scheme-1.

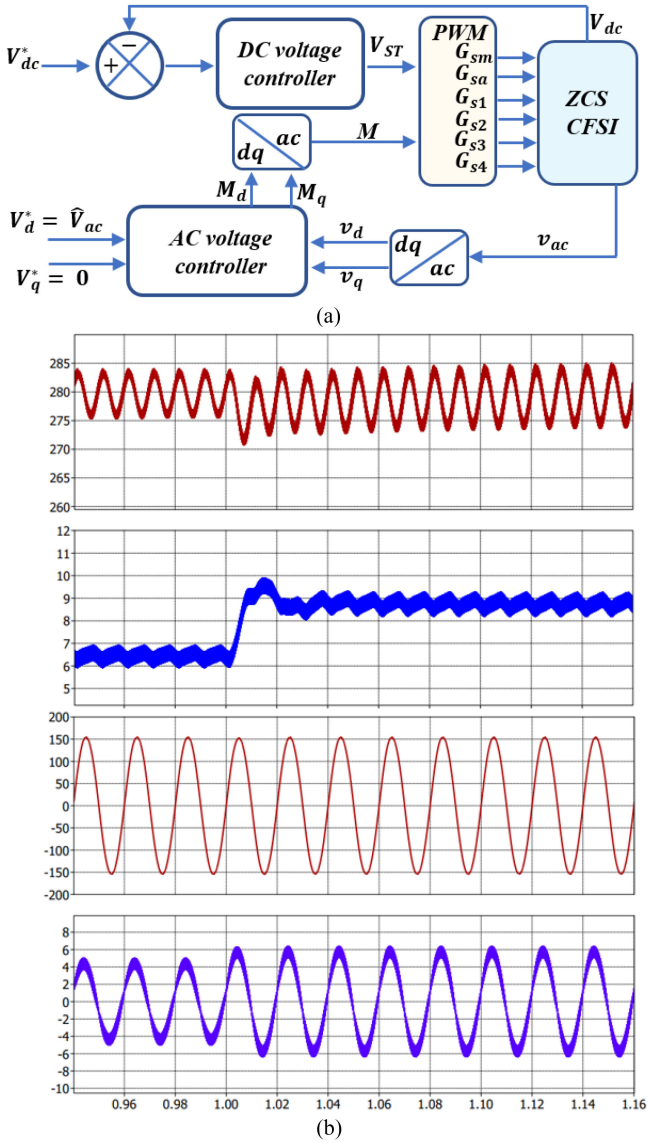

FIGURE 23. PLEXIM simulation of closed loop operation of ZCS-CFSI (a) block diagram representation (b) waveforms under a step load change.

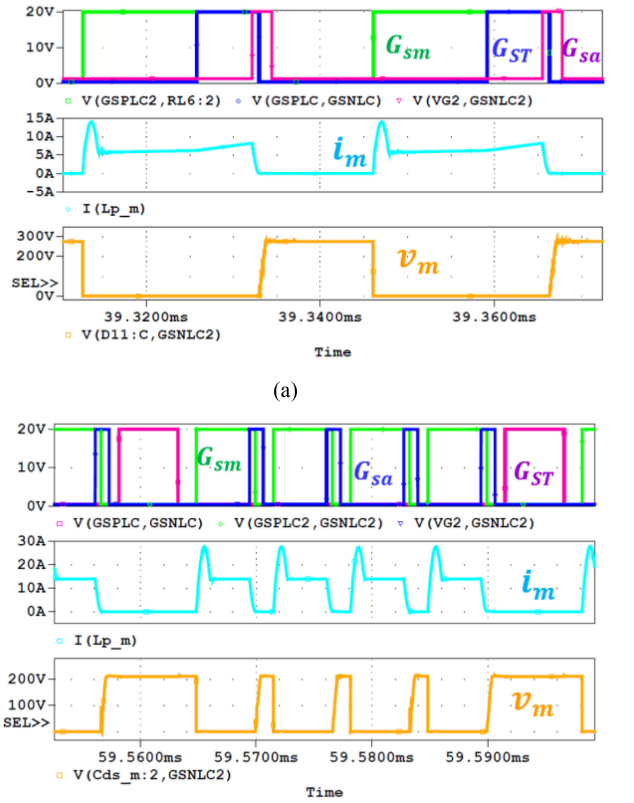

FIGURE 24. Verification of ZCS-CFSI with (a) Scheme-2, and (b) Scheme-6 discussed in Section II.

3.18% to 3.13% due to a decrease in the switching frequency component in the DC link voltage due to switching frequency.

The proposed topology is simulated for closed-loop operation in PLEXIM software. Fig. 23(a) shows the block diagram of the closed-loop implementation. Here, independent controllers separately control the dc voltage (V_{dc}) and ac peak voltage ($\hat{V}_{ac}$). The modulation index M is used as a control variable for modulating the voltage $\hat{V}_{ac}$. The output voltage v_{ac} is sensed and transformed into dq domain to act as input of the controller. The controller generates Md and Mq as modulation signal. Then, the inverse dq transformation is applied to obtain modulation index (M). The modulation index (M) is used to decide non-shoot through (non-ST) interval. A load step change of 1 A is introduced at t = 1s, resulting in an increase in input current. However, the controller regulates the peak ac voltage at 155 V, as shown in Fig. 23(b).

Section II discusses the operation of the CFSI in the different PWM schemes to improve the modulation index. Moreover, the converter is operated through PWM scheme-I for verification through simulation and experiment. As the auxiliary circuit integrated to achieve soft-switching operates for a small fraction of the switching cycle, the same soft-switching technique is equally applicable to other schemes. The soft-switching operation in remaining PWM schemes is

verified through PSpice simulation, and the results are shown in Fig. 24.

VI. CONCLUSION

In this paper, to improve the efficiency, the conventional topology of CFSI is modified by adding an auxiliary circuit. A new PWM scheme for the modified topology is proposed. The operating principle and different modes associated with the new PWM scheme are discussed in detail. Designing the auxiliary branch's parasitic components is explicitly discussed, and its effect on the variation of soft switching is examined. A lab prototype of ZCS-CFSI is built to validate the theoretical analysis. The efficiency of ZCS-CFSI is also compared with different PWM schemes. It is observed that the efficiency of the modified CFSI is improved by 2% at 450 W. From the detailed discussion, it has been concluded that the new topology has the potential to emerge as an efficient and high-power density solution for all inverter-based systems.

REFERENCES

[1] J. T. Bialasiewicz, "Renewable energy systems with photovoltaic power generators: Operation and modeling," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2752–2758, Jul. 2008.

[2] Fang Zheng Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[3] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

[4] R. Adda, O. Ray, S. K. Mishra, and A. Joshi, "Synchronous-reference-frame-based control of switched boost inverter for DC nanogrid applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1219–1233, Mar. 2013.

[5] S. S. Nag and S. Mishra, "Current-fed switched inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4680–4690, Sep. 2014.

[6] M. K. Nguyen, T. V. Le, S. J. Park, and Y. C. Lim, "A class of quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.

[7] A. V. Ho, T. W. Chun, and H. G. Kim, "Extended boost active-switched-capacitor/switched-inductor quasi-Z-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5681–5690, Oct. 2015.

[8] A. Gambhir, S. Mishra, and A. Joshi, "A modified PWM scheme to improve performance of a single-phase active front end impedance source inverter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 928–942, Jan./Feb. 2019.

[9] M. Nguyen and Y. Choi, "PWM control scheme for quasi-switched-boost inverter to improve modulation index," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4037–4044, May 2018.

[10] M. Nguyen, T. Tran, and Y. Lim, "A family of PWM control strategies for single-phase quasi-switched-boost inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1458–1469, Feb. 2019.

[11] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Dordrecht, Netherlands: Kluwer Academic Publishers Group, 2001.

[12] M. Nguyen, Y. Lim, and S. Park, "A comparison between single-phase quasi-Z-source and quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6336–6344, Oct. 2015.

[13] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, Dec. 1995.

[14] K. D. T. Ngo, "Analysis of a series resonant converter pulse width-modulated or current-controlled for low switching loss," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 55–63, Jan. 1988.

[15] G. Buja, M. Bertoluzzo, and K. N. Mude, "Design and experimentation of WPT charger for electric city car," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7436–7447, Dec. 2015.

[16] S. Samanta and A. K. Rathore, "Small-signal modeling and closed-loop control of a parallel–series/series resonant converter for wireless inductive power transfer," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 172–182, Jan. 2019.

[17] V. Vorperian, "Quasi-square-wave converters: Topologies and analysis," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 183–191, Apr. 1988.

[18] J. Kwon, W. Choi, and B. Kwon, "Single-switch quasi-resonant converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1158–1163, Apr. 2009.

[19] L. H. S. C. Barreto, E. A. A. Coelho, V. J. Farias, J. C. de Oliveira, L. C. de Freitas, and J. Joao Batista Vieira, "A quasi-resonant quadratic boost converter using a single resonant network," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 552–557, Apr. 2005.

[20] E. Jayashree and G. Uma, "Analysis, design and implementation of a quasi-resonant DC-DC converter," *IET Power Electron.*, vol. 4, no. 7, pp. 785–792, Aug. 2011.

[21] D. Yogi, A. Gambhir, and S. Mishra, "Zero current switching of CFSI using auxiliary circuit," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst.*, Chennai, India, 2018, pp. 1–6.

[22] J. J. Jafar and B. G. Fernandes, "A new quasi-resonant DC-link PWM inverter using single switch for soft switching," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 1010–1016, Nov. 2002.

[23] S. Mandrek and P. J. Chrzan, "Quasi-resonant DC-link inverter with a reduced number of active elements," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2088–2094, 2007.

[24] Y. Zhu, M. Chen, X. Lee, and Y. Tsutomu, "A novel quasi resonant soft-switching Z-source inverter," in *Proc. IEEE Int. Conf. Power Energy*, Kota Kinabalu, 2012, pp. 292–297.

[25] A. Mousavi and G. Moschopoulos, "A new ZCS-PWM full-bridge DC–DC converter with simple auxiliary circuits," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1321–1330, Mar. 2014.

[26] M. L. Martins, J. L. Russi, H. Pinheiro, J. R. Pinheiro, H. A. Grundling, and H. L. Hey, "Unified design for ZVT PWM converters with resonant auxiliary circuit," in *IEE Proc. - Electric Power Appl.*, vol. 151, no. 3, pp. 303–312, May 2004.

[27] X. Ding, H. Yuan, C. Zhang, and J. Zhang, "Soft-switching Z-source inverters with coupled inductor," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, 2014, pp. 2359–2363.

[28] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation For Power Converters: Principles and Practice*. Piscataway, NJ, USA: IEEE Press, 2003.

[29] S. Acharya and S. K. Mishra, "Interleaved current-fed switched inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7015–7030, Jul. 2020, doi: 10.1109/TPEL.2019.2954616.