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Grid Impact of Electric Vehicle Fast Charging Stations: Trends, Standards, Issues and Mitigation Measures - An Overview

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ABSTRACT With growing concern on climate change, widespread adoption of electric vehicles (EVs) is important. One of the main barriers to EV acceptance is range anxiety, which can be alleviated by fast charging (FC). The main technology constraints for enabling FC consist of high-charging-rate batteries, high-power-charging infrastructure, and grid impacts. Although these technical aspects have been studied in literature individually, there is no comprehensive review on FC involving all the perspectives. Moreover, the power quality (PQ) problems of fast charging stations (FCSs) and the mitigation of these problems are not clearly summarized in the literature. In this paper, the state-of-the-art technology, standards for FC (CHAdeMO, GB/T, CCS, and Tesla), power quality issues, IEEE and IEC PQ standards, and mitigation measures of FCSs are systematically reviewed.

INDEX TERMS Charging stations, electric vehicles, power quality, power system stability.

I. INTRODUCTION

Growing concern about climate change intensifies the trend towards decarbonization and interest in clean technology. As a substitute for internal combustion engine vehicles (ICEVs), EVs powered by renewable electricity, can reduce petroleum usage and greenhouse emission [1], [2]. Besides, new technologies on the powertrain of EVs, e.g., wide-band-gap-component based motor drive that improves battery-to-wheel efficiency [3], make EVs more competitive on energy saving.

The convenience of EV recharging significantly influences EV adoption and utilization. The charging power level is generally categorized into two classes - the slow charging and the FC. Typically, the former signifies the distributed charging at home, and public destinations, with the power rated lower than the maximum household power (e.g., 22 kW in European Union and 19 kW in the United States [4]). On the contrary, fast chargers have a higher power rating and are typically used in FCSs. The charging modes are standardized in IEC 61 851-1 [5] and SAE J1772 [1], according to the type of the input current (AC or DC) and the power level. In IEC 61 851-1, four charging modes are defined, where Mode 1, 2, and 3 are the AC charging mode and Mode 4 is DC charging mode. Moreover, only Mode 3 and 4 support the FC. In SAE J1772, the EV charging is classified as three levels, where Level 1 and 2 are the slow charging via AC on-board chargers (OBCs), and Level 3 is the FC via DC off-board charger. Due to the space and weight constraints of the AC OBC, it has a limited maximum power rating, e.g., 43 kW for Mode 3 in IEC 61 851-1. Thus, the mainstream FC is through the DC off-board charger that potentially offers higher charging power. For simplicity, the DC FC is referred to when FC is mentioned in this paper.

For most daily charging events, the energy demand can be satisfied by the overnight slow charging, whose grid impact is well studied [6]–[8]. Besides, slow charging also shows the features of an extended charging period and a wide distribution area, allowing for distribution system operators (DSOs) on planning and regulation. With the topologies allowing

bi-directional energy flow [9], [10], the vehicle-to-grid (V2G) function is developed to not only minimize the grid impacts of EV charging but also provide grid support, e.g. load balancing, frequency and voltage regulation [11]–[14].

For a better recharging experience for the EV drivers, the recharging time of EV at FCSs needs to be comparable to the refueling time of ICEVs. Hence, the power of FC keeps increasing in the past years. To distinguish with FC (rated at 50 kW), the state of art multi-hundred-kilowatt charging is named ultra-fast charging (UFC), which is gaining more attention in recent years [15]. Meanwhile, the FCSs also bring challenges to the grid. An FCS is essentially a power electronics-based grid. Like other counterparts, e.g., wind farms [16] and PV farms [17], FCSs' power quality and stability issue might occur. Moreover, FCS is a pulse load, which is an even more severe scenario than the intermittent renewables. Actually, a few power quality issues in terms of voltage imbalance, flicker, harmonics, supraharmonics, etc. [18], [19], have been reported, where the FCSs are seen as prime suspects.

Although the installation of FCS increases dramatically, it is still an emerging load to the power grid. The PQ standards dedicated to the FCS do not exist yet, without which the PQ assessment at FCSs is challenging. Nonetheless, referring to the IEEE PQ standards [20]–[23] and IEC 61 000 series [24]–[32], which are widely used, can be a feasible approach. In general, the power quality issues can be categorized into voltage level, voltage fluctuation, voltage unbalance, harmonic current distortion, harmonic voltage distortion, etc.

To fulfill these PQ standards, a few mitigation measures have been proposed or even applied in the industry. Tan *et al.* [33] propose a real-time charging navigation framework to overcome the impact of FCSs on voltage stability. Zhao *et al.* [34] propose a management method for FCS operators to regulate the EV's charging behavior. Energy storage systems (ESSs) can also be integrated into FCS to compensate for the pulsating charging load and reduce the required FCSs' grid connection capacity. A few studies have been done regarding the ESS sizing [35], and the power flow control of the ESS [36], [37]. For harmonic mitigation, the methods mainly include filter design with various damping methods [38], [39] and control. For the latter, the impedance-based approach is one of the very promising ones [16], [40]–[47], especially if several converters are connected in parallel in a weak grid, which is likely the FCS scenario. Much research has been done regarding the impedance modeling [43], [45] and shaping [41], [46], [47] for the fast charger's front end converter.

The rest of the paper is organized as follows. In Section II, the trend of FC, the state-of-the-art standards, and batteries and infrastructures for FC are investigated. Then, a survey on the measured and estimated PQ problems brought by FCSs is presented in Section III. The PQ standards, with which the performance of FCSs can be assessed, from IEEE and International Electrotechnical Commission (IEC) are reviewed and summarized in Section IV. The PQ issues' mitigation measures are then presented in Section V. The paper is concluded in Section VI.

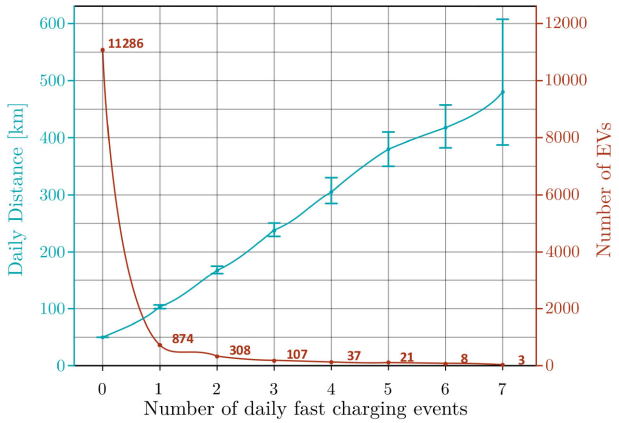


FIGURE 1. The relation between the daily distance traveled and the number of the FC events [48].

II. TRENDS OF FAST CHARGING

A survey [48] was done in 2017, revealing that most EVs only travel short distances and mainly rely on home charging. However, the survey also reflects a positive correlation between EV's daily driving distance and the number of FC events, as illustrated in Fig. 1. The same conclusion remains when the scope is per week. Such a positive correlation indicates that FC is needed for the EV drivers for long-distance trips. To alleviate the users' range anxiety and encourage them to use EVs for long-distance trips, many FC facilities have been installed in the past years, by EV manufacturers (e.g., Tesla) or energy companies (e.g., Shell).

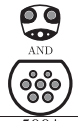
A. ULTRA-FAST CHARGING IS COMING

With the rollout of EVs, the total energy demand for EVs is expected to grow dramatically. The trend of energy demand for EV in the three primary markets is shown in Fig. 2(a) [51]. More specifically, although the slow ac charging will keep its dominant share through 2030, the penetration of DCFC will increase very significantly, as seen in Fig. 2(b).

Right now, the DC fast charger (DCFC) typically rates at 50 kW [52], which is developing towards ultra-fast charging. The average battery capacity of the mainstream EVs in the market is 60.1 kWh (317 km average range) [53]. Unlike the overnight-slow charging, 15-minute charging time is the maximum acceptable to most drivers during traveling [54]. To charge EVs in 15 minutes, the required power for various EV models [53] in the market is listed in Table 2. As seen, the desired charging power for the long-rang EV can reach up to 228 kW. The charging power can further increase as the battery capacity is increasing. In fact, 350 kW DCFC has already been developed [55] to meet the demand shortly.

Meanwhile, the FC standards are also in fast development to support UFC. The widely adopted FC standards comprise CCS (defined by EU), CHAdeMO (defined by Japan), and GB/T (defined by China), among which the CCS has Type 1 for the North American market and Type 2 for Europe and

TABLE 1. Status of FC standards [2], [49], [50]

Standard	CHAdeMO	GB/T	CCS Type 1	CCS Type 2	Tesla	ChaoJi
Compliant Standards	IEEE 2030.1.1 IEC 62916-3	IEC 62916-3	SAE J1772 IEC 62916-3	IEC 62916-3	No related items	CHAdeMO and GB/T (IEC and CCS not yet but is ongoing)
Connector Inlet						
Maximum Voltage (V)	1000	750	600	900	500*	1500
Maximum Current (A)	400	250	400	400	631*	600
Maximum Power (kW)	400	185	200	350	250*	900
Maximum Market Power (kW)	150	125	150	350	250	N.A.
Communication Protocol	CAN		PLC		CAN	CAN
V2X Function	Yes		No		Unknown	Yes
Start year	2009	2013	2014	2013	2012	2020

Note *: The specifications of Tesla Supercharger V3 is estimated based on the label of the Tesla Supercharger V3 at Fremont. [51]

TABLE 2. Statistics of the EVs on the Market in 2020 [53]

Model	Battery Capacity (kWh)	Range (km)	Required Charging Power (kW)*	Actual Maximum Charging Power (kW)
Mini Copper SE	28.9	180	69	49
BMW i3	37.9	235	91	49
Hyundai Kona	64	400	154	77
Tesla Model 3	72.5	450	174	250
Porsche Taycan Turbo S	83.7	425	201	262
Tesla Model S	95	515	228	250

Note * : Required average charging power to recharge the EV's battery from SoC = 20% to SoC = 80% in 15 minutes, where SoC means state of charge

TABLE 3. Battery Cells Cable of FC [56]–[59]

Company	Material of anode/cathod	Charging rate (Max.)	Energy density
CATL	Graphite/NMC	4 C	215 Wh/kg
Kokam	Graphite/NMC	4 C	152 Wh/kg
Microvast	PC/LMO	4 C	190 Wh/kg
Enevate	Si/NMC	9 C	350 Wh/kg

Note:
- NMC: Lithium Nickel Manganese Cobalt Oxide
- PC: Porous Carbon
- LMO: Lithium Manganese Oxide

Australia market [2]. The three FC standards have broad compatibility due to their compliance with the international standards (i.e., IEC 62 916, IEEE 2030.1.1, and SAE J1772) for both the AC and DC charging modes. Besides, as an important EV manufacturer, Tesla has its own FC standard adopted by only the Tesla Supercharger and EVs. The maximum charging power defined by these FC standards are different, where the lowest is 185 kW by GB/T 20 234.3-2015, and the maximum charging power reaches 400 kW by CHAdeMO, as shown in Table 1. To prepare for the demand to further increase the maximum charging power, the CHAdeMO association and China Electricity Council have co-developed a new standard, ChaoJi, with 900 kW as the maximum power, which is compatible with CHAdeMO and GB/T. Moreover, ChaoJi workgroup is working with CCS workgroup and IEC to make ChaoJi also compatible with CCS and IEC standards [49].

B. BATTERIES ARE GOING HIGH POWER

The battery technology also limits the maximum charging power. Besides, the high energy capacity of batteries is desired by customers as well so that the demand for long-range is satisfied.

The lithium-ion battery is the most popular one in the EV market because of its relatively higher energy and power density than other mobile battery technologies. The lithium-ion battery cell's energy and power density are significantly affected by the material used for the electrodes. By applying the state of art material, there are already commercial battery cells that can be charged with 4 C (15-min charging time) while keeping the energy density acceptable (i.e., $>$ 150 Wh/kg), as listed in Table 3 [56]–[59].

The battery's maximum charging power also depends on the thermal performance of the cell and the cooling in the cell and pack level. In [60], four battery packs' thermal performance with different battery cells and cooling conditions are simulated under the 350 kW charging power. It denotes that the batteries' temperature under UFC stays in the safe region if the low energy density (175 Wh/kg) battery cell is used. However, the cooling system in the study is substantially oversized. There are already EVs in the market rated at 270 kW and 83.7 kWh [61], a good balance between power and energy density. Besides, battery pack's voltage level is rising from 400 V to 800 V for UFC, which can reduce the weight of the cable and design challenges of its cooling system.

However, battery technology still needs to be improved to get a long lifespan. The capacity degradation of batteries can be significantly influenced by UFC, among other factors, including the operating temperature of the cell, the characteristics of the active material, the anode design, and the charging protocol (e.g., constant-current-constant-voltage

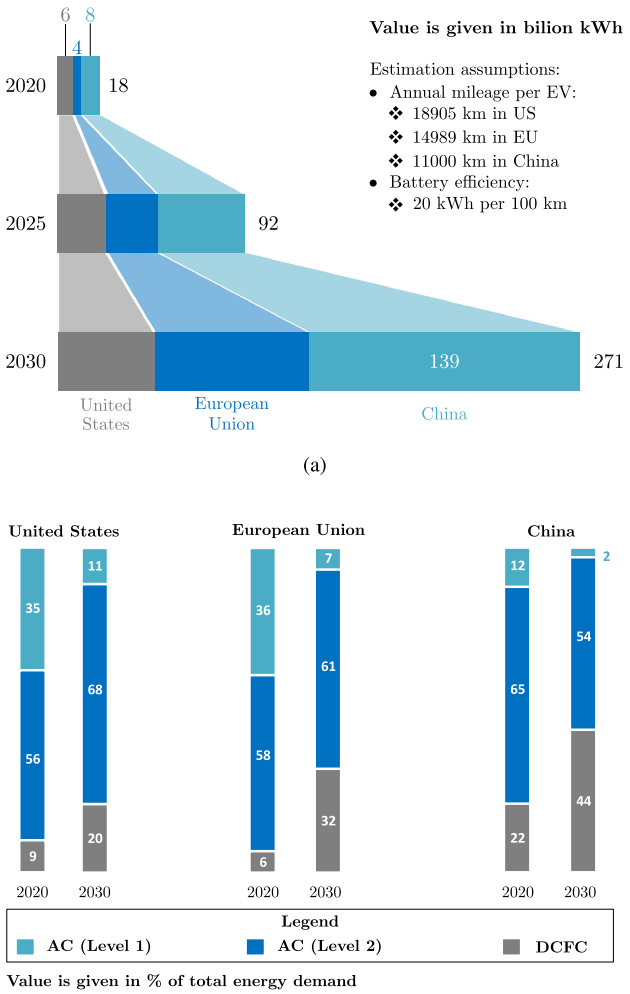


FIGURE 2. The energy demand for EVs: (a) Total energy demand (b) Energy demand by charging mode [51].

charging) [62]. Thus, more research on these aspects of batteries is needed before they can be reliably applied for UFC.

C. ARCHITECTURE OF ULTRA-FAST CHARGING STATION

Most FCSs are expected to be constructed along the expressway to offer FC service for long-distance trips. According to the configuration of Tesla's FCSs [63], an FCS comprises 10-12 150 kW DCFCs resulting in a total power capacity of 1.5-1.8 MW is normal. For such an FCS, the direct connection to the medium-voltage (MV) distribution network is preferred to avoid overloading of the low-voltage (LV) grid. In [2], [64]–[66], several approaches are proposed for the direct connection to MV grid for FCS.

The LV distribution network inside the FCS can be either AC or DC, as shown in Fig. 3 [2]. Compared with its DC counterpart, the AC distribution network is mature and adopted by most state-of-the-art FCSs [2], [64]. Nevertheless, the DC network configuration shows advantages on fewer conversion stages and simpler integration of chargers. Besides, as the

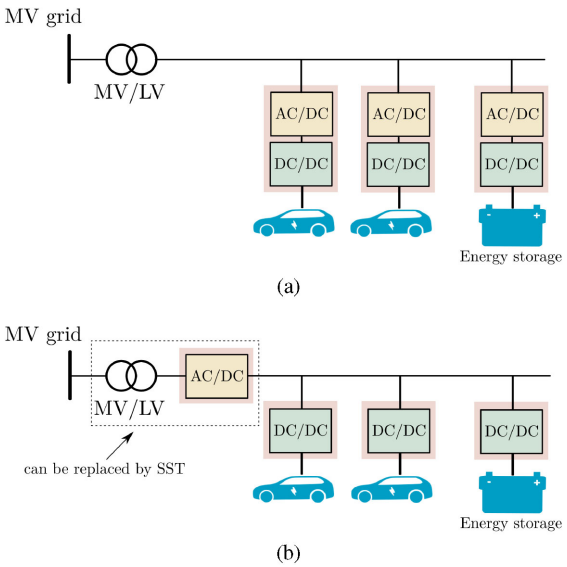


FIGURE 3. The structure of UFC station: (a) with AC distribution network (b) with DC distribution network where SST can be used alternatively [2], [64].

rectifier is centralized, it, together with the MV/LV line frequency transformer, can be replaced by a solid-state transformer (SST), which can significantly reduce the space, power losses, and cost of FCSs compared with the AC-coupled station [64]. As a promising concept, there is already a manufacturer planning to develop an SST-based FCS [67]. Despite this, this paper will focus on the AC-coupled FCS, which is still the mainstream solution for now and near future.

As shown in Fig. 4, the DCFC consists typically of two stages of conversion. The first stage is usually a step-up PFC to match the EV battery voltage (400 V - 800 V). The typical topologies for this stage include Vienna rectifier, conventional 2-level voltage source rectifier (VSR), and multi-pulse rectifier [68], [69] because of their features: a) low complexity, b) high reliability, c) low input current harmonics [70], [71].

Compared with the other two, the Vienna rectifier has three voltage levels. Hence, it requires less inductance for the input filter to fulfill the grid code regarding harmonics. Besides, as illustrated in Fig. 4, the voltage stress on the switches reduces by half. These two factors lead to improved efficiency and increased power density. However, the Vienna rectifier only allows unidirectional power flow. Another active front-end converter among the three is the conventional 2-level VSR. Due to two-level switching, it is less competitive regarding power density. However, it allows for bi-directional power flow. So, it is also widely used for on-board chargers (OBCs) on which the V2G functions are implemented. As for the last one, the multi-pulse rectifier, it is used mainly because of its simplicity. It is less attractive than the other two because it has severe distortion in the current draw from the grid.

For the second stage, typically used topologies are the half-bridge LLC, dual active bridge (DAB) [9], [10], and interleaved buck [72]–[74]. The galvanic isolation is needed

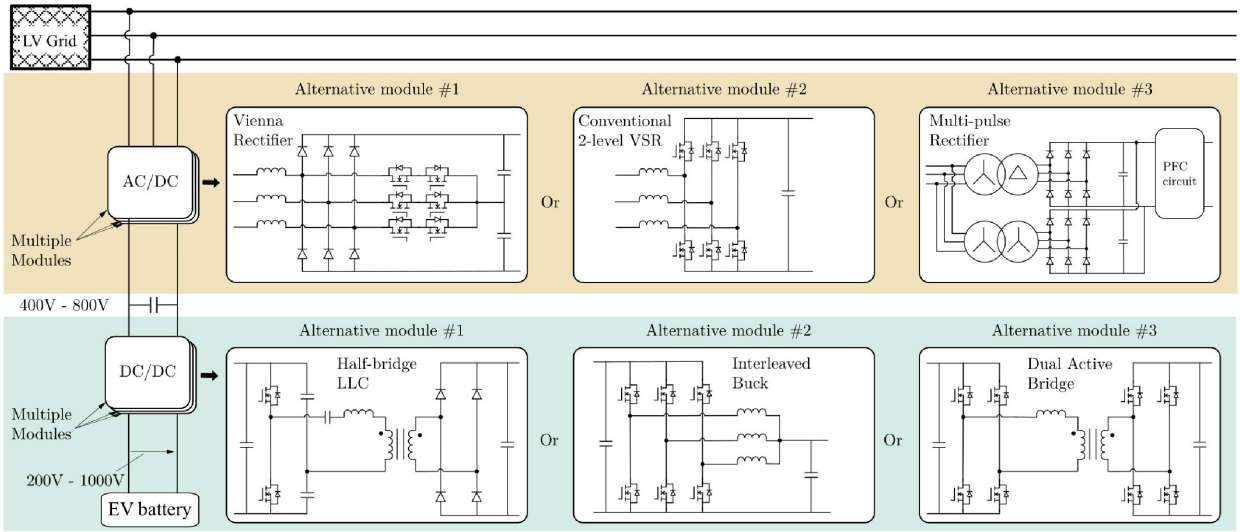


FIGURE 4. **Typical topologies of DC fast charger [68], [69], [72]–[74].**

in either the this stage or the first stage to provide the isolation between the EV and the grid, required by IEC 61 851-23.

Also, DCFCs generally use modular design [75] because a) the voltage and current stresses on components can be reduced, b) the DCFC can be compatible for the EVs with a wide range of voltage level in the market, c) the high efficiency can be maintained in the broad operation range of the charger, d) the cooling is easier as the heat source is spread [15], e) the charging power capacity of the DCFC can be fully utilized by charging several EVs with proper control despite the charging power for single EV has a wide range in the whole charging cycle. Especially for b) and c), as the battery voltage has a big range regarding the battery's SoC and different EV models might have 400 V system or 800 V systems, the DCFC is usually designed for the output voltage range from 200 V to 1000 V. With proper control strategy [76], modular design allows the submodules to switch between parallel and series connections to keep high efficiency in a wide output voltage range.

III. POWER QUALITY ISSUES

Compared with the overnight slow charging, FCS shows some different characteristics as follows:

- the charging power is high
- the load demand is centralised at the FCS
- the charging is mainly during daytime
- the load is more pulsating because of shorter charging time and higher power demand

Due to these features, FCS might create more severe issues in power quality. As mentioned in the previous section, FCS is usually connected to the MV distribution grid due to its high-power capacity. Thus, the scope of this paper is limited to the PQ inside and at the point of common coupling (PCC) of the FCS, which can be summarized as follows as reported or predicted in the literature: [17]–[19], [77]–[82]:

- Voltage fluctuation
- Harmonic stability
- Harmonic emission

The PQ at the FCS's PCC is influenced not only by the FCS itself but also the grid condition and the behaviour of the other loads/sources connected to the grid. For instance, the harmonic voltage at the FCS's PCC is determined by the FCS's harmonic emission, the harmonic voltage in the background voltage, and the grid impedance at FCS's PCC, which is discussed in details in Subsection III-C. Besides, the voltage fluctuation measured at the PCC is influenced by both the FCS's load profile and the other loads' behaviour (e.g., the start-up and shut-down of a motor) and how does the voltage fluctuation propagate from the point where the load cause the voltage fluctuation is connected to the FCS's PCC. The uncertainties on the grid condition, e.g., the harmonic voltage in the background voltage and impedance at the FCS's PCC, and FCS's load profile, make it difficult to discuss the FCS's impact on the distribution grid in general. However, the methodology for assessing the FCS's grid impact using some typical data (e.g., IEEE test feeder cases and representative load profile of FCS) can still be established. A typical load charging profile of EV is shown in Fig. 5(a) [83]. Based on the single EV load profile, the FCS's load profile can be estimated with a typical arrival time distribution of EVs at the FCS. As shown in Fig. 5(b), the arrival time distribution of EVs at an FCS can be assumed equivalent to the arrival time distribution of ICEVs at a petrol fuelling station [84].

A. VOLTAGE FLUCTUATION

The voltage fluctuation issues includes rapid voltage change (RVC) and flicker. To analyze the flicker problems brought by the FCS, a case study is carried out in [18]. The assumption used in the case study comprises: a) the typical arrival time distribution at the FCS [84], b) the Monte Carlo method for

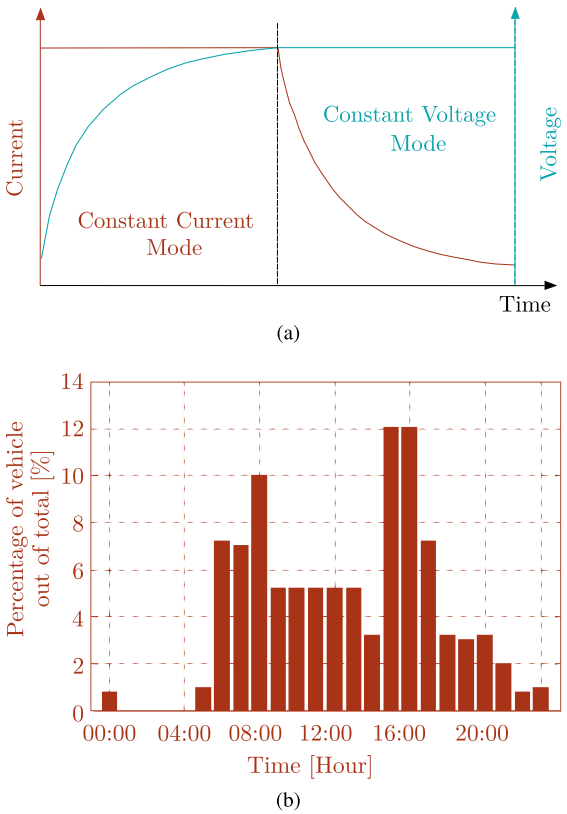


FIGURE 5. (a) The charging profile of an EV [83] and (b) the equivalent of arrival time distribution of EVs at an FCS, which is adapted from the arrival time distribution of ICEVs at a petrol fuelling station [84].

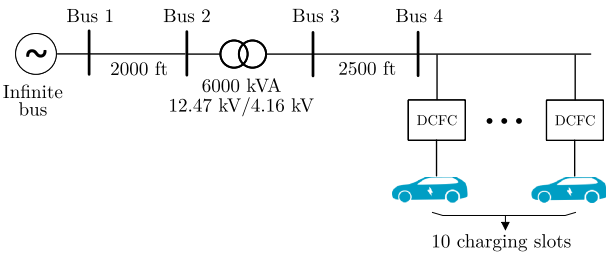


FIGURE 6. IEEE 4 bus test feeder used in [18] to simulate the voltage fluctuation induced by the EV charging with DCFCs.

probabilistic analysis, c) the IEEE 4 bus test feeders which is illustrated in Fig. 6. According to the results, the magnitude of the voltage fluctuation on Bus 4 is much higher when the DCFC's maximum charging power increases from 60 kW to 350 kW.

The flicker issue is also found at a bus station with a 120 kW charger [19], as seen in Fig. 7 where the short term flicker severity P_{st} exceeds the standard limit 1.0 on some days. In this specific case, the topology of the charger's front-end is the six-pulse diode rectifier. However, as the charging station is implemented with a wind generator, it is not clear that the measured flicker issue is mainly induced by either the variable wind generation or the charging.

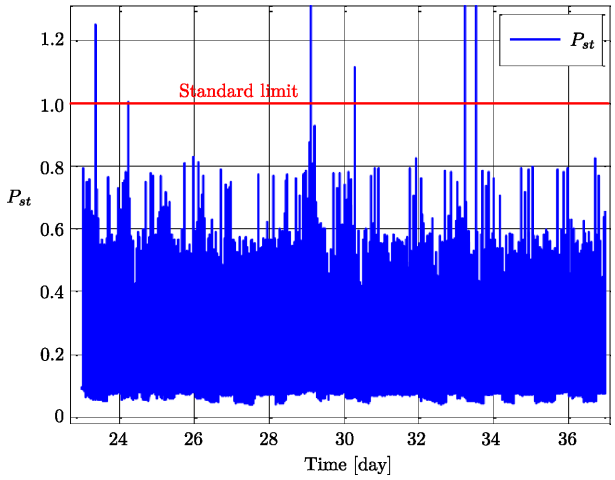


FIGURE 7. The flicker emission of a 120 kW charger at a bus station during April [19].

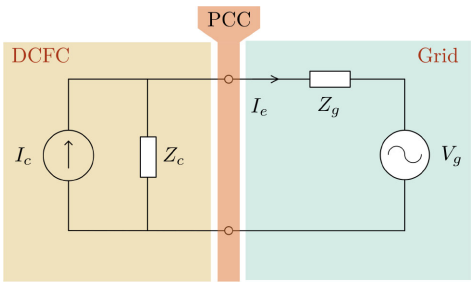


FIGURE 8. Impedance model of charger-grid system.

However, it can be expected that high-power DCFC will induce voltage fluctuation in the LV grid inside the FCS. When a DCFC starts and stops charging the EV, it causes a change in the load current. The LV network's grid voltage will fluctuate when the load current changes because of the cable resistance. Hence, the severity of the voltage fluctuation will increase when the DCFC's power grows.

B. HARMONIC STABILITY

Essentially, a DCFC is an active power converter with feedback control. The front-end converter of a DCFC is a voltage-source converter (VSC), which is connected to a voltage source on either DC side for inverter or AC side for rectifier. The output or input impedance of such a converter will behave like a negative resistance at some frequencies. If there is a resonant point in the same frequency range, instability will happen, which is the root cause of the instability of the power electronics-based system. As DCFC is also a power electronics-based system, stability issues can be expected. To analyze such problems, an impedance model-based approach, shown in Fig. 8 is often used [40]. The impedance model is a small-signal model in which the grid is simplified as the background voltage source V_g and the grid impedance Z_g at the PCC of the DCFC. On the other side, the DCFC is modeled

TABLE 4. Parameters of the Nonideal Power Grid and Converter in [77]

Nonideal power grid					
V_a,V_b,V_c	f_1	L_s	L_L		
110 Vrms	50 Hz	1.2 mH	180 μH		
Converter 1					
$U_{dc,ref}$	C_{dc}	L	R_L	r	f_s
360 V	1000 μF	3 mH	37 Ω	0.01 Ω	10 kHz
Converter 2					
$U_{dc,ref}$	C_{dc2}	L	R_L	r	f_s
360 V	1000 μF	3 mH	72 Ω	0.01 Ω	10 kHz

Note:
- V_a,V_b,V_c: Line to neutral voltage of phase a, b, and c, respectively
- f_1: line frequency • L_s: grid impedance
- L_L: Inductance between the two converters
- $U_{dc,ref}$: DC bus voltage • L: filter inductance
- C_{dc}: Capacitance of the DC bus capacitor
- R_L: Resistance of the load resistor • r: filter resistance
- f_s: switching frequency

as the harmonic current source I_c with the converter input impedance Z_c in parallel. The harmonic current source is used instead of the harmonic voltage source because DCFCs' input current is controlled to meet the charging demand. According to the impedance model, the harmonic current emission I_e can be calculated as (1)

$$I_e(s) = (I_c(s) - \frac{V_g(s)}{Z_c(s)})\frac{1}{1+\frac{Z_g(s)}{Z_c(s)}} \tag{1}$$

As seen, Z_g/Z_c is like an open-loop transfer function of a feedback control system. So it determines the stability of the system, and Nyquist stability criteria can be applied here. It also shows that the system's stability is a matter of matching between the grid impedance and the DCFC's input impedance. That's why, under the weak grid condition (i.e., Z_g is high), the converter input impedance Z_c plays a crucial role for system stability since the Nyquist curve of Z_g/Z_c has a chance to surround $(-1, 0)$.

Furthermore, the properly tuned single VSC, which is stable when solely connected to the grid, might become unstable when connected to the grid with several units in parallel, as reported in [77] and shown in Fig. 9. The parameters of the nonideal power grid and the VSCs is listed in Table 4.

Besides, due to the interaction between the Z_c and Z_g, a grid-tied VSC operates well when the V_{PCC} is clean and with 3% total harmonic distortion (THD), but it trips when the V_{PCC} is distorted with the maximum allowed THD set in EN 50 160 [17].

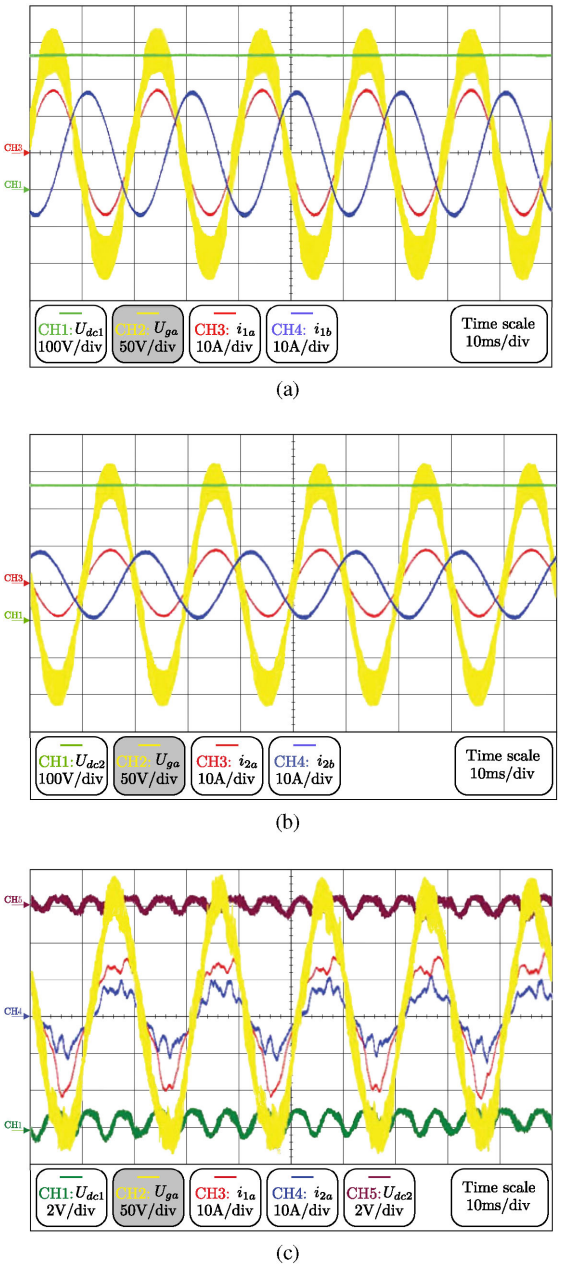


FIGURE 9. Waveform of two VSCs when: (a) the converter 1 is connected to the non-ideal power grid solely, (b) the converter 2 is connected to the non-ideal power grid solely and (c) the two converters are connected to the non-ideal power grid in parallel, where for example the U_{dc1}, U_{ga}, i_{1a} and i_{1b} is the dc bus voltage, phase a input voltage, phase a input current and phase b input current of the converter 1 respectively [77].

C. HARMONIC EMISSION

The harmonic current emission in (1) can be rewritten as

$$I_e(s) = \frac{Z_c(s)I_c(s)}{Z_c(s)+Z_g(s)} - \frac{V_g(s)}{Z_c(s)+Z_g(s)} \tag{2}$$

where the left-hand side term indicates the harmonic current generated by the harmonic current source, i.e., the VSC, while the right-side term indicates the harmonic current emanated from the distorted background voltage V_g.

The harmonic current of a commercial 50 kW DCFC, when the input power is 11 kW and 50 kW respectively, is measured in [78] and shown in Fig. 10. Due to the lack of grid voltage measurement, it is difficult to identify the harmonic current's primary source. The result is shown with the percentage of the fundamental current, making it challenging to evaluate the absolute harmonic emission (in Ampere) since the fundamental current keeps changing during a whole charging cycle.

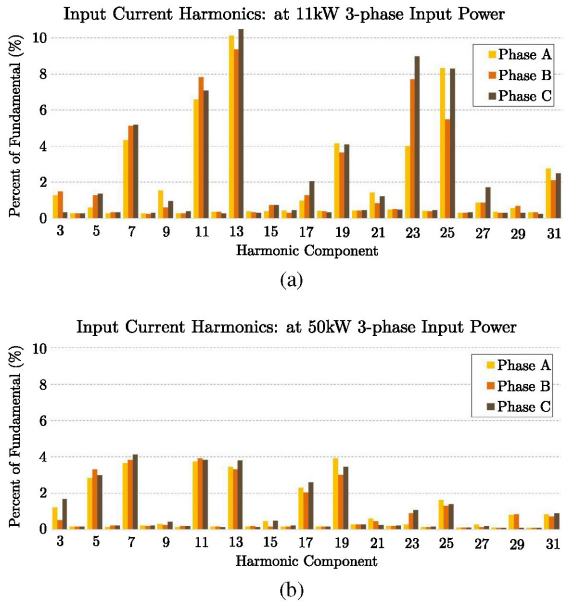


FIGURE 10. The individual harmonic current of the 50 kW DCFC when: (a) the input power is 11 kW (b) the input power is 50kW [78].

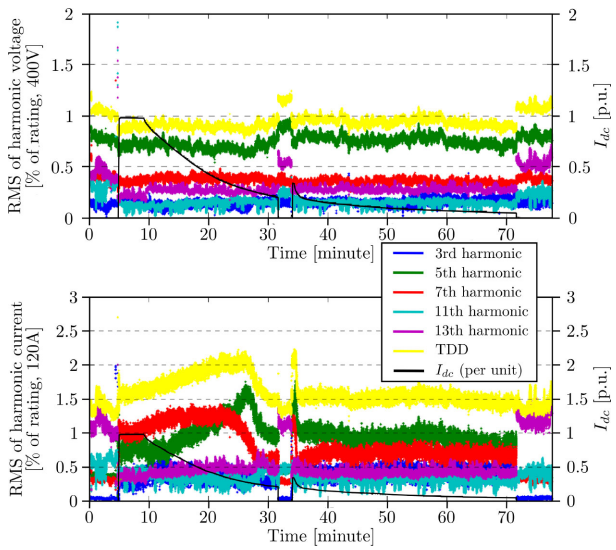


FIGURE 11. Main harmonic emission in the charging course of the 50 kW DCFC [79].

Alternatively, the total demand distortion (TDD) of the current, which is calculated using the root-mean-square (RMS) value of the maximum demand current as the base, is a better metric for assessing the harmonic current emission rather than the THD of the current [80], [85]. In a measurement [79], the TDD and the percentile of the main individual harmonic current to the rated DC output current in the whole charging cycle are recorded, as seen in Fig. 11. The result shows that the maximum harmonic current emission does not appear at the peak load.

D. SUPRAHARMONICS

The harmonic analysis in a conventional power system is normally performed on the harmonics with a frequency below 2 kHz. In the standards [20], [27], [29], [32], [86], the emission limits are given for up to 50th harmonic (2.0 or 2.4 kHz for a 50 or 60 Hz system respectively) for equipment rated $<$ 16A [86] and $>$ 16 A [27]. However, due to more integration of the power electronic-based system (e.g., DCFC and wind turbine), research interest on the supraharmonics (components within the frequency range 2 to 150 kHz) [87] is increasing, and to standard IEC 61 000-4-30 [88] an informative annex about this topic is added. The chargers, or more specifically converters, can be a source of supraharmonic distortions, as switching frequencies in the supraharmonic range are often used as efficiency- cost- and weight-effective solutions. Especially for OBCs in electric vehicles, where low weight and small size is even of more importance, the converters mostly use switching frequencies in the supraharmonic range as shown previously [89], [90].

As electric vehicles charge with relatively high power and a higher chance of more supraharmonic disturbances than other household equipment, their effect on a low-voltage installation can be tremendous. Supraharmonics can lead to different impacts on the LV grid and equipment connected to it. If a supraharmonic component with a significant amplitude is present in a weaker grid (with a higher impedance) this can also lead to a higher distortion of the voltage. This voltage distortion will then propagate additional supraharmonic currents through the installation, exposing more components and devices to it. Mainly because supraharmonic emission is still only partly standardized, devices are often not immune to disturbances in this frequency range. This can lead to additional heating of those and a reduced lifetime. Furthermore, audible noise (2–20 kHz falls into the human hearing range), malfunction of equipment (e.g., charging interruptions and high errors in energy metering), malfunction of power-line communication (PLC) and possibly tripping of residual current devices (RCDs) have been reported [81], [82].

Regarding DCFCs, which mostly have higher power than the OBCs and sometimes a different converter type, it is unknown if similar or other effects can be expected. Indicative measurements (by ElaadNL) of 22 DCFCs from 18 manufactures at reduced power showed that DCFCs could also be a very significant source of supraharmonic currents, with amplitudes higher than the OBCs, as seen in Fig. 12. Side note here is that DCFCs are often installed in another grid situation than AC chargers, making a smaller impact on the consumer installation. Nevertheless, this can lead to interaction between the DCFCs and impact the grid, which is still under investigation. Also, for these kinds of distortions from DCFCs, no standard exists yet. An example of currents from a DCFC at reduced power with supraharmonic components is shown in Fig. 13.

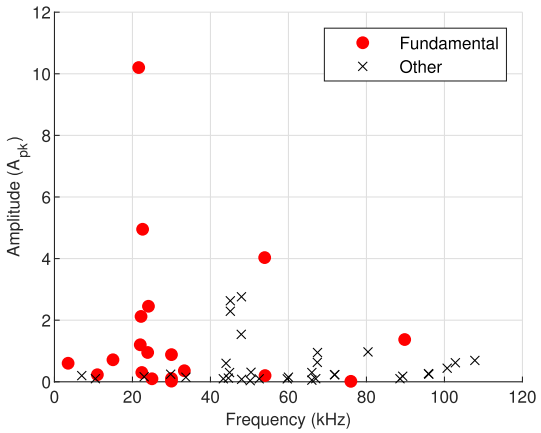


FIGURE 12. Supraharmonic emission of 22 DCFCs, showing the first (fundamental) switching component and multiples or unrelated (other) components.

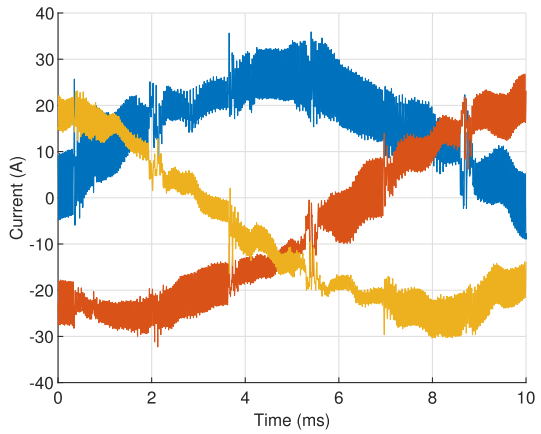


FIGURE 13. Supraharmonics in the 3-phase currents measured at the input of a DCFC.

IV. POWER QUALITY STANDARDS

As an emerging installation to the grid, FCS does not have dedicated PQ standards. Nonetheless, the general PQ standards can be used for assessment. Internationally, the most adopted PQ standards include IEEE PQ standards [20]–[23] and IEC 61 000 series [24]–[32], whose content related to the aforementioned PQ issues of FCSs are summarized in Table 5. For simplicity, the national grid codes are not compared here.

In general, both of the IEEE PQ standards and IEC 61 000 series provide the limits or the guidelines on setting limits for the PQ items, which can be assessed at the PCC. In detail, IEC 61 000 series mostly give only system compatibility and planning level. The equipment emission level is then calculated based on the system planning level and specifications. In the way, the emission level adapts to the specific system and more room for the normal operation of the system is reserved. To the contrary, IEEE PQ standards, which set fixed values as the limits, are much simpler, but also easier for use. Nonetheless, both of the IEEE PQ standards and IEC 61 000 series are categorized as follows,

A. RMS VOLTAGE TOLERANCE

The RMS voltage tolerance in normal operation for different voltage levels is specified in IEEE 1159 and IEC 61 000-2-4. As shown in Table 5, in both of the standards, $\pm 10\%$ tolerance is allowed for the long-term (i.e., $>$ 1 min) RMS voltage.

B. VOLTAGE FLUCTUATION

The voltage fluctuation consists of the RVC of the fundamental voltage and flicker. It is worth noting that RVC and flicker are sometimes overlapped on each other in assessment, but there is no clear correlation between the two [91]. Thus, in Table 5, the two limits are separated.

In IEC 61 000 series, only the compatibility level and planning level are given where the emission level is decided by the system operator or owner, according to the planning level and the system circumstance. In IEEE PQ standards, the content regarding the limit for voltage fluctuation is the same as that in IEC 61 000 series.

C. HARMONIC CURRENT DISTORTION

In IEC 61 000 series, the THD, which is the ratio of the RMS value of the sum of all the harmonic components up to 50th order to the RMS value of the fundamental component, is used for the standardization. For installations with the phase current rating higher than 16 A connected to the LV grid, the emission level at the PCC is limited in IEC 61 000-3-4 [27]. However, the limits are determined based on some assumptions that are representative for small residential loads [32], which might not be applicable for a high power, e.g., 350 kW, DCFC. IEC 61 000-3-14 [32] provides the guidelines on how to develop emission limits to prevent excessive voltage distortion in the LV grid. As for the emission level for installations connected to the MV grid, the recommended emission limits are not given in IEC 61 000-3-6 [29]. Instead, guidelines on how to set the emission level according to the situation in practice are provided.

In IEEE 519, the TDD, which is the ratio of the RMS value of the sum of all the harmonic components up to 50th order to the RMS value of the maximum demand current, is used for the standardization. The maximum demand current is a summation of DC component, fundamental component and all harmonic components. Besides, the recommended harmonic current emission is given in specific values for five different short-circuit ratio (SCR) values. A low SCR indicates a high grid impedance for a particular load whose load capacity is specified. In the weak grid scenario, the grid impedance is high. The grid voltage at PCC is more sensitive to the harmonic current emission from the load, so a lower harmonic current emission is allowed.

Compared with the IEC 61 000 series, IEEE 519 is less complicated to be applied. Although IEC 61 000 series provide enough flexibility, it might be difficult when applying

TABLE 5. Comparison of IEEE PQ Standards and IEC 61 000 Series Within the Scope of the FCS related [20]–[32]

		IEEE PQ standards		IEC 61000 series			
Voltage level for MV and LV grid		LV gird: V≤1kV MV grid: 1kV<V≤69kV		LV gird: V≤1kV MV grid: 1kV<V≤35kV			
		Level		Compatibility level		Emission (E) and Planning (P) level	
		Value	In standard IEEE	Value	In standard IEC	Value	In standard IEC
Voltage Level	MV grid	Normal operation tolerance: ±10%	1159	Normal operation tolerance: ±10%	61000-2-4	N.A.	
	LV grid	Normal operation tolerance: ±10%	1159	Normal operation tolerance: ±10%	61000-2-4		
Voltage Fluctuation	MV grid	Same as IEC 61000 series	1453	RVC: • ≤ 3% (Normally) • > 3% (Infrequently) Flicker: N.A.	61000-2-12	RVC (Indicative): • 2.5% - 6% (P) Flicker (Indicative): • $P_{st} = 0.9$ (P) • $P_{lt} = 0.7$(P) • Guidelines for setting emission level are given	61000-3-7
	LV grid		1453	RVC: • ≤ 3% (Normally) • > 3% (Infrequently) Flicker: • $P_{st} = 1$ • $P_{lt} = 0.8$	61000-2-2	RVC: • 3% - 6% (E) Flicker: • $P_{st} = (S_L/S_{TR})^{1/3}$ (E) • $P_{lt} = 0.65(S_L/S_{TR})^{1/3}$ (E)	61000-3-5
Voltage unbalance	MV grid	N.A.		$V_n = 2\% \times V_p$ (3% may occur)	61000-2-12	• $V_n = 1.8\% \times V_p$ (P) • Guidelines for setting emission level are given	61000-3-13
	LV grid	$V_n = 2\% \times V_p$	141	$V_n = 2\% \times V_p$ (3% may occur)	61000-2-2	• Planning level can equal to the compatibility level • Guidelines for setting emission level are given	61000-3-14
Harmonic Current	MV grid	TableVI	519	Compatibility level is given only for harmonic voltage		• Planning level is given only for the harmonic voltage • Guidelines for setting emission level are given	61000-3-6
	LV grid	TableVI	519			• Planning level is given only for the harmonic voltage • For $I_{eqp} > 75A$, guidelines are given for setting emission level	61000-3-4 61000-3-14
Harmonic Voltage	MV grid	Fig14	519	Fig14	61000-2-12	• Indicative planning level is shown in Fig14 • Guidelines for setting emission level are given	61000-3-6
	LV grid	Fig14	519	Fig14	61000-2-2	• Planning level can equal to the compatibility level • Guidelines for setting emission level are given	61000-3-14

Note:
- RVC : Rapid Voltage Change
- S_L: Apparent power of the load
- S_{TR}: Apparent power of the service transformer
- I_{eqp}: Rating phase current of the equipment
- V_n: Negative sequence voltage
- V_p: Positive sequence voltage

TABLE 6. Harmonic Current Limits in IEEE-519 [20]

	Maximum harmonic distortion of the individual harmonic order in percent of I_L					
I_{SC}/I_L	$3 \le h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h < 50$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

Note:
- Limits for even harmonics are 25% of the odd harmonic limits
- DC offset in current is not allowed
- I_L: maximum demand load current
- I_{SC}: maximum short circuit current at PCC

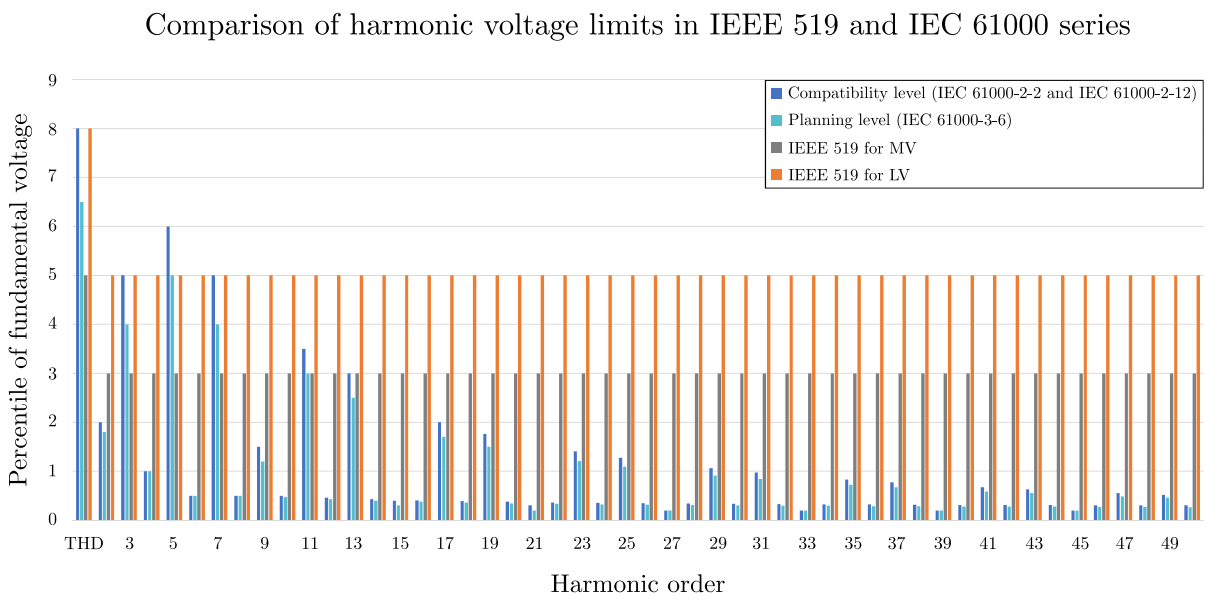


FIGURE 14. **Limits set for harmonic voltage in IEEE 519 and IEC 61 000 series [20], [24], [26], [29].**

them because, for instance, it requires network data and calculation of many factors as shown in Fig. 21. However, by following the IEC 61 000 series guidelines, the system's normal operation tends to be maintained easier without compromising the fairness between the customers. As shown in Table 6, IEEE 519 set harmonic current emission limits for five different SCR values regardless of, for instance, the system voltage level and supply system's capacity, which might lead to failing to keep the harmonic voltage limit set by its own [92]. However, compared with the counterpart, IEEE 519 might be more successful when assessing the harmonic current emission of DCFCs since it uses TDD as the metric for the assessment, which is, as aforementioned, preferred to reflect the harmonic emission level of chargers.

D. HARMONIC VOLTAGE DISTORTION

For harmonic voltage distortion, its compatibility level in MV grid is interpreted in the IEC 61 000-2-12, whereas the indicative planning level is introduced in IEC 61 000-3-6. Similarly, the guidelines for setting the harmonic voltage emission level is given instead of any specific values. In the LV environment, its compatibility level is introduced in IEC 61 000-2-2, whereas the guidelines for setting harmonic voltage emission level is provided in IEC 61 000-3-14. With a known impedance of the grid at PCC, the current and voltage emission level can be converted to each other.

In IEEE 519, the maximum THD of the grid voltage is given for the LV and MV grid respectively, which is illustrated in Fig. 14

E. VOLTAGE UNBALANCE

In LV grid, the negative sequence voltage should be lower than 2% of the positive sequence voltage, which is set in IEEE 141 and IEC 61 000-3-14. As for the large installation like the high power DCFC, the guidelines for deriving the device's emission level in the LV and MV grid are introduced in IEC 61 000-3-14 and IEC 61 000-3-13, respectively. Moreover, an indicative planning level of voltage unbalance in the MV grid is given in IEC 61 000-3-13. In contrast, no suggestion is given for the planning level of voltage unbalance in the LV grid. No IEEE standards exist regarding the voltage unbalance in the MV grid.

V. MITIGATION MEASURES

To fulfill these PQ standards, mitigation measures have been proposed or already applied in the industry. More details are as follows,

A. SMART CHARGING

Conventional smart charging strategy is effective for 6-8 h overnight low-power charging but not for FCSs, which happen randomly in a day and lasts for a short period (typically 15 mins).

To overcome the impact of FCSs on voltage stability, a real-time charging navigation framework, as seen in Fig. 15, is proposed [33] to attract EV drivers to recharge at off-peak hours to decrease the stress on the grid. The navigation framework also reduces the stress on the transportation system by guiding EV drivers to the closest FCS offering the desired charging price and charging power. With this framework, the DSO can influence the EV drivers' charging behaviour by manipulating the electricity price. A simulation is performed to investigate the effectiveness of the proposed approach. The simulation is based on a distribution system whose topology is the IEEE 34-node test feeder. The results reveal that the proposed approach can reduce the burden of the peak load.

Moreover, the FCS operator can coordinate the chargers according to the grid condition by altering the charging power.

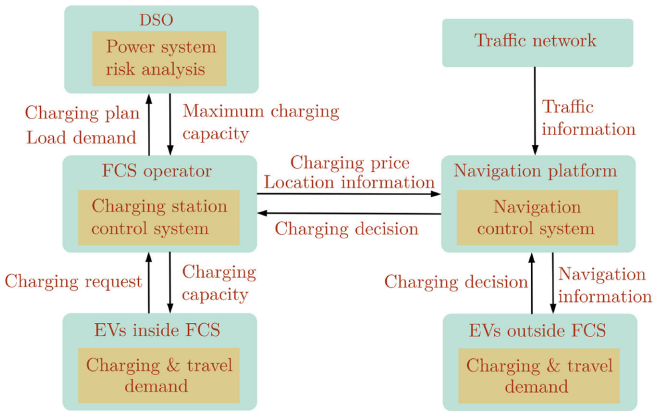


FIGURE 15. A EV charging navigation framework and FCS control system to decrease the risk of voltage sag and instability [33], [34].

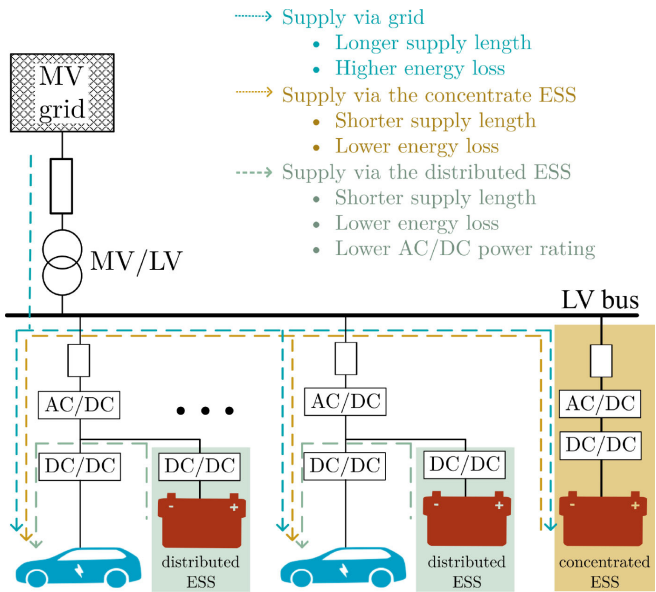


FIGURE 16. The BESS used in the FCSs can not only reduce the investment on the service transformer and cable but also the supply length and energy loss in transmission [35], [37].

In [34], a management method is proposed to regulate the EVs' charging behavior to decrease the FCS's impact on the power grid voltage. Simultaneously, the financial benefits of FCS operators and customers are also increased.

B. INTEGRATION OF ENERGY STORAGE

The application of ESSs in the power system is an emerging topic, as it can provide different ancillary services. The ESSs can be categorized into different types [93]. Typically, there are power and energy types, where the former has a higher power rating, and the latter has higher energy capacity [36].

Integrating an ESS into an FCS can mitigate the influence of the large-pulsating load of the FCS. As shown in Fig. 16, by integrating ESS, the high pulsating load demand is supplied through the ESS while the relative smaller and continuous load demand is supplied by the MV distribution gird via the service transformer and cable. Thus, the investment on the transformer and cable can be considerably reduced. Besides, the ESS supply can save energy loss in transmission because of the relatively shorter supply length than the MV grid. Moreover, the study in [35], where a simplified method is proposed to extract the optimized capacity of the ESS, concludes that the ESS can help to reduce the charging cost of the FCS. The control strategy for ESS is critical to make it function properly. In [37], where the flywheel is used to compensate the high impulsive load demand. The flywheel is controlled to maintain the DC link voltage of the DCFC, so that the pulsating power naturally is taken from the flywheel, and the impact on the grid is mitigated. In [36], the control strategy for the hybrid energy storage system is proposed so that the ESS can satisfy the demand of fast response and high energy capacity simultaneously.

Besides, the ESS can be integrated either inside the DCFC with multiport converters (MPCs) [94], [95] or directly in the LV distribution network with its own AC/DC and DC/DC converters. On the one hand, the former approach can reduce the AC/DC converter's power rating in the DCFC and provide a controllable operating point of the AC/DC converter without influencing the EV charging course. On the other hand, distributing ESS to DCFC might increase difficulty when coordinating the distributed ESS for high-level grid control, e.g., providing reserves for the grid.

C. IMPEDANCE BASED APPROACH

The harmonic mitigation measures of the grid-tied converters typically include power filter design and control. The switching frequency noise is normally tackled with power filter design (L-, LCL-filter, etc.) together with modulation strategies [97] (SPWM, SVPWM, DPWM, SHE, interleaving, etc.). The low-frequency harmonics (e.g., up to 1/10 of switching frequency) are more affected by control. Several advanced control strategies have been proposed to handle them, including multiple resonant controllers, repetitive controller, active damping [38] etc. These approaches work well when the grid is clean. But in weak grid conditions, especially when several grid-tied converters are connected to the same weak grid (FCS is in such a condition), they start to interact with each other and get harmonics amplified and create resonances (interharmonics), or even instability. In that scenario, the impedance-based approach can show the mechanism more clearly.

1) IMPEDANCE MODELLING OF DCFC

Many impedance modeling studies of 2-level-3-phase VSC can be found in the literature. Although the small-signal modeling and control of the Vienna rectifier (which is the mainstream front-end of DCFCs) are different from the 2-level-3-phase VSC, the difference can be neglected if the zero-sequence impedance is not of interest [98]. Thus, the impedance modeling method for general VSCs can also be used for DCFCs.

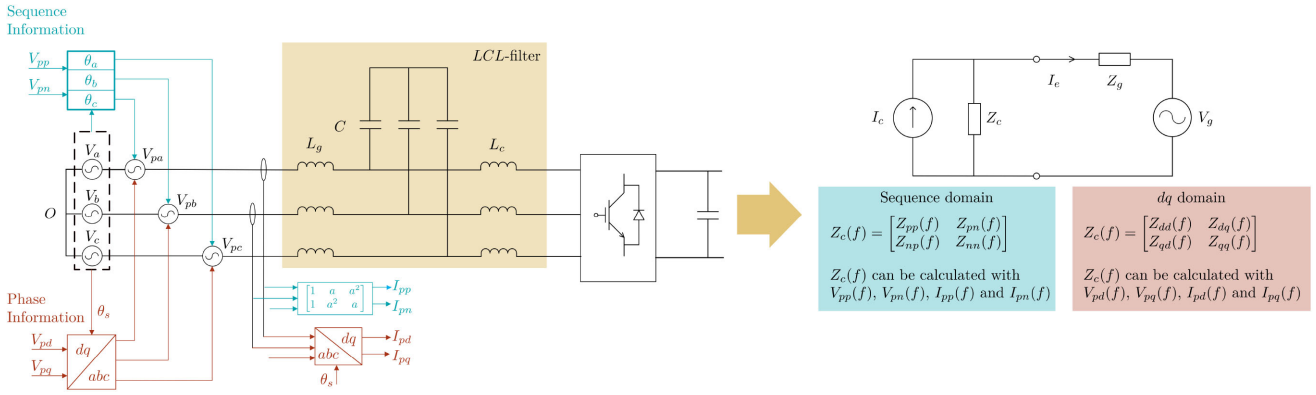


FIGURE 17. The input impedance of a typical DCFC using LCL-filter can be obtained in either the *dq* domain or sequence domain by injecting harmonic voltage at the frequency of interest and measure the response harmonic current at the same frequency of the injected harmonic voltage [43], [96].

In [43], the converter small-signal model is developed in dq domain. Hence, the actual grid phase is necessary. The resulting converter impedance Z_c is a two-by-two matrix due to the coupling between the d-axis and q-axis. For stability analysis, the generalized Nyquist Criterion (GNC) [45] can be used. To verify the developed model in dq domain, small harmonic voltage perturbation at a certain frequency aligned with the d-axis and q-axis, i.e., V_{pd} and V_{pq}, can be injected at the input terminal of the DCFC in two separate steps. In each step, the harmonic currents aligned with the d-axis and q-axis at the frequency of the injected harmonic voltage, i.e. I_{pd} and I_{pq} when V_{pd} is injected and I'_{pd} and I'_{pq} when V_{pq} is injected, are measured. Based on the measurement, the frequency related impedance can be derived by solving the equations in (3)

$$\begin{cases} V_{pd}(f) = Z_{dd}(f)I_{pd}(f) + Z_{dq}(f)I_{pq}(f) \\ 0 = Z_{dq}(f)I_{pd}(f) + Z_{qq}(f)I_{pq}(f) \\ 0 = Z_{dd}(f)I'_{pd}(f) + Z_{dq}(f)I'_{pq}(f) \\ V_{pq}(f) = Z_{dq}(f)I'_{pd}(f) + Z_{qq}(f)I'_{pq}(f) \end{cases} \tag{3}$$

The alternative approach is developing the impedance model in the sequence domain [96]. It is further improved in [99] by considering the frequency-coupling dynamics, which also results in a two-by-two matrix for the converter impedance Z_c due to the coupling between the positive sequence and negative sequence. For the model verification, the same approach used for verifying the dq domain impedance model can be used. The difference is that the injected harmonic voltage and the measured harmonic current are in the sequence domain. The methods to obtain the impedance model of a typical DCFC is illustrated in Fig. 17.

To ensure the accuracy of the impedance model in the dq domain, the phase of the grid voltage needs to be measured precisely, which is difficult to satisfy. However, such phase information is not necessary when implementing the impedance model in the sequence domain. Thus, the latter is easier to be implemented.

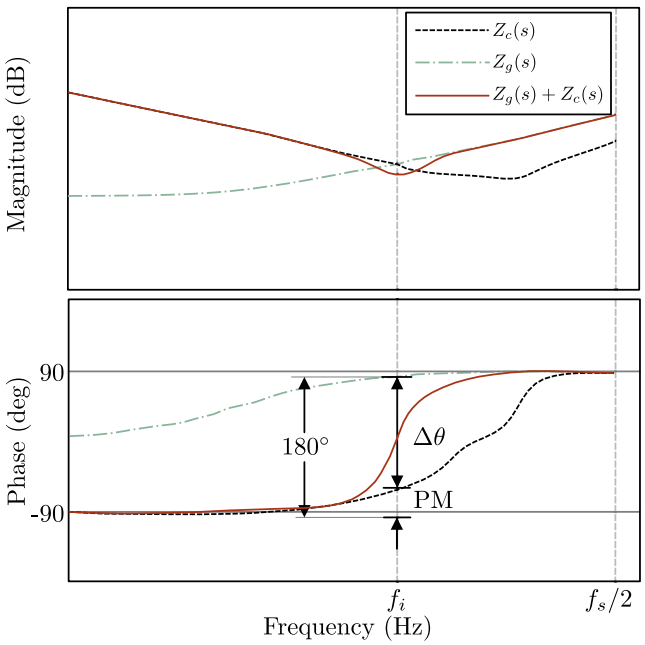


FIGURE 18. The frequency response of VSC impedance Z_c, grid impedance Z_g and the sum of them [47].

2) IMPEDANCE SHAPING OF DCFC

As aforementioned, the input impedance of the DCFC is crucial for: a) ensuring the stability of the charger-grid system, b) low harmonic current emission. Fig. 18 [47] shows the frequency response of a VSC impedance Z_c, grid impedance Z_g, and the sum of them. The magnitude of Z_c and Z_g intersect at frequency f_i, where a series resonance will happen if their phase difference $\Delta\theta = \theta(Z_g) - \theta(Z_c)$ approaches 180°. To improve the system stability and decrease the harmonic emission, it is crucial to shape the impedance Z_c so that the magnitude of Z_c at all frequencies is increased and the phase difference $\Delta\theta$ at f_i is decreased [47].

Based on the developed impedance model, the factors that influence the input impedance Z_c of a DCFC are shown in

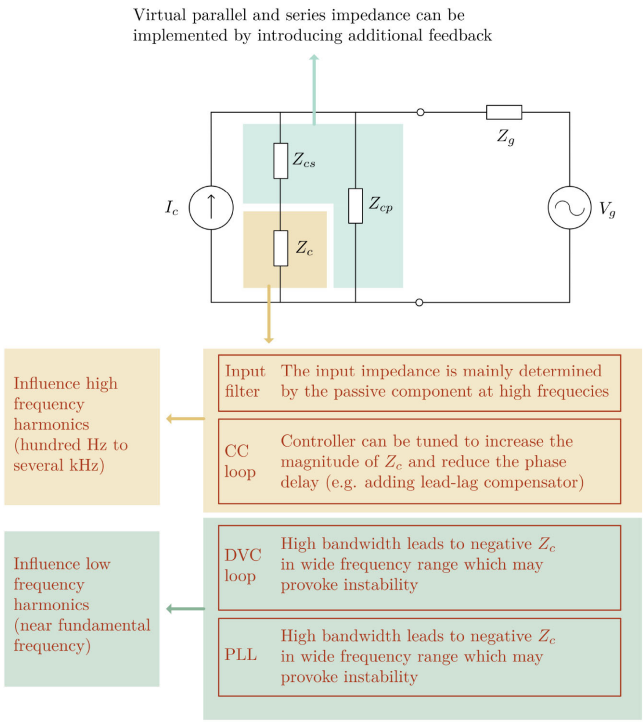


FIGURE 19. **The factors that have influence on the input impedance of the DCFC [38], [41], [43], [46], [47].**

Fig. 19 [38], [41], [43], [46], [47]. The Z_c is mainly influenced by the outer loop, i.e., the direct voltage control (DVC) loop and the phase lock loop (PLL), at the low-frequency range due to their low bandwidth [46]. The outer loop will introduce the additional phase delay in their bandwidth [43], [100] and decrease the magnitude of Z_c [100].

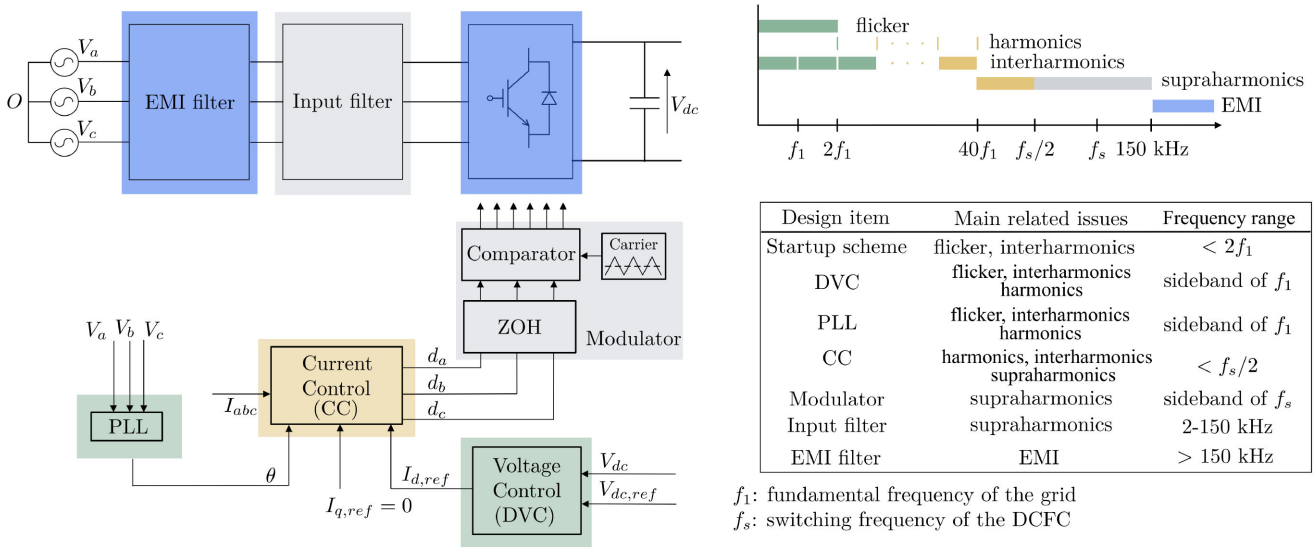
The inner loop, i.e., current control (CC) loop, has relatively higher bandwidth and influences till a higher frequency. [100] shows that the system's harmonic stability can be increased by adding a lead-lag compensator, which decreases the phase difference $\Delta\theta$, in the current controller. Moreover, the input impedance can also be shaped by introducing the virtual parallel and series impedance, which is implemented by introducing additional feedback [47]. Beyond the CC loop, the input impedance is also influenced by the input filter, especially in the high-frequency range beyond the bandwidth of the CC loop.

Furthermore, it is worth noting that the VSC input impedance depends on the operation point, or more specifically, the output (or input) power. Compared with the other type of VSC, DCFCs have more dynamic input power and a wider range of operation points related to the battery's SoC. This feature, together with unpredictable charging behaviour, introduces new challenges on maintaining the system's harmonic stability, and further research is needed.

F. DESIGN OF DC FAST CHARGERS

As presented in Section III, the main power quality issues induced by DCFCs are the degraded grid voltage profile and harmonic issues. To mitigate the power quality issues, it is essential to analysis the influence of the DCFCs' design on the power quality issues. A typical DCFC's design is illustrated in Fig. 20, where the relation between a specific design and the power quality issues that are most likely induced by the specific design is also shown. Analysis on each specific design is outlined as below:

1) Startup scheme; For a high-power DCFC, its startup has a significant influence on the grid voltage profile, which might lead to severe voltage fluctuation leading to flicker as shown in Fig. 7. The ramp startup can be applied to reduce the DCFC's startup's impact on the grid voltage profile. For instance, the maximum power rate of the DCFC is limited based on the DSO's command [37]. Instead of rising as a step, the DCFC's input current ramps up slowly. However, without an ESS integrated inside the DCFC, this approach fails to fully utilize the DCFC's power capacity.
2) PLL; As aforementioned, the PLL influences the converter impedance Z_c in the low-frequency range (near the grid's fundamental frequency) because of its bandwidth Z_c. The PLL introduces negative resistance at some frequencies, which introduces negative damping. Any harmonics and interharmonics, either preexisting in the grid or generated by the DCFC, will have increases in their amplitude due to weakening damping at the frequencies influenced by the negative resistance. In the worst case, harmonic instability might occur if the system shows negative damping at these frequencies. The PLL's bandwidth should be limited to low frequency, e.g., 20 Hz [101], to reduce the risk of the negative resistance induced by the PLL. The reason is, as found in [43], [101], the frequency range of the negative resistance has a positive relationship with the PLL's bandwidth. Besides, the PLL's dynamics induce frequency coupling, as the PLL usually tracks only the q-axis grid voltage [101]. Assuming a 450 Hz harmonic voltage exists in the background voltage, both - 350 Hz and 450 Hz harmonic current will be measured in the DCFC's input current. The minus sign indicates a negative sequence component [99]. Such a coupling effect introduces more challenges to DCFC's design. Besides, it is worth noting that the interharmonics with frequencies below $2f_1$ is related to flicker, which is also influenced by PLL design.
3) DVC; Like PLL, the bandwidth of the DVC loop is relatively lower than the other design items in the system. The DVC loop's stability is investigated, revealing that the DVC's stability is decreased by weaker grid conditions, increasing input power of VSC, or DCFC in the case here, and bandwidth closer to the PLL's bandwidth [102]. It is further revealed that the DVC introduces negative damping in the low-frequency range [41]. Hence, the flicker, harmonics, and interharmonics are influenced by DVC. To ensure stability and prevent severe power quality issues, the DVC should be designed considering the weak grid condition, the



Design item	Main related issues	Frequency range
Startup scheme	flicker, interharmonics	$< 2f_1$
DVC	flicker, interharmonics harmonics	sideband of f_1
PLL	flicker, interharmonics harmonics	sideband of f_1
CC	harmonics, interharmonics supraharmonics	$< f_s/2$
Modulator	supraharmonics	sideband of f_s
Input filter	supraharmonics	2-150 kHz
EMI filter	EMI	$>$ 150 kHz

f_1: fundamental frequency of the grid
f_s: switching frequency of the DCFC

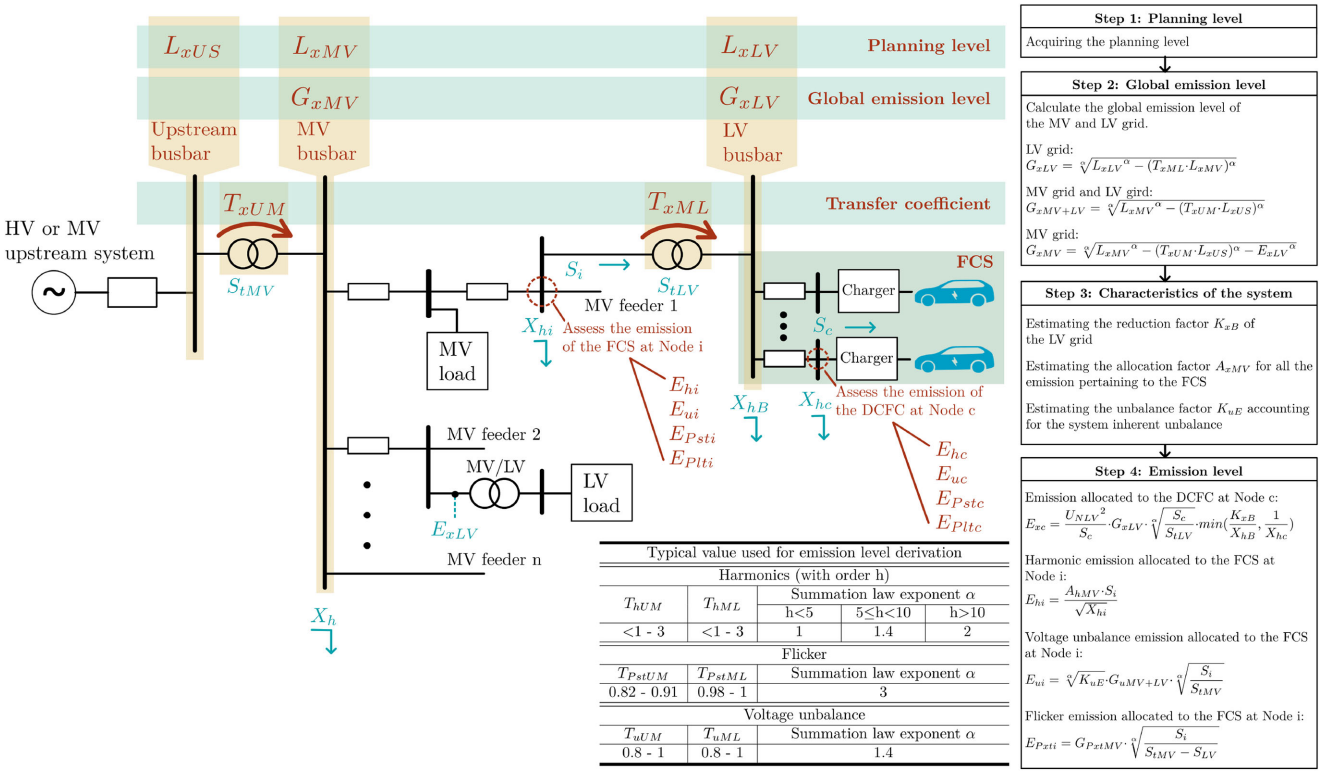
FIGURE 20. **Relation between the specific charger design and the power quality issues.**

complete DCFC's operation point, and the possible interaction with the other control loops in the system.

4) CC; As illustrated in Fig. 20, the CC loop influences higher frequencies. Several design aspects should be considered to ensure DCFC's stable operation and low harmonic emission when several DCFCs are connected in parallel. First of all, it is revealed in [103], [104], instability can be provoked by the interaction between the PLL and CC loop. The risk of stability can be reduced by reducing the PLL's bandwidth [103]. It is also revealed in [103] that the $\alpha\beta$-frame PR controller is more robust than the dq-frame PI controller against the PLL dynamics. Besides, as mentioned in [38], multiple resonant controllers can be implemented in the current control loop to null the harmonic with a certain order, e.g., 5th harmonic, in the DCFC's grid current. Besides, the CC loops of several DCFC in parallel have interaction between them, which might lead to instability, as shown in Fig. 9(c). It is a challenge for the designers to guarantee system stability with a fixed design in this scenario, which needs to be investigated more. Finally, as aforementioned in Subsection V-E1, the DCFC's input impedance Z_c can be shaped with several approaches to reduce the harmonic emission in the charger-grid system.
5) Input filter; The input filter is used to attenuate the switching frequency ripple injection into the grid in the range of 2-150 kHz [105]. As aforementioned, L-, LCL-filter, and the most used two for DCFCs. Compared with L-filter, LCL-filter shows better performance when the total inductance used is the same as the L-filter's inductance [105]. However, it also has two more zeros and two more poles [105], which introduces additional challenges on the system stability. However, the design of LCL-filter is well studied in [39] to ensure system stability. Besides, there is a challenge for designing an LCL-filter, with which the DCFC is stable, in various grid impedance conditions. For instance, the LCL-filter's resonance peak would change accordingly when the DCFC is connected to a grid having a different grid impedance. In this case, a proper designed stable CC loop with high bandwidth might become unstable [38]. To solve this issue, a control, namely active damping [38], is proposed for shaping the resonance peak of the LCL-filter without compromising the bandwidth of the CC loop.
6) Modulator; The PWM modulator can induce sideband (f_s) oscillations [41], which is normally in the range of 2-150 kHz. When connecting several DCFCs with the same design in parallel, it is better to synchronize their PWM to prevent sideband-harmonic instability, which is presented in [41].
7) EMI filter; EMI filter is used to attenuate the components in the range above 150 kHz in the DCFC's grid current. However, as EMI is out of the scope of power quality issues, it is not elaborated.

VI. CONCLUSION

This paper has reviewed the state-of-the-art technology and standards for EV fast charging, which clearly show the development towards UFC. Afterwards, the PQ issues introduced by FCSs and DCFCs are thoroughly reviewed. It shows that the main PQ problems brought by FCSs and DCFCs comprises the deteriorated voltage profile and excessive harmonic emission and amplification. Since PQ standards dedicated to FCSs do not exist yet, referring to the PQ standards for general installations is a feasible approach for FCS's PQ assessment. To fulfill these PQ standards, the mitigation measures are summarized with an emphasis on the impedance-based approach. In the end, it can be concluded the barrier for large adoption



Typical value used for emission level derivation

Harmonics (with order h)				
T_{hUM}	T_{hML}	Summation law exponent α		
		h<5	5≤h<10	h>10
<1 - 3	<1 - 3	1	1.4	2

Flicker		
T_{PstUM}	T_{PstML}	Summation law exponent α
0.82 - 0.91	0.98 - 1	3

Voltage unbalance		
T_{uUM}	T_{uML}	Summation law exponent α
0.8 - 1	0.8 - 1	1.4

Step 1: Planning level

Acquiring the planning level

Step 2: Global emission level

Calculate the global emission level of the MV and LV grid.

LV grid: $G_{xLV} = \sqrt[\alpha]{{L_{xLV}}^{\alpha} - (T_{xML} \cdot L_{xMV})^{\alpha}}$

MV grid and LV gird: $G_{xMV+LV} = \sqrt[\alpha]{{L_{xMV}}^{\alpha} - (T_{xUM} \cdot L_{xUS})^{\alpha}}$

MV grid: $G_{xMV} = \sqrt[\alpha]{{L_{xMV}}^{\alpha} - (T_{xUM} \cdot L_{xUS})^{\alpha} - {E_{xLV}}^{\alpha}}$

Step 3: Characteristics of the system

Estimating the reduction factor K_{xB} of the LV grid

Estimating the allocation factor A_{xMV} for all the emission pertaining to the FCS

Estimating the unbalance factor K_{uE} accounting for the system inherent unbalance

Step 4: Emission level

Emission allocated to the DCFC at Node c: $E_{xc} = \frac{{U_{NLV}}^2}{S_c} \cdot G_{xLV} \cdot \sqrt[\alpha]{\frac{S_c}{S_{tLV}}} \cdot min(\frac{K_{xB}}{X_{hB}}, \frac{1}{X_{hc}})$

Harmonic emission allocated to the FCS at Node i: $E_{hi} = \frac{A_{hMV} \cdot S_i}{\sqrt{X_{hi}}}$

Voltage unbalance emission allocated to the FCS at Node i: $E_{ui} = \sqrt[\alpha]{K_{uE}} \cdot G_{uMV+LV} \cdot \sqrt[\alpha]{\frac{S_i}{S_{tMV}}}$

Flicker emission allocated to the FCS at Node i: $E_{Pxti} = G_{PxtMV} \cdot \sqrt[\alpha]{\frac{S_i}{S_{tMV} - S_{LV}}}$

FIGURE 21. **The procedure for allocating the emission level of the FCS and DCFC. The FCS is connected to the MV distribution grid at Node i where the disturbance emission of the FCS need to be evaluated. The disturbance emission of DCFCs should be assess at their PCC e.g. Node c [29]–[32].**

of FCSs with PQ issue free is the lack of the following, which need much effort.

1) The dedicated PQ standards for evaluating the performance of FCSs. The existing standards might be too conservative for FCSs and DCFCs, especially for the harmonic emission.
2) Study on the coordination of several parallel DCFCs considering the interaction between them to maintain the PQ. At present, the analytical impedance model of the FCS by aggregating the DCFC model has not been proposed. More study is needed on either the impedance model or another approach to model the FCS for the system analysis.
3) The control strategy for the FCS operator that can compromise between decreasing the impact on the grid PQ and the customers' demand on the fast charging.

APPENDIX A. EMISSION LEVEL ALLOCATION

In the IEC 61 000 series [29]–[32], guidelines for allocating the installations' emission levels in the MV and LV environment are introduced. Overall, three stages are provided for the allocation. Among the three stages, Stage 2 is suitable for the installation that is the same as the FCS whose power capacity is high (e.g., 2–3 MW) and high power DCFC. Thus, Stage 2 is briefly summarized hereafter.

As shown in Fig. 21, to allocate the emission level of the FCS in the MV distribution network at Node i and the emission level of the DCFC in the LV distribution network at Node c, the critical four steps are as follows,

1) STEP 1: ACQUIRING SYSTEM PARAMETERS

To plan the emission that can be allocated to the FCS and the specific DCFC, the necessary system parameters are:

- The planning level of the emission to be assessed in different voltage level (i.e. L_{xLV}, L_{xMV} and L_{xUS}), where the subscript x denotes the type of the emission, i.e. h for harmonics, u for voltage unbalance, Pst for short-term flicker and Plt for long-term flicker. For simplicity, the denotations afterward are always the same and explained otherwise.
- The grid harmonic impedance X_h at the MV busbar, the grid harmonic impedance X_{hi} at the PCC of the FCS in the MV distribution grid, the grid harmonic impedance X_{hB} at the LV busbar of the FCS and the grid harmonic impedance X_{hc} at the PCC of the DCFC in the LV distribution grid inside the FCS. The subscript h denotes the harmonic order.
- The maximum power capacity S_{tMV} of the MV distribution network, the maximum power capacity S_{tLV} of the FCS, the agreed power S_i of the FCS, and the agreed power of the DCFCs (e.g., S_c for the DCFC at Node c in Fig. 21).

2) STEP 2: CALCULATING THE GLOBAL EMISSION LEVEL

To derive the emission level allocated to the FCS in the MV grid and DCFC in the LV grid, the global emission levels G_{xMV+LV}, G_{xMV} and G_{xLV}, which signify the emission can be shared by all the MV and LV installations, only the MV installations and only the LV installations respectively, are derived on beforehand. Based on the system parameters acquired in Step 1, these global emission levels can be derived considering the contribution of the disturbance transmitted from the upstream and downstream system.

The equations used for the derivation are shown in Fig. 21 in Step 2 block, where the summation law with the exponent α, the transfer coefficient T_{xML} for the disturbance transferred from the MV grid to the LV grid and the transfer coefficient T_{xUM} for the disturbance transferred from the upstream grid to the MV grid, are applied. The typical value of the T_{xUM}, T_{xML} and α for the different type of emission is given, which is shown at the bottom of Fig. 21.

It is worth noting that to derive the G_{xMV}, the disturbance, E_{xLV}, transmitted from the LV grid to the MV grid is needed. For flicker emission, the E_{PstLV} and E_{PltLV} are neglected because of the LV installations' small power capacity relative to the power capacity of the MV grid. As for the voltage unbalance, the G_{uMV} is not needed as G_{uMV+LV} is used instead. However, the LV grid's harmonic voltage can propagate to the MV grid, and the E_{hLV} need to be estimated. The estimation method is not elaborate here for simplicity.

3) STEP 3: DERIVING THE CHARACTERISTIC PARAMETERS OF THE POWER SYSTEM

In this step, the reduction factor K_{xB} of the LV grid, the allocation coefficient A_{xMV} of the installations in the MV grid, and the inherent unbalance coefficient K_{uE} of the whole MV and LV distribution grid are derived. The methods for derivation are introduced in the IEC 61 000 series, which is not elaborated here for simplicity.

4) STEP 4: DERIVING THE EMISSION LEVEL

Finally, the emission level can be derived with the equations shown in Fig. 21 in Step 4 block. In the equations, the U_{NLV} is the nominal phase-to-phase voltage of the LV grid, and the S_{LV} signifies the power capacity of the installations supplied directly by the other LV distribution grid except FCS. The allocated emission to the installation is dependent on the position of the PCC in the system and the agreed power of the installation.

To maintain the disturbance within the planning level, the emission E_{xi} at Node i where is the PCC of the FCS and emission E_{xc} at Node c where is the PCC of the DCFC need to be maintained below the allocated emission level.

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