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# Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Static Behavior

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**ABSTRACT** Transient simulation of complex converter topologies is a challenging problem, especially in detailed analysis tools like SPICE. Much of the recent literature on SPICE transistor modeling ignores the requirements of application designers and instead emphasizes detail, physical accuracy, and complexity. While these advancements greatly improve model accuracy, they also serve to increase computational complexity, making the resulting models less attractive to application designers. While some authors depart from this trend and present models which emphasize simulation speed, their results and analysis are limited to qualitative observation. This research develops a methodology to quantify the computational cost of model features and competitively benchmark models against each other. Additionally, it reviews recently published SiC MOSFET models and presents a trade study on several candidate models likely to fare well in complex application simulations. Finally, this study also identifies key considerations which should be carried forward into future model design.

**INDEX TERMS** Circuit simulation, convergence, LTspice, semiconductor device modeling, SiC MOSFET, SPICE, transistor modeling.

## I. INTRODUCTION

System models are a vital tool in the development of power electronic applications; they allow designers to optimize system performance [1], analyze electromagnetic compatibility (EMC) [2], and reduce the number of hardware iterations [3], [4]. The usefulness of time-domain system models in these roles is dependent on their accuracy, convergence reliability, and simulation speed. However, there are significant challenges in achieving all three criteria simultaneously [5], especially when modeling fast-switching semiconductors, such as wide-bandgap (WBG) devices [6], or multi-level converter topologies [7]. Because adoption of these two technologies is increasing in industry [1], [8], [9], application engineers have a strong motivation for understanding the performance tradeoffs associated with model design features.

The literature is replete with examples of SiC MOSFETs models. While most papers provide some means of model validation, they generally do not provide any means to quantify the performance of the presented model. The most common model validation technique is graphical overlay of experimental data and simulation predictions, usually for static characterization curves and double-pulse test (DPT) waveforms. However, without quantitative metrics, comparisons between papers is challenging. Inclusion of quantitative metrics, such as the root-mean-square (RMS) error of the forward curve prediction, could improve comparisons between models published by independent groups. Additionally, DPT comparisons provide minimal insight into model convergence or run-time for larger applications [10], so models intended for such applications should be evaluated in more complex

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circuits. This is part of a larger trend in the literature; computational complexity is rarely addressed and is generally limited to qualitative analysis instead of quantitative results.

Because visual comparisons are unsuitable for a detailed evaluation of prior art, this paper undertakes a different approach than a survey paper. Specifically, this paper describes the implementation and quantitative evaluation several recently published SiC MOSFET models in terms of suitability for realistic time-domain converter simulations. While this approach limits the number of models evaluated, it also offers deeper insight into the performance implications of modeling decisions that can be used to inform model selection and future model development.

This work is segmented into two primary domains of MOSFET behavior: static and dynamic. This division of behaviors is well established in the literature [2], [10]–[24], and is used to bisect the scope of this research into two manageable domains. As the conduction branch is a necessary, though not sufficient, condition for time domain evaluations, it will be considered first and form the foundation for a complementary publication. The conduction branch describes the dependence of channel current on gate-source voltage, drain-source voltage, and junction temperature [2]. These characteristics are critical for predicting conduction losses [25]. The complementary publication will investigate the dynamic behavior of the SiC MOSFET, which is critical for determining transient accuracy and switching losses [17].

Additionally, the scope of this study is limited to SiC MOSFET models that have been designed for time-domain application simulations. Further, this analysis emphasizes SPICE simulations, so models compatible or portable to SPICE were selected. These limitations in scope were necessary for clarity and concision.

The contributions of this work are as follows. First, this paper provides a targeted addition to the thorough survey of SiC MOSFET models presented in [26]. Second, it offers a quantitative comparison of recent modeling contributions, which is not possible from casual inspection of the relevant literature. Third, it proposes useful metrics for determining the suitability of MOSFET models for use in application simulations. Fourth, it provides a detailed trade study that quantifies the relative run-time performance of the considered models. From this study, it is identified that several MOSFET models presented recently are suitable for application design. Finally, from the study outcomes, this paper identifies key considerations for future model design. In total, this paper expands the current understanding of MOSFET modeling through quantitative analysis.

This manuscript is organized as follows. Section II provides a targeted survey of SiC MOSFET models relevant to application simulations. Additionally, it introduces the specific models evaluated in this study. Section III demonstrates the static accuracy and fitting difficulty of the models studied. Section IV details the trade study used to evaluate the run-time performance of the models considered. Similarly, Section V describes a focused evaluation of model convergence in application. Finally, Section VI presents the conclusions drawn from this work.

## II. LITERATURE REVIEW

A detailed review of the literature was conducted to identify appropriate candidate models for the study described in this paper. A comprehensive survey on WBG transistor modeling was conducted in 2015 [26], [27], but a significant amount of work has been presented on SiC MOSFET modeling in the last five years. This section offers a targeted extension to the survey of [26], [27] via a brief description of recent progress in SiC MOSFET modeling. This paper adopts the organization of modeling approaches into numeric, semi-numeric, physics, semi-physics, and behavioral categories as previously described in [26], [27]. Because of the emphasis on converter simulations, this review is focused specifically on recent physics, semi-physics, and behavioral models. Many numeric and semi-numeric models have also been presented since 2015, but cataloging their contribution is out of scope for this work. An overview of this targeted literature study is shown in Table 1.

### A. RECENT PHYSICS MODELS

Within the category of physics models, Mukunoki *et al.* present a new model with adjustable channel mobility in [17]. This parameter is used to simplify the computational complexity of the conduction branch without significantly impacting accuracy. Additionally, the model of $C_{GD}$ is expanded by capturing its dependence on $V_{GS}$ via gate-charge measurements under different bias conditions. Mukunoki *et al.* further expand upon this model in [18] by adding the $V_{GS}$ dependence of $C_{GS}$. He *et al*. present a detailed model defined in terms of process and layout parameters [28]. This not only allows accurate scaling to alternate chip dimensions but also enables design optimization by linking the time domain performance to the manufacturing process within SPICE [29]. In [30], Jouha *et al.* extend the McNutt model, originally presented in [31], via a channel length modulation term ($\lambda$). Additionally, the parameter extraction accuracy is improved via the Levenberg–Marquardt (L-M) optimization algorithm. Sakairi *et al*. present a modified version of the Angelov-GaN HEMT model [32] suitable for SiC MOSFETs in [2]. They also extend the static characterization region to the high-voltage, high-current (HVHC) region using analysis of switching transients. Finally, they extend the dynamic characterization to include the change in non-linear capacitance when the device is gated ON. Finally, Shintani *et al.* present a model based on surface potential, considering interface traps, that is fit over wide I-V, C-V, and temperature ranges in [33].

### B. RECENT SEMI-PHYSICS MODELS

Within the category of semi-physics models, there have been a number of important developments in the past five years. For example, in [34], Arribas *et al.* present a simplified version of the Shichman–Hodges' model [37] (Level 1). This adaptation

**TABLE 1** Recent SiC Power MOSFET Models

| First Author | Year | Model Level | Contributions | Sim. Tool |
|---|---|---|---|---|
| Mukunoki [17], [18] | 2016, 2018 | Physics | Adjustable channel mobility, $C_{GS}$ & $C_{GD}$ dependence on $V_{GS}$ | ANSYS Simplorer |
| He [28] | 2017 | Physics | SPICE model defined in detail by process and layout parameters | Not indicated |
| Jouha [30] | 2018 | Physics | Extends [31] via λ and L-M Optimized Parameter Extraction | Not indicated |
| Sakairi [2] | 2018 | Physics | Adapted Angelov GaN HEMT Model for SiC MOSFET, extend static characterization to HVHC region, characterize CV with device gated on | ADS |
| Shintani [33] | 2018 | Physics | Surface potential based model | SIMetrix |
| Arribas [34] | 2015 | Semi-Physics | Adapts Level 1 model for simpler extraction | LTspice |
| Fu [35] | 2015 | Semi-Physics | Introduces simplified description of JFET region | PSpice |
| Zhou [36] | 2018 | Semi-Physics | Extends Level 1 model to include effect of interface traps | LTspice |
| Riccio [19] | 2018 | Semi-Physics | Extends [20] with thermally dependent $I_{LEAK}$, out-of-SOA, and mobility degradation | SIMetrix |
| Mukunoki [21] | 2018 | Behavioral | Expanded output characterization to include $V_{DS}$ of 200 to 800 V | ANSYS Simplorer |
| Sochor [4] | 2019 | Behavioral | Continuous and widely defined equations for speed and accuracy | Not indicated |
| Li [10] | 2019 | Behavioral | Continuous model definition across all domains | PSpice |
| Endruschat [22] | 2019 | Behavioral | Universal FET model defined by simple equations and parameter tables | LTspice |

of the Level 1 model benefits from a simplified extraction process by removing reliance on empirical parameters unknown to the end user. In [35], Fu *et al.* simplify a model presented in their prior work [38] by modeling the JFET region of the SiC MOSFET with a dependent voltage source rather than a resistive network. Zhou *et al.* provide a modified Level 1 model that captures the influence of interface traps in [36]. This contribution is relevant for modeling SiC MOSFETs because interface traps are more prevalent in the SiC/$SiO_2$ interface than in Si/$SiO_2$. Riccio *et al.* extend the work originally published in [20] to include leakage over temperature, avalanche and short-circuit behavior, and mobility degradation dictated by high electric fields [19].

### C. RECENT BEHAVIORAL MODELS

Significant developments have also occurred within the category of behavioral models in the last several years. For example, Mukunoki *et al.* replace the physics-based conduction model of [17], [18] with a behavioral description in order to improve the run-time performance and remove proprietary geometric data from the modeling process in [21]. Additionally, this paper extends the static characterization of the model to include $V_{DS}$ from 200 to 800 V via load-short-circuit waveforms. In [4], Sochor *et al*. present a behavioral model in which drain current and interelectrode capacitances are defined by an ensemble of continuous equations with many parameters. These authors extend their static characterization of the considered devices of the considered devices to 800 V using the methodology identified in [2]. Additionally, these authors claim that explicit, continuous, and differentiable equations are optimal for simulation speed and robust convergence.

Li *et al.* develop a behavioral model that is continuously defined across all operating conditions, avoiding segmentation between domains [10]. These authors also propose a novel approach to model thermal dependence, in which $V_{GS}$ and $V_{DS}$ are scaled and shifted before calculating drain current. Endruschat *et al.* present a modified version of the Curtice model, originally published in [23], that is sufficiently flexible to accurately represent the behavior of GaN HEMTs or SiC MOSFETs in [22]. This model is implemented with simple analytical equations and parameters defined across operating conditions via lookup tables, which the authors recommend for fast simulation characteristics.

### D. MODELS SELECTED FOR TRADE STUDY

Of the models reviewed in the previous section, there are many excellent candidates for inclusion in a trade study of available SiC MOSFET models. However, only a subset of these models could be studied in this work. Accessibility of the models was a primary consideration, as not all models are published with sufficient detail to be reproduced. Another goal of the proposed study is to understand the tradeoffs between behavioral and physics-based models, which requires selection of at least one relevant model of each type. It is acknowledged that different types of models are suited for different purposes, and that designers should consider their modeling goals during model selection rather than focusing exclusively on quantitative metrics. Nevertheless, it is beneficial for practitioners to understand the computational and accuracy implications of model type selection.

Behavioral models may be the best choice for general application development due to their computational advantages. However, there can be subtle challenges with this type of model. For example, since behavioral models are usually defined and calibrated within the device safe operating area (SOA), they may produce inaccurate and misleading results during fault conditions such as avalanche, over-current, or gate stress. While additional behavior can be defined to capture fault conditions [19], each addition requires additional modeling effort to capture and also increases model complexity.

In addition, physics models can contain built-in dependence on process parameters. Studies involving variation in these parameters are of interest for device designers as they have important system performance implications. For example, in a

**TABLE 2 Models Selected for Trade Study**

| First Author | Model Title | Year | Description of Conduction Model |
|---|---|---|---|
| Sun [39] | Semi-Physics | 2014 | Level 1 model with ancillary features |
| Li [10] | Non-Segmented | 2019 | Behavioral current source with continuous definitions |
| Endruschat [22] | Modified Curtice | 2019 | Behavioral current source with parameter lookup tables |
| Hossain [46] | Physics | 2018 | Physically accurate description suitable for transient simulations |

topology with multiple devices in parallel, current sharing will be heavily influenced by small differences in $R_{DS(ON)}$ or $V_{TH}$ between parallel devices. Because physics models can include process parameter dependencies, known statistical variance in these parameters can be included in the composition of the model to determine the expected impact of such parameters on the resulting variance of $R_{DS(ON)}$ or $V_{TH}$ values [29]. Such a correlation is not practical to perform using behavioral models. Overall, the required features and appropriate metrics for models should be considered in light of their intended usage. The compact models selected for this study were chosen to represent a variety of features, implementation methods, and design goals.

The first model selected, referred to as the semi-physics model throughout this discussion, was presented by Sun *et al.* in [39]. It is a classical physics model that is adapted into a semi-physics model through the addition of auxiliary behavioral components. This is a common approach in the literature [14]–[16], [34], [36], [39]–[42]. The model core used in [39] is the Level 1 model. The Level 1 model does not capture the soft saturation characteristics of long channel devices [43], which is common among SiC MOSFETs. However, the Level 1 model offers substantially better run-time performance than alternative semi-physics models such as the Level 3 model [44]. The authors improve upon the conduction behavior of the Level 1 model through three additional thermal elements: a threshold voltage ($V_{TH}$) shift, variable drain resistance ($R_{DS}$), and current offset. Additionally, they use a standard diode model for third quadrant characterization.

The second model selected, referred to as the non-segmented model throughout this discussion, was presented by Li *et al.* in [10]. The non-segmented model is one of the most recent behavioral models published for describing the SiC MOSFET. The design of this model prioritizes run-time performance and convergence behavior, so this model is especially suitable for application simulations. The conduction branch of the non-segmented model is derived from a description of the transfer characteristic, originally presented by Angelov *et al.* [45], multiplied by a $V_{DS}$-dependent scaling equation. The authors stress the importance of using continuous equations to describe the static characteristics of the conduction branch as it transitions through cutoff, linear, and saturation regions. They claim that this continuous definition is optimal for more complex circuit simulations.

The third model selected, referred to as the modified Curtice model throughout this discussion, was presented by Endruschat *et al.* in [22]. This model is also one of the most recent behavioral models published in the literature, and its design prioritizes run-time performance and convergence behavior. The modified Curtice model is primarily designed for the GaN HEMT but is also described as a universal FET model. In [22], the authors support this claim by providing an example fitting of this model to the characteristics of a SiC MOSFET. The modified Curtice model uses parameter lookup tables defined at discrete operating conditions in order to capture device behavior. In order to determine the table values, the output equation is independently fit at each $V_{GS}$ bias condition represented in the forward curves. This streamlines the extraction process but does not guarantee the continuity achieved by the global approach of the non-segmented model. Therefore, each behavioral model is the result of fundamentally different assumptions.

The fourth and final model selected, referred to as the physics model throughout this discussion, was presented by Hossain *et al.* in [46]. The physics model was adapted for LTspice from Mudholkar's Saber model presented in [47]. This model captures soft saturation, variable capacitance (CV), temperature dependence, and self-heating effects. Additionally, it follows a simple parameter extraction sequence and avoids the need for proprietary process details by numerically fitting parameters such as base doping concentration, active area, and gate-drain overlap active area. The CV characteristics are modeled independently from the conduction characteristics and therefore can be fit separately. This independence was a key motivation in selecting this specific physics model as it allowed isolation of the conduction branch for this study.

In this paper, several metrics are used to evaluate the suitability of each model's conduction branch for converter simulations. First, the computational difficulty of fitting each model to empirical data is considered. Second, the RMS error of the simulated forward and transfer curves is used to quantify the accuracy of conduction predictions. Finally, the relative run-time performance of each model is evaluated through a detailed trade study.

## III. STATIC DOMAIN MODEL PERFORMANCE

### A. FIT APPROACHES AND CHALLENGES

In this section, the process of tuning each model to a common set of static characterization data is described. The static characterization data utilized for this purpose was obtained by the authors through measurement of a 1.2 kV, 25 mΩ SiC MOSFET sample (Cree C2M0025120D) [48]. While the same experimental data was used for tuning each model, a unique methodology for fitting each model is required due to their inherent differences. One of the primary strategies used to fit these models is global optimization (GO). GOs minimize a particular objective (such as RMS error of the forward curves) while evaluating various parameter sets. The method for determining the next parameter set can vary drastically between approaches (such as the genetic algorithm or particle swarm). In

general, GOs are slow to converge but have the advantage that they are resistant to selecting local minima. Multi-objective GOs, which create a Pareto optimal front, were not used in this work due to their high computational cost. The other class of algorithms employed in this work are from MATLAB's curve fitting toolbox. These algorithms minimize error between a predictor function and a two-dimensional dataset, rather than a single objective. While much faster than GOs, these algorithms are likely to select local minima. Finally, some parameters were derived analytically from the experimental data.

The Level 1 core of the semi-physics model cannot reliably be fit by simple algorithms because it has a relatively small number of interlocked parameters which determine its output over all regions with many local minima. Thus, a global optimization routine is used to fit the model to the forward and transfer data individually. The solver iterates between each characteristic, slowly approaching a parameter set which suitably predicts both. The preferred approach for fitting this type of model is to establish process parameters, such as channel length, from the device design. However, this proprietary information is unknown for the device under consideration. Instead, several values from a reasonable range were used as a starting point for tuning the remaining parameters. After tuning, the model variant with the lowest computed error was selected. For this model, elevated temperature behavior is represented by a $V_{TH}$ shift, $R_{DS}$ increase, and current offset. These parameters are independent of the Level 1 core and can be calculated from the experimental data.

A distinct advantage of the modified Curtice model is the simple process used to fit its parameters to experimental data. The characteristic conduction equation is independently curve-fit to each series of the forward data. The resulting parameters are then stored in a lookup table which SPICE linearly interpolates. Despite the simple tuning process, the modified Curtice model has several challenges. First, because the model is not tuned to the transfer data, the forward curves must have a small step between $V_{GS}$ values to achieve an accurate fit, which limits the possibility of using datasheet curves. Another challenge is that the characteristic conduction equation has many degrees of freedom and can easily become trapped in local minima, especially if the forward conduction data does not extend into the saturation region. For 1.2 kV SiC MOSFETs, saturation current at high $V_{GS}$ is often three times the current rating of the device. Pulsed curve tracer measurements at these operating conditions can suffer from inaccuracies due to device self-heating. Because the experimental data used in this study was limited to 100A, the modified Curtice model required additional manual tuning above $V_{GS}$ values of 10 V. The elevated temperature features of the modified Curtice model are implemented with a $V_{TH}$ offset, an $R_{DS}$ increase, and two parameter shifts within the condition equation. For this study, the necessary $V_{TH}$ and $R_{DS}$ changes were calculated from the experimental data while the parameter shifts were manually tuned.

The non-segmented model is first fit to the transfer data at low $V_{DS}$ bias (3 V was chosen in this work). Next, a scaling equation adjusts the transfer characteristic across $V_{DS}$. While the original authors [10] used a global optimizer to fit the scaling equation, this is a computationally intensive process. Leveraging the tuning framework developed for the modified Curtice model, the scaling equation was instead fit independently at each $V_{DS}$ value. The resulting parameter values were then fit with a continuous equation to match the original implementation. Altering the original model to use a different equation is a necessary step for using the non-segmented model. For users without access to the specialized modeling software used by the authors of the original manuscript, this approach is faster and provides more accurate results than a globally optimized equation. The thermal model requires global optimization due to the universal influence of shifting and scaling $V_{GS}$ and $V_{DS}$ in the calculation of drain current.

Unlike the other models, which were tuned using MATLAB's curve fitting toolbox, the physics model was tuned in IC-CAP with a combination of manual and automated steps. The manual tuning steps are conducted in order to identify parameter boundaries and avoid local minima. The physics model is tuned sequentially by first fitting threshold and transconductance parameters from the transfer characteristic data, followed by fitting the remaining conduction parameters to forward characteristic data. While this process requires fewer function evaluations than tuning the semi-physics model, it is nevertheless more challenging than tuning either of the two behavioral models. One benefit of the physics model tuning process is that it requires substantially less experimental data than tuning of the behavioral models.

There is significant variance in the computational requirements of tuning the four models considered in this study. If sufficient experimental data is available, the modified Curtice model is the least computationally expensive to tune overall. Tuning the non-segmented model at 25 °C with the proposed technique is also extremely efficient. However, tuning the thermal parameters of the non-segmented model is very expensive since it requires global optimization. The complexity of tuning the physics model is somewhere in the middle of the other models. The semi-physics model is the most computationally intensive model to fit as it requires global optimization for all parameters.

### B. FIT PERFORMANCE COMPARISON

The experimental data was collected using a Keithley Semiconductor Characterization System (SCS), shown in Fig. 1. Pulse time was set to 300 $\mu$s with the sampling window centered at 150 $\mu$s. The sampling window was adjusted to 50 $\mu$s for operating conditions greater than 10 V and 50 A to minimize inaccuracy due to self-heating at higher power levels. These sampling windows were identified and validated using an oscilloscope which monitored the experiment. For elevated temperature, a hotplate was used to heat the device, with temperature validated at the device. It is noted that the presented data in is a subset of the collected data, which was selected for clarity of comparison. The full dataset contains twenty-five $V_{GS}$ operating conditions for the forward curves

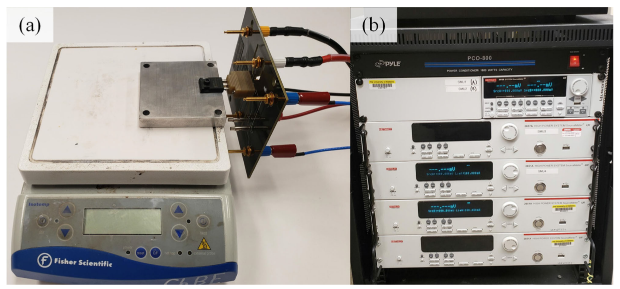



**FIGURE 1. Experimental test setup, (a) C2M0025120D mounted to hotplate, (b) Keithley Semiconductor Characterization System (SCS).**

and fourteen $V_{DS}$ operating conditions for the transfer curves. The full dataset is used for the fitting and RMS error evaluation of all models described in this manuscript.

In Fig. 2, the simulated conduction behavior at 25 °C is overlaid with the experimental data for each of the four models. The semi-physics model predicts hard saturation at higher currents, whereas the experimental data demonstrates soft saturation. This discrepancy reveals the primary limitation of the Level 1 conduction model and significantly penalizes the model's fidelity to SiC MOSFET behavior at high $V_{DS}$. The non-segmented model has the most accurate agreement for both the forward and transfer characteristics at 25 °C. The modified Curtice predicts the forward characteristics precisely but models the transfer characteristics somewhat less accurately. The transfer accuracy of this model could be improved by reducing the size of $V_{GS}$ step for the forward measurement to less than 1 V. Finally, while slightly less accurate than the behavioral models, the physics model also predicts the forward and transfer characteristics accurately.

The modified Curtice model's predicted transfer characteristics demonstrate several unexpected features. First, the predicted transfer curve at $V_{DS} = 2V$ shows an unusual deviation from the experimental data between $V_{GS} = 8\ V$ and $V_{GS} = 10\ V$. This result indicates that the parameters for $V_{GS} = 9\ V$ fit the forward curve poorly at low values of $V_{DS}$. This corresponds to the tuning algorithm accurately fitting the saturation region and poorly fitting the linear region. There is likely a different set of parameters that could resolve this discrepancy, but the flexibility of the conduction equation combined with the soft saturation of SiC MOSFET devices makes this problem challenging to eliminate systematically. The other unexpected feature of the transfer prediction for the modified Curtice model is the piecewise linear fit at $V_{DS} \geq 4\ V$.

This is a result of the manual tuning performed due to the limited current range of the experimental data. This problem would likely be resolved with the availability of additional experimental data.

Visual overlays such as those shown in are often the only validation presented for conduction models in the literature. In order to add quantitative analysis for both validation and comparison, specific accuracy metrics are required. In this study, RMS error is selected as the principal figure of merit for evaluating the accuracy of each model under consideration. This figure of merit is calculated from equation (1):

$$E_{RMS} = \sqrt{\frac{\Sigma_{i=1}^{n}\left(y_{exp,i} - y_{sim,i}\right)^2}{n}} \quad (1)$$

where n is the number of data points, $y_{exp}$ is the value measured in experiment, and $y_{sim}$ is the value predicted by simulation. Fig. 3 shows the RMS error of each considered model at three temperatures: 25 °C, 100 °C, and 150 °C. One RMS error value is computed for each curve of the forward and transfer characteristics. Thus, forward curve error is plotted as a function of $V_{GS}$ and transfer curve error is plotted as a function of $V_{DS}$. Additionally, RMS error values are computed for all available characterization data, including the curves omitted from.

Analysis of the forward error reveals that the semi-physics model demonstrates significant error near $V_{GS}$ of 8 V, which is a result of the hard saturation behavior predicted by the model. This trend is also observed in the transfer data above 15 V. As anticipated from the visual overlay, the non-segmented model demonstrates the lowest error at 25 °C and is closely followed by the modified Curtice model. The physics model has a slight increase in error at high $V_{GS}$ due to a modest mismatch in predicted $R_{DS(on)}$. The RMS error of transfer curves is relatively high for all models at values of $V_{DS}$ greater than 10 V. The semi-physics model exhibits the highest error in this region due to its incorrect prediction of hard saturation behavior. Additionally, Fig. 3 shows that the approach used by the non-segmented model for elevated temperature is significantly outperformed by the simpler thermal model used by the modified Curtice model. The thermal model of non-segmented model does not accurately predict the transfer curves for multiple $V_{DS}$ bias conditions because the increased channel resistance at high temperature is modeled by shifting and scaling $V_{DS}$. While this approach is able to predict the transfer characteristics very accurately at a single $V_{DS}$ bias condition, fitting multiple bias conditions simultaneously is not possible. The physics model, which is fit at all temperatures simultaneously, performs reasonably well at all temperatures. All the models demonstrate relatively high error for $V_{GS} = 8\ V$ at 150 °C. Overall, the modified Curtice is the most accurate model for predicting the conduction behavior of the considered SiC MOSFET at elevated temperature.

Fig. 4 presents the mean RMS error for each of the models at each temperature, calculated from the results shown in Fig. 3 using (1). This representation confirms that the RMS error of the non-segmented is lowest at 25 °C but increases substantially at elevated temperature. Additionally, the Curtice model exhibits only a modest increase in RMS error with temperature. Finally, the semi-physics model demonstrates the highest average error for all considered conditions.

Fig. 4 also presents a comparison of the cumulative me an RMS error for the forward and transfer curves of the models, the values for which are computed from the results of the first

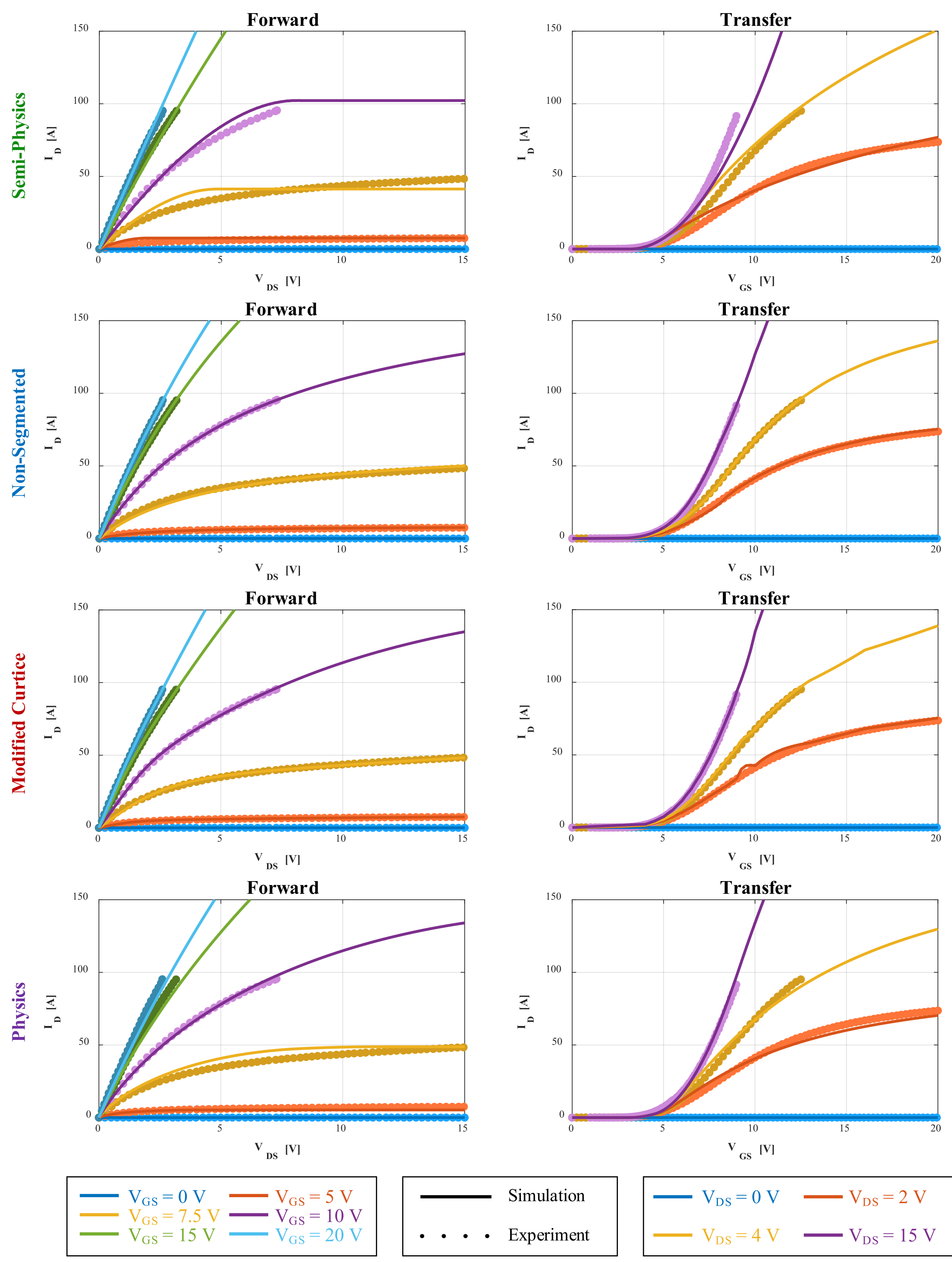



**FIGURE 2.** Static domain model overlay at 25 °C.

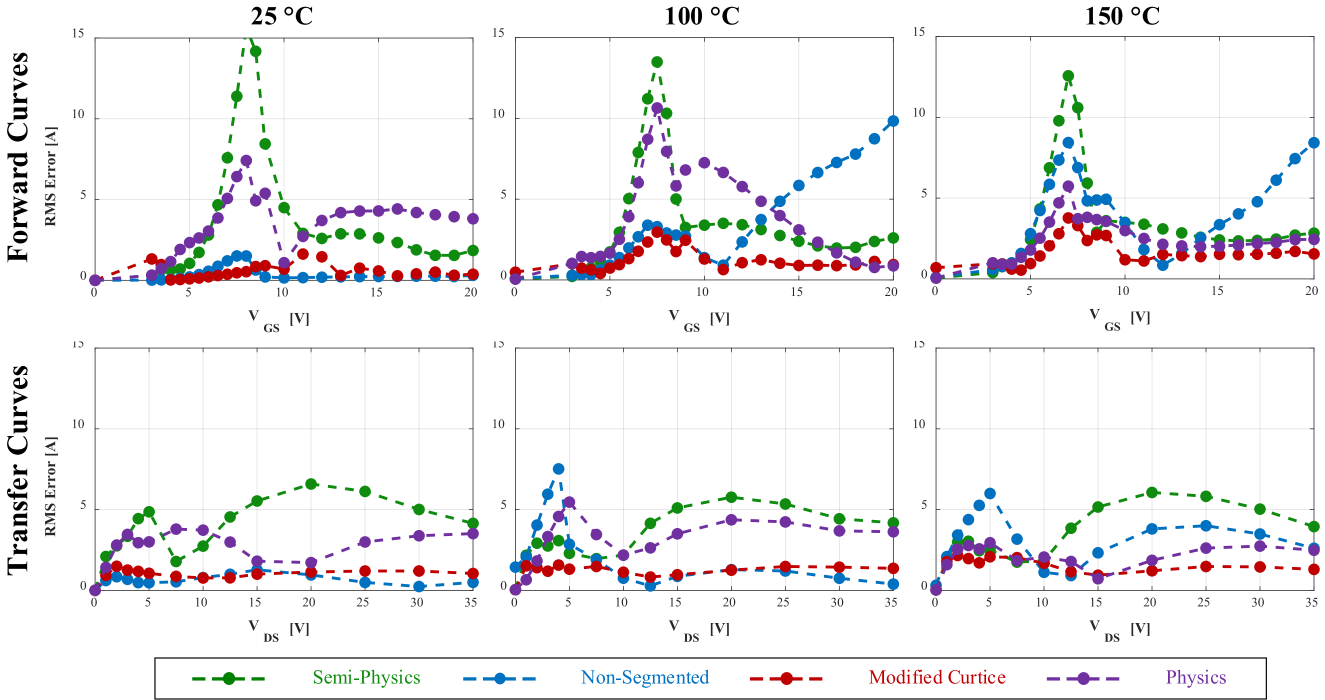



**FIGURE 3.** Equivalent RMS error for each conduction model at each temperature.

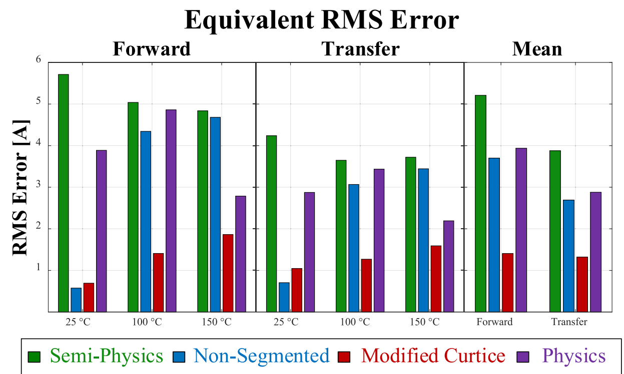



**FIGURE 4.** Equivalent RMS error for (a) forward, (b) transfer, and (c) mean over temperature.

two subplots of Fig. 4 using (1). This comparison can be used to rank the models by accuracy. The modified Curtice model demonstrates the lowest RMS error overall, followed by the non-segmented model due to its significantly increased error at elevated temperature. The physics model has slightly higher error than the non-segmented model but, due to its more accurate prediction of soft-saturation, significantly outperforms the semi-physics model, which produces the highest RMS error.

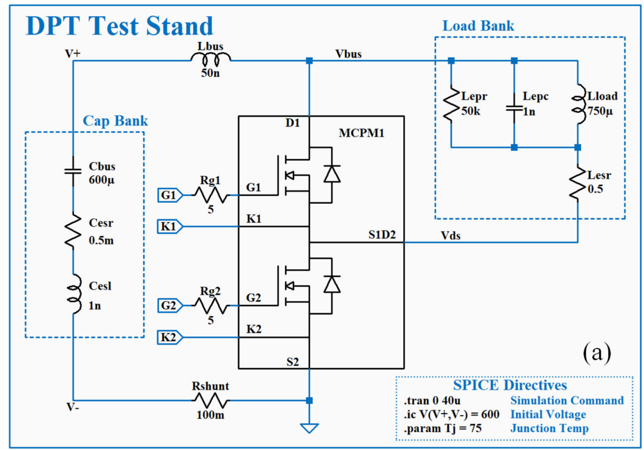
## IV. COMPUTATIONAL TRADE STUDY

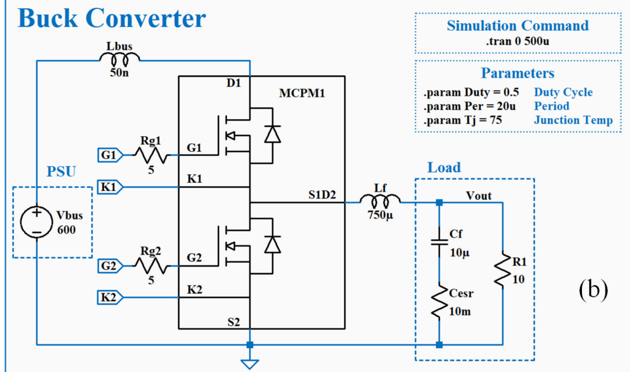
### *A. OVERVIEW OF SIMULATION STUDY*

Accuracy is a necessary but insufficient condition for establishing the suitability of a model for application simulations. Critically, models that do not converge, or that are unreasonably slow to do so, are of minimal benefit to application design. Therefore, a study was designed to quantitatively evaluate the relative computational performance of the considered models. MATLAB was used to build the simulations from templates, add circuit parameters, and execute LTspice via batch commands, as originally demonstrated in [41]. More than 250,000 unique simulations were run in the course of this work. All the models considered in this study were modified to use an identical interelectrode capacitance model, implemented with two behavioral current sources (for $C_{DS}$ and $C_{GD}$) and a static capacitor for $C_{GS}$. It is noted that the dynamic behavior of the models under study is out of scope for the present paper, but this alteration is required for a normalized comparison of the static conduction behavior of these models. To contextualize these results, the model provided by the SiC MOSFET device manufacturer was also included in the study [48].

Many commercial, free, and open source simulator platforms have been developed for SPICE. Selection of a platform is a necessary limitation of this analysis, but while the specific results of this paper will be contextualized within the LTspice platform, the relative performance of these models is likely to be similar in other simulators. The accessibility of LTspice, as well as its popularity for power electronics applications, make it an excellent choice for this analysis. Readers who wish to leverage this framework will also be able to conduct analysis in LTspice for direct comparisons to these results.

Three application simulations were developed for this study. First, a double-pulse test (DPT) circuit, shown in



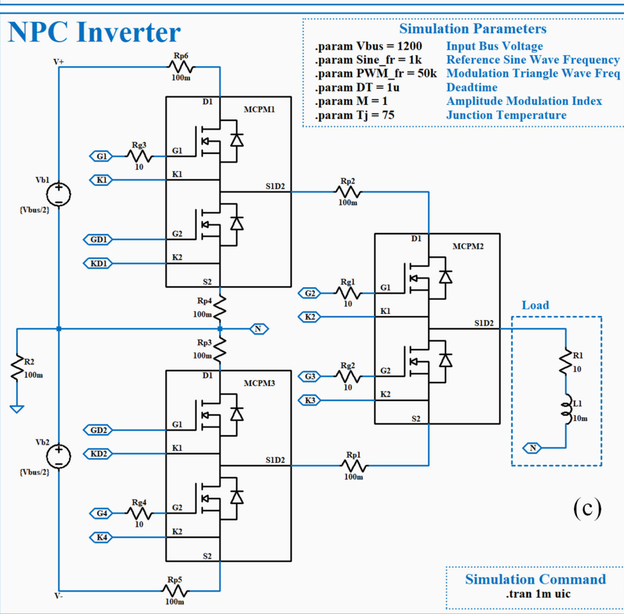




FIGURE 5. Schematic templates: (a) DPT, (b) buck converter, and (c) NPC inverter.

Fig. 5(a), was included for its simplicity and ubiquity. The DPT simulation was evaluated over a 40 $\mu$s transient duration. A notable feature of the DPT simulation in this study is the use of a charged capacitor bank rather than an ideal voltage source for the power supply. This setup reflects a common implementation of DPT testbed hardware but is more computationally complex than using an ideal voltage source. Second, a buck converter, shown in Fig. 5(b), was included to present a simple continuous converter simulation. Because this simulation has similar complexity to the DPT example but much longer transient duration (500 $\mu$s), it minimizes the influence of the operating point solution and startup. Third, the single-phase neutral-point-clamped (NPC) inverter, shown in Fig. 5(c), was included. The NPC inverter is the most complex simulation example considered in this study both because it is a multi-level topology and because it operates over the longest transient duration (1 ms). In addition, the NPC simulation is likely of the most interest to perspective application designers because it is comparable in complexity to many practical topologies. The NPC inverter simulation example demonstrated here was developed during the design of the SiC-based NPC prototype converter described in [49]. For each simulation evaluation, the circuit's operating conditions and specific parasitic element values were randomized between 40% and 160% of the nominal values shown on their respective schematics.

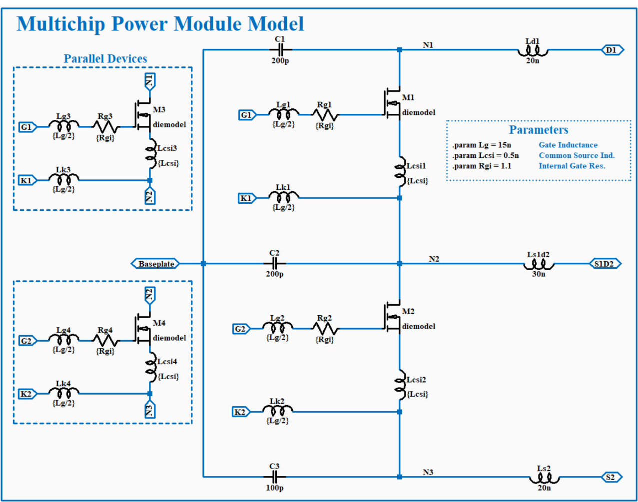



FIGURE 6. MCPM package model.

In the context of modular multi-level converters and similar practical topologies [50], the NPC example shown here is still a relatively modest simulation. Rather than developing additional unique converter templates, the multichip power module (MCPM) component shown in these examples was used as a modular building block. By changing the number of paralleled SiC MOSFET die at each switch position within this package, the complexity of the simulation can be granularly controlled, and larger converter topologies can be readily synthesized. Fig. 6 shows an example design of the MCPM component with two paralleled die per switch position. During this study, modules were simulated with 1, 2, 4, 8, 16, and 32 paralleled die per switch position. Each parallel device was fitted with individual circuit parasitics, as shown by the "Parallel Device" in Fig. 6.

In order to directly study the computational impact of combining SiC MOSFET devices in series, an additional module

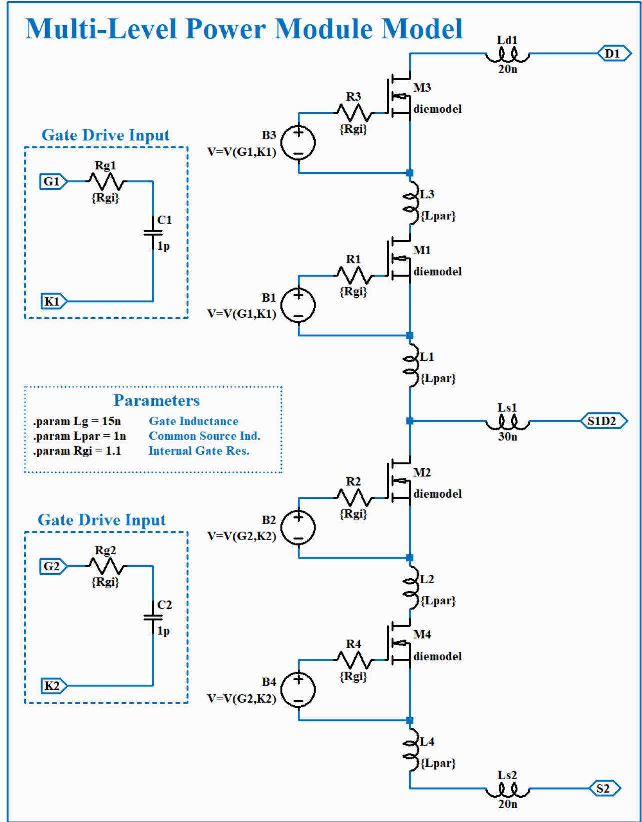



**FIGURE 7.** Multi-level MPCM package model.

type was introduced: the multi-level MCPM. Fig. 7 shows an example design of the multi-level MCPM with two series die per switch position. During this study, multi-level modules were simulated with 2, 4, 8, 16, and 32 series-connected die per switch position. Due to the computational complexity of this configuration, of the application simulations, only one was analyzed during this phase of study. Thus, these simulations utilize the DPT application circuit with a 40 $\mu$s transient duration. While these simulations do not directly represent a specific converter design, they provide a simple and effective mechanism for evaluating the performance of simulating an arbitrary number of converter levels.

Because of their strong influence on run-time, the simulation environment settings are critical. While LTspice users often leave the solver, integration method, and SPICE options set to their default values, these settings are rarely optimal for simulation run-time and convergence, especially for power electronics. Table 3 shows the SPICE configuration settings used in this simulation study, many of which were recommended for simulations utilizing the SiC MOSFET manufacturer model [51]. These selections play a critical role in determining the simulation time and were maintained for all models. It should be noted that these specific parameter values favor speed and convergence over accuracy and may not be optimal for all simulations, as discussed in Section VI. These options can be configured in the control panel within

**TABLE 3** SPICE Solver Parameters

| Class | Variable | Value |
|---|---|---|
| Engine and Solver | Solver | Normal |
| | Max Threads | 8 |
| | Matrix Compiler | Object Code |
| | Thread Priority | High |
| | Integration Method | Gear |
| | Noopiter | True |
| | Skip gmin Stepping | False |
| | gmin | $10^{-9}$ |
| Simulation Tolerance | abstol | $10^{-6}$ A |
| | chgtol | $10^{-12}$ c |
| | reltol | $10^{-3}$ % |
| | vntol | $10^{-3}$ V |
| Iteration Limits | itl1 | 1000 |
| | itl2 | 1000 |
| | itl4 | 1000 |
| | itl6 | 1000 |

LTspice or via a .option directive in the schematic. The maximum thread count specified in Table 3 is eight, which is the maximum for the CPU utilized in this study (Intel i7-7700k). Finally, the version of LTspice used in this analysis is Version XVII, update 11/06/2019.

### B. RESULTS OF SIMULATION STUDY

Fig. 8 shows the run-time performance for each model described in Table 2 and each topology shown in Fig. 5. The y-axis shows the average elapsed time per simulation while the x-axis shows the number of devices per switch position. For accuracy and consistency, the run-time for each simulation was extracted from the LTspice log file. Since each configuration exhibits run-to-run variance (even when limiting background computing tasks), each value shown is this figure represents the average of at least one hundred LTspice simulations. It is noted that a few points are omitted from the manufacturer model results due to convergence failures in these simulations, even with the relaxed tolerances described in Table 3.

The first three simulations of Fig. 8 (DPT, Buck, and NPC) clearly demonstrate the impact of increasing application complexity. As converter models increase in simulation time, number of devices, and topology levels, the corresponding run-time changes from under a second to over an hour. This demonstrates the critical role of simulation optimization in determining model usability and the motivation for identifying computational tradeoffs in model design. Designers should attempt to identify the level of complexity for the application topology under consideration when selecting an appropriate MOSFET model.

Additionally, a general trend emerges within the context of a given application example. On average, the marginal computation cost for adding parallel die is slightly greater than 1:1. In other words, doubling the number of paralleled devices more than doubles the simulation run-time. While this relationship is not perfectly consistent (especially in the difference of 1 and 2 devices), it is generally applicable across the

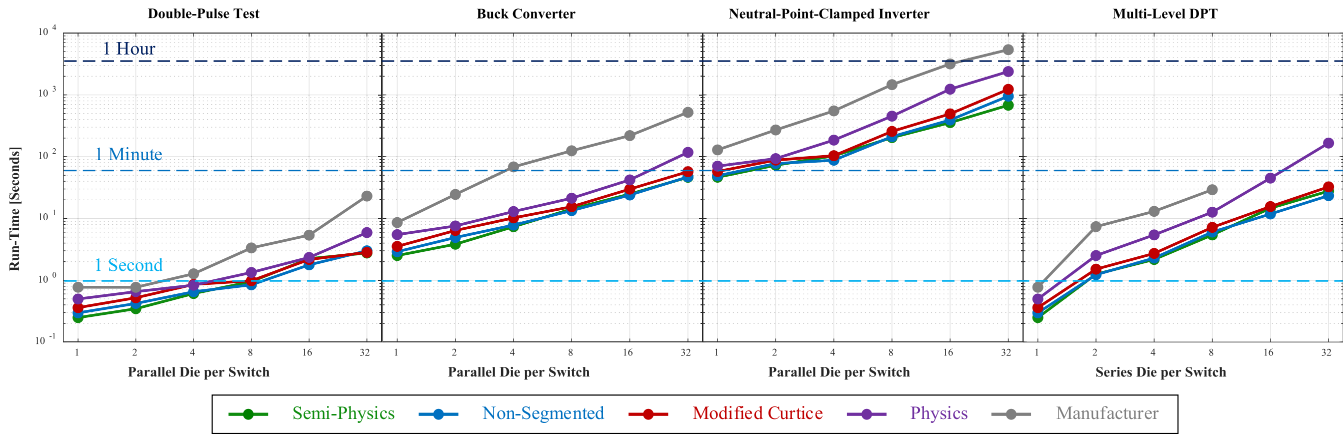



**FIGURE 8.** Mean run-time of the transistor models in four converter applications.

models, number of devices, and applications considered here. This relationship, however, is closer to 1:4 for the multi-level DPT application. Thus, while doubling the number of devices in parallel approximately doubles the run-time, doubling the number of devices in series increases the runtime by a factor of 8. This is because the multi-level design increases the number of interdependent nodes, and SPICE simulations are fundamentally solved through nodal analysis [52]. Thus, simulation complexity increases more quickly with the number of series devices than the number parallel devices.

Analyzing particular configurations within Fig. 8 provides additional insight into computational complexity trends. For example, the single-die DPT results reveal why this setup is insufficient for analysis of model run-time. For this configuration, the fastest model takes approximately 0.25 seconds to complete the simulation on average while the slowest model takes 0.78 seconds; such a difference is unlikely to be noticed by the user, even though there are significant performance differences between these models. Analysis of the buck converter configuration begins to reveal these differences. In this configuration, the fastest model takes approximately 2.5 seconds to complete, while the slowest model takes 8 seconds. Further, if the buck converter is simulated with the 32 transistor MCPM model, the semi-physics model completes the simulation in 46 seconds while the manufacturer model takes longer than 8 minutes. Evaluating the single die configuration of the NPC inverter reveals that employing a behavioral model can reduce simulation run-time by 70% compared to the manufacturer model.

A result that may be unexpected is that the semi-physics model is marginally faster than the behavioral models, despite using a more mathematically complex description. This is likely the result of internal optimization for the Level 1 MOSFET model within SPICE, which is not applicable when utilizing arbitrary sources. This improvement, although modest, is repeatable and generally consistent across the cases considered here. The non-segmented model follows closely in second place with a run-time penalty of 5% over the semi-physics model on average. It has a slight advantage in run-time,

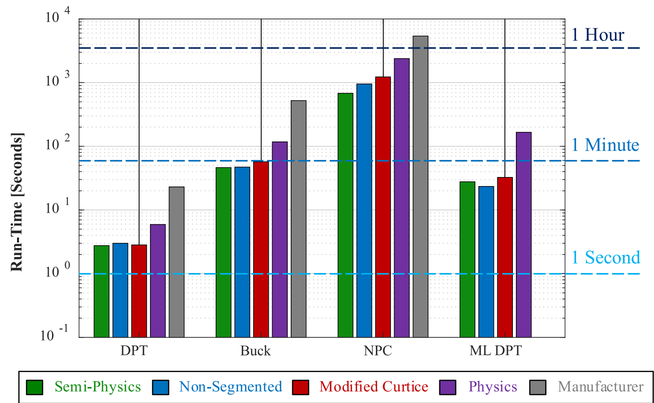



**FIGURE 9.** Mean run-time for each model and application with 32 die per switch position.

however, over the third-place modified Curtice model, which on average incurs a 28% run-time increase over the semi-physics model. The run-time difference between the non-segmented and modified Curtice models indicates that the focus on model flexibility comes at a modest penalty compared to focusing on model continuity. Finally, while the physics model is slower than the simplified transistor models, it outperforms the manufacturer model by a wide margin.

Fig. 9 shows a subset of the run-time results for the 32 die per switch-position configuration of each example application. This comparison better illustrates the relative performance specific to each model. For the NPC with 32 die, the run-time difference is 90 minutes for the manufacturer model versus 11 minutes and 20 seconds for the semi-physics model.

Fig. 10 shows the run-time (normalized by total SPICE iterations) versus matrix size for the NPC converter. In this analysis, the runtime increases with matrix size as $\mathcal{O}(N^{1.28})$ to $\mathcal{O}(N^{1.67})$. This range is in reasonable agreement with previous studies on the computational complexity of SPICE solvers. For example, Krapre reports that simulation run-time increases with circuit size as $\mathcal{O}(N^{1.2})$ for sequential matrix operations, which can be driven as low as $\mathcal{O}(N^{0.7})$ for optimized parallel computing architectures [53]. However, scaling

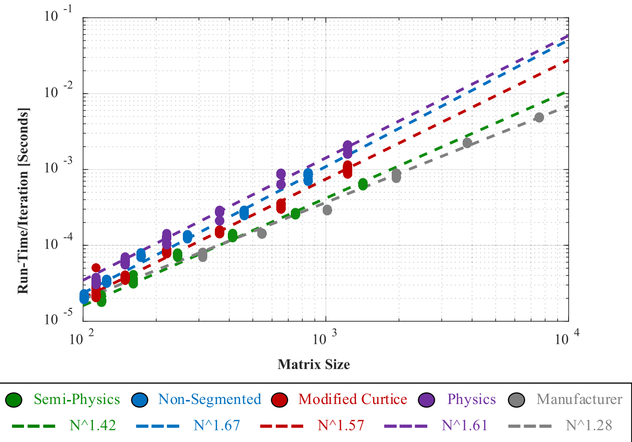



**FIGURE 10.** NPC simulation complexity, run-time versus matrix size.

**TABLE 4** Convergence Study

| Multi-Level DPT | | | |
|---|---|---|---|
| Die Per Switch Position | Default SPICE Options | Options Shown in Table III | Skip Initial Operating Point Solution (& Idealized Capacitor Bank) |
| Single | Convergent | Convergent | Convergent |
| 2 | Failure | Convergent | Convergent |
| 4 | Failure | Convergent | Convergent |
| 8 | Failure | Marginal[1] | Convergent |
| 16 | Failure | Failure | Convergent |
| 32 | Failure | Failure | Convergent |

1. Marginal Success: only convergent for DC operating points less than 10% rated voltage.

factor versus circuit size is best approximated by number of equations [54], which is not linearly related to matrix size. Since LTspice utilizes a proprietary parallel processing package [55], it is expected that the complexity dependence on circuit size falls between $\mathcal{O}(N^{0.7})$ and $\mathcal{O}(N^{1.2})$, while the complexity dependence on matrix size is slightly higher.

## V. CONVERGENCE STUDY

Unlike simulation run-time, convergence behavior does not scale predictably with the complexity of the model. This is in part because convergence is highly dependent on the SPICE simulation options as well as the circuit topology. It would be convenient to develop a simplified metric to quantitatively rank the relative convergence of the models considered in this study. However, such a metric is unlikely to generalize well. This metric would reflect the specific topology and simulation settings applied rather than providing much insight into the relative convergence of the models under consideration. Thus, a case study was conducted to evaluate trends in convergence behavior among the considered models. The convergence behavior of the manufacturer model has been previously studied in the literature [10]. This model was therefore utilized as a starting point for identifying regions of convergence. Table 4 presents the convergence behavior of the manufacturer SiC MOSFET model in the multi-level DPT application circuit for various SPICE options. The multi-level DPT application was selected for this study because it is an especially challenging simulation. For the purposes of this study, a simulation run was considered a convergence failure if one of the following conditions was met: (1) a convergence error was indicated by the solver, (2) the simulation stopped before the final time sample, or (3) if the mean value of a specific reference waveform was more than one order of magnitude different than its known value. In the authors' experience, any one of these conditions is likely to be met when LTspice encounters convergence difficulty in solving a complex converter simulation.

Table 4 indicates that, when using the default SPICE options, the manufacturer model cannot solve any of the multi-level DPT simulations. It is noted that the single-die DPT simulation is a traditional (non-multi-level) DPT. Altering the SPICE options according to the values recommended in Table 3 leads to a significant improvement in convergence behavior, but the model still does not converge in all cases. However, when skipping the initial operating point solution, LTspice can correctly solve any of the multi-level DPT simulations with either option set. It is noted that the SPICE options do not substantially influence convergence behavior when skipping the initial operating point solution. However, the options do have a significant impact on simulation runtime. For example, the 32 die-per-switch-position DPT configuration requires 37 minutes to solve with the default options, but only 20 seconds to solve using the options shown in Table 3.

The significant improvement in convergence behavior when skipping the initial operating point solution is related to the complexity of solving the DC bias conditions of this circuit. Combining transistor models in series creates many nodes with interdependent DC bias conditions. The multiple behavioral sources and conditional statements in the manufacturer model lead to a complex system matrix for the initial operating point. In general, there are a wide range of circuit topologies that have challenging DC operating point solutions; where viable, bypassing the DC solution can significantly improve convergence behavior.

This case study illustrates that the convergence behavior of a transistor model is highly dependent on the application circuit as well as the solver options employed. The multi-level application circuit studied in this section poses a particular challenge for the LTspice solver. However, in the authors' experience, less complex circuits often exhibit similar convergence failures with certain combinations of models and simulation options. For example, convergence challenges have been reported for simulation of a full-bridge inverter based on the manufacturer model considered here [10]. However, the present paper has demonstrated successful convergence of much more complex application circuits utilizing this model by careful adjustment of the SPICE simulation options.

Guidelines for achieving this type of improvement for generalized power electronics simulations can be found in textbooks such as [56] and [57]. For LTspice, one of the first parameters to adjust for improving convergence is the solver implementation. LTspice includes two separate internal solvers:

normal and alternate. The alternate solver has reduced round-off error (which improves internal accuracy) and will converge for many cases that cause difficulty for the normal solver. Because the alternate solver simulates at approximately half the speed of the normal solver [55], it should only be selected when convergence is a concern. For the convergence study shown in Table 4, selection of the alternate solver (with default SPICE options and including the solution of the initial DC operating point) leads to convergence for small simulations with eight or fewer series transistors but only marginal convergence for large simulations with sixteen and thirty-two series transistors.

## VI. CONCLUSION

This study provides a targeted extension to the existing literature on modeling the conduction behavior of SiC MOSFETs in SPICE. While the literature contains numerous examples of suitable SiC MOSFET models, few of these studies include quantitative metrics to facilitate comparisons and inform modeling decisions. From the perspective of application design, model accuracy and computational complexity must both be carefully considered to achieve models with practical utility. A detailed study that provides application designers with tools to evaluate the efficacy of existing SiC MOSFET models for this purpose is not currently available.

Therefore, in this paper, attention is given to quantifying the impact of trade-offs associated with particular modeling decisions. Instead of surveying all potential approaches described in the literature, this study considers a cross-section of the best available SiC MOSFET models in the behavioral, semi-physics, and physics categories. Each model is tuned to identical characterization data and evaluated side-by-side in terms of accuracy and computational complexity.

The resulting analysis provides useful guidance to practitioners in selecting models for use in application studies. First, it is recognized that the all models presented have suitably low RMS error for application design. Since all the transistor models are with 10% of the experimental data in operating area, accuracy of predicted of conduction losses will likely be limited by other factors such as the parasitic model, load model, or transistor variance. Additionally, these accuracy results specifically deal with the static behavior of the transistor; the dynamic accuracy is another important consideration which will receive treatment in a complementary manuscript.

Some of the findings presented herein are consistent with expectations. For example, the semi-physics model is shown to be the least accurate but most computationally efficient option. Other findings are less intuitive. For example, it is demonstrated that connecting SiC MOSFET models in series (as in a multi-level converter) is significantly more computationally demanding than connecting SiC MOSFET models in parallel. This finding may influence modeling decisions for emerging designs in the medium-voltage application space. Additional guidance is provided for addressing known challenges achieving simulation convergence both for model designers and application developers. The specific recommendations are targeted for the LTspice simulation environment, but many are generally applicable to any SPICE-compatible system.

The findings of this study project a roadmap for the development of optimized SiC MOSFET models going forward. For example, one possible future direction would be to combine different aspects of the presented models in a manner that blends the best aspects of each. To achieve this goal, it is necessary to first conduct a similar analysis of the dynamic behavior of the most promising SiC MOSFET models in the literature. That effort is currently underway and will be presented in a future publication.

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