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Single-Phase Five-Level Flying-Capacitor Rectifier Using Three Switches

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ABSTRACT In this paper, a unidirectional single-phase five-level PWM rectifier based on flying-capacitor topology operating as PFC is proposed. The main feature is the fact that the proposed converter has three active switches, therefore offering a cost reduction compared to traditional five-level topologies. The multilevel voltage operation reduces the weight and bulk of the magnetic devices. Moreover, 82% of the semiconductors are subject to one fourth to DC output voltage which allows the use of low voltage semiconductor devices. An extensive mathematical analysis, control-oriented modeling in addition to experimental results are presented in order to demonstrate the feasibility of the structure.

INDEX TERMS AC–DC power conversion, five-level, flying-capacitor, pfc, single-phase.

I. INTRODUCTION

Multilevel converters have several advantages over two-level topologies, such as reduced voltage stress on the semiconductor devices, reduction in filter size, and lower electromagnetic interference [1]–[10]. From this scenario the five-levels have gained popularity due to its advantages compared to three-level structures with respect to voltage reduction on the components, reducing the volume of inductors and larger power range [3]–[7]. Moreover, the five-level operation allows the voltage steps to be lower than those found in two/three-level, as a consequence, a current with less harmonic distortion can be obtained from the grid [11], [12]. It presents as drawbacks a larger number of components and relative control complexity, however, this latter has been minimized with the advancement and widespread use of digital processors DSPs and FPGAs [13].

Several structures of five-level are derived from well-known unidirectional three-level topologies [14]–[18] as VIENNA-Types [19], [20], Neutral Point Clampled (NPC) and Flying-Capacitor (FC) [3], [7]. Among these, the FC-based converters have gained prominence due to natural balancing FC voltages, excellent loss distribution among the switching devices, and easy modularity for more levels [2], [21]. In [22], [23] a single-phase five-level based on a double flying-capacitor has been proposed. It presents 10 semiconductors, four of which are switches, and 4 capacitors. It has as features the fact that both voltages across the active switches, fast diodes are subject to one-fourth of DC output voltage and the fault-tolerant capability. The circuit was later modified in [2], [24] for three-phase operation. Another variation of the FC has been proposed in [15]. It differs by the fact of the differential connection between two FC phase legs forming a semi-bridge FC rectifier. It presents just 8 semiconductors, which four are switches, and 3 capacitors. As a drawback the semiconductors are subject to half of the output voltage, limiting the voltage range operation. Following another approach [25] features a converter capable of imposing five-level voltage using for that purpose four active switches. Because of the low number of semiconductors in series in the current path the structure provides high efficiency. In contrast, due to components are subject to half the output voltage makes its use advisable for output voltages below 800 V.

The aforementioned topologies, as well as others [17], [26]–[28], have in common the presence of four active switches for the intent of performing five-level voltage at AC terminals. The number of active switches has a direct impact on the overall costs of the system because of the need for additional semiconductor, gate driver circuitry, and heat sink space allocation. Therefore, the reduced-switches-count structures become necessary to provide the overall cost reduction and increasing the reliability of a converter. Based on this conception, in this paper, a single-phase five-level flying-capacitor

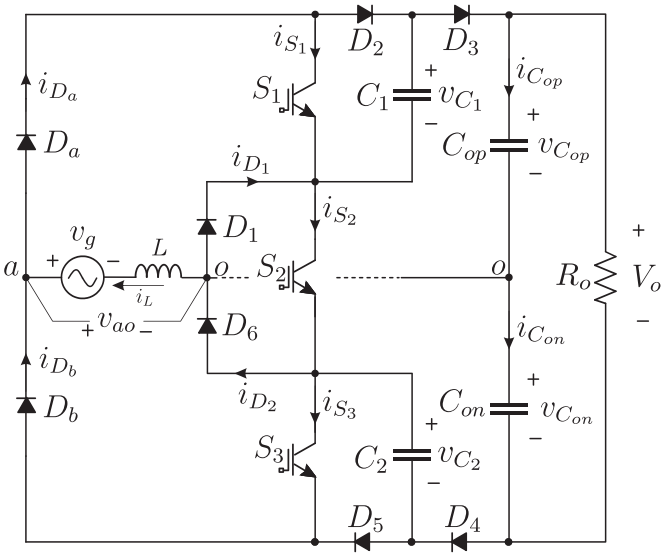

FIG. 1. Proposed five-level PFC PWM rectifier.

PWM PFC rectifier using only three switches is proposed. As well as presented by [22], [23], the proposed topology inherits the features of the flying-capacitor as the low voltage across the components, natural voltage balancing and good loss distribution, using for this propose three active switches only.

The paper is organized as follows: In Section II, the principle of operation and steady-state analysis are investigated. Modeling and control are discussed in Section III. The feasibility of the proposed topology and the effectiveness are verified by experimental results in Section IV. A comparison between single-phase PFC five-level rectifers are discussed in Section V. Finally, conclusions are drawn in Section VI.

II. PROPOSED CONVERTER AND PRINCIPLE OF OPERATION

The proposed rectifier is shown in Fig. 1.[1] It is composed by two flying-capacitor cells interconnected by diodes D_1, D_6, and switch S_2. The fact of having only three switches reduces the implementation cost and simplifies the modulation control. The voltages across the capacitors C_1 and C_2 present a natural balance with $\frac{1}{4}$ of the DC output voltage. The output capacitors C_{op} and C_{on} keep the half output voltage V_o. The semiconductors are subject to $\frac{V_o}{4}$, except the slow diodes D_a and D_b which are subject to $\frac{V_o}{2}$. Thus, the slow diodes can be implemented with standard fast or ultrafast silicon diodes with low forward voltage drop, while the fast diodes D_k, $k = \{n \in \mathbb{N} | 1 \leq n \leq 6\}$, would benefit from SiC or GaN semiconductor technology.

[1]In Fig. 1, the active switches are represented by IGBTs, but other switching devices such as MOSFETs, GaN HEMT can be used in the power circuit.

A. PRINCIPLE OF OPERATION

The operation stages, valid to the positive grid half-cycle, are shown in Fig. 2. For each grid half-cycle there are four topological states. The state 1 starts when the semiconductors S_1 and S_2 are both turned on. In this case the voltage between nodes a and o, v_{ao}, is zero and occurs the storage energy of the inductor L from voltage grid v_g [see Fig. 2(a)]. The state 2 starts when S_1 turned off and S_2 keep turned on. In this case $v_{ao} = V_o/4$ and the capacitor C_1 is charged [see Fig. 2(b)]. If $|v_g| < V_o/4$ then the inductor delivery energy to capacitor C_1. If $|v_g| > V_o/4$ then occurs the storage energy of the inductor L from voltage difference between v_g and $V_o/4$. The state 3 is determined by the turning on of S_1 and turning off of S_2. In this condition v_{ao} is again equal to $\frac{V_o}{4}$, however the capacitor C_1 is discharged, featuring in a redundant state [see Fig. 2(c)]. Therefore, the states 2 and 3 can be used for balancing the voltage across the capacitor C_1. The state 4 occurs when both S_1 and S_2 are turned off. In this condition the voltage v_{ao} is equal to $\frac{V_o}{2}$ and there is no current flow through the capacitor C_1, [see Fig. 2(d)]. During the negative grid half-cycle the converter has analogous operation, as can see in Fig. 3, and therefore, the description will be omitted herein.

The topological states are determined by the PWM modulation scheme shown in Fig. 4, according to direction of the input current i_L and amplitude of the modulation signal m. The switching pattern of the switches is generated by mean three comparators, where the modulation signal m compared with the triangular carried v_{tri_1} generates the signal for switches S_1 or S_3, depending on the signal of i_L. The switching pattern for switch S_2 is generated by mean of a second comparator which is employed a carrier signal v_{tri_2} shifted 180°. Ideally, for the same switching period, the three switches are fed with the same duty cycle.

Fig. 5 illustrates the ideal main waveforms for rectifier operating as PFC during one grid period. It can be seen the voltages v_g and v_{ao} beyond modulation signal m. Therein, two distinctive converter operating regions can be observed:

i) if $|v_g| \leq \frac{V_o}{4}$, the voltage $|v_{ao}|$ will alternate between the voltages 0 and $\frac{V_o}{4}$.

ii) if $|v_g| > \frac{V_o}{4}$, the voltage $|v_{ao}|$ will alternate between the voltages $\frac{V_o}{4}$ and $\frac{V_o}{2}$.

More details about Fig. 5 will be discussed in next subsection.

B. STEADY-STATE ANALYSIS

The steady-state analysis of the converter is performed under the following assumptions:

- The converter operates in continuous conduction mode CCM;
- All components are ideal;
- All capacitances are sufficiently large to maintain their voltages constant over a switching period T_s;
- The switching frequency f_s should be much higher than the grid frequency f_g. (voltage grid approximately constant within a switching period T_s).

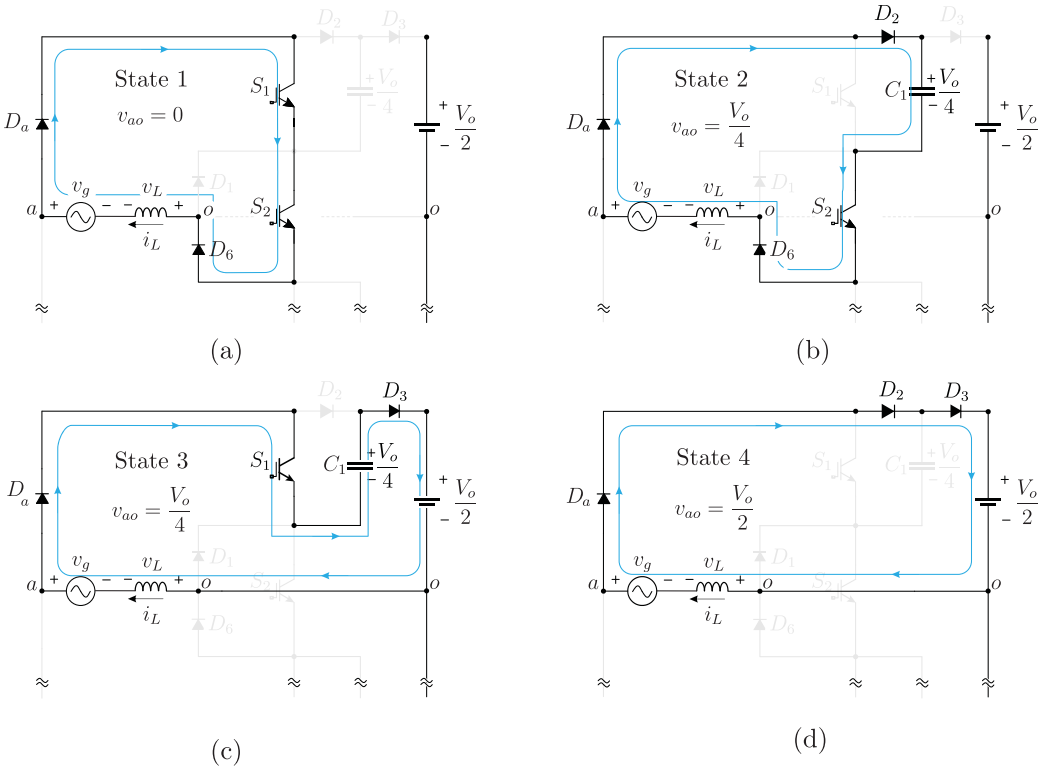

FIG. 2. Operational stages of proposed converter valid to positive half cycle of the grid; (a) S_1 and S_2 turned on (state 1): inductor stored energy from grid voltage; (b) S_1 turned off and S_2 turned on (state 2): transfer energy to capacitor C_1 (charging); (c) S_1 turned on and S_2 turned off (state 3): transfer energy to output (C_1 discharging); (d) S_1 and S_2 turned off (state 4): transfer energy to output.

Considering that both input voltage v_g and input current i_L are purely sinusoidal and high power factor operation, then

$$v_g = V_{\text{pk}} \cdot \sin(\omega t), \tag{1}$$

$$i_L = I_{\text{pk}} \cdot \sin(\omega t), \tag{2}$$

where V_{pk} and I_{pk} are the peak voltage and peak current input, respectively.

Neglecting the average voltage across the inductor L, calculated within the switching period T_s, then $v_g \approx \langle v_{ao} \rangle_{T_s}$, where $\langle v_{ao} \rangle_{T_s}$ represents the average voltage between nodes a and o, calculated within of T_s. This voltage is given as

$$\langle v_{ao} \rangle_{T_s} = \frac{V_o}{2}(1-d) \cdot \text{sign}\{i_L\}, \tag{3}$$

where d represents the duty cycle of the switches and sign$\{i_L\}$ represents the signal function of i_L. The duty cycle is related with modulation signal by $d = \frac{m}{V_T}$, where V_T is the peak of the triangular carrier [see Fig. 4]. Then, isolating d in (3) results in

$$d = \frac{m}{V_T} = 1 - M|\sin(\omega t)|, \tag{4}$$

where $M = \frac{2V_{\text{pk}}}{V_o}$ and it represents the modulation index.

C. INDUCTOR CURRENT RIPPLE

The envelope of normalized input current through the inductor is determined by

$$\overline{\Delta i}_{L,\text{pk-pk}} = \begin{cases} M\sin(\omega t) - 2M^2\sin(\omega t)^2, & \omega t \le \theta_1 \\ 3M\sin(\omega t) - 2M^2\sin(\omega t)^2 - 1, & \omega t > \theta_1, \end{cases} \tag{5}$$

where $\theta_1 = \arcsin(\frac{1}{2M})$ and correspond to the boundary of level transition [see Fig. 5], and $\overline{\Delta i}_{L,\text{pk-pk}}$ is given as

$$\overline{\Delta i}_{L,\text{pk-pk}} = \frac{\Delta i_{L,\text{pk-pk}} \cdot 4 \cdot L \cdot f_s}{V_o}. \tag{6}$$

The maximum value in (5) correspond to $\frac{1}{8}$. Thus, the inductance value can be calculated according to (7).

$$L = \frac{V_o}{32 \cdot f_s \cdot \Delta i_{L,\text{pk-pk}}} \tag{7}$$

D. CURRENT STRESSES

For the calculation of current stresses on all components should be observed both the time duration of the topological states and the current flow through them. The average and RMS current values for the semiconductors and capacitors as listed in Table I.

Fig. 7 shows the behavior of the normalized RMS currents in all components, weighted by input current peak I_{pk},

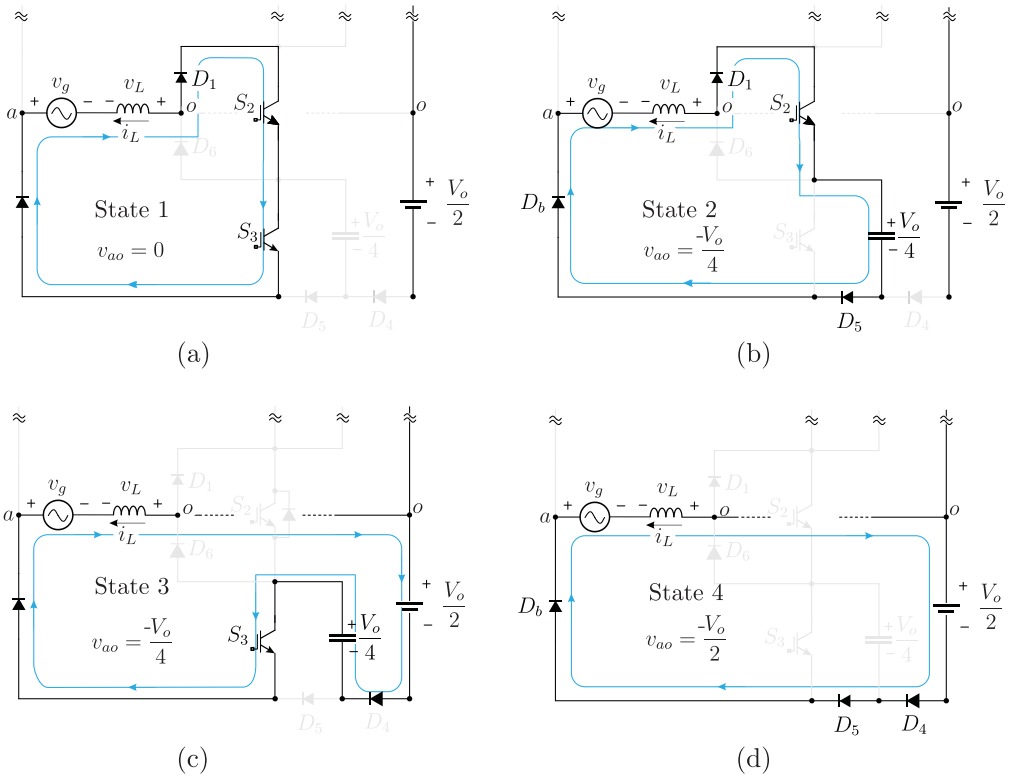

FIG. 3. Operational stages of proposed converter valid to negative half cycle of the grid; (a) S_1 and S_2 turned on (state 1): inductor stored energy from grid voltage; (b) S_1 turned off and S_2 turned on (state 2): transfer energy to capacitor C_1 (charging); (c) S_1 turned on and S_2 turned off (state 3): transfer energy to output (C_1 discharging); (d) both S_1 and S_2 turned off (state 4): transfer energy to output.

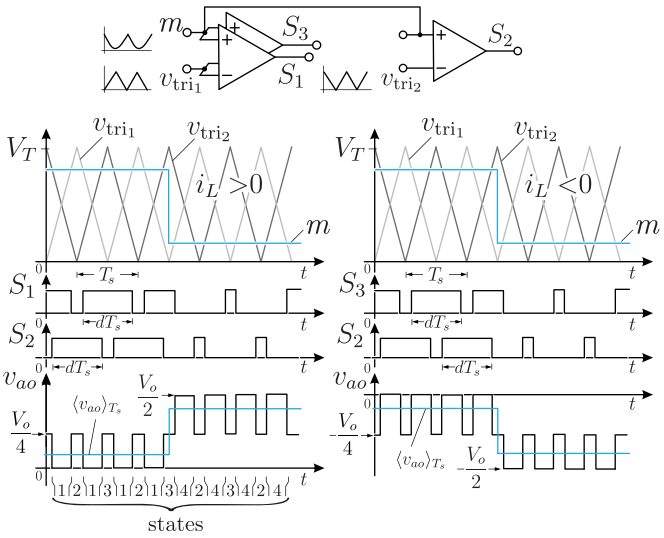

FIG. 4. PWM modulation scheme, switching pattern of switches, and voltage between the nodes *a* and *o*, v_{ao}, for both half cycles of the input current i_L. The switch S_1 must operate for $i_L > 0$ while S_3 remains turned off. For $i_L < 0$ the switch S_3 must operate while S_1 remains turned off.

defined as

$$I_{x,\mathrm{rms}} = \bar{I}_{x,\mathrm{rms}} \cdot I_{\mathrm{pk}}, \tag{8}$$

where x corresponds to the semiconductor or capacitor element. Fig. 6 shows the behavior of the normalized average

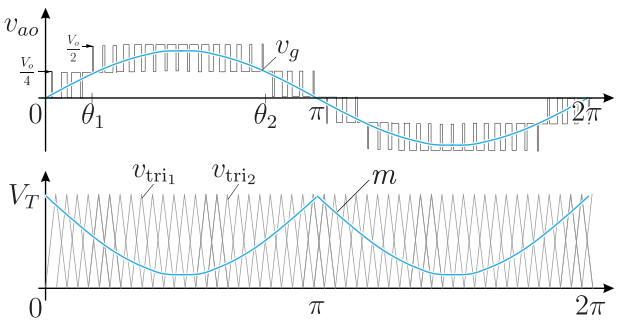

FIG. 5. Idealized waveforms for high power factor operation valid to $M > \frac{1}{2}$.

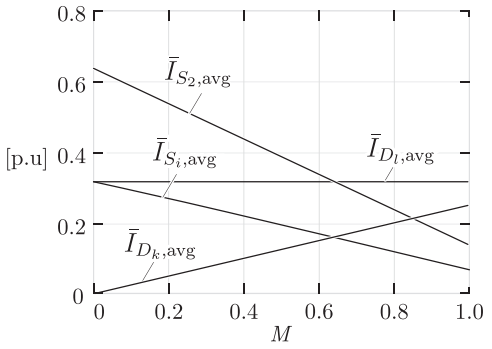

FIG. 6. Normalized average current stresses as function of the modulation index M: $I_{\mathrm{avg}} = \bar{I}_{\mathrm{avg}} \cdot I_{\mathrm{pk}}$, $i \in \{1, 3\}$, $k = \{n \in \mathbb{N} | 2 \leq n \leq 5\}$, $l \in \{a, b\}$.

TABLE 1. Average and RMS Current in the Semiconductors and Capacitors for PFC Operation: $k = \{n \in \mathbb{N} | 2 \le n \le 5\}$ and $\beta = -6\theta_1 + 3\sin(2\theta_1) + 2M\cos(3\theta_1) - 18M\cos(\theta_1)$

x	$I_{x,\text{avg}}$	$I_{x,\text{rms}}$
S_1, S_3	$\frac{I_{\text{pk}}(4-\pi M)}{4\pi}$	$\sqrt{\frac{I_{\text{pk}}^2(3\pi-8M)}{12\pi}}$
S_2	$\frac{I_{\text{pk}}(4-\pi M)}{2\pi}$	$\sqrt{\frac{I_{\text{pk}}^2(3\pi-8M)}{6\pi}}$
D_1, D_6	$\frac{I_{\text{pk}}(4-\pi M)}{4\pi}$	$\sqrt{\frac{I_{\text{pk}}^2(3\pi-8M)}{12\pi}}$
D_k	$\frac{I_{\text{pk}}M}{4}$	$\sqrt{\frac{I_{\text{pk}}^2 2M}{3\pi}}$
D_a, D_b	$\frac{I_{\text{pk}}}{\pi}$	$\sqrt{\frac{I_{\text{pk}}^2}{4}}$
C_1, C_2	0	$\begin{cases} \sqrt{\frac{I_{\text{pk}}^2 2M}{3\pi}}, & M \le \frac{1}{2} \\ \sqrt{\frac{6I_{\text{pk}}^2(3\pi+8M+\beta)}{6\pi}}, & M > \frac{1}{2} \end{cases}$
C_{op}, C_{on}	0	$\sqrt{\frac{I_{\text{pk}}^2 M(32-3\pi M)}{48\pi}}$

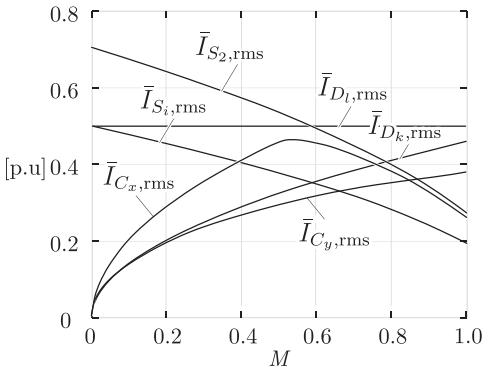

FIG. 7. Normalized rms current stresses as a function of the modulation index M: $I_{\text{rms}} = \bar{I}_{\text{rms}} \cdot I_{\text{pk}}$, $i \in \{1, 3\}$, $k = \{n \in \mathbb{N} | 2 \le n \le 5\}$, $l \in \{a, b\}$, $x \in \{1, 2\}$, $y \in \{op, on\}$.

currents in all semiconductors, weighted by input current peak I_{pk}, defined as

$$I_{x,\text{avg}} = \bar{I}_{x,\text{avg}} \cdot I_{\text{pk}}, \tag{9}$$

where x corresponds to the semiconductor element.

E. FLYING-CAPACITORS VOLTAGE RIPPLE

The flying-capacitors C_1 and C_2 present just high-frequency voltage ripple which the maximum value is determined by

$$\Delta V_{C_k,\text{pk-pk}} = \frac{I_{\text{pk}}}{4M \cdot C_k \cdot f_s}, \; k \in \{1, 2\}, \tag{10}$$

where $\Delta V_{C_k,\text{pk-pk}}$ represents the maximum peak-to-peak voltage ripple across the flying-capacitors.

F. DC-LINK VOLTAGE RIPPLE

The choice procedure of the output capacitor is similar to conventional single-phase PFC rectifiers. It is based on 120 Hz voltage ripple and is given as

$$C_{op} = C_{on} > \frac{P_o}{\pi f_g V_o \cdot \Delta v_{o,\max}}, \tag{11}$$

where $\Delta v_{o,\max}$ represents the maximum voltage ripple across the output capacitors.

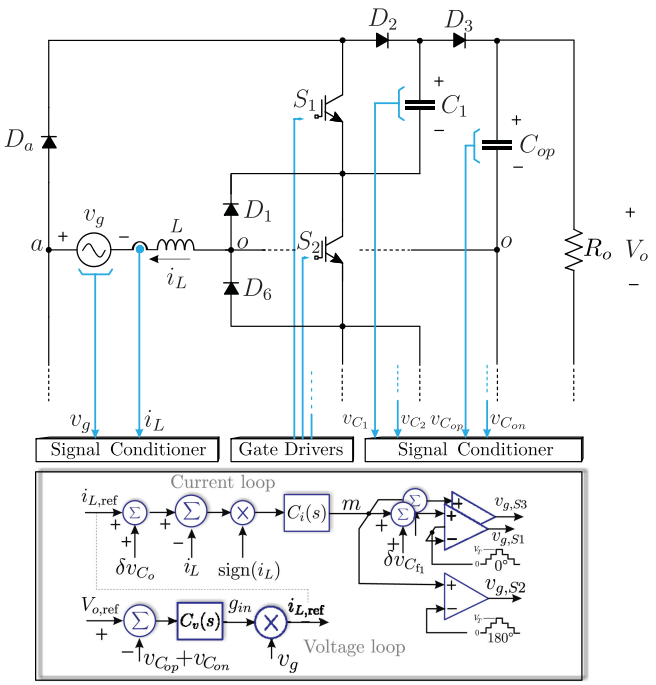

FIG. 8. Control strategy for voltages and input current to PFC operation.

III. CONTROL STRATEGY AND SYSTEM MODELLING

A. CONTROL STRATEGY

A Suitable PWM control scheme for operation as PFC to the proposed converter is shown in Fig. 8. Basically, there are two main control loops responsible for the output voltage control and by the input current control. For output voltage control is necessary to measure the voltages across the capacitors C_{op} and C_{on}. These voltages are compared with a voltage reference $V_{o,\text{ref}}$, where the voltage error feeds the voltage regulator $C_v(s)$. This regulator is responsible for generating a conductance signal, namely g_{in}. This signal multiplied by the input voltage v_g will produce the current reference shape, $i_{L,\text{ref}}$. In order to minimize the distortions on the $i_{L,\text{ref}}$ the output of $C_v(s)$ should be as constant as possible. This imposes that the bandwidth of the voltage control loop should be restricted to much less than the line frequency.

The current loop begins by comparing i_L and $i_{L,\text{ref}}$. Before entering the current regulator $C_i(s)$ the current error signal is multiplied by the signal of i_L. The output signal of $C_i(s)$ produces the modulation signal m which it is synthesized by the PWM modulators. In order to ensure a small current error, the dynamic of $C_i(s)$ should be fast.

To avoid unbalancing voltage across the capacitors, additional loops are necessary. The balancing voltage across

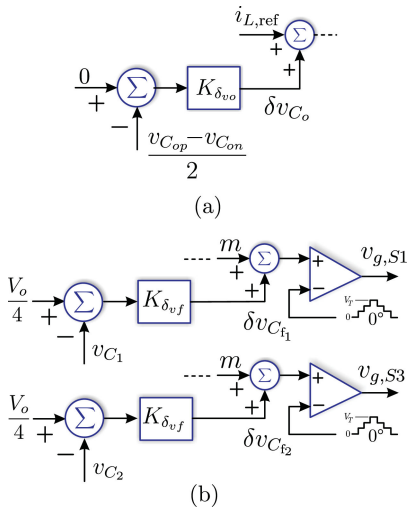

FIG. 9. Additional loops to ensure the balancing voltage across the capacitors: (a) balancing voltage across the capacitors C_{op} and C_{on}; (b) balancing voltage across the capacitors C_1 and C_2.

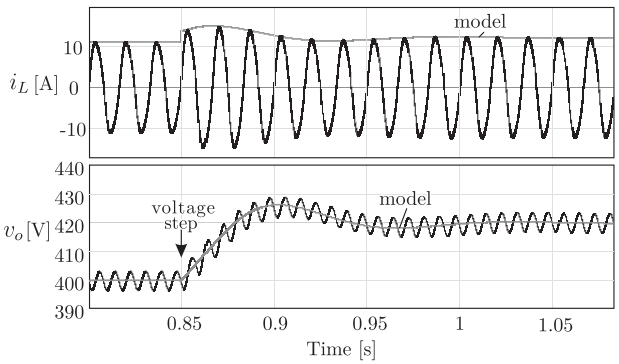

FIG. 10. Comparison between theoretical model and simulation result to a step on the output voltage reference from 400–420 V at $t = 0.85$ s. Parameters used in the simulation: $L = 300$ μH, $V_{g,\text{pk}} = 180$ V, $f_g = 60$ Hz, $f_s = 50$ kHz, $C_1 = C_2 = 10$ μF, $C_{op} = C_{on} = 2$ mF, $P_o = 1$ kW.

the dc-link capacitors is ensured through the block diagram shown in Fig. 9(a). This loop consists basically of forcing the voltage deviation in the output capacitors to be zero. For this, the output δv_{C_o} is added to the current reference $i_{L,\text{ref}}$ producing a small offset on it.

The balancing voltage across the flying-capacitors C_1 and C_2 is ensured through the block diagram shown in Fig. 9(b). As discussed in Section II-A the charging and discharging process of the flying-capacitors C_1 and C_2 is achieved by topological states 2 and 3 [see Figs. 2–3]. For instance, if the voltage of the capacitor C_1, v_{C_1}, is greater than its reference value ($V_o/4$), so a negative current should be imposed to this capacitor. This is achieved by increasing the time duration of the topological state 3 in relation to topological state 2 [see Fig. 2(b)–(c)], ie. the duty cycle of S_1 should be slightly larger than duty cycle of S_2. On the other hand, if $v_{C_1} < V_o/4$, then the duty cycle of S_1 should be slightly smaller than duty cycle of S_2. Thus, the topological state 2 will have a time duration larger than topological state 3.

Therefore, the balancing voltage of C_1 and C_2 can be accomplished by adjusting the conduction time of switches S_1 and S_3, depending on the grid cycle. This adjustment is accomplished by the signal δv_{C_f} which added the modulation signal m changes the duty cycle of S_1 and/or S_3.

B. SYSTEM MODELING

1) CURRENT TRANSFER FUNCTION

Assuming that output capacitors have very large capacitance then they may be ignored for current loop control. Thus, the transfer function related input current i_L with modulation signal m in the frequency domain is

$$G_i(s) = \frac{i_L(s)}{m(s)} = \frac{-V_o}{2 \cdot V_T \cdot s \cdot L}. \tag{12}$$

2) OUTPUT VOLTAGE TRANSFER FUNCTION

It is assumed that $C_j \gg C_k$, $j \in \{op, on\}$, $k \in \{1, 2\}$. The transfer function relating output voltage v_o with conductance signal g_{in} yields in a nonlinear equation. This expression can be extracted and linearized from the energy conservation principle for an AC line cycle, such that

$$p_{in} = p_L + p_{C_{op}} + p_{C_{on}} + p_{R_o}, \tag{13}$$

where,

$$\left\{ \begin{array}{c} p_{in} = \dfrac{g_{in} V_{g,\text{pk}}^2}{2},\ p_L = \dfrac{1}{2} L \dfrac{dI_{g,\text{pk}}^2}{dt}, \\ p_{C_y} = \dfrac{1}{2} C_y \dfrac{d\left(\frac{v_o}{2}\right)^2}{dt},\ p_{R_o} = \dfrac{v_o^2}{R_o},\ y \in \{op, on\} \end{array} \right\}. \tag{14}$$

Substituting (14) into (13) and applying small perturbations around the average value of the output voltage and conductance signal, and, finally, extracting the linear terms, the following transfer function is obtained:

$$G_{v_o}(s) = \frac{\tilde{v}_o(s)}{\tilde{g}_{in}(s)} = \frac{\left(\dfrac{V_{g,\text{pk}}^2}{2} - s \cdot L \cdot I_{g,\text{pk}}\right)}{\left(\dfrac{V_o}{4} s \left(C_{op} + C_{on}\right) + \dfrac{2V_o}{R_o}\right)}. \tag{15}$$

The terms $\tilde{v}_o(s)$ and $\tilde{g}_{in}(s)$ in (15) represent small ac variations around of the average value of V_o and g_{in}, respectively.

Fig. 10 shows a comparison between mathematical models and simulation results for a step voltage reference. It is shown the behavior of input current i_L and output voltage v_o operating in closed-loop. It can be seen that both the theoretical model and simulation results have the same behavior so that equations (12) and (15) can be employed in the control design.

IV. EXPERIMENTAL RESULTS

A 1-kW laboratory prototype of the proposed unidirectional single-phase PFC flying-capacitor rectifier has been built and tested according to shown in Fig. 11. The main specifications are given in Table II. The list of the employed semiconductor

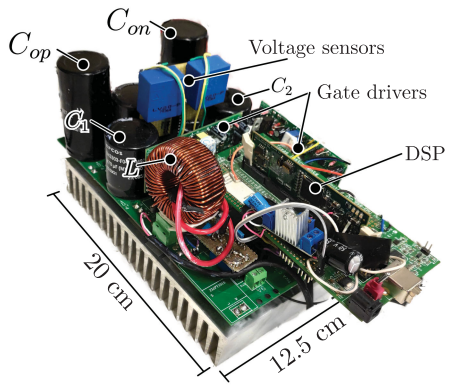

FIG. 11. Implemented 1-kW five-level unidirectional single-phase PFC rectifier prototype.

TABLE 2. Main Specification

Specification	Value
Input RMS voltage, $V_{g,\text{rms}}$	127 V
Output voltage, V_o	400 V
Grid freq., f_g/ switching freq., f_s	60 Hz/ 50 kHz
Rated output power, P_o	1 kW

TABLE 3. List of Components Employed in the Lab Prototype

Component	Description/ value
Input inductor, L	300 μH - Magnetics©-77440A7 71 turns /15 AWG
Capacitors $C_k, k \in \{1,2\}$	470 μF - B43501-S977-M33
Capacitors, $C_j, j \in \{op, on\}$	1 mF - CD293 - 250 V- Suntan
Semiconductor Device MOSFET	IRFP4768PbF - 250 V/ 93 A
Semiconductor Device DIODE	IDH16G65C5 - 600 V/ 16 A

devices and passive components are given in Table III. Both modulation and control algorithms were realized with the floating-point digital signal controller TMS320F28335 DSP Texas instruments. All the tests were carried out with resistive load.

The performance of some of the main waveforms of the proposed converter operating in steady-state and at rated power is shown in Fig. 12. It can be seen the output voltage v_o, inductor current i_L, grid voltage v_g and voltage between nodes a and o, v_{ao}. It shows that the inductor current presents sinusoidal shape and in phase with grid voltage, performing, therefore, high power factor operation. The output voltage v_o is regulated at rated value. Additionally, the formation of five-level at voltage v_{ao} is observed.

Fig. 13 shows the behavior of the voltages across the capacitors of the proposed topology. There can be seen the voltage across the capacitors v_{C_1}, v_{C_2}, $v_{C_{op}}$ and $v_{C_{on}}$. A good voltage regulation can be observed, where the voltages $v_{C_{op}}$ and v_{on} are subjected to $V_o/2$ (200 V) and voltages v_{C_1} and v_{C_2} are subjected to $V_o/4$ (100 V), according to as predicted by the theory analysis.

Fig. 14 shows the behavior of the output voltage v_o and voltages across the switches S_1, S_2 and S_3. As predicted by the theory analysis, the voltages across the switches are clamped

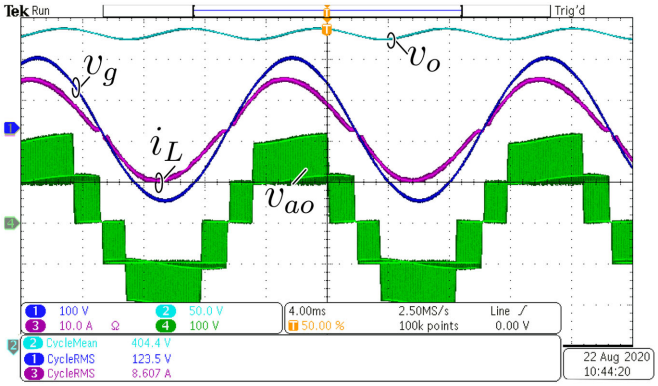

FIG. 12. Experimental results of the proposed converter operating at rated power: grid voltage v_g, channel 1 (100 V/div); output voltage v_o, channel 2 (50 V/div); input currents i_L, channel 3 (10 A/div) and voltage v_{ao}, channel 4 (100 V/div).

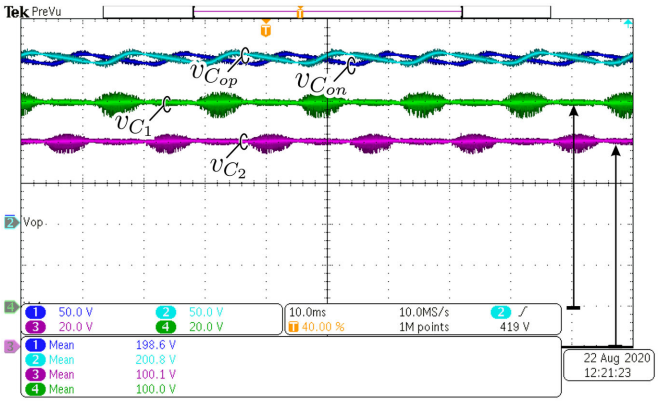

FIG. 13. Experimental results of the proposed converter operating at rated power: voltage across the capacitor C_{on}, v_{on}, channel 1 (50 V/div); voltage across the capacitor C_{op}, $v_{C_{op}}$, channel 2 (50 V/div); voltage across the capacitor C_2, v_{C_2}, channel 3 (20 V/div); voltage across the capacitor C_1, v_{C_1}, channel 4 (20 V/div).

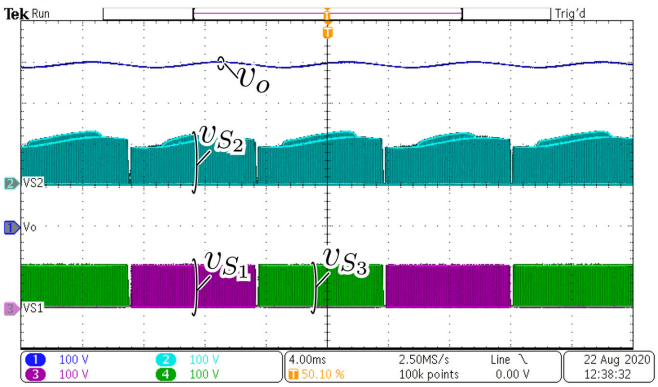

FIG. 14. Experimental results of the proposed converter operating at rated power: output voltage, v_o, channel 1 (100 V/div); voltage across the switch S_2, v_{S_2}, channel 2 (100 V/div); voltage across the switch S_1, v_{S_1}, channel 3 (100 V/div); voltage across the switch S_3, v_{S_3}, channel 4 (100 V/div).

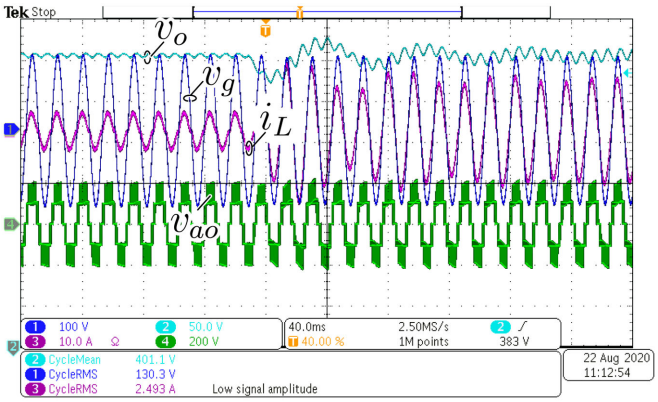

FIG. 15. Experimental results of the proposed converter under a 50% to 100% load-step: grid voltage, v_g, channel 1 (100 V/div); output voltage, v_o, channel 2 (50 V/div); inductor current i_L, channel 3 (10 A/div); and voltage v_{ao}, channel 4 (200 V/div).

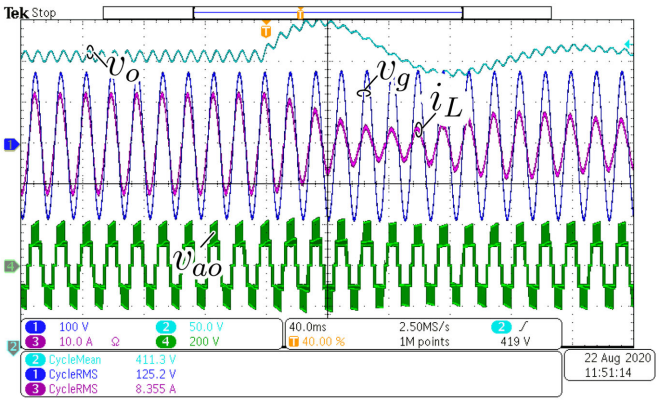

FIG. 17. Experimental results of the proposed converter under a 100% to 50% load-step: grid voltage, v_g, channel 1 (100 V/div); output voltage, v_o, channel 2 (50 V/div); inductor current i_L, channel 3 (10 A/div); and voltage v_{ao}, channel 4 (200 V/div).

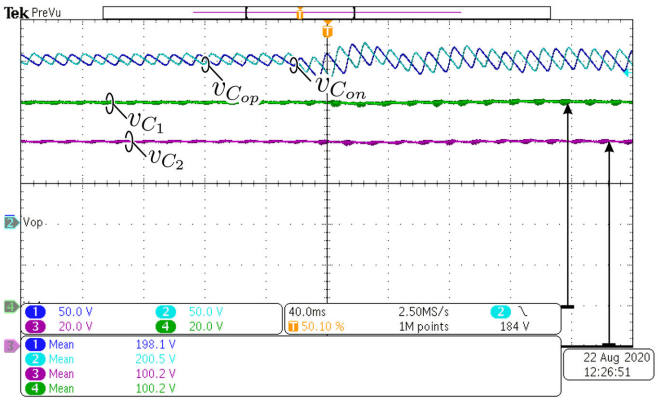

FIG. 16. Experimental results of the proposed converter under a 50% to 100% load-step: voltage across the capacitor C_{on}, $v_{C_{on}}$, channel 1 (50 V/div); voltage across the capacitor C_{op}, $v_{C_{op}}$, channel 2 (50 V/div); voltage across the capacitor C_2, v_{C_2}, channel 3 (20 V/div); and voltage across the capacitor C_1, v_{C_1}, channel 4 (20 V/div).

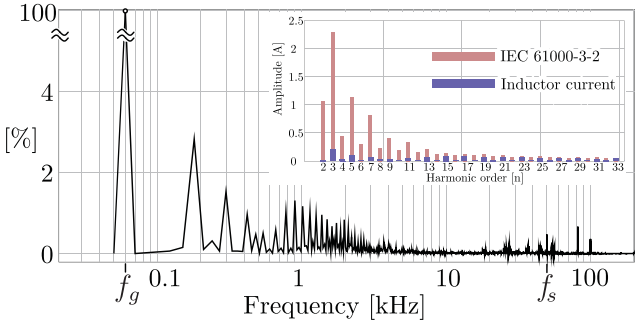

FIG. 18. Input current harmonic spectrum for rated power condition.

to $V_o/4$ (100 V). This feature allows obtaining low switching losses. During the operation the switch S_2 switching on both positive and negative grid cycle while the switches S_1 and S_3 switching just one-half cycle.

Fig. 15 presents the dynamic performance of the proposed converter for a load step: from 50% to 100%P_o. It can be seen that output voltage presents an undamped behavior. This occurs due to the voltage regulator action $C_v(s)$ [see Fig. 8]. This dynamic performance can be improved with readjustment of $C_v(s)$.

Fig. 16 shows the dynamic performance of the voltages across the capacitors for a load step: from 50% to 100%P_o. It can be seen that during the transient both voltage pairs $\{v_{C_{op}}, v_{C_{on}}\}$ and $\{v_{C_1}, v_{C_2}\}$ do not present voltage deviations among themselves. Fig. 17 presents the dynamic performance of the proposed converter for load step: from 100% to 50%P_o. Again, a good dynamic performance can be seen in this test. It is shown that after a disturbance the output voltage returns to rated value without affecting the quality of the inductor current.

The input current harmonic spectrum as a percentage of the fundamental component for the proposed converter operating at rated power is shown in Fig. 18. The current spectrum was obtained from the current shown in Fig. 12, which a $\text{THD}_i = 5.6\%$ was obtained. The harmonic components are compared to the limits of the IEC 61000-3-2 standard for class A equipment, which have been met for the measured load condition. The efficiency has been measured with a FLUKE Norma 4000 power analyzer and the results are shown in Fig. 19. The maximum efficiency achieved was 95.13%.

V. COMPARATIVE AND DISCUSSION

Table IV shows a qualitative comparison of the proposed converter with other unidirectional five-level topologies. Among these topologies, the converter presented by [22] has greater similarities with the proposed converter. It can be seen that the proposed converter has two more diodes than [22]. However, the one switch elimination provides the reduction of isolated gate driver circuitry, as well as other hardware resources, which may allow the overall cost reduction. Moreover, a higher simplicity of modulation scheme is obtained if the

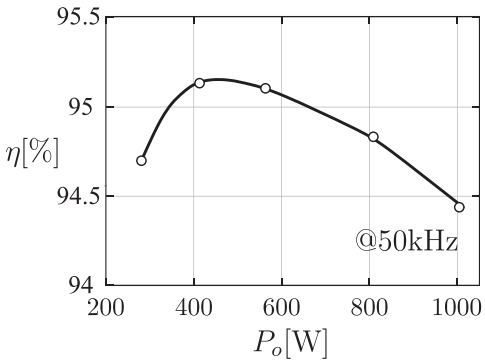

FIG. 19. Measured efficiency as a function of output power for the proposed converter.

TABLE 4. Comparison of the Proposed Converter With Other Unidirectional Five-Level Topologies

Parameter	Topology				
Reference	[15]	[22]	[25]	[26]	Proposed converter
Active switches	4	4	4	4	3
Voltage across the active switches	$V_o/2$	$V_o/4$	$V_o/2$	$V_o/2$	$V_o/4$
Fast diodes	4	4	6	4	6
Voltage across the fast diodes	$V_o/2$	$V_o/4$	$V_o/2$	$V_o/2$	$V_o/4$
Slow diodes	0	2	0	0	2
Capacitors	3	4	2	3	4
Voltage across the capacitors	$V_o/2$	$V_o/4$	$V_o/2$	$V_o/2$	$V_o/4$

number of active switches is reduced. In contrast, the topology in [22] may be more efficient due to the fact that it has three semiconductors in series in the current path during the energy storage stage, whereas the proposed topology presents four semiconductors for the same condition [see Fig. 2(a)–(b)].

VI. CONCLUSION

In this paper, a unidirectional single-phase five-level rectifier based on the FC topology was presented. The proposed topology combines the advantages of FC converters as the use of lower voltage-rating devices, natural balancing FC voltages, and good loss distribution among the switching devices. Compared with conventional single-phase five-level structures, this new multilevel converter offers the possibility of power factor correction using only three active switches. This feature allows overall cost reduction through the cutback of gate driver circuitry, and modulation/control complexity, which can be an attractive alternative for the industry.

An extensive mathematical analysis comprising steady-state and dynamic modeling has been presented. A suitable control scheme that allows the control of output voltage, balancing FC voltage, input current also has been described. Finally, a 1-kW/ 127 V to 400 V/ 50 kHz laboratory prototype has been built and tested, where experimental results attest to the feasibility of this technology concept.

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