Adaptive Model Predictive Controller to Reduce Switching Losses for a Capacitor-Less D-STATCOM

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ABSTRACT In the post-industrial digital-economy, motors powering manufacturing have been replaced by computers powering ecommerce - with significant financial losses attributable to poor power quality (PQ). At the same time, increasing penetration of distributed generation and constant power loads complicate the job for the electric utilities to deliver high-quality electrical power. Traditionally, voltage source converters provide PQ compensation; the backbone of these converters, however, are large electrolytic capacitors (e-caps), which have well-known failure rates. A D-STATCOM that does not use e-caps was shown to increase the converter service life and increase the reliability of the power system; finite control set model predictive control (MPC) was shown to achieve high fidelity tracking for multi-objective cost functions. However, high fidelity (to achieve low total harmonic distortion) results in high switching frequency, which increases losses and device stresses, and reduces the overall converter reliability. This paper improves the capacitorless D-STATCOM by investigating an adaptive MPC that trades-off high-fidelity performance and switching frequency, subject to IEEE 519 THD standards, to achieve good-enough performance. The method is verified experimentally in a 7.5 kVA D-STATCOM hardware prototype. The results show a reduction in switching frequency by over 30% compared with the MPC methods that prioritize high-fidelity alone.

INDEX TERMS D-STATCOM, harmonics compensation, model predictive control, matrix converter, power quality, reactive power compensation.

NOMENCLATURE

T_S	Sampling time
k	Discrete sample time step
σ	Switching configuration number, $\sigma \epsilon [1, .., 27]$
j	Phase Line $j \epsilon [A, B, C]$
V_{oj}	Per-phase output voltage of the matrix converter
I_{oj}	Per-phase output current of the matrix converter
L_{MCj}	Per-phase output inductors
$R_{L_{MCj}}$	Per-phase parasitic resistance on output inductors
V_{Busj}	Per-phase input voltage of the filter
V_{ej}	Per-phase input filter output voltage (matrix converter input voltage)
$\dot{V}_{ej}$	Per-phase first order derivative of the input filter output voltage (matrix converter input voltage)
I_{cj}	Per-phase input filter output current (matrix converter input voltage)
$\dot{I}_{cj}$	Per-phase first order derivative of the input filter output current (matrix converter input voltage)
I_{ej}	Per-phase output current of the filter
R_{fj}	Per-phase parasitic resistance of the filter inductors
L_{fj}	Per-phase filter inductors
C_{fj}	Per-phase filter capacitors
i_{cj}^*	Reference input current in the MPC cost function
i_{oj}^*	Reference output current in the MPC cost function
λ_1, λ_2	MPC cost function weighting factors
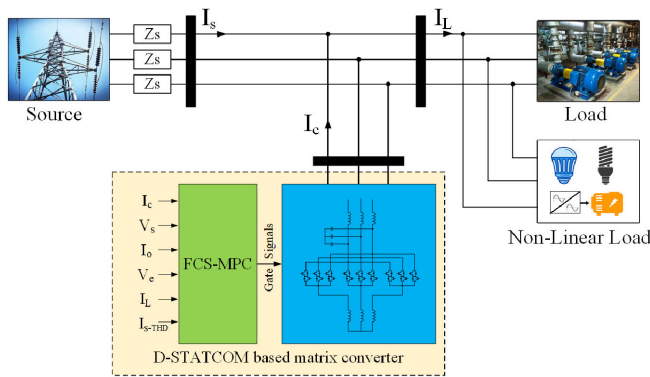
FIGURE 1. Capacitor-less D-STATCOM based matrix converter.

θ	Tracking error margin
Th	Tracking error margin threshold
ΔTh	User-defined increment for tracking error threshold
β	Lower bound of user-defined THD operation range. Adaptive cost function penalizes THD below $\beta\%$
B	Upper bound of user-defined THD operation range (for IEEE 519 specifies B = 5

I. INTRODUCTION

Solar photovoltaic accounted for 2.3% of the 2018 US electrical generation and is projected to account for 17.5% of the total generation mix by 2050 [1]. The US transportation industry is evolving, with electric vehicles projected to account for up to 76% of vehicle miles traveled by 2050 [2]. Distributed energy resources like photovoltaic integration redirect power flow in the system [3]. Constant power loads are replacing passive linear loads and have destabilizing effects on the grid as they act as a negative incremental impedance [4]. In short, power quality on the utility grid has become a critical challenge for the post-industrial digital-economy era. In Europe, the estimated power quality problems cost industry and commerce about 10 billion euro per annum. The cost to address this problem, however, is estimated at 5% of the cost [5], [6].

Different control devices such as fixed capacitor banks (CBs) [7]–[9] or switched capacitors and inductors as in static VAR compensators (SVC) [10], [11] have been used to provide reactive power support to the distribution network. However, these devices provide a fixed or stepwise amount of reactive power. D-STATCOM is another interesting solution to improving power quality as it provides both dynamic reactive power and harmonic compensation at an appropriate bus that needs conditioning within the distribution network. The main building block of the traditional D-STATCOM is the voltage source converter (VSC) with voluminous energy-storing electrolytic capacitors (e-caps). More than 30% of power converter failures are due to the electrolytic capacitors, and these capacitors are subjected to accelerated failures, especially in hot environments [12], [13]. A capacitor-less power quality compensator, as shown in Fig. 1, is capable of performing the functions of a standard D-STATCOM while also increasing

the service life of the converter, hence increasing the overall reliability of the power system [14]. The proposed topology is based on a matrix converter (MC) and inductive energy storage, which is controlled using a finite control set model predictive control (MPC) [15]–[19]. Our proposed configuration is different from CSI topology, in our configuration that is based on MC topology, bidirectional IGBT modules are used as power switches, while in CSI topology, reverse voltage blocking capabilities are needed which makes the configuration more complex and reduce the efficiency compared with the traditional topologies [20].

Finite control set model predictive control (MPC) is a model-based [21] control method that can include multi-objective optimization [22], constrained control [23], adaptive control [24] and online auto-tuning of weighting factors [14] all in a single controller that exhibits fast dynamic tracking [25]. Well-known, MC control strategies are primarily based on Venturini modulation and space vector modulation (SVM) [26]. Examples of MC control strategies include repetitive control [27], resonant control [28], proportional integral control (PI) [29], [30], sliding-mode control [31], [32]. MPC is more flexible than other control strategies as it can accommodate different variables, with constraints and additional system requirements (such as reactive power, common-mode voltages, switching losses, voltage unbalance, etc.) [22]–[24]. MPC cost function allows multi-objective control within one control loop, which makes MPC simpler to implement compared to other control strategies [15]. MPC controlled MC has been shown to outperform other control strategies in transient operation [33] and shows a faster dynamic response [34], [35]. Improved performance, efficiency, and flexibility simplify meeting standards and operational limits demanded by the evolving industry [36], [37].

Unlike fixed-frequency pulse width modulation techniques, MPC in power electronics operates using a variable switching frequency that depends on sampling frequency and the operating conditions. Achieving high fidelity performance for low total harmonic distortion (THD) in D-STATCOM, often results in high switching frequency. On the one hand, switching losses on a semiconductor are directly proportional to switching frequency [38]. On the other hand, operating at THD much lower than 5% as specified by IEEE 519-2014 recommended practice and requirements for harmonic control [39] is not rewarded within the power system. This paper hypothesis is that there is a trade-off between switching fast enough to achieve acceptable fidelity and low enough to achieve acceptable losses and switch stresses.

Many MPC approaches have been used in literature to reduce switching frequency while keeping current distortion within standardized limits. One solution considers reducing the sampling frequency of the MPC regulator by adding a term in the cost function that penalizes switching frequency and predicting the switching frequency from every possible future switching state [37], [40]. However, slower sampling reduces dynamic performance during transients (i.e., longer settling time during transients). In [40]–[43], the authors included the

switching efforts (number of commutations required to move from the current state to the next) in the cost function to reduce the average switching frequency.

The contribution of this paper is an adaptive MPC controller that penalizes high fidelity performance in a capacitorless D-STATCOM, within permissible THD standards, to reduce switching frequency and switching losses. In other words, the fidelity of high switching frequency is optimized simultaneously with an eye toward reducing losses by lowering the switching frequency. Penalizing high fidelity performance is principally allowing a margin of tracking error within the cost function, without the need for adding additional terms to the cost function. The margin of tracking error has an adaptive threshold that is adjusted according to the state of the converter (i.e., transient vs. steady-state). The result is an adaptive MPC based controller for the capacitorless D-STATCOM that operates within THD standards, operates at a reduced switching frequency, and tracks transients effectively. The proposed idea is verified using simulation and a 7.5 kVA D-STATCOM hardware prototype. Results show a reduction in switching frequency using the proposed technique, which penalizes fidelity, by over 30% compared with the MPC methods that prioritize fidelity. Such results are significant since switching losses are reduced, and overall system efficiency and reliability is increased.

II. MPC FRAMEWORK OF THE POWER CONVERTER

The performance of the converters depends primarily on the control strategy and the reference current detection technique used. MPC is a feedback control algorithm that uses a model of the system to predict a future output of the power converters. When applying MPC on MC, it is required to model the input currents, output currents, and voltages of the MC system. Since MC has a finite number of switching states, the MPC is used to predict system variables only for those possible switching states to evaluate the cost function. One of the advantages of the MPC is the ability to use several constraints in the cost function. As such, typical variables such as currents and voltages can be controlled while achieving additional goals such as reactive power control, switching frequency, and THD reduction.

A. REFERENCE CURRENT DETECTION USING SRF

Synchronous rotating reference frame (SRF) method has been adopted in this paper to generate the reference current to the MPC [44], [45]. As shown in Fig. 2, the load currents and voltages are measured, filtered, and reference currents are extracted according to the synchronous reference frame (SRF) method. SRF theory is based on the transformation of currents in synchronously rotating $d-q$ frame [46]–[48]. The transformation to the $d-q$ reference frame from the ABC reference frame is given in (1):

$$\begin{bmatrix} \text{Id} \\ \text{Iq} \\ \text{I0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & (\omega t + 2\pi/3) \\ -\sin(\omega t) & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$
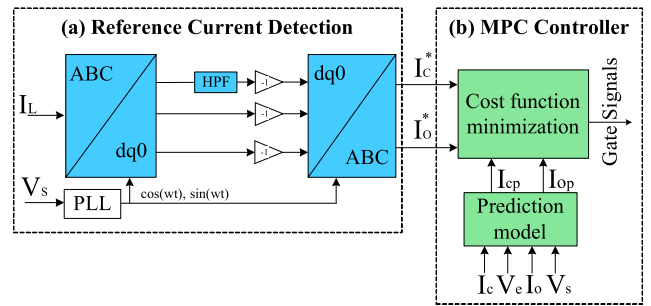
FIGURE 2. D-STATCOM Controller. (a) Reference current detection using SRF method, (b) MPC controller.
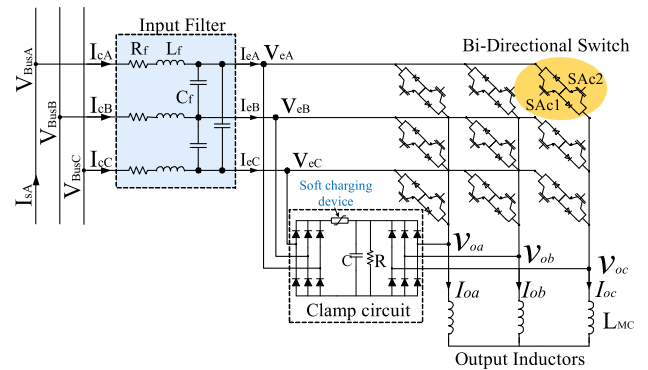
FIGURE 3. Detailed D-STATCOM system on the matrix converter.

$$\cdot \begin{bmatrix} I_{\text{LA}} \\ I_{\text{LB}} \\ I_{\text{LC}} \end{bmatrix} \tag{1}$$

In the SRF method as in Fig. 2, the three-phase load current is measured, then transformed to the $dq0$ reference frame to extract the active and reactive current components of the load current. The extracted current components consist of a dc part that represents the fundamental component of the current and the ac part that represents the harmonics. Using a high pass filter (HPF), the harmonic component can be extracted and then transformed back to the ABC reference frame to be used as a reference current for the controller.

B. MPC METHOD FOR THE MATRIX CONVERTER

The direct matrix converter (MC) topology is used in this application. MC is comprised of nine bidirectional switches. Each switch is made of two anti-parallel IGBT, and diode pairs support bidirectional current flow, as shown in Fig. 3. The MC is connected to the bus through an input filter L_f, C_f, R_f, which is used to eliminate switching-frequencies and harmonics from propagating to the rest of the network.

1) MATRIX CONVERTER MODEL

The output voltages and input currents of the MC were calculated according to (2) and (3) as a function of MC input voltages, output currents and the switching function. Normally, the matrix converter is fed by a voltage source, and, for this reason, the input terminals should not be short-circuited. On the other hand, the load has an inductive nature typically,

and, for this reason, an output phase must never be opened. A clamp circuit, as shown in Fig. 3 is usually employed to protect the converter from surges coming from the input and output sides. These surges are caused by spikes during switches commutation or faults in the output inductors. In normal operation, the clamp circuit has no influence on the MC operation. And in cases of emergency shutdown or sudden interruption of the output currents, the energy stored in the output inductors will be discharged in the clamp without creating dangerous overvoltage [49]. A large-current will flow in the circuit to charge the clamp capacitors when the converter is connected to the grid. To limit the amount of current, a soft-charging circuit can be added to charge the capacitors smoothly. A simple thermistor can be connected after the rectifier circuit to enable soft-charging to the capacitors. Also, a resistor with parallel contactors can be used as well to prevent the inrush current.

The switching function of a single switch can be defined as in (4) [50]. A complete table of variables and parameters is presented in the nomenclature section at the beginning of the paper.

$$\begin{bmatrix} V_{oA} \\ V_{oB} \\ V_{oC} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \cdot \begin{bmatrix} V_{eA} \\ V_{eB} \\ V_{eC} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_{cA} \\ I_{cB} \\ I_{cC} \end{bmatrix} = \underbrace{\begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix}}_{M} \cdot \begin{bmatrix} I_{oA} \\ I_{oB} \\ I_{oC} \end{bmatrix} \quad (3)$$

$$S_{Aj} + S_{Bj} + S_{Cj} = 1 \quad \forall \quad j \in [A, B, C] \quad (4)$$

where M is the instantaneous transfer matrix. V_{oj} and I_{oj} are the output voltages and current at the inductive energy storage of the matrix converter, respectively, with $j \in [A, B, C]$. V_{Busj} and V_{ej} are the per-phase input and output voltages of the filter. While V_{Busj}, and I_{cj} are the input voltages and currents of the matrix converter, and S is the switching function between the MC phases with $j \in [A, B, C]$. Proper choice of S will lead to a phase-reversal of the current so that the inductive load appears capacitive at the input to the MC to supply reactive power to the network [19], [51].

2) LOAD MODEL OF MC
The three-phase inductors connected at the output side of the MC are used as an energy storage instead of capacitor banks employed in VSCs. The output currents of the MC shown in Fig. 4, are modeled using the per-phase differential equation:

$$L_{MCj} \frac{di_{oj}(t)}{dt} = v_{oj}(t) - R_{LMCj} i_{oj}(t) \quad (5)$$

where $v_{oj}(t)$ is the per-phase output voltage of the MC, $i_{oj}(t)$ is the per phase output current of the MC, L_{MCj} and R_{LMCj} is the per-phase inductance and parasitic resistance of the output chokes. The continuous-time derivative in (5) is approximated using the forward Euler method for each kth discrete sample
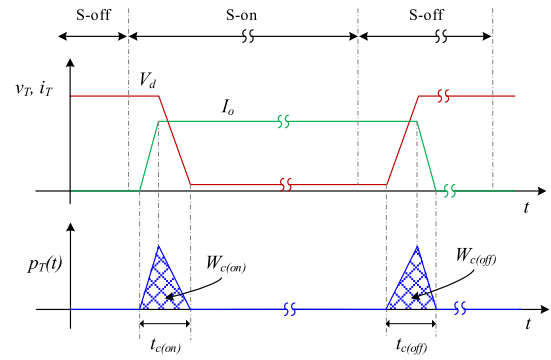
FIGURE 4. Linearized switching characteristics for a switch showing voltage and current when the switch is turned on/off. The bottom figure shows the switching power losses over time.

time steps:

$$\frac{di_{oj}(t)}{dt} \approx \frac{i_{oj}(k+1) - i_{oj}(k)}{T_S} \quad (6)$$

From (5) and (6), the discrete-time model estimates the current at the next sample $(k + 1)$ is given as

$$i_{oj}^{\sigma}(k+1) = \left(1 - \frac{R_{LMCj} T_s}{L_{MCj}}\right) i_{oj}(k) + \frac{T_s}{L_{MCj}} v_{oj}(k) \quad (7)$$

3) INPUT FILTER MODEL
Input filters are required in power electronics converters to eliminate the high-order harmonics generated by converter switching to going back to the supply. The input filter shown in Fig. 3 can be represented using Kirchhoff's voltage and current equations as:

$$V_{Busj}(t) = R_{fj} i_{cj}(t) + L_{fj} \frac{d}{dt} i_{cj}(t) + V_{ej}(t) \quad (8)$$

$$i_{cj}(t) = i_{ej}(t) + C_{fj} \frac{d}{dt} V_{ej}(t) \quad (9)$$

where $i_{cj}(t)$ and $i_{ej}(t)$ are the input and output currents of the filter with inductors L_{fj} and capacitors C_{fj}, R_{fj} is the per-phase parasitic resistance of L_{fj}. The state-space model of the filter can be written as:

$$\begin{bmatrix} \dot{V}_{ej}(t) \\ \dot{I}_{cj}(t) \end{bmatrix} = A_c \begin{bmatrix} V_{ej}(t) \\ i_{cj}(t) \end{bmatrix} + B_c \begin{bmatrix} V_{Busj}(t) \\ i_{ej}(t) \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} \dot{V}_{ej}(t) \\ \dot{I}_{cj}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix}}_{A_c} \begin{bmatrix} V_{ej}(t) \\ i_{cj}(t) \end{bmatrix}$$

$$+ \underbrace{\begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix}}_{B_c} \begin{bmatrix} V_{Busj}(t) \\ i_{ej}(t) \end{bmatrix} \quad (11)$$

Finally, the discrete-time model of the input filter using zero-order hold and sample time Ts is given by:

$$\begin{bmatrix} V_{ej}(k+1) \\ i_{cj}(k+1) \end{bmatrix} = A_q \begin{bmatrix} V_{ej}(k) \\ i_{cj}(k) \end{bmatrix} + B_q \begin{bmatrix} V_{Busj}(k) \\ i_{ej}(k) \end{bmatrix} \quad (12)$$

C. MPC FOR D-STATCOM APPLICATION

Fig. 2 illustrates the system structure with the proposed controller. The objective is to control the reactive power, input and the output currents of the D-STATCOM [19]. The input reactive power and the input current of the converter can be written in orthogonal coordinates as:

$$i_{cn}^{\sigma}(k+1) = A_{q(2,1)}V_{en}(k) + A_{q(2,2)}i_{cn}(k)$$
$$+ B_{q(2,1)}V_{Busn}(k) + B_{q(2,2)}i_e(k) \quad (13)$$

The cost function J is given as

$$J^{\sigma} = \lambda_1 \left(|I_{cA}^{\sigma} - i_{cA}^{*}| + |I_{cB}^{\sigma} - i_{cB}^{*}| + |I_{cC}^{\sigma} - i_{cC}^{*}| \right)$$
$$+ \lambda_2 \left(|I_{oa}^{\sigma} - i_{oa}^{*}| + |I_{ob}^{\sigma} - i_{ob}^{*}| + |I_{oc}^{\sigma} - i_{oc}^{*}| \right) \quad (14)$$

where J is the cost function and I_{cj} is the MC input current and I_{oj} is the MC output current with $j \in [A, B, C]$. Reference values i_{cj}^{*} and i_{oj}^{*} are the MC reference input and output currents respectively. The weight factors λ_1, λ_2 are adjusted to priorities the different parts of the cost function.

III. AN ADAPTIVE COST FUNCTION THAT PENALIZES FIDELITY

Unlike fixed-frequency pulse width modulation techniques, finite control set MPC in power electronics operates using a variable switching frequency. Unconstrained MPC controllers operate on frequencies that are only bounded by the sampling frequency of the controller unit. Controller unit clock speed and code complexity, factor into determining the maximum allowable sampling frequency. The result is system operation at a high switching frequency lower than the sampling frequency. Operating at high frequencies for a long time increases switching losses. One solution is to consider slowing down the sampling time of the MPC regulator by adding a term in the cost function that penalizes switching frequency [37]. Slowing down the MPC algorithm worsens dynamic performance measures (i.e., longer settling time during transients), which accordingly diminishes system fidelity.

A. BACKGROUND ON SWITCHING LOSSES IN POWER ELECTRONICS

Losses in the power semiconductor devices increase as switching frequency increases (the number of times the switches turn on or off). Consider the generic switching characteristics shown in Fig. 4. The energy dissipated in the switching device during the turn-on transition can be approximated as:

$$W_{c(on)} \simeq \frac{1}{2}V_d I_o t_{c(on)} \quad (15)$$

The energy dissipated in the switching device during the turn-off transition can be approximated as:

$$W_{c(off)} \simeq \frac{1}{2}V_d I_o t_{c(off)} \quad (16)$$

The average switching power loss in the switch due to the switching transitions can be approximated based on (15) and (16) [38], and is given by

$$P_s = \frac{1}{2}V_d I_o f_s \left(t_{c(on)} + t_{c(off)} \right) \quad (17)$$

According to (17), the switching power loss in a semiconductor switch varies linearly with the switching frequency f_s and the switching time t_c. Operating at low switching losses is important to increase the overall efficiency and reduce the operating temperature of the converter. This temperature reduction results in reduced thermal stress on the semiconductor devices and other onboard sensors, and the result will be an increase in converter service life and a decrease in maintenance cost [38].

B. APPLICATION OF ADAPTIVE MPC COST FUNCTION FOR D-STATCOM

In a capacitor-less D-STATCOM, illustrated in Fig. 1, system fidelity can be quantified by the total harmonic distortion (THD) of the source current. The IEEE 519-2014 recommended practice and requirements for harmonic control, in electric power systems, specify 5% as the THD requirement for power systems [39]. Meeting THD requirements is sufficient and is expected. Minimizing THD much lower than 5% is not rewarded within the power system.
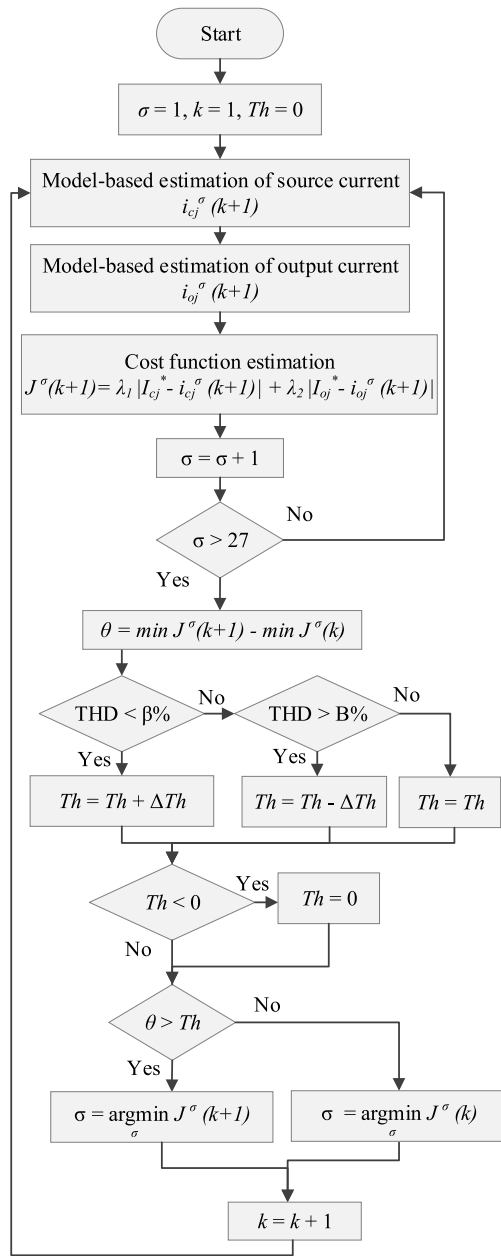
The challenge is to develop a variable controller that can use high switching frequency during transients to improve the model fidelity and to operate at a lower frequency during steady-state while meeting THD requirements ($THD <$ B%). The flowchart in Fig. 5 illustrates an approach to optimize between fidelity and switching frequency. The overall objective is to penalize high fidelity performance with THD lower than β %. The value of β can be set by the designer, i.e. 4%.

After estimating the output current and source current relations at the interval $(k + 1)$ as in (7) and (13) respectively, the cost function at the interval $(k + 1)$ for each of the 27 states is calculated as in (14). The minimum error value $\min J^{\sigma}(k+1)$ is determined and compared to the minimum error value of the previous cycle to determine the tracking error margin,

$$\theta = \min J^{\sigma}(k+1) - \min J^{\sigma}(k) \quad (18)$$

In MPC algorithms that prioritize fidelity, θ must converge to zero. A tracking error threshold (Th) is introduced to eliminate the need for switching if θ is below Th, hence permitting a larger margin of tracking error that can adapt to system performance. The value for Th is adjusted according to the source current THD as is shown

$$Th = \begin{cases} Th + \Delta Th, & THD < \beta\% \\ Th - \Delta Th, & THD > B\% \\ Th, & \beta\% < THD < B\% \end{cases} \quad (19)$$

FIGURE 5. A flowchart for an algorithm that penalizes high fidelity to operate within the IEEE 519-2014 regulations while reducing switching frequency.

TABLE I. System Parameters

PARAMETER	VALUE
Voltage, $V_{LL,rms}$	415 V
Frequency	50Hz
Source impedance (L_s)	3.5mH
Linear load power	4.1kVA, pf=0.812
Non-Linear load power	1000W
Non-linear load output capacitor	400 uF
Clamp circuit capacitance C	150 uF at 900V,
Clamp circuit resistance R	47k Ω, 7 Watt
Output chokes inductance L_{MC}	36mH
Input filter parisitic resistance R_f	1 Ω
Input filter inductance L_f	2mH
Input filter capacitor $C_{f/ph}$	18 uF
Sampling time T_s	40µs
Weight factor λ_1	2
Weight factor λ_2	1
Threshold value	0 - 3
THD operation range setting in adaptive cost function (Fig. 5)	$\beta = 3.5$ B = 5

where σ indicates the switching configuration number from 1 to 27 that is commanded to the capacitor-less D-STATCOM gate drivers.
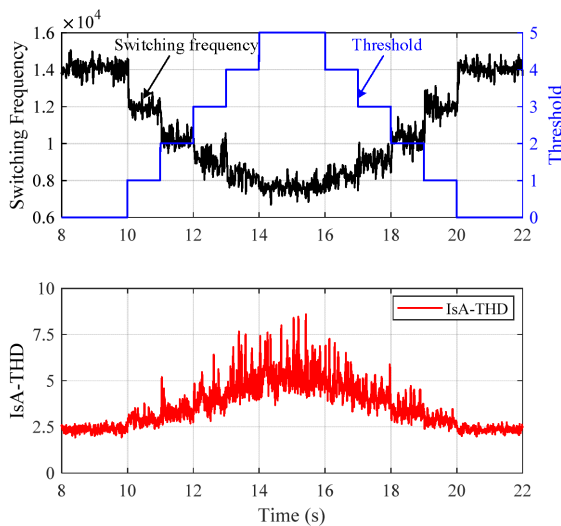
The principle of an adaptive MPC controller that penalizes high fidelity performance, as in Fig. 5, is allowing a margin of tracking error within the cost function; without the need for adding additional terms to the cost function. The margin of tracking error has an adaptive threshold that is adjusted according to the state of the converter (i.e., transient vs. steady-state). The result is an adaptive MPC based controller for the capacitorless D-STATCOM that operates within THD standards, operates at a reduced switching frequency, and tracks transients effectively.

IV. SIMULATED AND EXPERIMENTAL RESULTS
This section presents the simulation and experimental results necessary to validate the effectiveness of the proposed adaptive MPC. Table I shows the system parameters used to obtain both simulation and experimental results.

A. SIMULATION RESULTS
MATLAB/Simulink environment has been used to perform all the simulation studies based on the model shown in Fig. 1. The simulation parameters are listed in Table.I. First, a simulation is performed to study the impact of different threshold values on source current distortion (THD) and average switching frequency. Fig. 6 shows the impact of varying the tracking error margin, Th, within a threshold ranging from 0 to 3 on the variation to average switching frequency and source current THD. It can be noted that selecting a threshold value between 3 and 4 guarantees that the source THD will be less than 5%, and the average switching frequency will be reduced from 12 to 8 kHz.

where, ΔTh is a designer-defined increment/decrement value based on desired system performance. If the value of θ is below Th, this indicates the capacitor-less D-STATCOM operating conditions have not remarkably changed since the previous sampling time; hence, the controller maintains the last configuration switching. Otherwise, the algorithm commands changing the switching state to the configuration that minimizes $J^\sigma(k+1)$ as is shown in

$$\sigma = \begin{cases} \min J^\sigma(k+1), & \theta > \text{Th} \\ \min J^\sigma(k), & \theta < \text{Th} \end{cases} \quad (20)$$
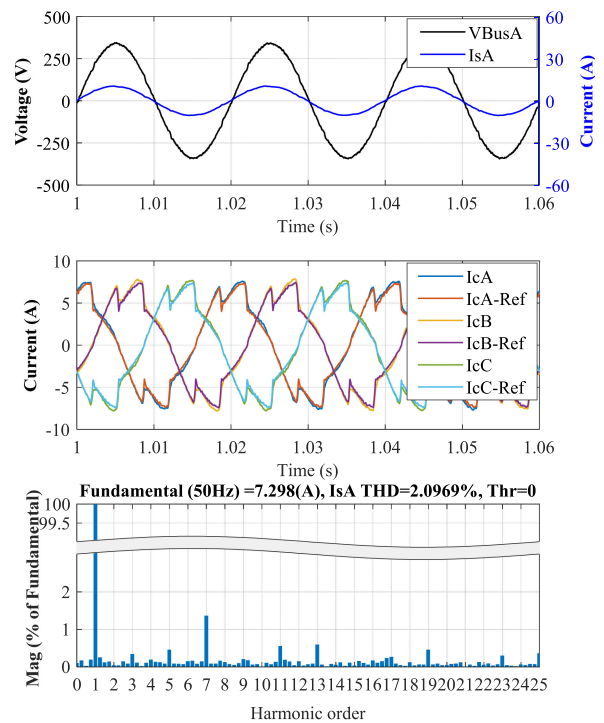
FIGURE 6. Simulation results of the impact of threshold value variation on switching frequency and source current THD.
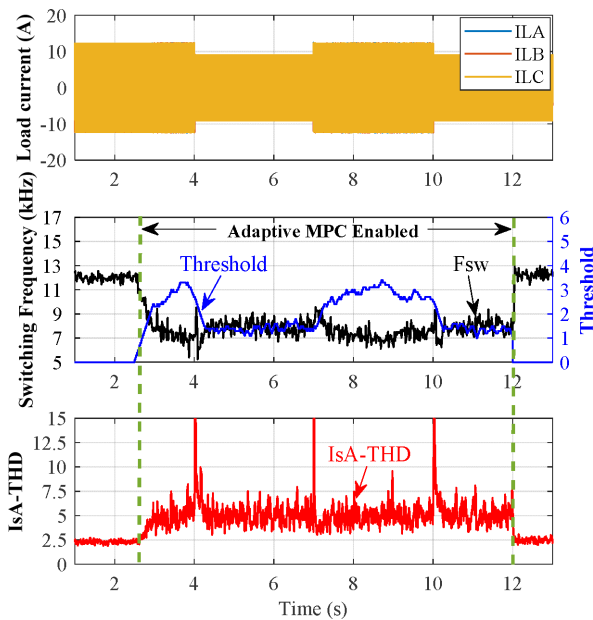
FIGURE 7. Simulation results showing the operation of the adaptive MPC. Fsw is reduced and IsA THD is in the range of 5%.
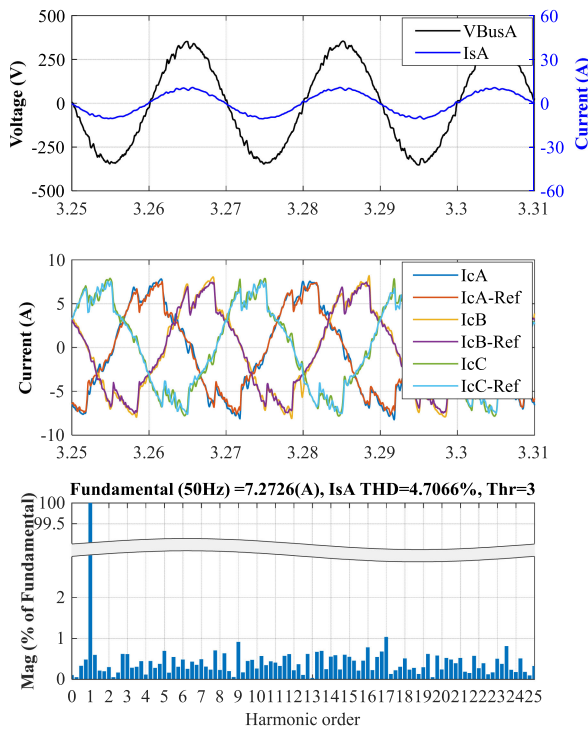

FIGURE 8. Simulation results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 0).

In the simulation results, Fig. 7, the THD for the source current is within the range $\beta = 3.5$ and B = 5 while the adaptive MPC is enabled. Before time 2.5 s and after time 12 s, the adaptive MPC is disabled; hence, the THD value drops to 2.5%, and the switching frequency is high at 12 kHz. the system is operating at high fidelity with a switching frequency. High fidelity operation (THD $<< 5\%$) is not rewarded within the power system, and results in high switching frequency and switching losses. THD values greater than 5%, in Fig. 7 are due to transients during step changes in the load at times = 4 s, 7 s, and 10 s. At time 2.5 s, when the adaptive MPC

algorithm is enabled, the threshold value rises until it settles around $Th = 3.5$, the switching frequency falls to about 7 kHz, and the THD is within the 5% standard. At time 4 s, the first step-change in current occurs, the error margin Th drops, to keep the THD within the limits, until it settles around $Th = 1.2$; the switching frequency rises to about 8 kHz, the settling time until the THD is within regulation is 0.5 s. At time 7 s, a second step-change in load current occurs, the error margin Th rises until it settles around $Th = 3$; the switching frequency falls to about 7 kHz, the settling time until the THD is within regulation is 0.5 s. At time 10 s, the final step-change in load current occurs, the error margin Th drops until it settles around $Th = 1.5$; the switching frequency rises to about 8 kHz, the settling time until the THD is within regulation is 0.5 s. Additionally, the adaptive MPC algorithm depends on the mean value of the THD measurements over 500 samples (1 cycle), so the instantaneous value of THD is expected to be fluctuating around the value THD = 5% between time 2.5 s and 12 s.

Fig. 8 shows the simulation results of the source voltage and current waveforms of the D-STATCOM system with a threshold value $Th = 0$, "MPC cost function that prioritizes fidelity." It can be seen that the D-STATCOM provides power factor correction, so the source voltage and currents are in phase and also provide harmonic power compensation so that the total harmonic distortion of source current is 2.1%.

The performance of the D-STATCOM with a threshold value of 3, "MPC that penalizes fidelity", is shown in Fig. 9. It
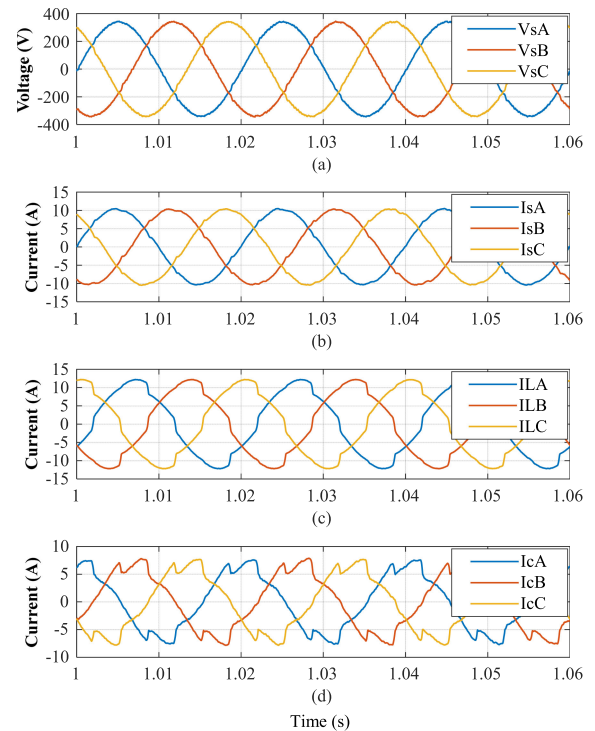
FIGURE 9. Simulation results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 3).

FIGURE 10. Simulation results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 0).

can be observed that the performance of the D-STATCOM is still within the acceptable range (THD = 4.7%), provided that the switching frequency is reduced by more than 35% from 12 kHz to 7 kHz.
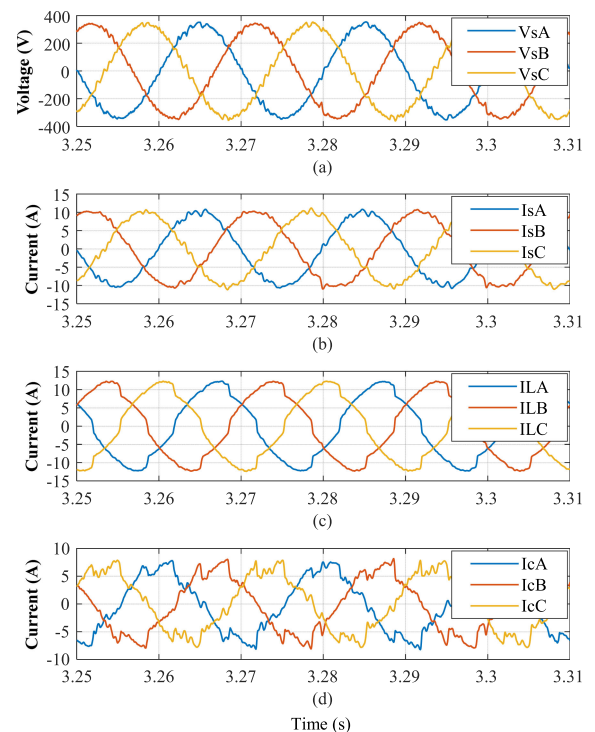
The simulation results of the three-phase quantities of source voltages (V_s), source currents (I_s), Load currents (I_L), and D-STATCOM current are presented in Fig. 10, and Fig. 11. In Fig. 10, the three-phase quantities are shown when the threshold value is 0, while Fig. 11 presents the same benefits when threshold values are around 3. It can be noticed that there are some distortions in the waveforms in Fig. 11 compared with Fig. 10 because the controller forced the system to run at a lower switching frequency in order to reduce switching losses.

B. EXPERIMENTAL RESULTS

The proposed control algorithm was verified experimentally in the renewable energy and advanced power electronics research laboratory at Texas A&M University at Qatar. The system consists of a 7.5 kVA capacitor-less D-STATCOM based matrix converter topology, as shown in Fig. 12. A dSPACE Scalexio is used to control the D-STATCOM system. The controller consists of a processing unit to run the MPC algorithm and other protection codes, and dSPACE LAbBox[TM] that have four FPGA modules to perform measurements using 16 bit ADC, four-step commutation, and hardware protection.
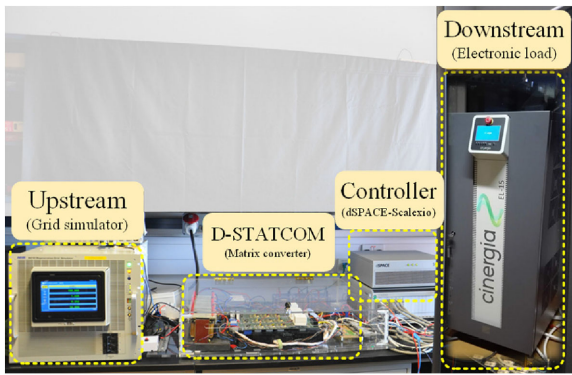

FIGURE 11. Simulation results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 3).
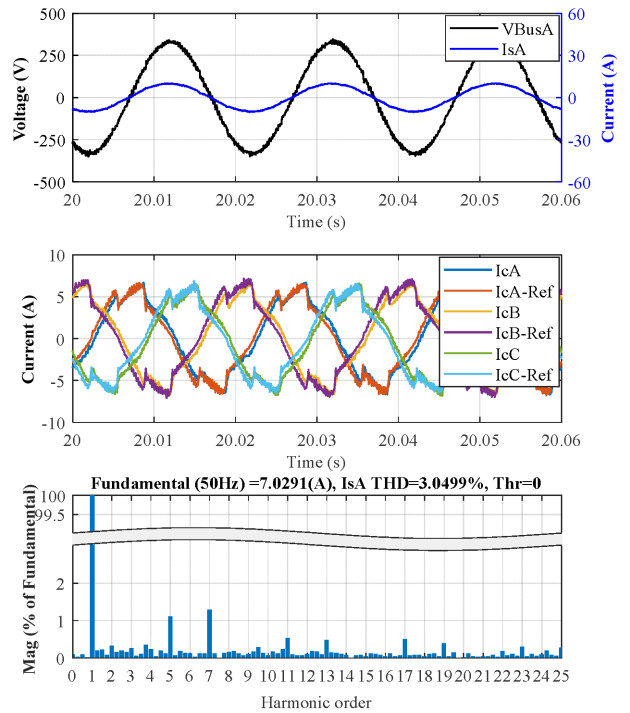
FIGURE 12. Hardware setup of a 7.5 kVA capacitor-less D-STATCOM system representing one bus in a radial destitution system The upstream system is emulated by the grid simulator and the downstream loads are emulated by the electronic load for proof of concept.
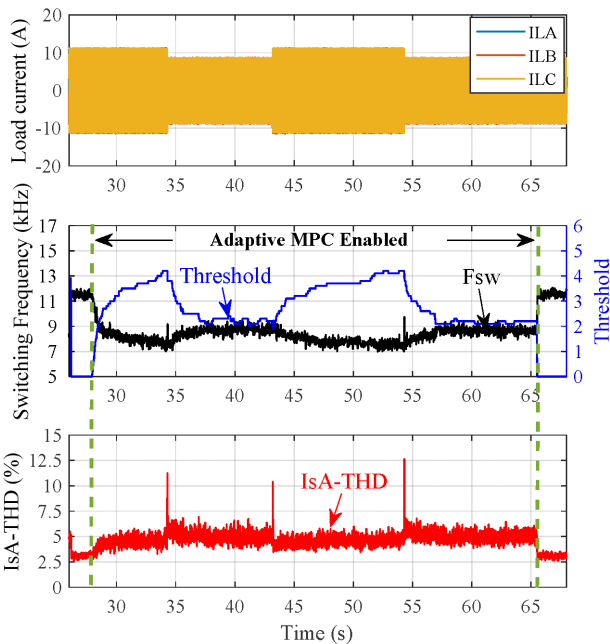
FIGURE 13. Experimental results showing the operation of the adaptive MPC. Fsw is reduced and IsA-THD is in the 5% range.
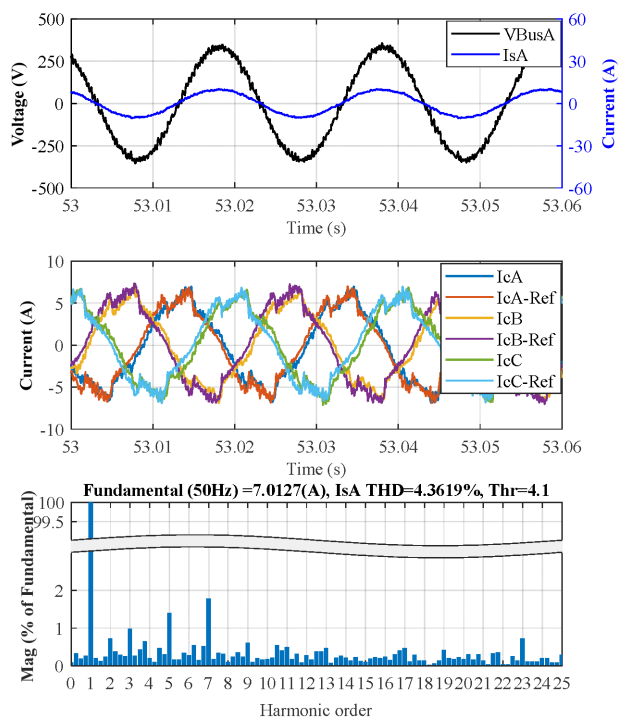

FIGURE 14. Experimental results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 0).

A 12 kVA three-phase grid simulator (NHR-9410) with series impedance is used to emulate the upstream side of the distribution network. Downstream (load side) is emulated using Cinergia 15 kVA electronic load. dSPACE ControlDesk software is used to supervise and control the experiment in real-time and view and store the experimental results and modify the desired control parameters during the experiment.

Initially, Fig. 13 presents the experimental results showing the performance of the proposed approach during dynamic loading. It can be seen that the adaptive MPC is enabled at time after 15 s and disabled at time after 65 s. As can be observed, the average switching frequency (in kHz) was around 12 kHz when the threshold value was 0. After time 15 s, the threshold value is changing adaptively according to

the load variations, and the average switching frequency is decreasing from 12 kHz to the 8 kHz range. When the load current change, the threshold value adjusts itself automatically to maintain a lower switching frequency with acceptable source current THD. It can be depicted that the average switching frequency is reduced by 35% (from 12 kHz to 8 kHz). Explanation of the simulation results in Fig. 7 also applies to experimental results in Fig. 13.

Fig. 14 illustrate the experimental results of the system with adaptive MPC are disabled (threshold value of zero) during the time of 20 s. It can be seen that the source voltage and current are in phase; this means that the D-STATCOM provides power factor correction function, and the D-STATCOM current tracking its reference and the source current THD is in the range of 3%.

Fig. 15 shows the experimental results after enabling the adaptive MPC in the time of 52 s and when the threshold value is around 4. It can be noted that the adaptive controller algorithm was able to operate the D-STATCOM device by providing power factor correction and harmonic compensation, as in Fig. 12 with a lower switching frequency of 8 kHz provided that the source current THD with 5% range.
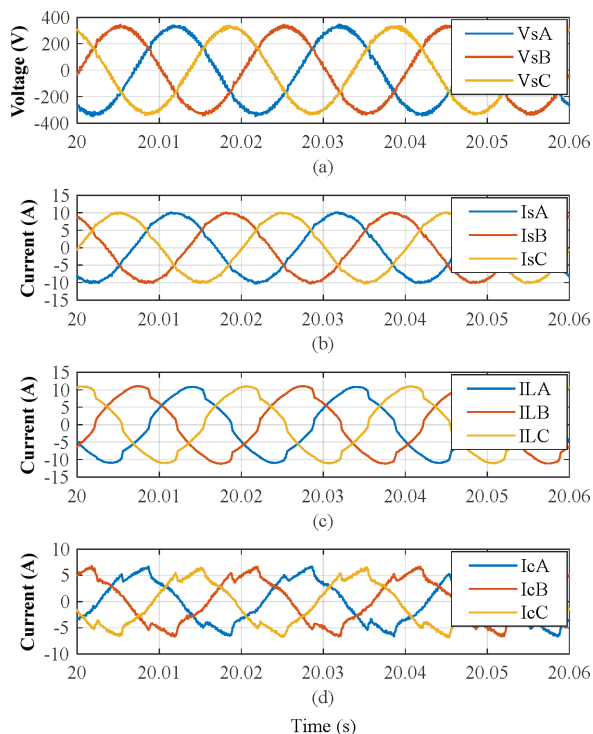
The experimental results of the three-phase quantities of source voltages (V_s), source currents (I_s), Load currents (I_L) and D-STATCOM current are presented in Fig. 16 and Fig. 17. in Fig. 16, the three-phase quantities are shown when the threshold value is 0, while Fig. 17 presents the same benefits when threshold values are around 3. It can be noticed that

FIGURE 15. Experimental results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 3).

FIGURE 16. Experimental results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 0).
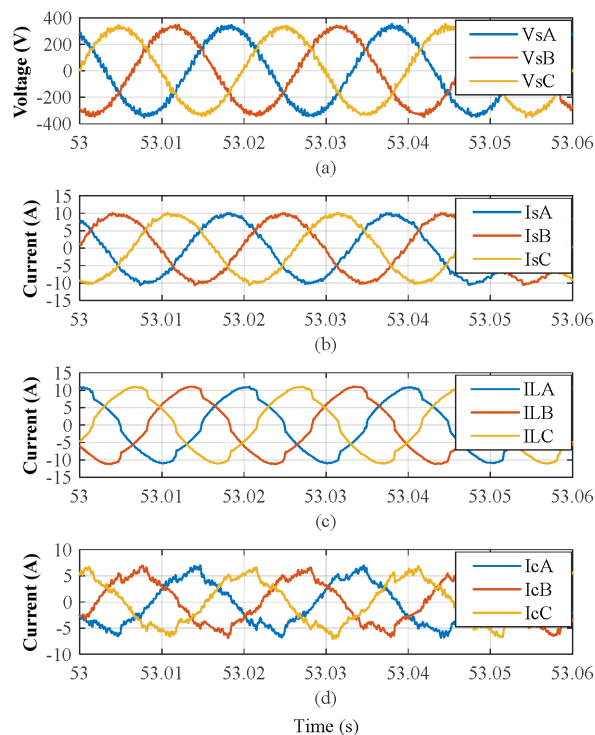
FIGURE 17. Experimental results showing source voltage and current, D-STATCOM compensation currents tracking, and source current THD. (Threshold = 3).

there are some distortions in the waveforms in Fig. 17 compared with Fig. 16 because the controller forced the system to run at lower switching frequency in order to reduce switching losses.

V. CONCLUSION

This paper presented an adaptive MPC controller that penalizes high fidelity performance in a capacitorless D-STATCOM, within permissible THD standards, to reduce switching frequency and switching losses. Penalizing high fidelity performance is principally allowing a margin of tracking error within the cost function, without the need for adding additional terms to the cost function. The margin of tracking error has an adaptive threshold that is adjusted according to the state of the converter (i.e., transient vs. steady-state). The result is an adaptive MPC based controller for the capacitorless D-STATCOM that operates within THD standards, operates at a reduced switching frequency, and tracks transients effectively. Simulation and experimental results presented in this paper for a 7.5 kVA capacitor-less D-STATCOM demonstrate that increasing the error threshold in the MPC cost function results in reducing switching frequency by 33% while increasing total harmonic distortion with IEEE 519-2014 5% standards. The benefit of the proposed system is reducing switching losses and improving overall system reliability.

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