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Modular Multilevel Converter Switching Frequency Harmonics Analysis and Suppression Through Cell Voltage Control

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ABSTRACT This paper investigates the impact of reference's bias on the high frequency voltage spectrum for the modular multilevel converters (MMC). Analytical solution of the voltage spectrum under carrier Phase Shifted Pulse Width Modulation (PSPWM) is derived using double Fourier integral analysis. The distribution of the switching frequency voltage harmonics is found to be directly related to the ratio between the dc-link voltage and the cell voltage. A control method utilizing this phenomenon is thereby proposed to suppress switching frequency harmonics in the Differential Mode Voltage (DMV) and Common Mode Voltage (CMV). Cell voltage control trade-offs considering different cell numbers, different ac voltages, 3rd harmonics injection, and cell voltage stress are also investigated. The analysis and control method are validated through experiments on a 1.25 megawatt MMC testbed.

INDEX TERMS Common mode voltage, differential mode voltage, double Fourier integral, harmonics suppression, modular multilevel converter, phase-shifted PWM, switching harmonics.

I. INTRODUCTION

Due to the high modularity, high scalability, low semiconductor device stress, low switching losses, and low output harmonics, the Modular Multilevel Converter (MMC) is an increasingly attractive topology for high- and medium-voltage systems [1], [2]. With the development of the High Voltage Direct Current (HVDC) transmission, MMC is widely adopted to convert the power between high voltage alternative current and HVDC [3], [4]. Correspondingly, the MMC is also established in medium-voltage (MV) system applications, such as, motor drives [5], Static Synchronous Compensators (STATCOMs) [6], energy storage systems [7], and shipboard power conversion units [8], [9].

Many carrier based MMC modulation methods have been proposed over the last few decades [10]–[15], most of them are phase shifting and level shifting variations. Space vector modulation and stair case modulation are also applied in MMC [16], [17]. The algorithm complexity of the space vector modulation techniques grows exponentially with the number of levels in the converter [16]. Staircase modulation is simple for implementation, and it becomes a viable alternative for the modulation of the MMC with increased cell numbers and output voltage levels [17]. Phase Shifted Pulse Width Modulation (PSPWM) equally distributes the switching events between different cells, so the power is evenly distributed in cells. The capacitor voltage is also easier to balance using PSPWM [12], [13]. Level-shifted Phase Disposition Pulse Width Modulation (PDPWM) is confirmed to have less output voltage distortion than PSPWM [12], [14]. However, cells energy is not evenly distributed using PDPWM, e.g. more power is handled by the first cell of each arm with more switching events [15]. In this paper, PSPWM was applied and discussed.

Analytical solutions provide accurate harmonics components of a PWM waveform. Therefore, the voltage spectrum of various modulation strategies can be calculated and compared theoretically. Moreover, the modulation methods can be optimized to regulate the voltage harmonics and improve the

converter performance, based on the insights gained from analytical solutions. The most well-known analytical method for determining the harmonic components of a PWM waveform is a Two-Dimensional (2-D) double Fourier integral analysis, which is comprehensively introduced in [18]. To avoid the complex 2-D Fourier integral, several 1-D Fourier integral methods are proposed for specific topologies based on the original reference superposition [19], [20]. In [19], separated references and a pair of phase modulated sawtooth functions generate the sideband groups of the PWM spectrum for two-level converters. In [20], multilevel waveforms are separated into a summation of two-level pulse trains with the PDPWM strategy. Using the PWM voltage analytical solution, more depth of understanding and design improvement of converters is established; such as, calculation of inverter dc-link current harmonics [21], Common Mode (CM) voltage reduction [22], [23], sampling delay effects characterization [24], and Magn etic core loss calculations [25].

Compared with the cascaded H-bridge multilevel converters [18], there is significant bias in the arm voltage reference of an MMC. The bias, named as D, is previously treated as a fixed number [12], [13], [26], [27]. In these research, the D was neglected during the 2-D Fourier analysis and added to the solution afterwards. Although this approach can significantly reduce the complexity of analysis, but it also causes inaccuracy due to the nonlinear feature of the double Fourier integration. Instead, as will be shown in Section II, effect of the bias D is a change in the upper and lower bounds of the integration. As a result, the harmonic distribution of an MMC, when considering D, appears to be very different from that of a CMC and other voltage source converters.

The first contribution of this paper is to introduce D as a variable in the early stage of double Fourier analysis for the PSPWM controlled MMC. A harmonic control coefficient is identified to represent the impact of D on high frequency harmonics. Differential Mode Voltage (DMV) and Common Mode Voltage (CMV) spectrum are derived, and the switching frequency harmonic distribution in CMV and DMV are presented with closed form equations. The second contribution is a new control method proposed for reducing MMC's CMV and DMV switching harmonics. Experimental results obtained using a 1.25 MW MMC testbed are presented to validate the analytical solutions as well as the control method.

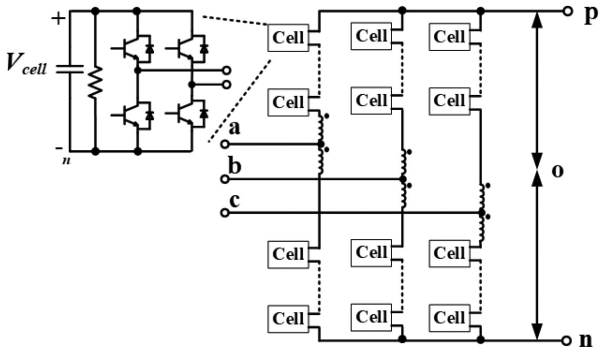


FIGURE 1. Circuit topology of MMC.

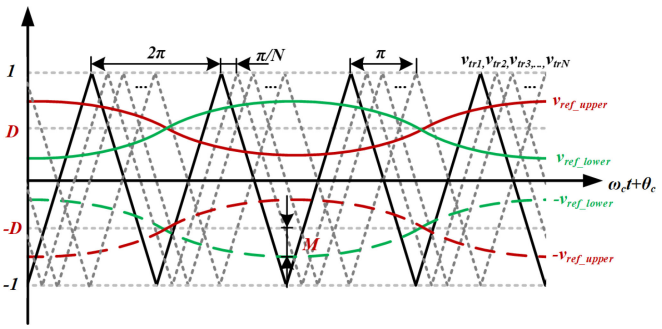


FIGURE 2. PSPWM strategy of MMC.

II. ANALYTICAL SOLUTION OF MMC WITH PSPWM

A. CIRCUIT CONFIGURATION OF MMC

The MMC topology is shown in Fig. 1, a full bridge cell is chosen here for dc-fault handling capability [2]. It is built with six arms, each arm consisting of N full-bridge cells in series. Each cell is able to generate positive, zero, and negative output voltages. A coupled inductor is connected in each phase to reduce the dc ripple. Zero potential reference point is marked in the figure as '0'.

Phase-shift modulation is applied, as shown in Fig. 2. The carriers are the same for upper and lower arms. The carriers $v_{tr1}, v_{tr2}, v_{tr3},...,v_{trN}$ are shifted by π/N in each cell. The modulation reference voltage for a single phase is listed in (1), where ω_0 is the fundamental frequency and θ_0 is the phase angle. For the upper and lower branch, the ac reference is the same while the dc reference is of opposite polarity. The dc modulation index D and ac modulation index M are defined by (2) and (3), where V_{dc} and V_{ac} are the dc-link voltage and the ac phase voltage magnitude, respectively.

$$\begin{cases} v_{ref\_upper} = M\cos(\omega_0 t + \theta_0) + D \\ v_{ref\_lower} = -M\cos(\omega_0 t + \theta_0) + D \end{cases} \tag{1}$$

$$D = \frac{V_{dc}}{2NV_{cell}} \tag{2}$$

$$M = \frac{V_{ac}}{NV_{cell}} \tag{3}$$

B. ANALYTICAL SOLUTION FOR SINGLE CELL

Double Fourier integral analysis is utilized in this paper to determine the MMC voltage harmonics [18], the process for CMC and MMC half-bridge are shown in Fig. 3 and Fig. 4. In Fig. 3(a) and Fig. 4(a), CMC and MMC has the same double-edge carriers and the same ac modulation index, while MMC reference has an additional bias. In Fig. 3(b) and Fig. 4(b), x and y axis are the carrier frequency time-line and the fundamental frequency time-line, which is defined in (4). The PWM waveform is deconstructed as a two-dimensional function of the reference and carrier phase spaces, resulting

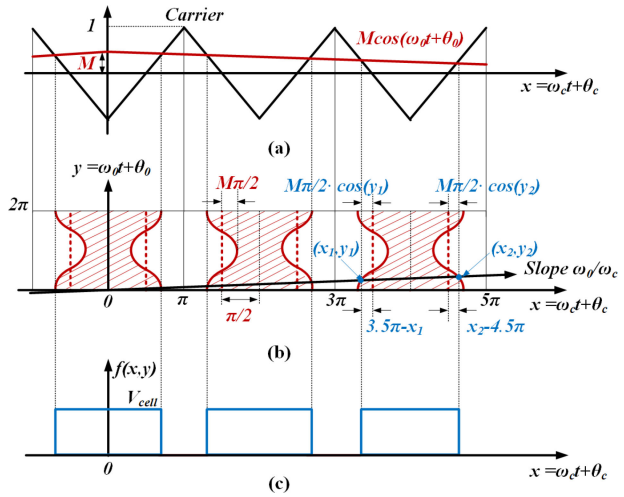


FIGURE 3. CMC Half-bridge switching: (a) double-edge PWM, (b) *x*, *y* plane showing intersection of reference with unit cells, and (c) resulting PWM voltage.

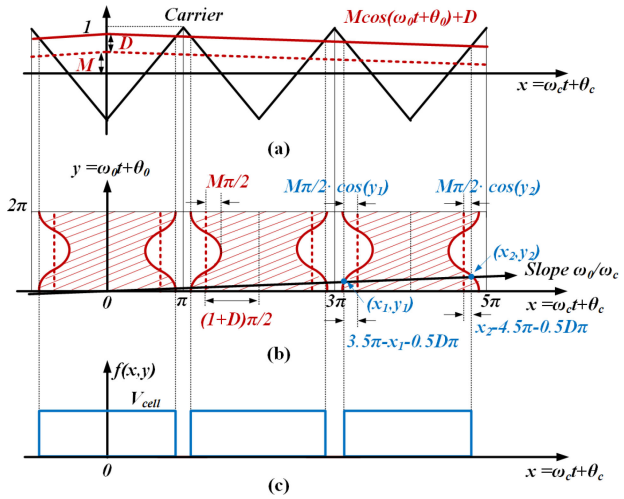


FIGURE 4. MMC Half-bridge switching: (a) double-edge PWM, (b) *x*, *y* plane showing intersection of reference with unit cells, and (c) resulting PWM voltage.

in a separately periodic function in each dimension. ω_c is the carrier frequency and θ_c is the phase angle. The ω_0/ω_c slope line is the solution trajectory, which has two intersections with the y axis reference voltage within every carrier period. Those intersections corresponds to the actual switching instant in the switching devices. As shown in Fig. 3(c) and Fig. 4(c), $f(x, y)$ is the switched output voltage and V_{cell} is the cell capacitor voltage.

$$\begin{cases} x = \omega_0 t + \theta_0 \\ y = \omega_c t + \theta_c \end{cases} \tag{4}$$

In order to calculate the switching instant time for double-edge modulation MMC, an example is shown in Fig. 3(b) and Fig. 4(b) between 3π and 5π carrier period. The intersection point magnitude can be expressed in both x and y axis, dc modulation index D is introduced due to the reference bias. For the MMC upper arm single cell half-bridge leg, the switching instant can be expressed as

$$x_1 = 2\pi p - \frac{\pi}{2}\left(1 + D + M\cos\left(y_1\right)\right) \quad p = 0, 1, 2 \ldots, \infty \tag{5}$$

for $f(x, y)$ changing from 0 to V_{cell}, and

$$x_2 = 2\pi p + \frac{\pi}{2}\left(1 + D + M\cos\left(y_2\right)\right) \quad p = 0, 1, 2 \ldots, \infty \tag{6}$$

for $f(x, y)$ changing from V_{cell} to 0.

After the modulation, $f(x, y)$ can be calculated by the double Fourier integration (7). The real and imaginary coefficients are obtained by (8). The carrier index variable m and the base band index variable n define the frequency of each harmonic component of the switched phase leg output voltage.

$$f(x, y) = \frac{A_{00}}{2} + \sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\left[A_{mn}\cos\left(mx + ny\right) + B_{mn}\sin\left(mx + ny\right)\right] \tag{7}$$

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+D+M\cos y)}^{\frac{\pi}{2}(1+D+M\cos y)} V_{cell}e^{j(mx+ny)}dxdy \tag{8}$$

Based on (7) and (8), half-bridge output voltage v_{hb} is derived in (9). Unlike the conventional half-bridge switched output voltage [18], dc modulation index has added a trigonometric function coefficient on the harmonics magnitude in MMC. The trigonometric function coefficient is different for the even sidebands and the odd sidebands.

$$\begin{aligned} v_{hb} = {} & (1 + D)\frac{V_{cell}}{2} + \frac{MV_{cell}}{2}cos(x) \\ & + \frac{2V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(Mm\frac{\pi}{2}\right) \\ & \times \sin\left(\left(Dm + m + n\right)\frac{\pi}{2}\right)\cos\left(my + nx\right) \end{aligned} \tag{9}$$

In the full-bridge cell, the output voltage is the subtraction of two half-bridge outputs with an opposite reference and same carrier. The full-bridge output voltage v_{hb} is derived in (10) based on (9). There are only even carrier multiples and their fundamental sideband components.

$$\begin{aligned} v_{fb} = {} & DV_{cell} + MV_{cell}cos(x) \\ & + \frac{2V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(Mm\pi\right) \\ & \times \sin\left(\left(2Dm + 2m + n\right)\frac{\pi}{2}\right)\cos\left(2my + nx\right) \end{aligned} \tag{10}$$

C. ANALYTICAL SOLUTION FOR A THREE-PHASE MMC

With the PSPWM, y axis carriers are shifted by π/N among N cells. The arm voltage v_{upper} is the sum of all the cells,

as derived in (11), based on (10). There are $2Nm$ times carrier multiples and fundamental sideband components. It is similar for the lower arm analytical solution derivation, the only difference is to change D to $-D$.

$$\begin{aligned} v_{upper} &= DNV_{cell} + MNV_{cell}\cos(x) \\ &+ \frac{2V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n(MNm\pi) \\ &\times \sin\left((2DNm + 2Nm + n)\frac{\pi}{2}\right)\cos(2Nmy + nx) \end{aligned} \tag{11}$$

Based on the upper and lower arm switched voltage solution, the single phase dc output voltage $v_{dc\_a,b,c}$ can be derived in (12). There are $2Nm$ times carrier multiples and their $2n$ times fundamental sideband components.

$$\begin{aligned} v_{dc\_a,b,c} &= v_{upper} + v_{lower} = 2DNV_{cell} \\ &+ \frac{4V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{2n}(MNm\pi) \\ &\times \sin(DNm\pi)\cos\left((2Nm + 2n)\frac{\pi}{2}\right)\cos(2Nmy + 2nx) \\ &\left(\theta_0 \text{ in } x \in \left\{0, -\frac{2}{3}\pi, \frac{2}{3}\pi\right\}\right) \end{aligned} \tag{12}$$

The rail to rail dc bus voltage is the averaged summary of the phase leg voltages in (12). This dc side DMV, referred as v_{DM}, is presented in (13). v_{DM} includes $2Nm$ times carrier multiples and their $6n$ times fundamental sideband components.

$$\begin{aligned} v_{DM} &= \frac{v_{dc\_a} + v_{dc\_b} + v_{dc\_c}}{3} = 2DNV_{cell} \\ &+ \frac{4V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{6n}(MNm\pi) \\ &\times \underbrace{\sin(DNm\pi)}_{\text{Bias Impact}}\cos\left((2Nm + 6n)\frac{\pi}{2}\right)\cos(2Nmy + 6nx) \end{aligned} \tag{13}$$

Based on the upper and lower arm switched voltage solution, the single phase ac output voltage v_{a,b,c_0} can be derived in (14). There are $2n+1$ times fundamental sideband components around $2Nm$ times carrier multiples.

$$\begin{aligned} v_{a,b,c\_0} &= \frac{v_{upper} - v_{lower}}{2} = MNV_{cell}\cos(x) \\ &+ \frac{2V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{2n+1}(MNm\pi) \\ &\cos(DNm\pi)\sin\left((2Nm + 2n + 1)\frac{\pi}{2}\right) \\ &\cos(2Nmy + (2n+1)x) \\ &\left(\theta_0 \text{ in } x \in \{0, -\frac{2}{3}\pi, \frac{2}{3}\pi\}\right) \end{aligned} \tag{14}$$

In the 3-phase MMC, CMV is equally important as DMV, which is the excitation source of ground leakage current and essential to grounding fault investigation [22], [28]. The v_{CM} is derived by (15), in which the harmonics are $6n+3$ times fundamental sideband components around $2Nm$ times carrier multiples.

$$\begin{aligned} v_{CM} &= \frac{v_{a\_0} + v_{b\_0} + v_{c\_0}}{3} \\ &= \frac{2V_{cell}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_{6n+3}(MNm\pi) \\ &\underbrace{\cos(DNm\pi)}_{\text{Bias Impact}}\sin\left((2Nm + 6n + 3)\frac{\pi}{2}\right) \\ &\cos(2Nmy + (6n+3)x) \end{aligned} \tag{15}$$

III. ANALYSIS OF MMC VOLTAGE REFERENCE BIAS IMPACT ON THE SWITCHING FREQUENCY HARMONICS

A. HARMONIC CONTROL COEFFICIENT

The analytical results in section II reveals the bias D can affect every high-frequency components in the voltage spectrum, see the red highlighted terms in (13) and (15). In this research, their absolute value are defined as harmonic control coefficients, as shown in (16). In the spectrum of other voltage source converters [18] and previous analytical solutions for MMC, similar terms in the equivalent position are always discrete values of 0 and 1. As a comparison, the harmonic control coefficients are continuous value ranging from 0 to 1.

$$\begin{cases} k_{dm} = |\sin(DNm\pi)| \\ k_{cm} = |\cos(DNm\pi)| \end{cases} \tag{16}$$

By choosing the combination of D and N, the harmonic control coefficient can be used for harmonics selection. Modifying k_{dm} and k_{cm} can regulate the harmonic distribution between DMV and CMV. $k_{dm} = 0$ means harmonics are 0 in DMV at $2Nmf_c$, while the $2Nmf_c$ harmonics are maximum in CMV, and vice-versa. It should be noted that, according to (16), harmonics of DMV and CMV can not be removed simultaneously. Trade-offs need to be made according to CM and DM requirements and their corresponding loop impedance.

B. CELL VOLTAGE GRANULARITY

In engineering practice, the D can not be controlled too far away from 0.5 otherwise it will significantly increase the voltage stress or cause over-modulation. A practical solution for D under certain CMV or DMV requirements can only be found with enough cell number N. To further explore the trade-off between voltage stress and voltage harmonic under different cell number, we name $V_{dc}/V_{cell} = 2DN$ as the voltage granularity, then harmonic control coefficient can be written in the form of (17). It is shown that the reference bias impact on the MMC switched voltage harmonics is essentially through the voltage granularity. As shown in Fig. 5, the harmonic control coefficient in DMV/CMV is solely affected by the voltage

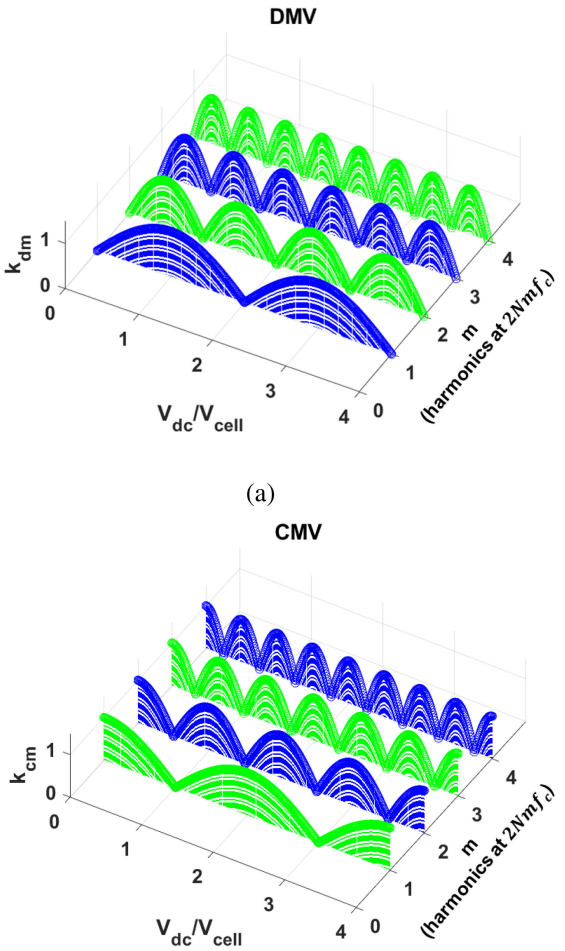


FIGURE 5. harmonic control coefficient with different cell voltage granularity: (a) DMV; and (b) CMV.

granularity.

$$\begin{cases} k_{dm} = \left|\sin\left(\frac{V_{dc}}{V_{cell}} m\frac{\pi}{2}\right)\right| \\ k_{cm} = \left|\cos\left(\frac{V_{dc}}{V_{cell}} m\frac{\pi}{2}\right)\right| \end{cases} \tag{17}$$

The ideal operational condition to remove $2Nmf_c$ harmonics in CMV or DMV is listed in (18). Generally, when V_{dc}/V_{cell} is even, k_{dm} is 0 for all the $2Nmf_c$ harmonics in DMV, which means the DMV switching frequency harmonics can be completely removed. Meanwhile k_{cm} is maximum 1 for all the $2Nmf_c$ harmonics in CMV, the CMV contains the maximum switching frequency harmonics. On the other hand, when V_{dc}/V_{cell} is odd, switching frequency harmonics is 0 at $2Nf_c$, $6Nf_c$, $10Nf_c$, etc. for CMV, and 0 at $4Nf_c$, $8Nf_c$, $12Nf_c$, etc. for DMV.

$$\frac{V_{dc}}{V_{cell}} = \begin{cases} \frac{even}{m}\ (k_{dm}=0) \\ \frac{odd}{m}\ (k_{cm}=0) \end{cases} \tag{18}$$

(harmonics is 0 at $2Nmf_c$)

From above analysis, following conclusions can be found:

1) To have minimum DMV at nominal condition, the MMC should be designed with even cell number in each arm.
2) To have minimum CMV at nominal condition, the MMC should be designed with odd cell number in each arm.
3) In any operation condition, there is always a cell voltage can achieve nearly zero DMV. As a result, an MMC can be designed with no dc loop inductance. The cost for doing so is additional voltage stress.
4) In any operation condition, there is always a cell voltage can achieve minimum CMV. The cost for doing so is additional voltage stress.
5) Minimum DMV and minimum CMV can't be achieved at the same time.

IV. PROPOSED CELL VOLTAGE CONTROL METHOD TO SUPPRESS THE VOLTAGE HARMONICS

A. TARGET CELL VOLTAGE CALCULATION

Since the the cell voltage granularity changes the harmonic control coefficient, the cell voltage V_{cell} can be controlled to suppress the voltage harmonics. There is another constrain for the cell voltage value selection, $D + M \leq 1$. For a specific V_{dc}, there could be multiple V_{cell} values to match (18), only the minimum V_{cell} is discussed in this paper.

When the V_{cell} is controlled to the value in (19), MMC operates at minimum DMV mode. All the switching frequency harmonics can be removed from DMV, and there is no need for DM filters in the system.

$$V_{cell} = \frac{V_{dc}}{2floor\left(\frac{\frac{N}{(1-k_{3rd})Vac}}{\frac{V_{dc}}{}}+1\right)}(DMV) \tag{19}$$
$$(k_{dm} = 0 \text{ at } 2Nmf_c, m = 1, 2, 3\ldots)$$

When the V_{cell} is controlled to the value in (20), MMC operates at minimum CMV mode. Partial CMV switching frequency harmonics ($2Nmf_c$ harmonics when m is odd) can be removed, including the lowest switching frequency harmonics which matters most in the CM filter design.

$$V_{cell} = \frac{V_{dc}}{2floor\left(\frac{\frac{N}{(1-k_{3rd})Vac}}{\frac{V_{dc}}{}}-\frac{1}{2}\right)+1}(CMV) \tag{20}$$
$$(k_{cm} = 0 \text{ at } 2Nmf_c, m = 1, 3, 5\ldots)$$

In (19) and (20), k_{3rd} is the 3^{rd} harmonics injection percentage. In some applications, if specific DMV/CMV frequency harmonics need to be removed (e.g. for EMI purpose), V_{cell} can also be derived accordingly based on (18).

B. CELL VOLTAGE CONTROL AT DIFFERENT OPERATION CONDITIONS

1) RECTIFIER APPLICATION

When the ac voltage is fixed (e.g. 3.3 kV $l-l$). The target V_{cell} from (19) and (20) is calculated at different V_{dc}, as

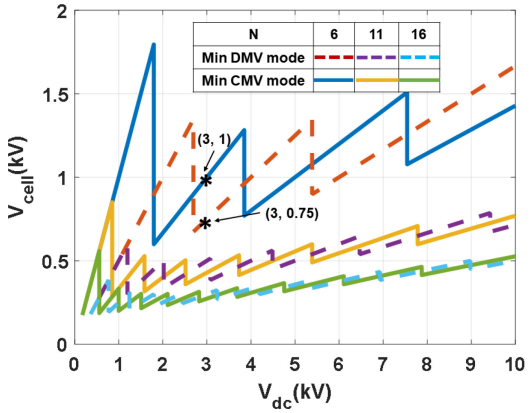


FIGURE 6. V_{cell} for minimum DMV/CMV mode with different cell numbers (V_{l-l} = 3.3 kV).

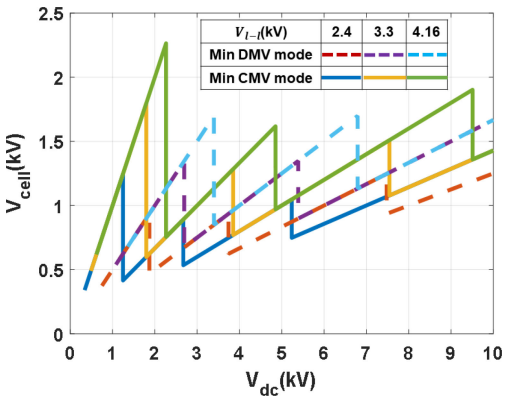


FIGURE 7. V_{cell} for minimum DMV/CMV mode with different ac voltages (N = 6).

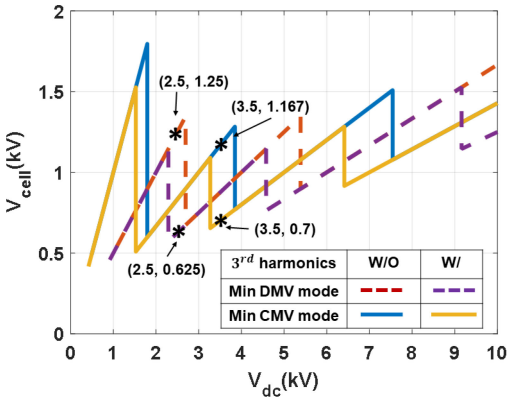


FIGURE 8. V_{cell} for minimum DMV/CMV mode with 3^{rd} harmonics injection (V_{l-l} = 3.3 kV, N = 6).

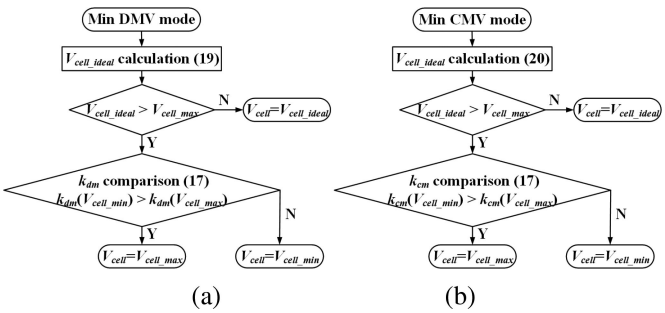


FIGURE 9. Cell voltage control algorithm to minimize the voltage harmonics: (a) minimum DMV mode, and (b) minimum CMV mode.

shown in Fig. 6. The target V_{cell} changes as sawtooth pattern with increased V_{dc}. When the cell number increases, the V_{cell} value reduces and its pattern becomes almost linear with the increased V_{dc}. In Fig. 6, V_{dc} does not reach 0 because there is no target V_{cell} can match (19) (20) with the condition $D + M \leq 1$.

2) INVERTER APPLICATION

When the ac side voltage changes, the maximum dc modulation index changes. Therefore, the target V_{cell} from (19) and (20) changes accordingly, as shown in Fig. 7. When the ac voltage reduces, the target V_{cell} value reduces.

3) WITH 3^{rd} HARMONICS INJECTION

The third harmonic injection is a widely used method to increase the dc bus voltage utilization and improve the system efficiency [29]. With the same ac voltage, 3^{rd} harmonics injection is able to reduce the ac modulation index, which means larger dc modulation index can be realized. Then, the required V_{cell} can be reduced for the minimum DMV/CMV mode. As shown in Fig. 8, when k_{3rd} is 15%, the required V_{cell} is reduced. However, in applications such as PV, 3^{rd} harmonic injection can not be used because it would generate large ground leakage current due to the small capacitive impedance in the common mode loop [22].

4) WITH LIMITED CELL VOLTAGE RANGE

The maximum cell voltage is usually limited by its switching device or the capacitor's voltage rating. If the required V_{cell} is larger than such limitation, the DMV/CMV harmonics cannot be suppressed ideally. However, the V_{cell} can still be optimized within the rating to achieve the minimum voltage harmonics. To avoid over modulation, there is also a minimum voltage limitation, as shown in (21).

$$V_{ac}/N + V_{dc}/2N = V_{cell\_min} \leq V_{cell} \leq V_{cell\_max} \tag{21}$$

When the ideal V_{cell} is not in the range of (21), harmonic control coefficient variation between V_{cell_min} and V_{cell_max} is less than 1/4 triangular cycle, as shown in Fig. 5. Therefore, the minimum DMV/CMV mode is either at V_{cell_min}, or at V_{cell_max}. The cell voltage control algorithm to minimize the voltage harmonics is shown in Fig 9. An optimized V_{cell} is selected based on which cell voltage generates the smaller harmonics. After the control algorithm is applied, the design example of the optimized V_{cell} is shown in Fig. 10 with a cell voltage rating of 1 kV. Sometimes minimum DMV/CMV mode operates at V_{cell_max}, sometimes operates at V_{cell_min}.

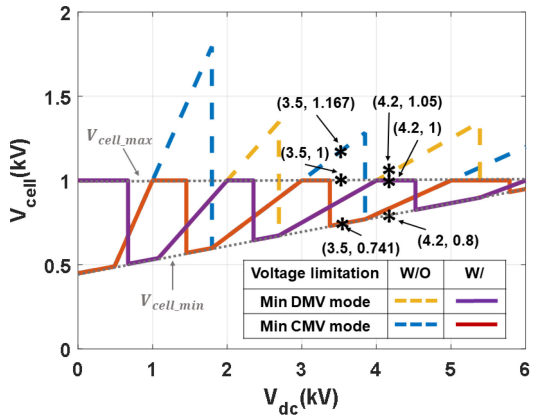


FIGURE 10. V_{cell} for minimum DMV/CMV mode with limited V_{cell} range (V_{l-l} = 3.3 kV, $N = 6$).

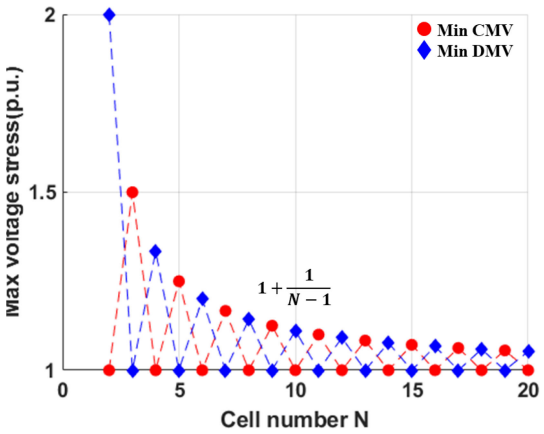


FIGURE 12. Maximum voltage stress for the proposed method with different N.

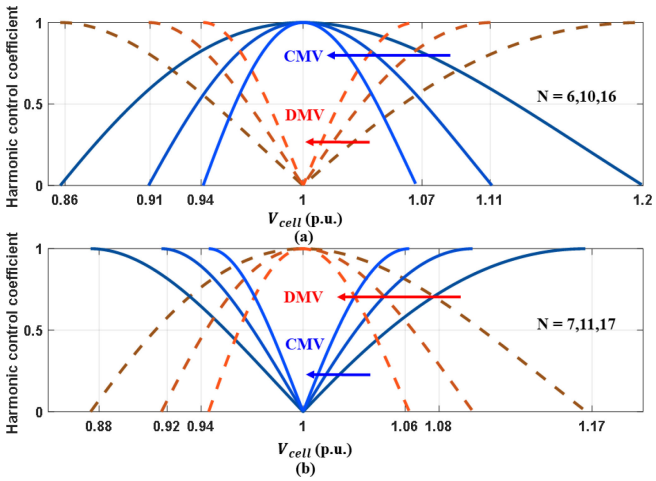


FIGURE 11. Harmonic control coefficient regulation with different V_{cell}: (a) even cell numbers, and (b) odd cell numbers.

C. VOLTAGE STRESS ANALYSIS FOR THE PROPOSED METHOD

The drawback of adjusting cell voltage is additional voltage stress applied on the cell capacitors and power semiconductors. Based on (16), the DMV and CMV harmonic control coefficient regulation with different cell voltage is shown in Fig. 11. The cell voltage is normalized to the nominal operation, where $D = 0.5, NV_{cell} = V_{dc}$. By changing the cell voltage, the harmonics are redistributed between DMV and CMV. When the cell number is even, the normal operation is in the minimum DMV mode. When the cell number is odd, the normal operation is in the minimum CMV mode. D reduces with larger V_{cell} and increases with smaller V_{cell}.

When the cell number changes, the V_{cell} for minimum DMV/CMV can be calculated by (19) and (20). The required V_{cell} is $1 - 1/(N + 1)$ p.u., 1 p.u., or $1 + 1/(N - 1)$ p.u.. Therefore, the maximum voltage stress for the proposed method is $1 + 1/(N + 1)$ p.u., as shown in Fig. 12. Larger the cell number, less the voltage stress.

TABLE 1. MMC Testbed Parameters

Items	Value
AC voltage	3.3 kV $l-l$
DC voltage	0-6 kV
DC Load	40 Ω
Cell numbers per arm N	6
Cell capacitance	2.1 mF
Coupled inductance (DC)	2.5 mH
Coupled inductance (AC)	0.75 mH
Cell capacitor voltage rating	1 kV
Switching frequency f_c	1 kHz

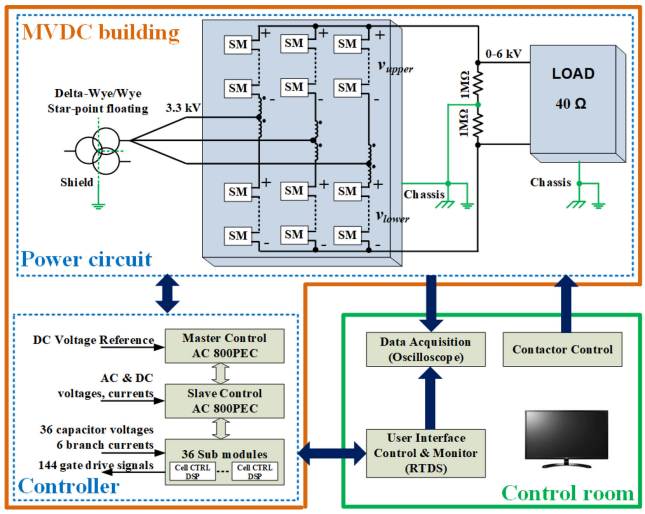
V. EXPERIMENTAL VERIFICATION

A. TESTBED INTRODUCTION

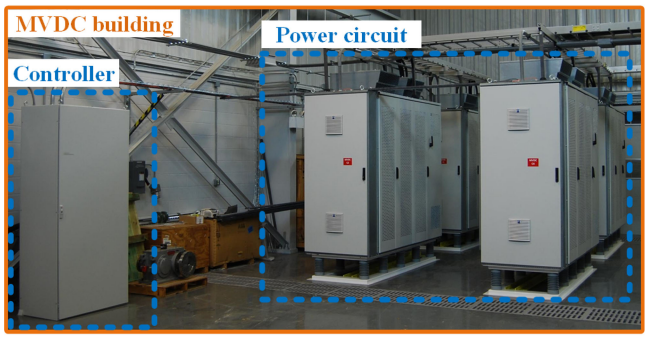
FSU-CAPS is equipped with a multi-functional MW-scale MVDC testbed comprised of four 1.25 MW full-bridge MMCs. The details of this test bed are described in [30] and [28]. The experimental setup is illustrated in Fig. 13 and the system electrical parameters are listed in Table 1.

The power circuit is controlled by the ABB AC800PEC controllers, the test operation is implemented through a Real Time Digital Simulator (RTDS). The AC source for the MMC converter is a dual winding transformer, Δ:Y-Y step down, rated for 2.8 MVA, 12.47 kV / 3.3 kV at 60 Hz. The MMC converter is a 6 kV dc amplifier operated in voltage source control mode, acting as a standalone ac to dc rectifier. The midpoint divider and midpoint connection to chassis provides electrical symmetry between the dc rails during steady state operation. Each of the individual phases of the ac and dc cable sections are shielded and connected to building ground.

Six arm voltages are measured for verification. The DMV/CMV are calculated based on (22). High-voltage differential probes (Probemaster 4241A) are used in the test, with a bandwidth from DC to 70 MHz. The voltage data are captured using a Tektronix MSO58 oscilloscope set to capture



(a)



(b)

FIGURE 13. MMC system configuration: (a) diagram, and (b) hardware.

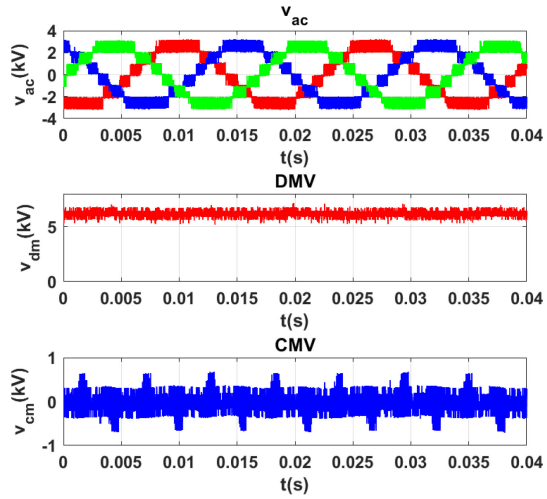


FIGURE 14. Experimental voltage waveforms with D = 0.5.

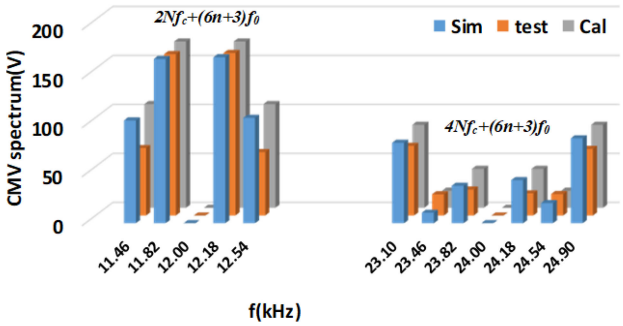


FIGURE 15. CMV harmonics comparison with D = 0.5.

at 6.25 MS/s with calculated 16-bit vertical resolution.

$$\begin{cases} v_{CM} = \dfrac{v_{upper_a} - v_{lower_b} + v_{upper_b} - v_{lower_b} + v_{upper_c} - v_{lower_c}}{6} \\ v_{DM} = \dfrac{v_{upper_a} + v_{lower_b} + v_{upper_b} + v_{lower_b} + v_{upper_c} + v_{lower_c}}{3} \end{cases} \tag{22}$$

B. VOLTAGE HARMONICS ANALYTICAL SOLUTIONS VALIDATION

Two cases are selected to compare the DMV/CMV analytical solutions with the ideal Matlab simulation and the experiment. One is minimum DMV mode validating the CMV spectrum, the other one is minimum CMV mode validating the DMV spectrum. The system parameters are listed in Table 1, $V_{cell} =$ 1 kV.

Case 1 is the normal operation mode, with $D = 0.5$, $V_{dc} =$ 6 kV, the output power is 0.9 MW. The experimental waveforms are shown in Fig. 14. As discussed in Section IV, case 1 is the minimum DMV and maximum CMV mode. CMV spectrum comparison of case 1 is shown in Fig. 15.

Case 2 is $V_{dc} = 5$ kV and $D = 0.42$, the output power is 0.625 MW. The experimental waveforms are shown in Fig. 16. As discussed in Section IV, case 2 is the minimum CMV and maximum DMV mode. DMV spectrum comparison of case 2 is shown in Fig. 17.

From Fig. 15 and Fig. 17, it can be observed that the calculation and simulation have exactly the same frequency distribution and the error in amplitude of each harmonic is negligible. The experiment results also have exactly the same frequency distribution, the CMV spectrum peak difference at 12 kHz is 2.9% and the DMV spectrum peak difference at 12 kHz is 13.2.% . In the experiment, the voltage spectrum magnitude is smaller than the calculation and the ideal simulation due to the dead time effect and the device conducting resistance.

C. VOLTAGE HARMONICS SUPPRESSION WITH DIFFERENT V_{cell}

In order to validate the proposed switching frequency voltage harmonics suppression method, the experiment is operated at 3 kV V_{dc} with regulated V_{cell}. The system parameters are listed in Table 1. As shown in Fig. 6, the calculated V_{cell} is 1 kV for the minimum CMV mode and 0.75 kV for the minimum DMV mode.

MMC is operated at minimum DMV mode in Fig. 18, the DMV harmonics are suppressed to 23 V when $V_{cell} = 0.75$ kV,

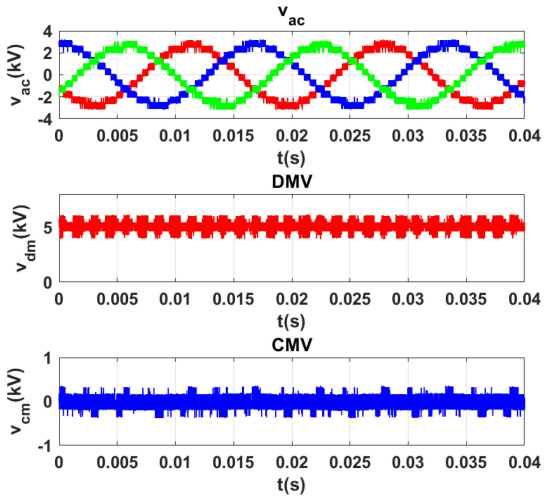


FIGURE 16. Experimental voltage waveforms with D = 0.42.

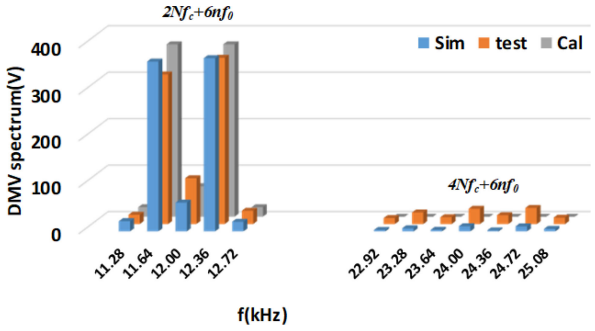


FIGURE 17. DMV harmonics comparison with D = 0.42.

meanwhile the DMV is at it's peak value. MMC is operated at minimum CMV mode in Fig. 19, the CMV harmonics are suppressed at 12 kHz, 36 kHz when $V_{cell} = 1$ kV, meanwhile the DMV is at it's peak value. With regulated V_{cell}, the 12 kHz harmonic peak can be reduced by 94% in DMV (from 359 V to 23 V) and 90% in CMV (from 109 V to 11 V).

D. VOLTAGE HARMONICS SUPPRESSION WITH 3rd HARMONICS INJECTION

When there is 3^{rd} harmonics injected, the required cell voltage can be reduced within particular dc voltage range, as shown in Fig. 8. Two cases are implemented with 15% 3^{rd} harmonic injection to validate the harmonics suppression method.

When the dc voltage is 2.5 kV, the required cell voltage to suppress the DMV harmonics is 1.25 kV if there is no 3^{rd} harmonics. Based on (19), with the 15% 3^{rd} harmonic injection, the value is reduced to 0.625 kV. As shown in Fig. 20, the DMV harmonics are suppressed to 21 V.

When the dc voltage is 3.5 kV, the required cell voltage to suppress the CMV harmonics is 1.167 kV if there is no 3^{rd} harmonics. Based on (20), with the 15% 3^{rd} harmonic injection, the value is reduced to 0.7 kV. As shown in Fig. 21, the CMV harmonics are well suppressed.

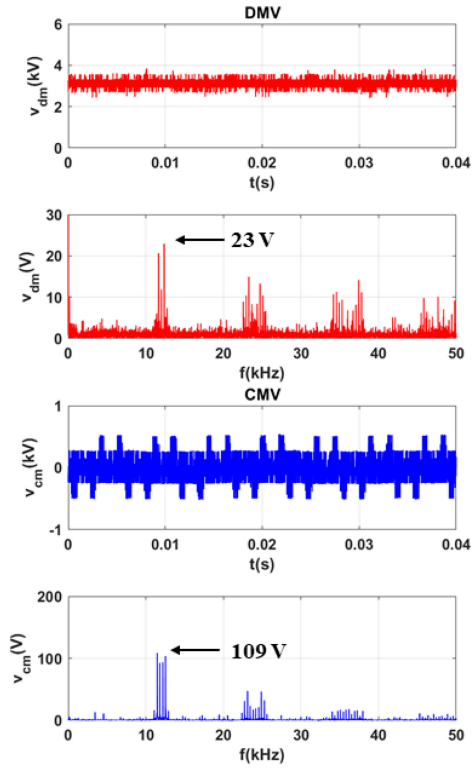


FIGURE 18. Voltage harmonics experimental results at minimum DMV mode ($V_{dc} = 3$ kV, $V_{cell} = 0.75$ kV).

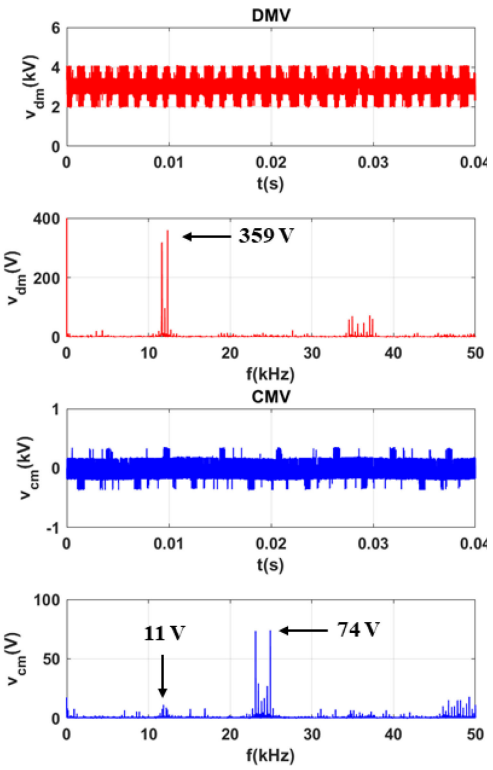


FIGURE 19. Voltage harmonics experimental results at minimum CMV mode ($V_{dc} = 3$ kV, $V_{cell} = 1$ kV).

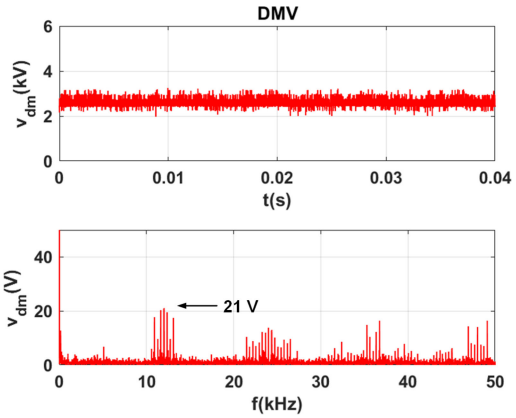


FIGURE 20. $V_{cell} = 0.625$ kV, $V_{dc} = 2.5$ kV, minimum DMV mode with 3^{rd} harmonics injection.

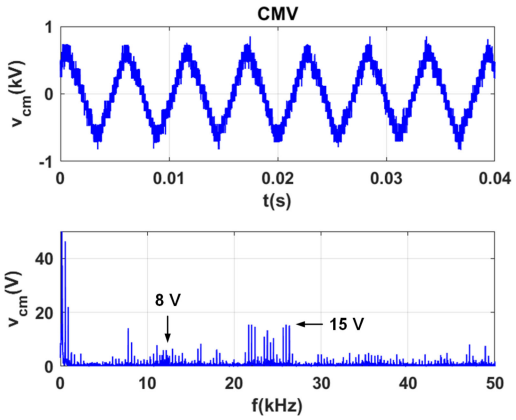


FIGURE 21. $V_{cell} = 0.7$ kV, $V_{dc} = 3.5$ kV, minimum CMV mode with 3^{rd} harmonics injection.

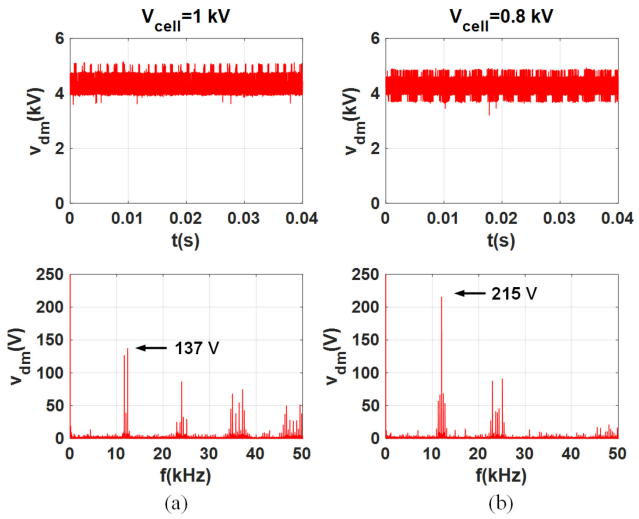


FIGURE 22. $V_{dc} = 4.2$ kV, V_{cell} selection for minimum DMV mode with limited V_{cell} range: (a) maximum V_{cell}, and (b) minimum V_{cell}.

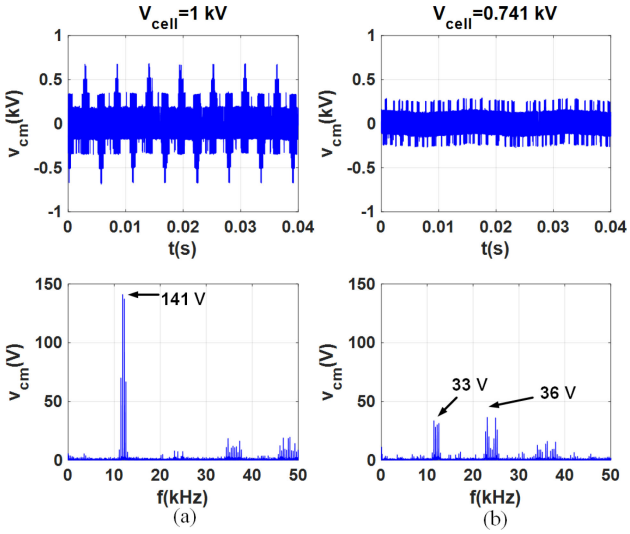


FIGURE 23. $V_{dc} = 3.5$ kV, V_{cell} selection for minimum CMV mode with 1 kV V_{cell} limitation: (a) maximum V_{cell}, and (b) minimum V_{cell}.

E. VOLTAGE HARMONICS SUPPRESSION WITH LIMITED CELL VOLTAGE RANGE

Although the voltage harmonics cannot be reduced ideally to zero with the cell voltage rating limitation, the cell voltage can still be optimized to suppress the harmonics. Two cases are tested to show how to choose the cell voltage to suppress the DMV/CMV harmonics with a 1 kV cell voltage max limitation, based on Fig 9.

When the dc voltage is 4.2 kV, the ideal cell voltage for DMV suppression is 1.05 kV. With limited cell voltage range, V_{cell_max} (1 kV) generates minimum DMV harmonics, as shown in Fig. 22. When the dc voltage is 3.5 kV, the ideal cell voltage for CMV suppression is 1.167 kV. With limited cell voltage range, V_{cell_min} (0.741 kV) generates minimum CMV harmonics, as shown in Fig. 23. The result is consistent with the calculation in Fig. 10.

VI. CONCLUSION

In this paper, analytical voltage spectrum solutions of the PSPWM controlled MMC are derived and verified. A switching frequency voltage harmonics suppression method through cell voltage control is proposed and validated. With proposed control, total DMV harmonics can be removed and partial CMV harmonics including the largest harmonic and its sidebands can be removed. The cell voltage optimization method under limited adjustable voltage range and analysis of different typical operation conditions were also presented. The analysis and proposed control methods are verified on a 1.25 MW commercial MMC testbed.

Although the experiments are performed on the MMCs with full bridge cells, the proposed analysis and control can also be applied to half-bridge MMCs. With the proposed method, the switching frequency harmonics components can

be redistributed between CMV and DMV, between ac side and dc side. Thus providing an additional degree of freedom for optimizing the power filter and EMI filter.

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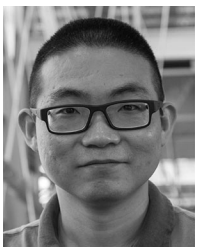

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