IEEE Open Journal of
Power Electronics

Received 24 February 2020; revised 31 March 2020; accepted 10 April 2020. Date of publication 16 April 2020;
date of current version 11 May 2020. The review of this article was arranged by Associate Editor Min Chen.

Digital Object Identifier 10.1109/OJPEL.2020.2987782

A 1.5 kW Radio-Frequency Tunable Matching Network Based on Phase-Switched Impedance Modulation

ANAS AL BASTAMI [1] (Student Member, IEEE), ALEXANDER JURKOV [2] (Student Member, IEEE), DAVID OTTEN [1], DUY T. NGUYEN [2] (Member, IEEE), AARON RADOMSKI [2] (Member, IEEE), AND DAVID J. PERREAULT [1] (Fellow, IEEE)

[1] Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA
[2] MKS Instruments, Inc., Rochester, NY 14623 USA

CORRESPONDING AUTHOR: ANAS AL BASTAMI (e-mail: abastami@mit.edu)

This work was financially supported by MKS Instruments, Inc.

ABSTRACT Dynamically-tunable impedance matching is a key feature in numerous radio-frequency (RF) applications at high frequencies (10 s of MHz) and power levels (100s–1000 s of Watts and above). This work develops techniques that enable the design of high power tunable matching networks (TMN) that can be tuned orders of magnitude faster than with conventional tunable impedance matching techniques, while realizing the high power levels required for many industrial applications. This is achieved by leveraging an emerging technique – known as phase-switched impedance modulation (PSIM), which involves switching passive elements at the rf operating frequency – that has previously been demonstrated at rf frequencies at up to a few hundred Watts. In this paper, we develop design approaches that enable it to be practically used at up to many kilowatts of power at frequencies in the 10 s of MHz. A detailed analysis of the factors affecting the losses as well as the tradeoffs of a basic PSIM-based element is provided. Furthermore, it is shown how incorporating additional stages to the PSIM-based element, including impedance scaling and / or the addition of series or shunt passive elements, influences the losses and enables the efficient processing of high power levels given the limitations of available switches. A PSIM-based TMN that matches load impedances to 50 Ω and delivers up to 1.5 kW of power at frequencies centered around 13.56 MHz is implemented and tested over a load impedance range suitable for various industrial plasma processes.

INDEX TERMS Impedance matching, impedance transformation, impedance modulation, plasma generation, phase-switched impedance, PSIM, tunable matching network, antenna tuning unit, capacitively-coupled plasma.

I. INTRODUCTION

A wide range of existing and emerging applications require the delivery of radio-frequency (rf) power into widely-varying loads at power levels up to several kilowatts and beyond. Examples include magnetic resonance imaging [1], [2], wireless communications [3], wireless power transfer [4]–[8], and plasma generation [9], [10]. The wide variation in load impedance in many of these applications makes it challenging to achieve efficient rf power generation while maintaining acceptable loading of the rf amplifier or inverter, and providing accurate control of power delivered to the load.

RF amplifiers and inverters are typically designed to operate efficiently into a fixed load impedance, and the performance of many high-frequency (HF, 3–30 MHz) and very high frequency (VHF, 30-300 MHz) switched-mode power amplifiers/inverters degrades quickly with variations in load impedance, e.g., [11]–[13]. This variation in load impedance is commonly addressed by utilizing a tunable matching network (TMN) between the load and the generator [5], [6], [10], [14]–[17]. The TMN matches the varying load impedance to a fixed input impedance (e.g., 50 Ω) suitable for driving by the amplifier. Conventional TMN designs have adjustable

passive components that are dynamically tuned, such as by using servo motors to mechanically adjust a set of variable capacitors or inductors, or by using reconfigurable capacitor and/or inductor banks, or by using high-power varactors [18], [19]. While such tuning methods can be effective, they often result in systems that are bulky, costly, limited in resolution, and have slow response to changes in load impedance. This slow response, for example, can be of concern to semiconductor manufacturing industries, which utilize modern rapid multi-step plasma processes to meet increasing demands for manufacturing very thin films and finer features. Such processes result in rapid load impedance steps taking place at intervals as short as 10 s of microseconds, posing challenges to conventional TMN designs.

Other approaches addressing load impedance variations without using a TMN have been proposed in the literature; however, they each have their own limitations. In [10], for example, an approach utilizing a resistance compression network is proposed to achieve narrow-range loading of the power amplifier. While this can be effective in many applications, it requires a specially-configured set of loads which might not be desirable nor practical in some applications. While other approaches of achieving resistance compression without requiring such a special set of loads have been proposed (e.g, [20]), it is not possible to achieve control of input impedance with arbitrary precision. In [7], [21], another approach is proposed where the inverters are configured to directly drive the varying load impedance; this, however, can result in substantial over-rating of the constituent inverters, which may not be desirable.

The concept of using a passive element switched at an ac operating frequency to realize an effective variable impedance has been known for some time (e.g., [22], [23]). Recently, it was shown in [9] that this technique can be successfully realized at high frequencies (10 s of MHz) and used to create high-bandwidth tunable matching networks. In particular, [9] demonstrated that a capacitor switched under ZVS conditions (using, for e.g., a GaN transistor in parallel with the capacitor) could be employed for efficient, high-bandwidth impedance matching at up to 10 s of MHz and 100 s of Watts.

This paper further develops this technique, termed phase-switched impedance modulation (PSIM), to enable the design of TMNs that can efficiently process high (multi-kilowatt) power levels at high frequencies (10 s of MHz) with extremely fast modulation bandwidth, such that it can address the needs of high-power applications such as industrial plasma processing. In Section II, we provide a detailed analysis and characterization of losses in a basic PSIM element, and demonstrate how impedance scaling as well as incorporating series and shunt passive elements affect these losses and can be used to improve the power processing capability of a PSIM TMN given limited transistor ratings. Section III discusses the design of a prototype 1.5 kW TMN based on the models and insights developed in the paper. Section IV presents experimental results and evaluates the performance of the proposed TMN. Finally, Section V concludes the paper.

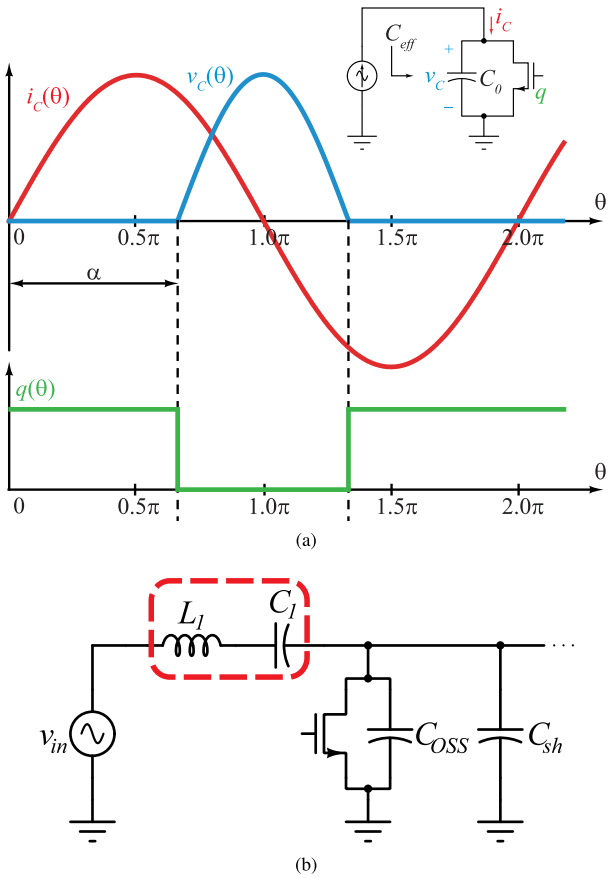

FIGURE 1. **(a): Structure and operation of a basic PSIM capacitor; (b): Conceptual schematic of a shunt PSIM switch with additional capacitance C_{sh} and an input filter for suppressing harmonic content at the input.**

II. LOSS CHARACTERISTICS OF A PSIM ELEMENT

A. THE BASIC PSIM CAPACITOR

Fig. 1(a) illustrates the basic concept of a PSIM element based on a capacitor in parallel with a switch forming a variable shunt capacitor. As described in [9], [22]–[25], by modulating the switch on and off at the input rf frequency with timing controlled for zero-voltage switching, one can realize an effectively variable capacitance (at the fundamental frequency) with the effective capacitance depending upon the duration of the switch on-time. This technique allows an effective capacitance to be modulated on an rf cycle-by-cycle basis. As illustrated in Fig. 1(b), this PSIM element would usually be realized as a transistor (possibly in parallel with an external capacitor) combined with a filter to remove the harmonic content generated by the PSIM element. By combining this PSIM variable capacitor with other elements (not shown), one can realize tunable matching networks with extremely rapid tuning times (orders of magnitude faster than conventional approaches) [9], [24], [25].

In order to utilize PSIM at power levels of several kilowatts and beyond, it is important to analyze how the losses in a PSIM switch scale as a function of the design elements. Consider a PSIM element comprising a transistor with output

capacitance C_{OSS} along with an additional parallel capacitance C_{sh} as shown in Fig. 1(b), such that the total capacitance is $C_0 = C_{OSS} + C_{sh}$. It was shown in [9], [24], [25] that at the fundamental frequency, assuming linear capacitance C_0, the ratio of the effective shunt capacitance C_{eff} synthesized by modulating switch on-time through angle α (see Fig. 1(a)) to capacitance C_0 can be expressed as follows:

$$\frac{C_{eff}}{C_0} = \frac{\pi}{\pi - \alpha + \sin\alpha\cos\alpha}. \tag{1}$$

The net current i_C flowing through the parallel combination of C_0 and the switch is ideally purely sinusoidal, as shown in Fig. 1(a). We can express the magnitude of the current in terms of C_{eff} and the fundamental component of v_C. The LC tank in Fig. 1(b) is ideally series-resonant at the fundamental frequency to remove any harmonic components, resulting in the fundamental component of v_C being equal to v_{in}. Therefore, we have:

$$|i_C| = \omega C_{eff}|v_{in}|\,, \tag{2}$$

where ω is the angular fundamental frequency. To compute the conduction loss in the PSIM switch, we calculate the rms current through the PSIM switch (neglecting loss in the switch output capacitance for simplicity). Note that when the switch is on, the current that flows through it is equal to the current i_C. When the PSIM switch is off, no current flows through it. Thus, the switch rms current $i_{sw,rms}$ can be expressed as follows:

$$\begin{aligned} i_{sw,rms} &= \sqrt{\frac{1}{2\pi}\int_{-\alpha}^{\alpha} |i_C|^2 \sin^2(\omega t)\, d(\omega t)} \\ &= \frac{|i_C|}{\sqrt{2}}\sqrt{\frac{\alpha - \sin\alpha\cos\alpha}{\pi}} \\ &= \frac{|i_C|}{\sqrt{2}}\sqrt{1 - \frac{C_0}{C_{eff}}}\,, \end{aligned} \tag{3}$$

where the last step is obtained by plugging in equation (1).

The conduction loss in the PSIM switch P_{cond} can now be computed as $i_{sw,rms}^2 R_{DS,ON}$, where $R_{DS,ON}$ is the dynamic on-state resistance of the switch [26]–[28]. Plugging in equations (2) and (3) and simplifying yields the following exact equation:

$$P_{cond} = R_{DS,ON}\omega^2 C_0^2 \left(\frac{C_{eff}}{C_0}\right)\left(\frac{C_{eff}}{C_0} - 1\right)\frac{|v_{in}|^2}{2}. \tag{4}$$

Recall that $C_0 = C_{OSS} + C_{sh}$ is the total shunt capacitance when the switch is off. By expressing C_{sh} as some multiple of C_{OSS}, i.e. $C_{sh} \equiv \gamma C_{OSS}$ with multiplier γ, we can re-write equation (4) as follows:

$$\begin{aligned} \frac{P_{cond}}{|v_{in}|^2/2} &= \omega R_{DS,ON} C_{OSS} \cdot (1+\gamma) \cdot \omega C_0 \\ &\quad \cdot \left(\frac{C_{eff}}{C_0}\right)\left(\frac{C_{eff}}{C_0} - 1\right). \end{aligned} \tag{5}$$

In a typical TMN application, a known input resistance R_{in} (such as 50 Ω) is often desired, which implies that the input power is $|v_{in}|^2/(2R_{in})$. Thus, one can think of equation (5) as being proportional to the fraction of input power that is lost in the TMN due to the PSIM conduction loss, which is directly connected to the achievable TMN efficiency. Furthermore, expressed this way, equation (5) explicitly shows the dependence of this fractional power loss on factors of parameters related to device properties ($R_{DS,ON}$ and C_{OSS}), external capacitance (γ), and TMN topology (C_0 and C_{eff}). Another useful way to arrange this information is to explicitly express conduction loss as a function of switch *peak* voltage in addition to the other parameters. It is shown in Appendix A that the conduction loss can be approximated as follows:

$$\begin{aligned} P_{cond} = 0.35 &\underbrace{\omega R_{DS,ON} C_{OSS} V_{sw,pk}^2}_{\substack{\text{Device}\\ \text{Performance}}} \cdot \underbrace{(1+\gamma)}_{\substack{\text{External}\\ \text{Capacitance}\\ \text{Factor}}} \cdot \overbrace{\omega C_0}^{\substack{\text{Minimum}\\ \text{Susceptance}}} \\ &\cdot \underbrace{\sqrt{\left(\frac{C_{eff}}{C_0}\right)}\left(\frac{C_{eff}}{C_0} - 1\right)}_{\substack{\text{PSIM}\\ \text{Modulation}\\ \text{Ratio}}}, \end{aligned} \tag{6}$$

where $V_{sw,pk}$ is the peak transistor off-state voltage. Equation (6) allows one to readily see the effects device selection and circuit choices have on loss and design of a PSIM-based TMN. For example, it can be seen in (6) that for a given device voltage rating, $R_{DS,ON}C_{OSS}$ becomes an important figure of merit for implementing PSIM, as it is in some switched-mode rf power amplifier applications [29].

Equations (5) and (6) reveal the direct connection of the maximum required value of C_{eff}/C_0 to both PSIM loss metrics. Since this ratio, termed capacitance modulation ratio, is a function of the TMN circuit design and topology, the equations can be used to quickly evaluate the performance of different candidate topologies and compare them for suitability in a given PSIM-based TMN application. For instance, an important feature revealed by the equations is that the dependence of loss on C_{eff}/C_0 is superlinear, and thus it is generally desirable to select TMN topologies that achieve the required impedance match with the lowest shunt PSIM capacitance modulation possible. Another implication of equations (5) and (6) is that it is ideally advantageous to realize - to the extent possible - the shunt capacitance C_0 entirely using the PSIM switch's output capacitance C_{OSS} without resorting to any additional external capacitance C_{sh}. This corresponds to γ in the equations being as close to zero as possible, thereby reducing losses.

However, because the output capacitance C_{OSS} of available power switches, including GaN and SiC devices, is generally nonlinear and highly dependent on the switch drain voltage, this results in a dependence of the required capacitance modulation on the operating power level even for a fixed load

impedance (as will be demonstrated experimentally in section IV). Since C_{OSS} typically decreases with higher drain voltages, the PSIM switch modulation angle needs to be increased at higher power levels in order to maintain a given required effective shunt capacitance. The effects of such nonlinearities are reduced with the use of discrete parallel capacitance. Likewise, these equations do not address the fact that device capacitance may be more lossy in practice than high-quality-factor discrete capacitors, or that exclusively using device capacitance may be difficult as regards cost and packaging. For these reasons it is often desirable to implement some portion of the capacitance as discrete capacitance. The choice of C_{sh} is thus a tradeoff between minimizing switch conduction losses while maintaining acceptable C_{OSS} loss, C_{OSS} nonlinearity, and size / cost of switches.

Note that while Fig. 1 explicitly shows only a single PSIM switch, the loss equations apply even when several PSIM switches are utilized in parallel as a single switch. In the latter case, P_{cond} represents the *total* conduction loss in all switches, and γ represents the ratio of external shunt capacitance C_{sh} to the *total* output capacitance of all the PSIM switches NC_{OSS}, where N is the number of switches (i.e., $\gamma \equiv C_{sh}/(NC_{OSS})$). In addition to conduction loss, another form of PSIM switch loss that needs to be considered in the design process is the loss due to the charging / discharging of the transistors' output capacitance C_{OSS} (which is often not well represented as ohmic conduction loss). This loss mechanism is addressed in detail in [30]–[34].

B. IMPEDANCE SCALING FOR PSIM CAPACITORS

In many applications, given the limitations of device voltage ratings of available switches, the operating power level requirements may prohibit the direct use of the circuit in Fig. 1(b) at the desired input impedance level. To illustrate this, suppose the circuit in Fig. 1(b) is part of a TMN that maintains a 50 Ω input impedance. At just 1 kW of input power, the input voltage magnitude, which is equal to the magnitude of the fundamental component of the PSIM switch voltage in Fig. 1(b), is about 316 V. This corresponds to PSIM switch *peak* voltages exceeding 630 V, which approaches or exceeds the voltage rating of many available GaN devices. Thus, it is crucial to address topological considerations in designing PSIM-based TMNs and their intersection with the device considerations.

Fig. 2 introduces an impedance scaling stage that scales down the voltages in the circuit of Fig. 1(b) by a factor of k. The currents in turn scale up by a factor of k, resulting in the PSIM switch operating at impedance levels that are a factor of k^2 lower. Therefore, the following relations hold for the parameters in the transformed circuit relative to the original values:

$$|v'_{in}| = |v_{in}|/k, \tag{7}$$

$$C'_0 = k^2 C_0, \tag{8}$$

$$\left(C_{eff}/C_0\right)' = C_{eff}/C_0, \tag{9}$$

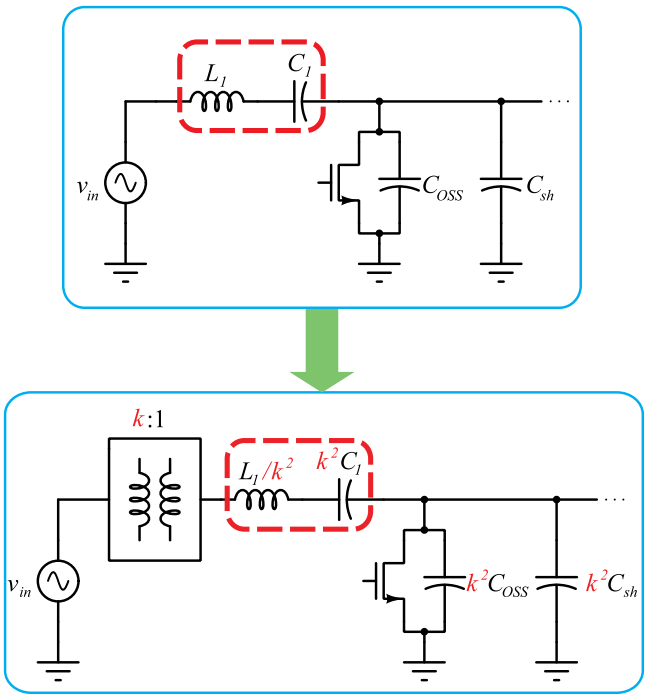

FIGURE 2. Circuit resulting after scaling voltages / currents by a factor of k.

where the primed variables denote the transformed quantities when referred to the original untransformed circuit. This allows us to plug these primed quantities directly into equations (5) or (6) to obtain the PSIM conduction loss in the transformed circuit. Note that the capacitance modulation ratio C_{eff}/C_0 is unaffected by the scaling since it is only a function of the TMN topology and the range over which the load impedance varies.

It can be seen that the expression for the PSIM conduction loss is *unaffected* by the addition of the scaling stage in Fig. 2; this can be advantageous in a number of ways. First, it can be used to lower the voltages on the PSIM switch(es), which can be useful in high power applications with high input voltage levels. Second, the scaling stage allows increasing C_0 (and allowed C_{OSS}) by a factor of k^2 without sacrificing PSIM conduction loss. This in turn can be achieved by paralleling more PSIM devices, resulting in a reduction of *per switch* PSIM conduction loss by a factor of k^2. Furthermore, in many impedance matching applications (for e.g., in many plasma systems) where the full load impedance range needs to be stepped up by some amount to provide a desired input impedance, a fixed scaling up network can be part of the overall matching system, and can very efficiently provide at least part of the load impedance transformation. Essentially, the addition of a scaling stage provides the ability to optimize a design to best take advantage of the voltage capabilities of a given class of semiconductor devices, independent of the voltages required for a given power and impedance level.

In general, the selection of the scaling factor is a tradeoff between achieving acceptable PSIM peak voltages, and

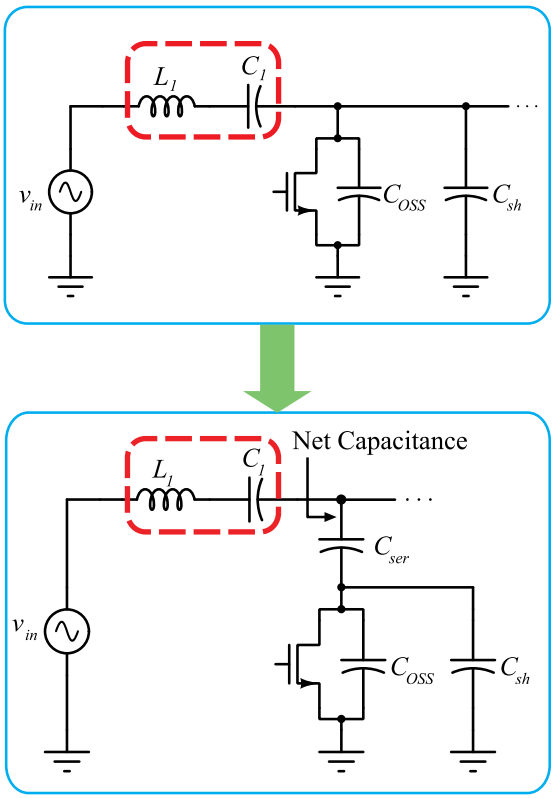

FIGURE 3. Circuit showing the addition of series capacitance C_{ser}.

implementing the PSIM switches with a reasonable number of paralleled devices, while maintaining acceptable cost and complexity of the scaling stage. In addition to impedance scaling, more degrees of freedom may sometimes be needed to achieve an acceptable tradeoff, as discussed in the next section.

C. PSIM WITH ADDITIONAL SERIES CAPACITANCE

In a TMN application, the minimum and maximum required shunt capacitance (and thus the capacitance modulation ratio as well) is directly related to the TMN architecture, the range of load impedance to be matched, as well as the desired impedance to match to. In the implementation in Fig. 1(b), the minimum capacitance seen at the input is C_0, realized entirely by the switch output capacitance C_{OSS} as well as any external C_{sh}. The maximum capacitance C_{eff} is achieved by modulating the PSIM switch as described earlier.

Another approach for realizing the required minimum and maximum shunt capacitance is to combine a PSIM capacitor with another fixed capacitance C_{ser} in series, as shown in Fig. 3. This has the advantage of providing voltage division to the switch drain node, and can thus be used as another design handle along with scaling. In addition, C_{ser} somewhat decouples the switch drain node from the rest of the circuit elements, which can improve the harmonic content of the voltage waveform.

To evaluate the effect of adding series capacitance on the PSIM conduction loss, we follow a procedure similar to that in section A. As before, we start by computing the current entering the PSIM switch node:

$$|i_C| = \omega C_{net} |v_{in}|\,, \tag{10}$$

where $C_{net} \equiv C_{eff} || C_{ser}$ is the net capacitance realized by the combination of the PSIM capacitor and C_{ser}. Equation (3) still holds, and thus we have the following expression for conduction loss:

$$P_{cond} = R_{DS,ON}\omega^2 C_{net}^2 \left(1 - \frac{C_0}{C_{eff}}\right) \frac{|v_{in}|^2}{2}. \tag{11}$$

To obtain better insight from the PSIM loss equation, we define C_{min}, the minimum net shunt capacitance as $C_{min} = C_0 || C_{ser}$. Using the definitions of C_{min} and C_{net}, it can be shown (by eliminating C_{ser}) that the following holds:

$$\frac{C_{min}}{C_{eff}} = \frac{C_{min}}{C_0} + \frac{C_{min}}{C_{net}} - 1. \tag{12}$$

Now, equation (11) can be re-written as follows:

$$P_{cond} = R_{DS,ON}\omega^2 C_{net}^2 \left(\frac{C_0}{C_{min}}\right)\left(\frac{C_{min}}{C_0} - \frac{C_{min}}{C_{eff}}\right) \frac{|v_{in}|^2}{2}. \tag{13}$$

Finally, plugging in relation (12) into (13), recalling the definitions of C_0 and γ, and re-arranging terms yields this expression for PSIM conduction loss:

$$\frac{P_{cond}}{|v_{in}|^2/2} = \omega R_{DS,ON} C_{OSS} \cdot (1+\gamma) \cdot \omega C_{min} \cdot \left(\frac{C_{net}}{C_{min}}\right)\left(\frac{C_{net}}{C_{min}} - 1\right). \tag{14}$$

This equation is analogous to equation (5), with C_0 replaced by C_{min}, and C_{eff} replaced by C_{net}. This means that for a given minimum and maximum net shunt capacitance, the PSIM conduction loss is *unaffected* if that shunt capacitance is realized as a combination of PSIM and a fixed series capacitor. It is important to note, however, that achieving a given net capacitance with the addition of C_{ser} necessitates higher PSIM capacitance modulation ratios and thus higher PSIM switch modulation angles compared to the case when no series capacitance is added. This is because a larger variation in the PSIM capacitor is needed to realize a given required range of net overall capacitance. Therefore, there is an inherent tradeoff between the achievable reduction in switch peak voltage due to capacitive division, and the switch conduction angle.

A major result of the topological modifications presented in this section as well as the prior section shows that the switch peak voltage, modulation ratio, and loss can be traded off by utilizing such topological variants in appropriate ways. This enables the development of TMN designs capable of processing high power levels given the limitations of available active devices. Combined with recent advances in wide bandgap power semiconductor devices (e.g., GaN and SiC devices), this opens up the use of PSIM in numerous applications at high powers and high frequencies.

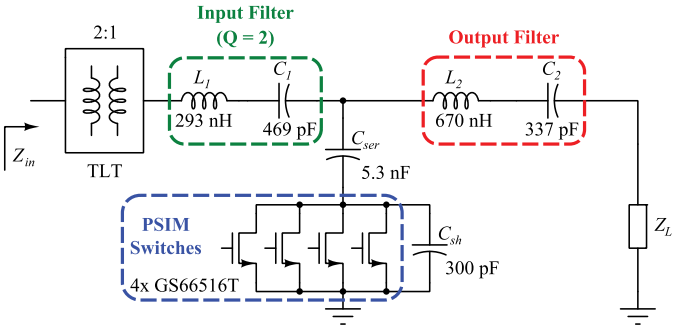

FIGURE 4. Structure of the high power PSIM-based TMN and its various constituent stages with the desired component values.

III. PROTOTYPE PSIM-BASED TMN DESIGN AND IMPLEMENTATION

The above analyses are demonstrated in the development of a 13.56 MHz, 1.5 kW PSIM-based TMN that is suitable for industrial plasma applications. It provides matching from load impedances varying in resistance between 0.5 Ω to 2 Ω, and in reactance between -j10 Ω to -j25 Ω, to 50 Ω; this matching range was selected for an industrial plasma processing application that utilizes a capacitively-coupled plasma. The resulting design, shown in Fig. 4, is based on a step-up L-matching network, having its shunt variable element realized by a PSIM capacitor stage, and its series variable element realized by an LC resonant tank which provides dynamic frequency tuning (DFT) with a ±10% tuning range about 13.56 MHz [9], [10].

In an L-match, the range of required shunt capacitance is directly related to the range of load resistances to be matched. Loads with the highest resistive component (i.e., 2 Ω) require the least shunt capacitance while loads with the lowest resistance (i.e., 0.5 Ω) require the highest shunt capacitance to successfully achieve matching. Thus, given a desired 50 Ω input impedance match, the resistive load range uniquely determines the minimum shunt capacitance as well as the required capacitance modulation. For this load range, the required overall L-match shunt capacitance range is 2 nF to 4.4 nF.

Likewise, the range of required reactance variation in the L-match series element depends on the range of load reactance variation. Since in this application the load reactance range is entirely capacitive, the L-match series element will always be inductive. Loads with the most negative reactance (i.e., -25 Ω) require the highest series inductance, and vice versa. For the load range in this application, the range of required series reactance is 12.6 Ω to 31.2 Ω.

The TMN makes use of each of the design techniques discussed in section II-B and II-C, respectively. In particular, it utilizes a transmission-line transformer (TLT) [35]–[37] to implement a scaling stage at the input. It also utilizes a fixed capacitance in series with the PSIM capacitor to improve the operating range of the PSIM switch and provide increased linearity. Fig. 4 shows an overview of the system; we describe it in terms of four stages. The first is the transmission-line transformer at the input which provides impedance scaling. The second stage is the input filter stage which prevents harmonics arising from the PSIM switching action from reaching the input port of the match. Next is the output filter stage, which both provides filtering to the load and realizes the second variable element of the L-match through DFT. The final stage is the PSIM power module, which consists of the PSIM capacitor, additional external shunt capacitor, the additional series capacitor, as well as auxiliary cooling and gate driving systems. These four stages are each treated in detail in the subsequent subsections.

A. TRANSMISSION-LINE TRANSFORMER (TLT)

The first stage of the TMN shown in Fig. 4 is a scaling stage that enables the operating voltage of the PSIM circuitry to be decoupled from that required at the TMN input. At an output power level of 1.5 kW the input power can exceed 2 kW, which corresponds to input voltage magnitudes close to 500 V at 50 Ω input impedance. With a direct PSIM realization (as shown in Fig. 1(b)), this would result in *peak* PSIM switch voltages exceeding 1.2 kV, beyond the ratings of many high-frequency power switches. The scaling stage is a partial means through which the required switch voltage may be reduced. In the demonstration system, the transmission-line transformer scaling stage provides 2:1 scaling in voltage, or equivalently, a 4:1 scaling in impedance. The PSIM circuitry can thus operate at a factor of two lower voltage than required at the input (and at a factor of two higher current), simplifying its design with available high-frequency switches. While a voltage scaling factor of 2 is not alone sufficient to bring the peak voltages down to acceptable levels, it provides an acceptable tradeoff in resulting circuit component values, transformer size, and complexity; we describe an addtional technique used for reducing the PSIM switch voltage in the subsection on the PSIM switch module.

The scaling stage is implemented as a transmission line transformer (TLT) [35]–[39]. As compared to other techniques (tuned transformers, matching networks, etc.), transmission-line transformers have the benefits of providing load-independent and frequency-independent (broadband) voltage transformation, and can achieve quite high efficiencies. Limitations of transmission-line transformers are that they do not typically provide electrical isolation, and there are significant limitations in available transformation ratios at low complexity. As the design of transmission-line transformers is not widely understood, we treat this stage in detail.

As shown in Fig. 5(a), the 2:1 (in voltage) Guanella-type transformer utilized here consists of two transmission lines, each having characteristic impedance Z_0. Each transmission-line pair is passed through the windows of a set of toroidal ferrite cores in order to suppress any common-mode currents such that the two conductors of each transmission line can be approximated as carrying equal and opposite currents. The transmission line sections are selected as being short enough (less than an eighth of a wavelength at the frequency range of operation) such that we can approximate the differential voltages at the two ends of each transmission line as being equal.

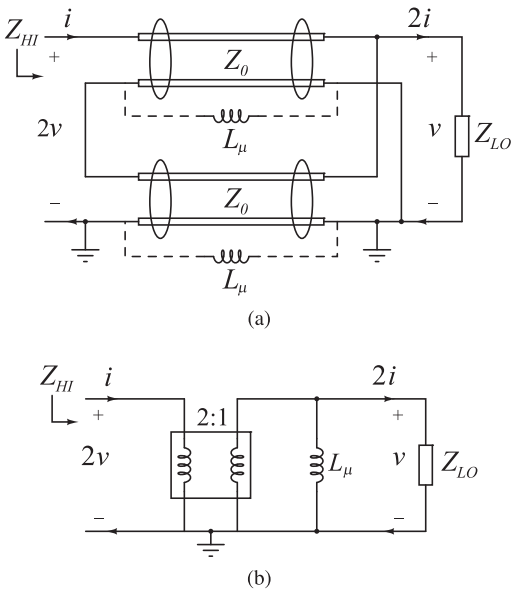

FIGURE 5. Structure and equivalent circuit model of a 2:1 Guanella-type TLT. (a): TLT basic structure showing the interconnections of the transmission lines with common-mode inductance L_μ; (b): Equivalent circuit model using an ideal transformer. To maximize bandwidth, Z_0 is chosen as $\sqrt{Z_{HI}Z_{LO}}$.

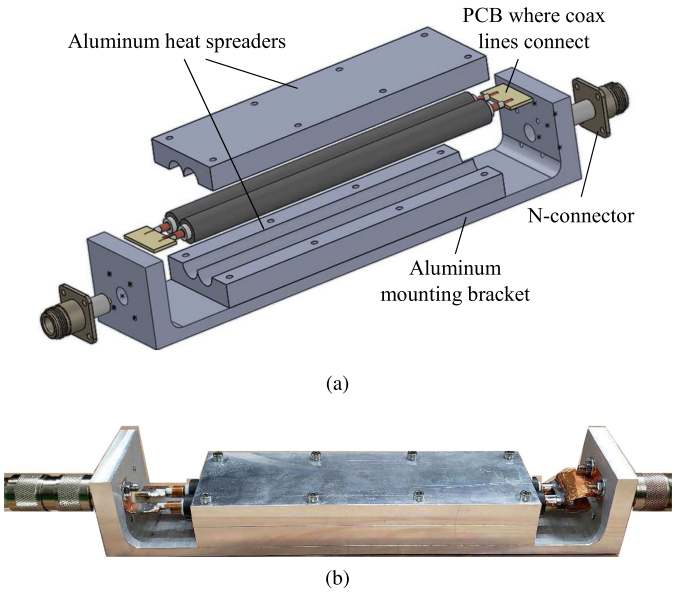

FIGURE 6. (a): 3D model of the TLT in exploded view; (b): Photo of the implemented TLT.

The terminals of these lines are connected in series on the high-impedance side, and in parallel on the low-impedance side.

The distributed inductance and capacitance of the transmission lines enables the TLT to transform waveforms over a wide bandwidth, with upper and lower frequency bounds determined by the design of the TLT and the impedance levels (voltage to current ratios) of the waveforms being processed. The lower frequency boundary of the TLT is determined by the finite impedance to common-mode currents on the transmission lines. This is represented in Fig. 5(a) as an inductance L_μ in parallel with each transmission line, where the value of L_μ is determined by the single turn of the transmission line conductors on the ferrite cores [35]–[39]. At the desired operating frequencies, L_μ should be large enough such that the common-mode currents imposed on the transmission-line pairs are much smaller than the load current. Fig. 5(b) shows an equivalent circuit model for the TLT circuit in Fig. 5(a), where the inductance appears in parallel with the low-side impedance Z_{LO}. This gives the following transfer function between Z_{HI} and Z_{LO}:

$$\frac{Z_{HI}}{Z_{LO}} = \frac{4sL_\mu}{sL_\mu + Z_{LO}}. \tag{15}$$

Therefore, at the operating frequency range, the common-mode impedance $|\omega L_\mu|$ needs to be much larger than the load impedance $|Z_{LO}|$ to avoid any magnitude or phase errors introduced by the pole in equation (15). Equivalently, the low frequency cut-off f_L given below should be much lower than the lowest operating frequency f_{min}:

$$f_L = \frac{Z_{LO}}{2\pi L_\mu} \ll f_{min} \tag{16}$$

The design of the TMN targets a frequency range that is $\pm 10\%$ about 13.56 MHz, so f_{min} is about 12.2 MHz. f_L can thus be reasonably chosen to be around 1 MHz, which results in a minimum required $L\mu$ of about $2\,\mu$H. The characteristic impedance is chosen to be the geometric mean of the high-side and low-side impedances: $Z_0 = \sqrt{Z_{HI}Z_{LO}}$, which ensures proper termination of the lines and maximizes the TLT bandwidth [35]–[37]. This design targets a 50 Ω desired input impedance, resulting in $Z_{HI} = 50\,\Omega$, $Z_{LO} = 12.5\,\Omega$, and $Z_0 = 25\,\Omega$.

The 2:1 Guanella TLT was implemented in a binocular structure as shown in Fig. 6(a) and 6(b). Each transmission line was implemented as a 25 Ω RG141 coax cable enclosed in a series-stack of 14 toroid cores (Fair Rite 61 material, part #: 5961001901). This implementation results in a calculated L_μ of about $2.1\,\mu$H. The cores were selected to provide the required common-mode inductance while keeping core losses to a minimum. This loss arises due the common-mode voltage across L_μ of the top transmission line of Fig. 5(a) driving flux inside the cores. By inspecting Fig. 5(a), it can be seen that the common-mode voltage is half of the input voltage. At a worst-case input power of about 2.5 kW (with a 50 Ω match), this voltage peaks at about 250 V, which results in about 6.5 W of core loss. (By contrast, the grounding scheme used in the proposed design imposes zero common-mode voltage on the bottom transmission line, and no core losses in the associated cores; we employ the second set of cores only to allow the use of other grounding schemes if so desired).

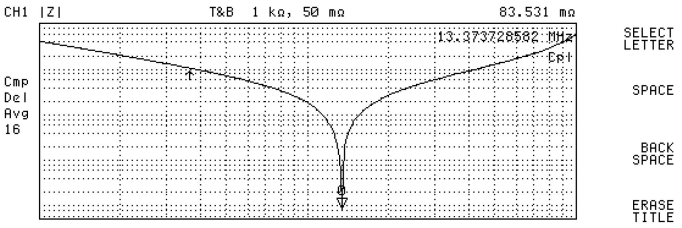

FIGURE 7. Measured magnitude of the impedance of the input filter at its resonant frequency. The impedance minimum is at around 13.37 MHz.

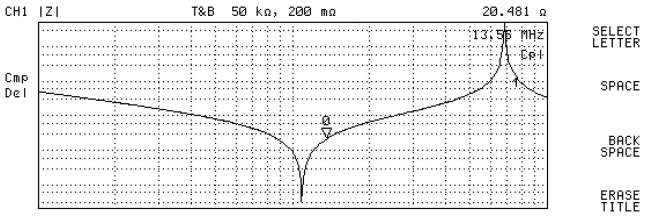

FIGURE 8. Measured magnitude of the impedance of the output filter at 13.56 MHz. It can be seen that the desired reactance range can be achieved by varying the frequency about 13.56 MHz. The impedance minimum is at 10.9 MHz, and the maximum peak is at around 69 MHz.

To manage the thermal dissipation at this worst-case power, a cooling structure was built as shown in Fig. 6(a) and 6(b). The Aluminum heat spreaders were machined to fit directly on the TLT structure to effectively absorb the heat generated from core loss. The two small PCBs shown were used to make the series and parallel connections of the transmission lines. The outer Aluminum bracket serves both as a mounting structure, as well as a ground connection for the TLT's input and output terminals.

The implemented TLT was tested prior to its use in the full TMN system. With 50 Ω connected to its primary side, the secondary impedance was measured as 12.5 Ω with no more than 3° of phase shift across the operating frequencies. Furthermore, its efficiency was measured as approaching 99% at an input power level of more than 1 kW.

B. INPUT FILTER

The input filter, formed by L_1 and C_1 in Fig. 4, serves both to prevent the harmonic content generated by the PSIM switch from propagating to the input, and to help ensure that the currents driving the PSIM network are approximately sinusoidal. It is designed to be series resonant at 13.56 MHz, and its characteristic impedance was chosen to provide a loaded quality factor of 2 with respect to a resistive load of 12.5 Ω. This provides an acceptable tradeoff between adequate filtering under matched conditions, while limiting the effect of varying the TMN operating frequency by 10%.

The inductor L_1 was implemented using 3 turns of 0.25″ silver-plated copper tubing, with an inner diameter of 38 mm, and a winding pitch of 13.35 mm. The measured inductance value was about 373 nH, with a quality factor Q of about 580 at 13.56 MHz. C_1 was tuned to resonate with the inductor at 13.56 MHz, resulting in a value of about 372 pF. This was implemented using 3x 2.5 kV 100 pF P90 ceramic capacitors (ATC100 C, ATC Corp.) in addition to 3x 2.5 kV 24 pF P90 ceramic capacitors (HQCC, AVX Corp.). Fig. 7 shows the measured magnitude of the impedance of the L_1C_1 tank at its resonant frequency.

C. OUTPUT FILTER

The output filter, comprised of L_2 and C_2, serves both as the second variable element of the L-match, as well as a filter to ensure sinsusoidal output current. The LC tank realizes a variable reactance by utilizing dynamic frequency tuning (DFT) [9], [10], whereby small variations in the system operating frequency are used to dynamically modify the effective reactance of the tank. The LC tank is selected such that over a frequency range between 12.2 MHz and 14.9 MHz (i.e., ±10% about 13.56 MHz), the net reactance varies from 12.6 Ω to 31.2 Ω (this is the reactance range that is required by the L-match for the given load range to achieve 12.5 Ω at the secondary of the TLT).

The inductor L_2 was implemented using 4 turns of 0.375″ silver-plated copper tubing, with an inner diameter of 58 mm, and a winding pitch of 19.53 mm. The measured inductance value was around 709 nH, with a quality factor Q of about 600 at 10.9 MHz. The output inductor Q is a dominant factor in the power loss and thus the efficiency of the TMN system, owing to the high current levels flowing through the low-resistance output loads (for e.g., delivering 1.5 kW into 0.5 Ω corresponds to 77.5 A of peak current). It is therefore desired to implement an inductor having the highest possible quality factor. Furthermore, at such power levels, the inductor voltage approaches 5 kV, and thus care must be taken in the layout to provide adequate clearances. At the highest predicted current, the estimated loss in the inductor amounts to about 270 W. C_2 was implemented using 10x 7.2 kV 15 pF P90 ceramic capacitors (HQCE, AVX Corp.), as well as 10x 7.2 kV 18 pF NP0 ceramic capacitors (HQCE, AVX Corp.). The peak voltage on C_2 approaches 3.5 kV, and thus a voltage rating of 7.2 kV was chosen to provide adequate safety margin. Dividing the capacitance this way also ensures adequate current sharing, resulting in no more than 4.2 A of worst-case peak current in each capacitor. The total implemented capacitance has a value of 330 pF. Fig. 8 shows the measured magnitude of the impedance of the L_2C_2 tank at 13.56 MHz.

D. PSIM POWER MODULE

The PSIM power module serves to realize the shunt variable reactance required by the L-match to achieve a resistance of 12.5 Ω at the TLT secondary (or equivalently, 50 Ω at the TMN input). It consists of PSIM switches and their associated auxiliary circuitry (gate drivers, dc supply, and bypass capacitors), series fixed capacitance C_{ser}, shunt external capacitance C_{sh}, and a thermal management system.

As described earlier and illustrated in Fig. 4, the PSIM capacitor (denoted here as C_{psim}), along with the fixed series

capacitance C_{ser}, realize the shunt capacitance required by the L-match. To fully specify the values of these two quantities, two constraints must be satisfied. First, the series combination of the two capacitors must realize a range of 2 nF to 4.4 nF, imposed by the load range of the L-match. Second, the capacitors must provide sufficient voltage division to the PSIM drain node to maintain acceptable peak voltages well within the operating limits of the selected power devices, while simultaneously keeping an acceptable range of PSIM capacitance modulation. Note that the worst-case PSIM drain voltage occurs at the highest operating power level and when the shunt capacitance is at its minimum, corresponding to loads having the highest resistance (i.e., 2 Ω).

The switch was selected to have a low $R_{DS,ON}C_{OSS}$ product to minimize the conduction losses, as implied by equations (5) and (6). In addition, it was selected to substantially realize most of the required shunt capacitance (at least 2 nF) such that minimal external shunt capacitance is required, while maintaining a practical number of devices, thereby ensuring compact layout and adequate synchronization between all devices. It is also desired to select a switch having low junction-to-case thermal resistance to facilitate cooling. The top-cooled GaN Systems 650 V rated GS66516 T switch was selected to realize the PSIM capacitor, owing to its low $R_{DS,ON}C_{OSS}$, its favorable junction-to-case thermal resistance of 0.3 °C/W, and its ability to realize the required capacitance with a few devices, as will be seen shortly. For this device, an operating peak voltage limit of about 400 V provides adequate safety margin.

At a worst-case input power of about 2.5 kW into 50 Ω, the peak voltage of the fundamental component of the L-match shunt capacitor is 250 V. Relating this peak of the fundamental voltage to the actual peak of the switch drain is possible if C_{OSS} were constant with respect to voltage (see Appendix A); however, it is difficult to obtain a similar result analytically for a voltage-dependent C_{OSS}. From the equations in Appendix A, it can be inferred that the ratio of the peak voltage to the peak of the fundamental varies roughly between 2 and 3 over typical range of conduction angles. The upper part of this range is practically limited to about 130°, corresponding to a capacitance modulation factor of about 8; note that higher PSIM conduction angles result in significantly higher harmonic distortion levels, which are undesirable. Furthermore, very short switch off-times are hard to realize in practice at these frequencies given the gate rise and fall times of available devices. Therefore, an approximate voltage ratio of 2.5 can be used to approximate the switch peak voltage to a first order. Using this factor, it can be seen that if we desire to keep the peak switch voltage below 400 V, the series capacitor C_{ser} must divide down the voltage applied to the PSIM module by a factor of about 1.56; this sets one of the two constraints.

The second constraint is satisfied by ensuring that the series combination of C_{psim} and C_{ser} adequately realizes the range of required L-match shunt capacitance. With a minimum operating power of about 200 W, the aforementioned constraints were satisfied when C_{ser} was about 5.3 nF, and when four GS66516 T switches were used in conjunction with a small external fixed shunt capacitance C_{sh} of 300 pF, as shown in Fig. 4. This resulted in a predicted capacitance modulation factor just below 8. The worst-case total PSIM conduction and C_{OSS} charging / discharging losses were estimated via extensive simulations of the TMN across the full load range to be about 130 W, or about 32 W per switch.

The GaN switches and C_{sh}, implemented using 8x 1.5 kV 39 pF NP0 ceramic capacitors (VJ1111, Vishay), were soldered on a $2'' \times 2''$ PCB shown in Fig. 9(a). In practice, the value of C_{ser} can be experimentally adjusted to cancel any parasitic series inductance in the PSIM branch at the operating frequency, and to address inaccuracies in the device simulation models. One way of achieving this is to gradually increase the operating power level with the load having the highest resistance (which demands highest voltage levels), and monitor the switch peak voltage. Parasitic inductance or device model inaccuracies may result in higher than predicted switch peak voltages; in such cases, the value of C_{ser} can be lowered to reduce the switch peak voltage as needed. In this system, it was adjusted to 3 nF, which was implemented using 20x 1 kV 150 pF C0G ceramic capacitors (VJ1111, Vishay) soldered on two separate $1.05'' \times 0.85''$ two-layer PCBs as shown in Fig. 9(b). This mounting arrangement ensured equal current sharing between the capacitors to avoid overheating.

Fig. 9(c) shows the bottom of the PCB with the PSIM switches. The precisely symmetric layout of the switches in Fig. 9(c) and their associated gate driving circuitry in Fig. 9(a) ensures substantially equal current sharing among all switches as well as synchronized gate drive waveforms. To effectively absorb the heat from these switches, a custom-built $0.1''$ thick silver-plated copper heat spreader, shown in Fig. 9(d), was mechanically attached and soldered to the bottom of the PCB as shown in the photos. For high design margin it was desired to keep the junction temperature of the switches at about 85 °C, which is achievable if the heat spreader surface is maintained at about 60 °C. At 130 W of switch losses and an ambient temperature of about 30 °C, this requires a cooling system that can achieve an effective thermal resistance of 0.2 °C/W from the surface of the spreader to ambient. This was accomplished by the forced-air cooling system shown in Fig. 9(e), which consists of a silver-plated Dynatron A25 copper heatsink, with a 24 V San Ace B97 fan blower (part #: 9BMB24P2G01) that provides air flow at up to 47.3 cubic feet per minute (CFM); this cooling scheme achieves the required thermal resistance. Fig. 10 shows a photo of the developed TMN. It can be seen from the photos that in this configuration, the switches need to have a low-resistance path through which current flows to the system ground, namely, the chassis. This is accomplished via the two silver-plated copper L-brackets shown in Figs. 9(e) and 10, which establish the ground connection to the chassis. The overall TMN box dimensions were about $14'' \times 14'' \times 5,''$ providing a shield to contain emissions from coreless magnetics, with an Aluminum lid covering the enclosure from the top. This shielding arrangement is typical of commercially-manufactured TMNs. Table 1 shows a

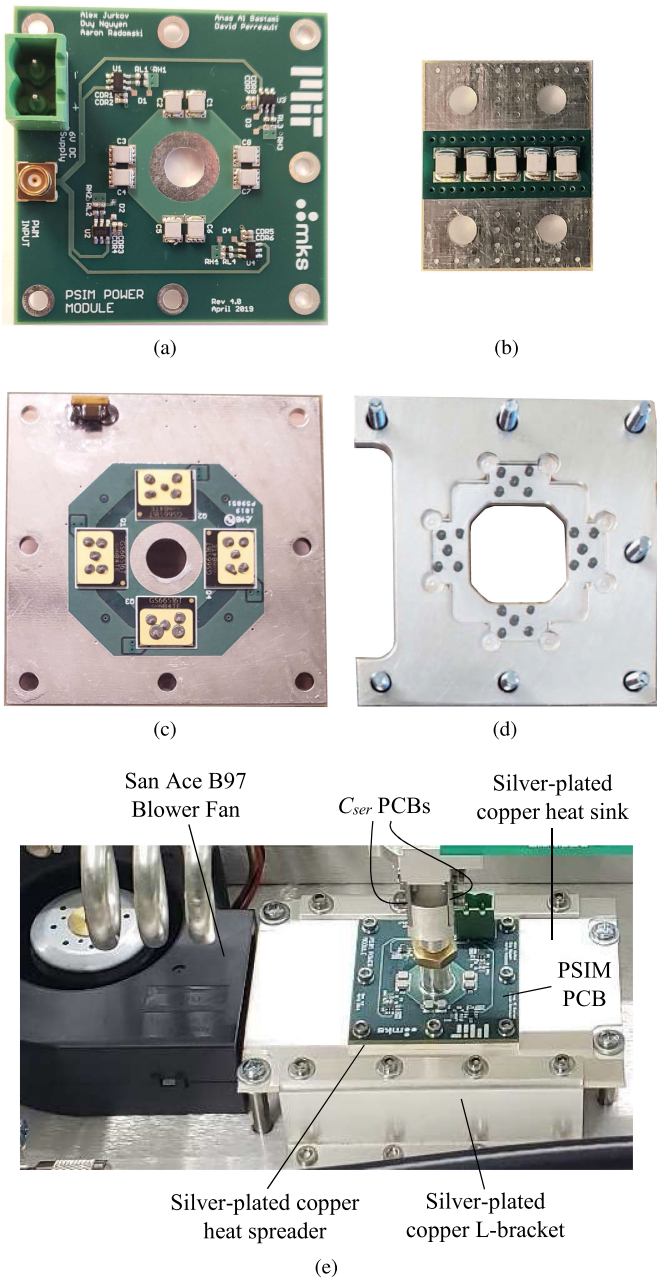

FIGURE 9. (a): Top view of PCB showing the PSIM switch drivers, shunt capacitance C_{sh}, PWM input, and dc supply; (b): Top view of one of two PCBs forming series capacitance C_{ser}; (c): Bottom view of the PSIM PCB showing the switches, with solder paste on the source-connected cooling pad; (d): Heat spreader designed to solder to the cooling pads of the switches; and (e): Close-up photo of the full PSIM power module, with the heat sink and its L-brackets to establish a low-resistance ground connection, fan blower, and mechanical connections of the PCB-heat-spreader unit to the heat sink.

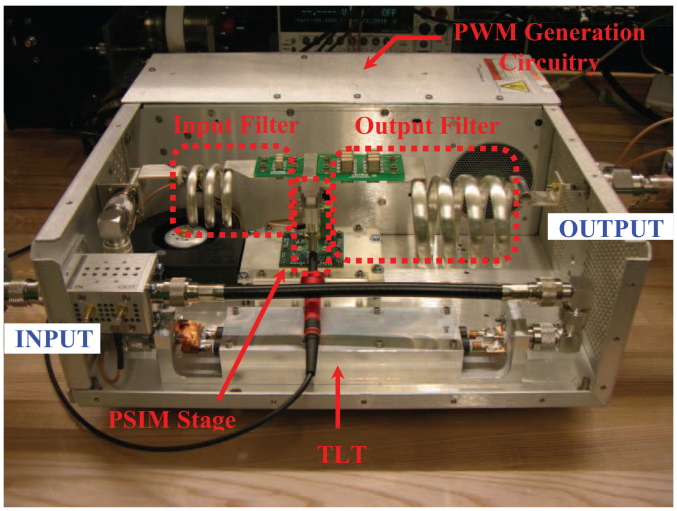

FIGURE 10. Photograph of the power stage of the high power PSIM-based TMN from input (left) to output (right) when the enclosure is open.

TABLE I Actual Implemented Component Values for the Matching System in Fig. 10

Component	Value	Implementation
C_1	372 pF	3x 2.5 kV 100 pF P90 ceramic capacitors (ATC100C, ATC Corp.), and 3x 2.5 kV 24 pF P90 ceramic capacitors (HQCC, AVX Corp.)
L_1	373 nH	3 turns of 0.25" silver-plated copper tube, inner diameter = 38 mm, pitch = 13.35 mm.
C_2	330 pF	10x 7.2 kV 15 pF P90 ceramic capacitors (HQCE, AVX Corp.), and 10x 7.2 kV 18 pF NP0 ceramic capacitors (HQCE, AVX Corp.)
L_2	709 nH	4 turns of 0.375" silver-plated copper tube, inner diameter = 58 mm, pitch = 19.53 mm.
C_{ser}	3 nF	20x 1 kV 150 pF C0G ceramic capacitors (VJ1111, Vishay).
C_{sh}	312 pF	8x 1.5 kV 39 pF NP0 ceramic capacitors (VJ1111, Vishay).
PSIM Switches	-	4x GaN Systems GS66516T.
Fan Blower	-	24 V San Ace B97 (Part #: 9BMB24P2G01).
Heat Sink	-	Dynatron A25 skived fin copper heat sink.
TLT	50 Ω:12.5 Ω	Series-parallel connection of two 25 Ω RG141 transmission lines, each placed inside a series-stack of 14x Fair Rite 61 material cores (Part #: 5961001901); custom-built Aluminum mounting bracket and spreaders.

summary of all components used to realize the TMN. (Note that silver-plating was utilized to prevent corrosion of parts made of copper).

The control of the PSIM switches was achieved using phase-locked loop (PLL)-based scheme described in detail in [9], [24], which generates pulse-width-modulation (PWM) synchronized to a reference provided by the rf power amplifier. This scheme was implemented in a separate PWM generation board (not shown here). The PWM signals were fed directly to the PWM input as can be seen in Fig. 9(a). All PWM generation and control circuitry were separately enclosed in another metal compartment within the overall system enclosure to prevent any contamination due to EMI arising from the coreless inductors. Furthermore, appropriate

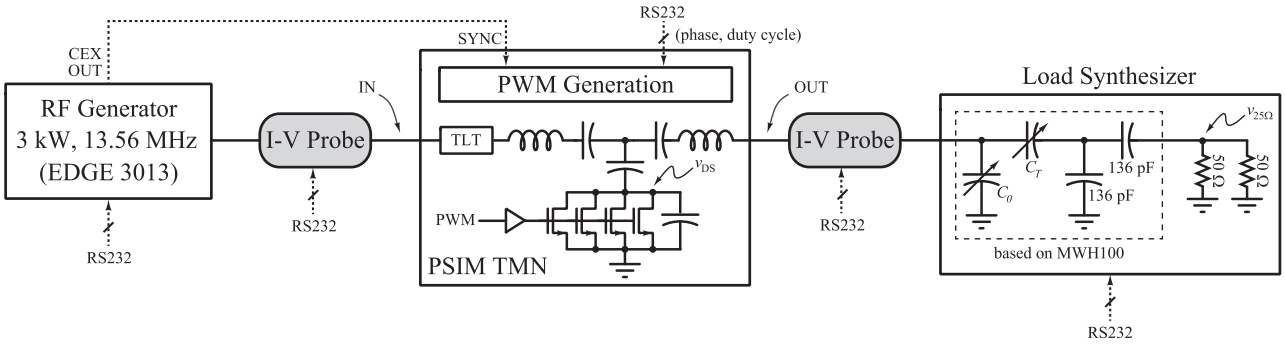

FIGURE 11. Measurement setup used to test the TMN. The setup consists of a 3 kW rf generator, the implemented TMN, a load synthesizer that generates the desired load range, and two I-V probes for impedance measurement.

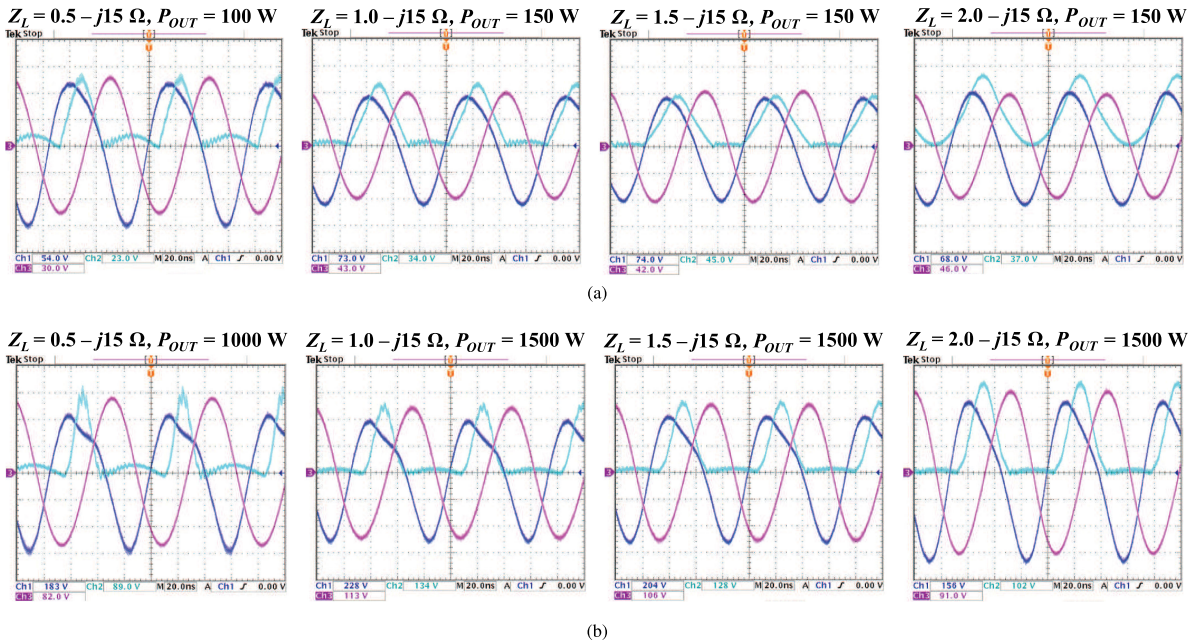

FIGURE 12. Scope waveforms showing FET drain-source voltage (cyan), TMN input voltage (dark blue), and voltage across the two paralleled 50 Ω coax resistors (purple). The waveforms shown are for various synthesized loads running at (a): low output power levels (100 W or 150 W), and (b): high output power levels (1000 W or 1500 W), while achieving a 50 Ω input impedance. In the rightmost plot of (a), no switch conduction is needed to achieve the desired 50 Ω match.

isolation and filtering was utilized in the PWM generation and control circuitry to protect against conducted EMI from the power stage.

IV. EXPERIMENTAL RESULTS

Fig. 11 shows the experimental setup used to evaluate the performance of the implemented TMN. The setup consists of an rf generator, the implemented TMN, a load synthesizer, as well as I-V probes at the TMN input and output, capable of measuring impedance and power, among other parameters. The rf generator (EDGE 3013, MKS Instruments Inc.) is a liquid-cooled rf power amplifier, with the capability of adjusting the frequency about 13.56 MHz. The load range of interest was synthesized using two parallel 500 W, 50 Ω coax resistors (Termaline 8201, Bird Electronic Corp.) connected via a tunable matching network (MWH-100, MKS Instruments Inc.), as shown in Fig. 11. The rf generator provides the reference to the PWM generation circuitry used to command the switching of the PSIM switches. The I-V probes (Model #: 000-1106-117, MKS Instruments Inc.) provide in-line sensing of instantaneous voltage and current and their ratio, providing instantaneous measurements of rf impedance and power flow.

For each load tested, the input power was gradually increased to achieve output power levels from 100 W up to a maximum target output power of 1.5 kW. Once a desired load impedance was set and synthesized, the duty cycle of the PWM pulses and operating frequency were adjusted as needed to obtain a 50 Ω input match with no reflected power. In some cases, the PWM pulses were also phase-shifted to prevent reverse conduction of the switches.

Figs. 12(a) and 12(b) show the measured waveforms of the TMN matching various loads (0.5-j15 Ω, 1.0-j15 Ω, 1.5-j15 Ω, and 2.0-j15 Ω) to 50 Ω at output power levels

ranging from 100 W up to 1.5 kW. The measured waveforms in each scope screen shot show the input voltage (dark blue), the output voltage across the two paralleled 50 Ω resistors (purple), and the switch drain-source voltage (cyan). Since the reactive portion of these loads was the same, the operating frequency was about the same, at around 13.89 MHz. It can be seen from Fig. 12 that the TMN successfully achieves a 50 Ω input impedance for several loads across a wide operating power range, while simultaneously maintaining acceptable peak PSIM switch voltages and sinusoidal output voltage waveforms.

The scope waveforms reveal two features that confirm our predictions about the system. First, at a given operating power level, as the load resistance decreases (going from right to left in both Figs. 12(a) and 12(b)), higher PSIM conduction angles can be observed. This matches our prediction that a higher net shunt capacitance is required to achieve a 50 Ω match for loads with lower resistance. Second, it can be seen that for a given load (e.g., the rightmost scope shots in Figs. 12(a) and 12(b)), maintaining a 50 Ω input impedance at higher power levels requires higher PSIM switch conduction angles. This confirms our prediction that at higher power levels, the higher switch drain voltages result in a reduction in its output capacitance C_{OSS}, which in turn necessitates higher conduction angles to achieve the net shunt capacitance required by the L-match. These trends are further illustrated in Figs. 13(a) and 13(b), which show the switch duty cycles required to achieve a 50 Ω input impedance for the full range of loads tested at 200 W and 1.5 kW, respectively. It can be seen that the implemented TMN design had very good utilization of the dynamic range of the switch with respect to duty cycle; the duty cycles used to achieve a 50 Ω match ranged from 25% up to 70%, which was well within the capability of the PWM generation and gate driving circuitry.

Figs. 14(a) and 14(b) show the measured peak drain-source voltage of the switches as well as the overall TMN efficiency while providing a 50 Ω input impedance match for two loads with the highest and lowest resistance, respectively, across the full operating power range. It can be seen from Fig. 14(a) that the peak switch voltage successfully remains below the imposed limit of 400 V, with a peak voltage of 357 V at 1.5 kW of output power. For loads having the highest resistance component, exemplified by the load shown in Fig. 14(a), a TMN efficiency of about 90% was achieved, even at higher power levels where PSIM modulation was not negligible (see rightmost scope shot in Fig. 12(b)). The TMN efficiency for loads having the lowest resistance was just below 70%, as shown in Fig. 14(b). The majority of power loss in this TMN was due to the limited quality factor of the output inductor and is therefore not related to the performance or characteristics of the PSIM module. Inductors in conventional impedance matching systems have comparable losses at similar operating conditions; this problem can be alleviated by using an inductor having a higher quality factor. (These high inductor losses, especially at high output current levels, were the reason that the highest operating output power was limited to 1 kW for

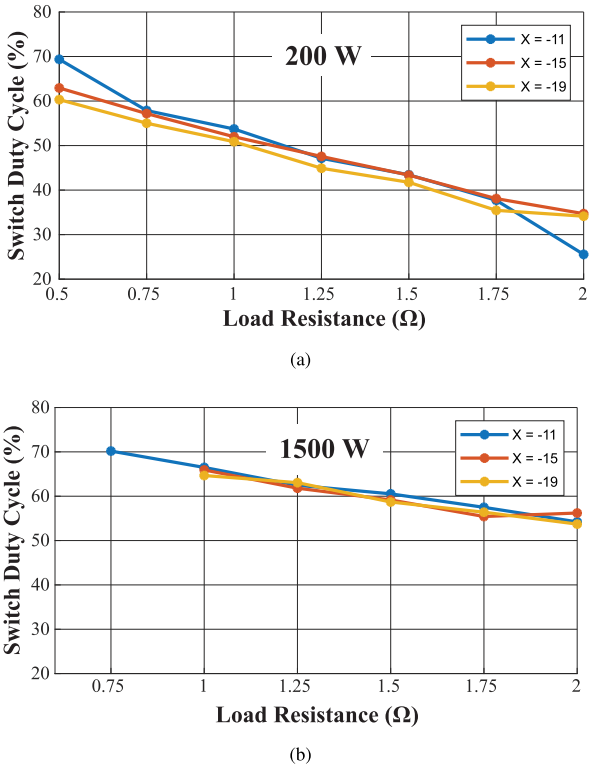

FIGURE 13. Measured switch duty cycle plotted against the resistive component of the load range for different load reactance values. The results shown are with the TMN providing a 50 Ω input impedance match at output power levels of (a): 200 W, and (b): 1500 W. For a given power level, loads having the lowest resistance component require higher switch duty cycles. Furthermore, for a given load, higher duty cycles are required at higher output power levels, owing to the nonlinearity of the transistors' output capacitance C_{OSS}.

loads having the lowest resistance). Fig. 15 shows a thermal camera shot of the TMN system delivering 1.5 kW to a load $Z_L = 2.0\text{-}j15\ \Omega$ in steady-state. It can be seen that the operating temperatures of the various system components are acceptable, with a peak of 45.5 °C at the output filter capacitors. This suggests that the designed thermal management system adequately cools the PSIM switches.

To gain further insight into the distribution of losses in the PSIM TMN, Table 2 shows the loss values obtained from simulating the two loads in Fig. 14 for both the PSIM TMN as well as for a conventional TMN (with no PSIM elements) having the same inductor quality factors, assuming ideal (lossless) tunable capacitors. The results further confirm that a dominant portion of total loss is due to losses in the output inductor L_2. In addition, it can be seen that under similar operating conditions, similar inductor loss values are observed in a conventional TMN design. Despite the additional switch losses in the PSIM TMN, the benefit of having the ability to match impedance orders of magnitude faster than conventional TMNs makes PSIM an attractive technique for many applications. Extensive simulations show that the demonstrated PSIM TMN circuit settles within no more than 5 μs, ignoring the time needed for impedance measurement

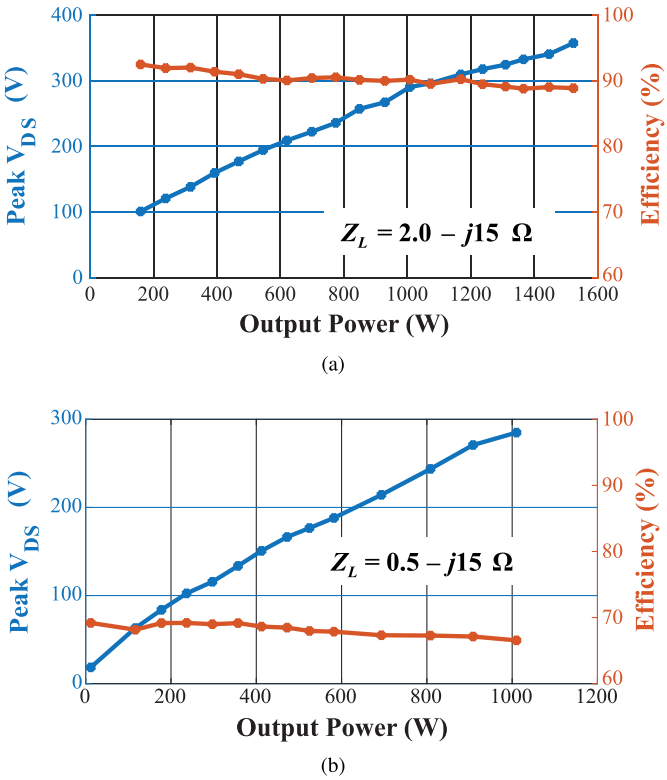

FIGURE 14. Measured peak drain-source voltage of the switches (blue) and overall TMN efficiency (orange) while providing a 50 Ω input impedance match, with (a): $Z_L = 2.0\text{-}j15\ \Omega$, corresponding to the load having the maximum resistive component within the load impedance range, and (b): $Z_L = 0.5\text{-}j15\ \Omega$, corresponding to the load having the lowest resistive component within the impedance range. The highest peak voltage is about 357 V, and the lowest efficiency is about 67%.

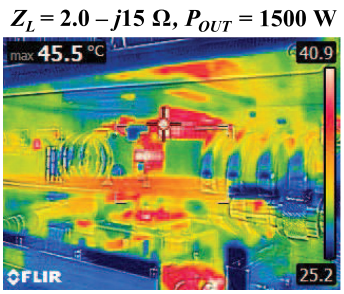

FIGURE 15. Thermal camera shot showing peak measured temperature with the TMN providing a 50 Ω input impedance for $Z_L = 2.0 - j15\ \Omega$ at 1500 W of output power.

TABLE II Simulated Loss Breakdown for the Loads in Fig. 14

	PSIM TMN		Conventional TMN	
Z_L (Ω)	2.0-j15	0.5-j15	2.0-j15	0.5-j15
P_{out} (W)	1493	1107	1493	1104
P_{L_1} (W)	6.9	5.9	6.9	6.0
P_{L_2} (W)	93.7	267	89.9	263
$P_{sw,cond}$ (W)	21.6	85.0	-	-
$P_{sw,Coss}$ (W)	22.8	7.3	-	-
η	91.1%	75.2%	93.9%	80.4%

and control and rf generator response. In practice, the achievable PSIM response bandwidth may be primarily limited by the latency with which impedance can be measured, as well as the bandwidth of the control circuitry and the response of the rf generator. While slightly more efficient, conventional TMNs with capacitors that are mechanically-adjustable via servo motors have response times on the order of a few seconds.

V. CONCLUSION

This work advances the design of PSIM-based TMNs for high-power rf applications. In particular, the contributions in this work include (a) a detailed analytical characterization of losses and tradeoffs in a PSIM element, (b) design options that leverage the TMN power processing capability given limited voltage and current ratings of available switches, and (c) the design and experimental verification of a 1.5 kW, 13.56 MHz PSIM-based TMN that maintains a 50 Ω input impedance for a load impedance varying in resistance between 0.5 Ω to 2 Ω, and in reactance between -j10 Ω to -j25 Ω (commensurate with industrial plasma processing applications). The demonstrated performance of the high power PSIM TMN along with the detailed loss characterization and tradeoffs of the PSIM element open up the use of PSIM in numerous applications at high powers and high frequencies.

APPENDIX A
APPROXIMATION OF PSIM CONDUCTION LOSS

It is desired to re-express equation (5) in a form that explicitly shows the peak voltage of the PSIM switch. This can be done by expressing $|v_{in}|$ as a function of the PSIM peak voltage. From Fig. 1(a), we can express the PSIM switch voltage as follows:

$$v_C = \begin{cases} 0 & 0 \le \omega t \le \alpha \\ \frac{|i_C|}{\omega C_0}(\cos\alpha - \cos(\omega t)) & \alpha \le \omega t \le 2\pi - \alpha \\ 0 & 2\pi - \alpha \le \omega t \le 2\pi \end{cases} \tag{17}$$

Thus, from equation (17), it can be seen that the switch peak voltage is given by:

$$V_{sw,pk} = \frac{|i_C|}{\omega C_0}(1 + \cos\alpha) \tag{18}$$

The magnitude of the fundamental component of v_C, which is equal to the input voltage $|v_{in}|$, can be obtained via Fourier analysis. Noting that the PSIM voltage is an even function, the magnitude of the fundamental component is readily computed as follows:

$$\begin{aligned} |v_C|_1 &= \frac{1}{\pi}\int_{\alpha}^{2\pi-\alpha} \frac{|i_C|}{\omega C_0}(\cos\alpha - \cos(\omega t))\cos(\omega t)\, d(\omega t) \\ &= \frac{|i_C|}{\omega C_0}\left(\frac{\pi - \alpha + \sin\alpha\cos\alpha}{\pi}\right) \end{aligned} \tag{19}$$

Combining the last two equations, using the fact that $|v_C|_1 = |v_{in}|$, and squaring both sides yields the following

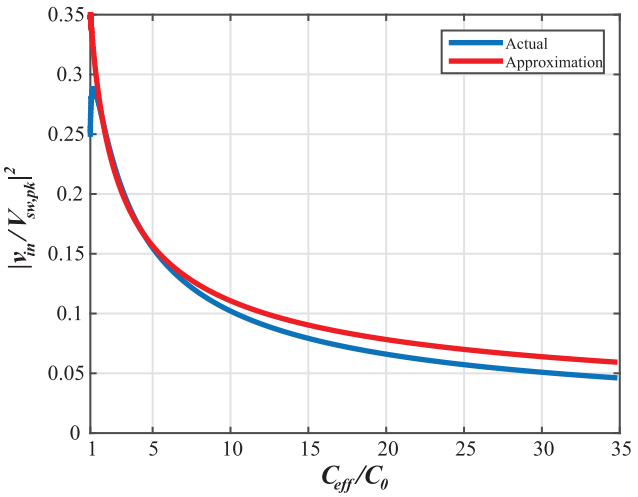

FIGURE 16. Comparison of the actual (blue) and approximated relation (red) between $|v_{in}^2/V_{sw,pk}^2|$ as a function of the PSIM capacitance modulation ratio C_{eff}/C_0.

relation between $|v_{in}|^2$ and $V_{sw,pk}^2$:

$$|v_{in}|^2 = \left|\frac{\pi - \alpha + \sin\alpha\cos\alpha}{\pi(1+\cos\alpha)}\right|^2 V_{sw,pk}^2 \tag{20}$$

The fraction in this expression is only a function of α; however, it cannot be algebraically expressed in terms of only C_{eff}/C_0 due the transcendental nature of the function. A simple approach to proceed from here is to use a simple approximation of the ratio of $|v_{in}|^2$ to $V_{sw,pk}^2$ from equation (20). One such possible approximation is given below.

$$|v_{in}|^2 \approx \frac{0.35}{\sqrt{C_{eff}/C_0}} V_{sw,pk}^2 \tag{21}$$

To illustrate the accuracy of this approximation, Fig. 16 shows a plot of the ratio using exact equations (shown in blue), along with a plot of the approximation used (shown in red). It can be seen that our choice of the approximating function is reasonably accurate for a very wide range of PSIM capacitance modulation ratios (well beyond the typical practical range used). The discrepancy at values of C_{eff}/C_0 in the vicinity of 1 is insignificant since the conduction losses are in the vicinity of zero at those values (see equation 5).

Using this approximation, the PSIM conduction loss can be expressed as desired:

$$P_{cond} = 0.35\omega R_{DS,ON} C_{OSS} V_{sw,pk}^2 (1+\gamma)\omega C_0 \cdot \sqrt{\left(\frac{C_{eff}}{C_0}\right)}\left(\frac{C_{eff}}{C_0} - 1\right) \tag{22}$$

ACKNOWLEDGMENT

The authors would like to thank the Qatar Foundation Research Division for their financial support of author Anas Al Bastami and MKS Instruments for supporting the research.

REFERENCES

[1] S. Sohn, J. T. Vaughan, and A. Gopinath, "Auto-tuning of the RF transmission line coil for high-fields magnetic resonance imaging (MRI) systems," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Jun. 2011, pp. 1–4.
[2] A. Abuelhaija, K. Solbach, and A. Buck, "Power amplifier for magnetic resonance imaging using unconventional Cartesian feedback loop," in *Proc. German Microw. Conf.*, Mar. 2015, pp. 119–122.
[3] F. H. Raab *et al.*, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
[4] B. Regensburger *et al.*, "High-performance large air-gap capacitive wireless power transfer system for electric vehicle charging," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, Jun. 2017, pp. 638–643.
[5] S. Sinha, A. Kumar, and K. K. Afridi, "Improved design optimization of efficient matching networks for capacitive wireless power transfer systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 3167–3173.
[6] E. Waffenschmidt, "Dynamic resonant matching method for a wireless power transmission receiver," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6070–6077, Nov. 2015.
[7] W. D. Braun and D. J. Perreault, "A high-frequency inverter for variable-load operation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 706–721, Jun. 2019.
[8] A. Kumar, S. Sinha, and K. K. Afridi, "A high-frequency inverter architecture for providing variable compensation in wireless power transfer systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 3154–3159.
[9] A. S. Jurkov, A. Radomski, and D. J. Perreault, "Tunable impedance matching networks based on phase-switched impedance modulation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 947–954.
[10] A. Al Bastami *et al.*, "Dynamic matching system for radio-frequency plasma generation," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1940–1951, Mar. 2018.
[11] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 41–53, Jan. 2007.
[12] N. O. Sokal, "Class-E RF power amplifiers," *QEX*, pp. 9–20, Jan./Feb. 2001.
[13] L. Roslaniec, A. S. Jurkov, A. Al Bastami, and D. J. Perreault, "Design of single-switch inverters for variable resistance/load modulation operation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3200–3214, Jun. 2015.
[14] R. Whatley, T. Ranta, and D. Kelly, "CMOS based tunable matching networks for cellular handset applications," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Jun. 2011, pp. 1–4.
[15] Y. Lim, H. Tang, S. Lim, and J. Park, "An adaptive impedance-matching network based on a novel capacitor matrix for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4403–4413, Aug. 2014.
[16] G. J. J. Winands, A. J. M. Pemen, E. J. M. van Heesch, Z. Liu, and K. Yan, "Matching a pulsed power modulator to a corona plasma reactor," in *Proc. 16th IEEE Int. Pulsed Power Conf.*, Jun. 2007, pp. 587–590.
[17] J. Fu and A. Mortazawi, "Improving power amplifier efficiency and linearity using a dynamically controlled tunable matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 3239–3244, Dec. 2008.
[18] F. C. W. Po, E. de Foucauld, D. Morche, P. Vincent, and E. Kerherve, "A novel method for synthesizing an automatic matching network and its control unit," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 58, no. 9, pp. 2225–2236, Sep. 2011.
[19] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1110–1118, May 2009.
[20] E. Chung and J. Ha, "Resonant network design methodology based on two-port network analysis considering load impedance variation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2019, pp. 2178–2183.
[21] D. J. Perreault, "A new architecture for high-frequency variable-load inverters," in *Proc. IEEE 17th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 2016, pp. 1–8.
[22] P. Sen, P. Biringer, and R. Segsworth, "Thyristor-controlled single phase variable inductor," *IEEE Trans. Magn.*, vol. 3, no. 3, pp. 240–245, Sep. 1967.

[23] W.-J. Gu and K. Harada, "A new method to regulate resonant converters," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 430–439, Oct. 1988.
[24] A. S. Jurkov, "Techniques for efficient radio frequency power conversion," Ph.D. dissertation, Electr.Eng. Comput. Sci., , Massachusetts Inst. Technol., Cambridge, MA, USA, 2019.
[25] D. Perreault and A. Jurkov, "Tunable matching network with phase-switched elements," U.S. Patent 9,755,576, Sep. 2017.
[26] D. Jin and J. A. del Alamo, "Methodology for the study of dynamic on-resistance in high-voltage GaN field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3190–3196, Oct. 2013.
[27] B. J. Galapon, A. J. Hanson, and D. J. Perreault, "Measuring dynamic on resistance in GaN transistors at MHz frequencies," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, Jun. 2018, pp. 1–8.
[28] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic on-resistance in GaN-on-Si HEMTs: Origins, dependencies, and future characterization frameworks," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5581–5588, Jun. 2020.
[29] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault, "New architectures for radio-frequency dc-dc power conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 380–393, Mar. 2006.
[30] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "C_{OSS} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10 748–10 763, Dec. 2018.
[31] M. Guacci *et al.*, "On the origin of the C_{oss} -losses in soft-switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019.
[32] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. Rivas-Davila, "An investigation into the causes of COSS losses in GaN-on-Si HEMTs," in *Proc. 20th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 2019, pp. 1–7.
[33] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019.
[34] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. Rivas-Davila, "Output capacitance loss characterization of silicon carbide schottky diodes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 865–878, Jun. 2019.
[35] E. Rotholz, "Transmission-line transformers," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 4, pp. 327–331, Apr. 1981.
[36] A. Eroglu, "High-power transmission line transformer design for plasma generators," *IEEE Trans. Plasma Sci.*, vol. 42, no. 4, pp. 969–975, Apr. 2014.
[37] W. A. Davis and K. Agarwal, *Radio Frequency Circuit Design*. Hoboken, NJ, USA: Wiley, 2001.
[38] G. Guanella, "New method of impedance matching in radio-frequency circuits," *Brown Boveri Rev.*, vol. 31, no. 9, pp. 327–329, Sep. 1944.
[39] C. Trask, "A tutorial on transmission line transformers," Aug 2005, pp. 1–7. [Online]. Available: http://home.earthlink.net/%7Echristrask/TraskTLTTutorial.pdf