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Drain-Source Synchronous Rectifier Oscillation Mitigation in Light-Load Conditions

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ABSTRACT The increasing usage of LLC-type dc-dc converters in utility, automotive, and power distribution applications has led to a push for a further increase in the converter's operating load range and efficiency. The secondary-side rectifier remains one of the lossiest areas in the converter, alluring designers to synchronous rectification (SR). One method is drain-source SR for cyclically adaptive, closed loop SR. However, when utilized, a severe current oscillation can be observed. An increase in SR duty cycle results in an increase in conduction time of the SR channel over the body diode. This issue becomes increasingly prevalent due to the usage of wide band-gap MOSFETs with high reverse drops and low sensed signal strength. This results in a current oscillation effect, leading to inconsistent SR operation, output ripple, and high EMI. In this paper, the issue is root caused analyzed. A method of improving drain-source SR for light-load SR operation is proposed. The method is prototyped on an FPGA to alleviate the issue on a 600-V_{in}/340-V_{out} 2.5-kW LLC-DCX (DC transformer) power converter.

INDEX TERMS dc-dc power converters, power electronics, rectifiers, pulse width modulation converters.

I. INTRODUCTION

As the usage of high voltage power electronics becomes more prevalent, *LLC*-based resonant converters are experiencing widespread attention due to its voltage isolation capabilities, energy conversion efficiency, and power density. *LLC* converters can be found in many applications requiring efficient step-up, step-down, and high voltage (HV) isolation. In recent times, these applications have included solid state transformers (SSTs), automotive power conversion, datacenters, and server power supplies [1]–[4]. Along with the increase in *LLC* usage has been a push for wider load range, for example in applications that operate in standby mode where the primary switches are still on [5]–[7]. This is commonplace in open-loop *LLC* converters, where burst-mode is impractical due to high output ripple [8]. These requirements provide new challenges to face in synchronous rectification (SR), which is generally implemented as an afterthought. In this paper, a current oscillation phenomenon is discovered by the authors when implementing SR on *LLC* converters. The issue is root caused, analyzed, and a solution is developed to improve SR algorithms.

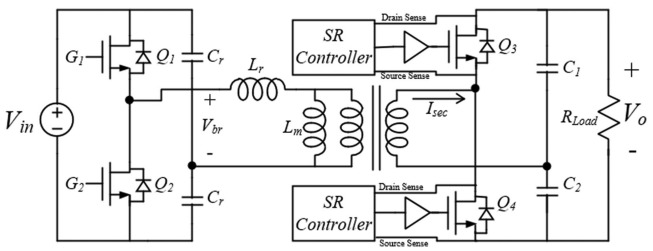

FIGURE 1. *LLC*-DCX circuit with SR voltage doubler.

An *LLC* converter is an isolated dc-dc converter that utilizes a resonant tank and transformer to provide a soft switched, efficient means of power conversion. When operated in open-loop, the converter is coined a DC-transformer, or "DCX" due to the fixed voltage step ratio as dictated by the transformer

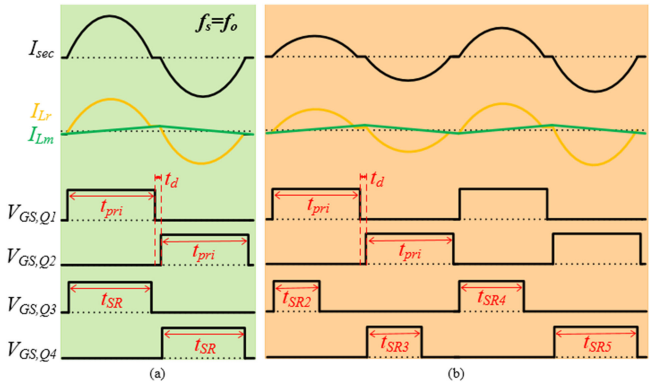

FIGURE 2. **Key waveforms of *LLC* converter with (a) stable SR driving and (b) current increase from a SR duty cycle increase.**

turns. Fig. 1 depicts a *LLC*-DCX with a fixed voltage step-down ratio, and Fig. 2(a) key voltage and current waveforms for the converter, where full SR conduction, ideally 50% duty cycle, is defined relative to the full switching period. The resonant nature of power conversion in *LLC* converters necessitates a rectifier to produce a dc output. The rectifier diodes become hotspots for undesirable conduction loss due to ohmic losses during rectification from the diode forward drop. Synchronous rectification is a technique implemented to reduce losses by replacing rectifier diodes with switches, typically a MOSFET, which operate synchronously with diode conduction. By redirecting current through a more efficient rectification path, the conduction loss from diode can be eliminated [9]–[12].

Many SR methods exist for use in *LLC* converters, including self-driven [13]–[16], open loop [17], [18], current sensed [19]–[30], and voltage sensed [31]–[35]. Each method other than open-loop utilizes a form of current sensing to determine the SR duty cycle. Open-loop SR utilizes the primary-side controller to drive the secondary-side SR switches at a fixed duty cycle without any feedback [17], [18]. While simple, it leaves much to be desired due to inaccurate switching moments. Since the secondary-side current waveforms change across load, open-loop SR can create instances where the turn-off moment is before or after the zero current moment, leading to parallel diode losses, or to reverse current conduction [17]. Furthermore, open-loop SR requires a physical connection between the primary and secondary-side. This is a hurdle for high voltage isolation requirements, as traditional signal isolation methods are not capable of sustaining continuous high voltage for isolation in the case of a failure [1], [2]. Possible methods that are capable of HV insulation are prohibitively expensive when scaled, such as fiber optics. Another form of SR is current sensing, which utilizes a current sensing mechanism such as a transformer to determine SR turn-on and turn-off moments [19]–[30]. This method allows for precise switching moments at the expense of necessitating additional digital or analog processing circuitry to convert the current signal into SR drive signals. As a result, this method is still undesirable due to the expense and board area needed. Finally, among the many voltage-sensed methods [31]–[35] in SR are two commercialized methods: volt-second, and drain-source sensing. The volt-second method utilizes both the output voltage and the SR switch's drain-source voltage signal to determine turn-on and turn-off moments [31]. This method is completely standalone, and requires no primary-side signal. As a result, the primary-to-secondary side voltage isolation issue is avoided. However, due to the volt-second algorithm, the sensing voltages cannot be blocked or clamped. This limits the applicable voltage range for this method of SR. On the other hand, drain-source SR utilizes only the SR switch's drain-source signal in order to determine the proper turn-on and turn-off moments [9]–[11]. However, since the turn-on and turn-off sampling moments are at low voltage, this method operates properly even when a voltage clamp above these voltages is implemented, which allows for high voltage operation [36]. As a result, the drain-source SR method was selected for implementation in this paper.

In this paper, the authors discovered a current oscillation phenomena when an *LLC* resonant converter is implemented with closed loop SR. An increase in SR duty cycle from the controller causes an increase in the resonant current as shown in Fig. 2(b), which propagates into an oscillation. This issue is not limited to drain-source SR, and has been replicated on current-sensed SR systems as well. A possible solution is to manually disable SR completely during the oscillating conditions. For lower voltage systems, disabling SR is the simple solution. However, this can result in poor rectifier efficiency, and an external method of control and additional sensing components for load conditions will need to be added. Furthermore, this is not feasible for high voltage converters with voltage isolation requirements between the primary and secondary sides. Many SR controllers already implement light-load shutdown by measuring the SR conduction time. However, these mechanisms also result in periodic duty cycle jumps [9], [10], which can also contribute to triggering oscillations. When the SR conduction period drops below a threshold, the controller turns off SR for some fixed period. Periodically however, the SR controller is enabled to sample the conduction period again. This results in a jump in SR duty cycle even in supposedly "disabled" conditions. As a result, the current oscillation phenomena will still exist with current SR algorithms.

The objective of this paper is to root-cause and analyze the oscillation issue, explore the effects of noise on the sensed signal, and finally propose an improvement on SR to eliminate the oscillation issue.

II. CURRENT OSCILLATION PHENOMENA

When operating the *LLC* converter in areas with poor SR signal strength, such as with low secondary side currents and/or low SR switch channel resistance ($R_{DS,on}$), the SR duty cycle is susceptible to perturbation, which can initiate oscillation. Since SR controllers do not offer sequential control

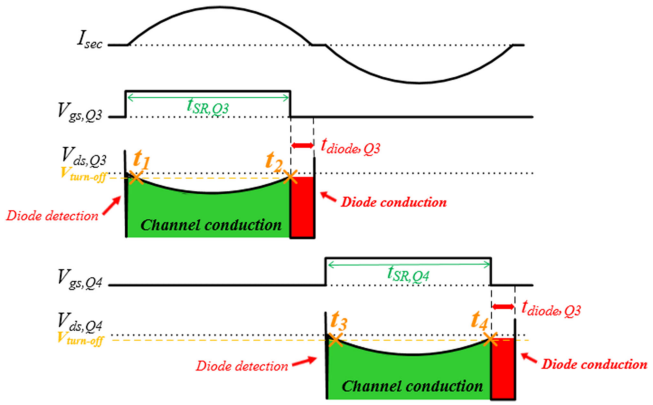

FIGURE 3. SR waveforms with SR switch channel and body diode conduction.

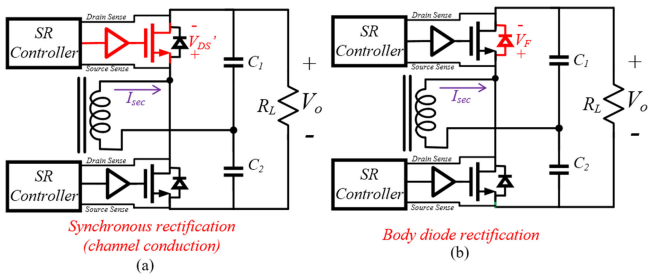

FIGURE 4. Rectifier voltage drop between channel and diode conduction.

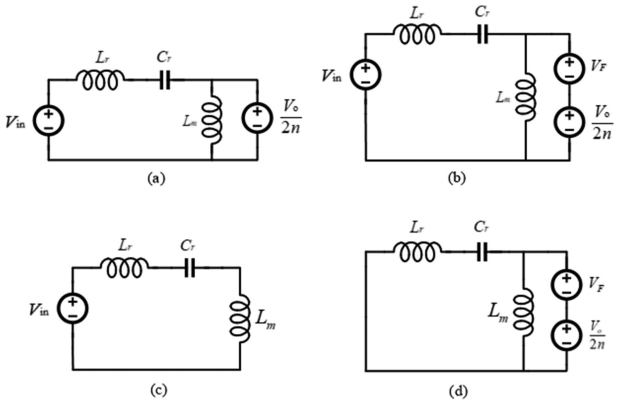

FIGURE 5. Equivalent *LLC* circuit models during: (a) Mode 1: SR (switch channel) conduction, (b) Mode 2: Diode conduction, (c) Mode 3: Discontinuous, and (d) Mode 4: Discharging.

logic, it is unable to prevent nor limit the current oscillation effect.

In SR, the duty cycle for the secondary-side rectifier switch is determined based on the secondary-side current waveform. Because the *LLC* secondary-side current waveform is pseudo-sinusoidal, the turn-on and turn-off moments vary across load. An early-turn off issue occurs from parasitic inductance in the sensing loop [37]–[42], resulting in parallel-diode conduction. Additional parallel-diode conduction can occur from the SR chip sensing discrepancies. The amount of parallel-diode conduction time has a direct relationship to the amount of output current. Therefore, an oscillation can be triggered between the SR controller and the *LLC* converter due to interdependency. An increase in SR duty cycle results in an increase of current, resulting in an oscillation when the duty cycle is perturbed. The susceptibility of this oscillation increases at noisy SR signal operating conditions.

Fig. 3 shows key SR waveforms with partial parallel diode conduction. There are two current paths during rectification: through the SR switch channel, or through the parallel diode, shown in Fig. 4. The amount of conduction time in each state is determined by the SR controller. The controller detects the initial parallel-diode conduction when the SR switch is off. The controller then turns the SR switch on, and SR occurs. As the current through the SR switch decreases, the drain-source voltage decreases. Once the drain-source voltage has dropped to the turn-off voltage, shown in t_2 and t_4 in Fig. 3, the switch is turned off. The remaining current is caught by the parallel-diode. Here, we see that each rectification state correlates with a certain rectification voltage drop.

During SR, the rectifier loop experiences a voltage drop of V_{DS}' as shown in Fig. 4(a). V_{DS}' is the product of the channel resistance and the drain-source current. This voltage drop is very small, typically in the range of millivolts. On the other hand, the diode conduction voltage drop is much larger. More channel conduction results in greater secondary-side current, and a large difference between V_{DS}' and V_F results in a system that is prone to oscillate. A reduction in average diode conduction time causes the output voltage to rise. Thus, a change in the amount of parallel diode conduction has a similar effect as a load transient.

The effects between SR and diode conduction states can be explained through steady-state circuit models. The state trajectory depicts the energy in the resonant tank, which is directly related to the secondary-side current. The resonant tank loss and channel resistance is assumed to be negligible, and the output capacitance C_o is omitted since $C_o \gg C_r$. When combined with SR, there are four operation modes during each half cycle. The equivalent circuits under different operation modes of the positive half cycle for a half bridge *LLC* resonant converter with a voltage doubler rectifier is shown in Fig. 5. Since the negative half cycle can be derived similarly to that of the positive half cycle, only the latter is presented in this paper.

Mode 1: The primary switch Q_1 turns on and the resonant current flows through the channel of the secondary-side switch Q_3. In this mode, the magnetizing inductor L_m is clamped by the output voltage and the equivalent circuit is shown in Fig. 5(a) [43].

The resonant current i_{Lr} and voltage across the resonant capacitor v_{Cr} can be expressed as (1) and (2), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos\left(\omega_{r0}\left(t-t_0\right)\right) + \frac{\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}\right)}{Z_{r0}}\sin\left(\omega_{r0}\left(t-t_0\right)\right) \quad (1)$$

$$v_{Cr}(t) = \left(V_{in}-\frac{V_o}{2n}\right)-\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}\right) \times\cos\left(\omega_{r0}\left(t-t_0\right)\right)+Z_{r0}i_{Lr0}\sin(\omega_{r0}(t-t_0)) \quad (2)$$

where V_{in}, and V_o represent the *LLC* converter input and output voltage, respectively. $\omega_{r0}=1/\sqrt{L_r\cdot 2C_r}$ is the resonant angular frequency, and $Z_{r0}=\sqrt{L_r/(2C_r)}$ is the impedance of the resonant network. From (1) and (2), the trajectory equation is given by (3).

$$\left(v_{Cr}(t)-\left(V_{in}-\frac{V_o}{2n}\right)\right)^2+\left(i_{Lr}(t)\cdot Z_{r0}\right)^2 = \left(V_{in}-\frac{V_o}{2n}-v_{Cr0}\right)^2+\left(i_{Lr0}\cdot Z_{r0}\right)^2 \quad (3)$$

(3) behaves as a circle with the center at $(V_{in}-V_o/2n,\,0)$ and radius R_1 depends on the initial conditions v_{Cr0} and i_{Lr0} given as (4).

$$R_1=\sqrt{\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}\right)^2+\left(i_{Lr0}\cdot Z_{r0}\right)^2} \quad (4)$$

Mode 2: The primary switch Q_1 remains on, but the resonant current flows through the parallel diode of the secondary-side switch Q_3. This mode is similar to Mode 1, but the voltage drop of the bode diode V_F is included in the equivalent circuit as shown Fig. 5(b). The time domain equations of the state variables i_{Lr} and v_{Cr} in this mode are given in (5) and (6), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos\left(\omega_{r0}\left(t-t_0\right)\right) + \frac{\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n}\right)}{Z_{r0}}\sin\left(\omega_{r0}\left(t-t_0\right)\right) \quad (5)$$

$$v_{Cr}(t) = \left(V_{in}-\frac{V_o}{2n}-\frac{V_F}{n}\right)-\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n}\right) \times\cos\left(\omega_{r0}\left(t-t_0\right)\right)+Z_{r0}i_{Lr0}\sin\left(\omega_{r0}\left(t-t_0\right)\right) \quad (6)$$

Similar to Mode 1 the trajectory behaves as a circle as well, but the center changes to $(V_{in}-V_o/2n-V_F/n,\,0)$ and the radius R_2 is derived as (7).

$$R_2=\sqrt{\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n}\right)^2+\left(i_{Lr0}\cdot Z_{r0}\right)^2} \quad (7)$$

Mode 3: Occurs when the switching frequency is lower than the resonant frequency. Under this mode Q_1 remains on, but there is no current flowing to the secondary side. The magnetizing inductor L_m joins the resonance and the equivalent circuit is as shown in Fig. 5(c). The time domain equations of the state variables i_{Lr} and v_{Cr}, in this mode are given in (8) and (9), respectively.

$$i_{Lr}(t)=i_{Lr0}\cos(\omega_{r1}(t-t_0))+\frac{(V_{in}-v_{Cr0})}{Z_{r1}}\sin(\omega_{r1}(t-t_0)) \quad (8)$$

$$v_{Cr}(t)=V_{in}-(V_{in}-v_{Cr0})\cos(\omega_{r1}(t-t_0)) + Z_{r1}i_{Lr0}\sin(\omega_{r1}(t-t_0)) \quad (9)$$

where $Z_{r1}=\sqrt{(L_r+L_m)/2C_r}$ is the characteristic impedance, and $\omega_{r1}=1/\sqrt{(L_r+L_m)\cdot 2C_r}$ is the resonant frequency. The trajectory is obtained from (8) and (9).

$$(v_{Cr}(t)-V_{in})^2+\left(\frac{i_{Lr}(t)\cdot Z_{r0}}{Z_{r0}/Z_{r1}}\right)^2 = (v_{Cr0}-V_{in})^2+(i_{Lr0}\cdot Z_{r1})^2 \quad (10)$$

From (10), we can see this behaves as an ellipse with a center $(V_{in},\,0)$.

Mode 4: Occurs when the switching frequency is higher than the resonant frequency. Under this mode Q_1 turns off and Q_2 turns on. Since it follows Mode 2 the resonant current will continue flowing through the parallel diode of the secondary-side switch Q_3. The equivalent circuit is as shown in Fig. 5(d) and the time domain equations of the i_{Lr} and v_{Cr} can be given as (11) and (12), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos(\omega_{r0}(t-t_0)) - \frac{\left(v_{Cr0}+\frac{V_F}{n}+\frac{V_o}{2n}\right)}{Z_{r0}}\sin(\omega_{r0}(t-t_0)) \quad (11)$$

$$v_{Cr}(t) = -\left(\frac{V_F}{n}+\frac{V_o}{2n}\right)+\left(v_{Cr0}+\frac{V_F}{n}+\frac{V_o}{2n}\right) \times\cos(\omega_{r0}(t-t_0))+Z_{r0}i_{Lr0}\sin(\omega_{r0}(t-t_0)) \quad (12)$$

The trajectory is similar to Mode 1 with the center changes to $(-V_o/2n-V_F/n,\,0)$ and radius depends on the initial conditions V_{cr0} and I_{Lr0}.

The derived Modes I-IV are graphed in Fig. 6 and plotted alongside the simulated trajectory to verify (1)–(12) for three operating conditions, when the *LLC* with SR operates below the resonant frequency ($f_s < f_o$), at the resonant frequency ($f_s = f_o$), and above the resonant frequency ($f_s > f_o$). The steady state waveforms for the three operating conditions are shown below depicting the operating modes: with the *LLC* converter operating below the resonant frequency ($f_s < f_o$), at the resonant frequency ($f_s = f_o$), and above the resonant frequency ($f_s > f_o$) in Fig. 7. Since the oscillation phenomena and underlying cause of the oscillation can be found in all three operating conditions, only the $f_s = f_o$ model is used to explore the state trajectory under diode and channel conduction.

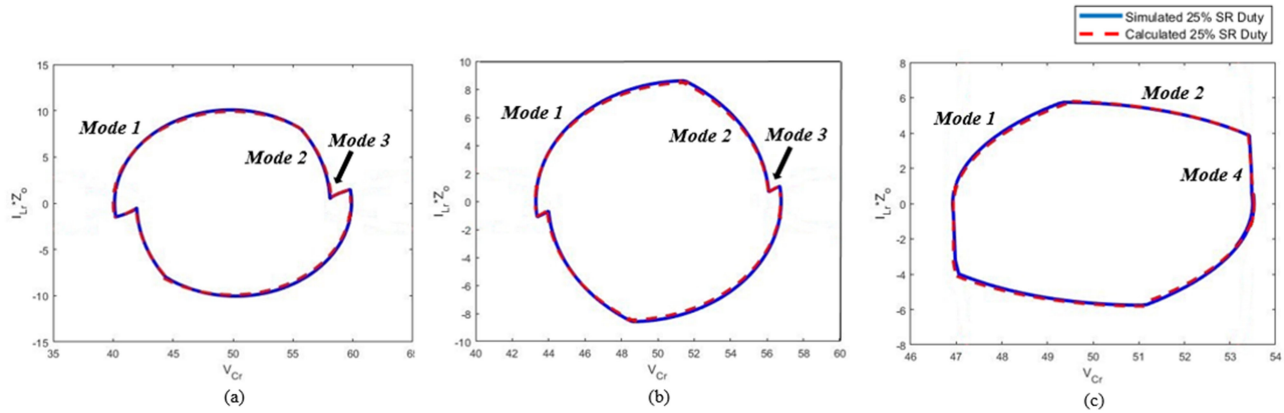

FIGURE 6. Resonant tank trajectory modes at 25% SR duty cycle at (a) $f_s < f_o$, (b) $f_s = f_o$, (c) $f_s > f_o$.

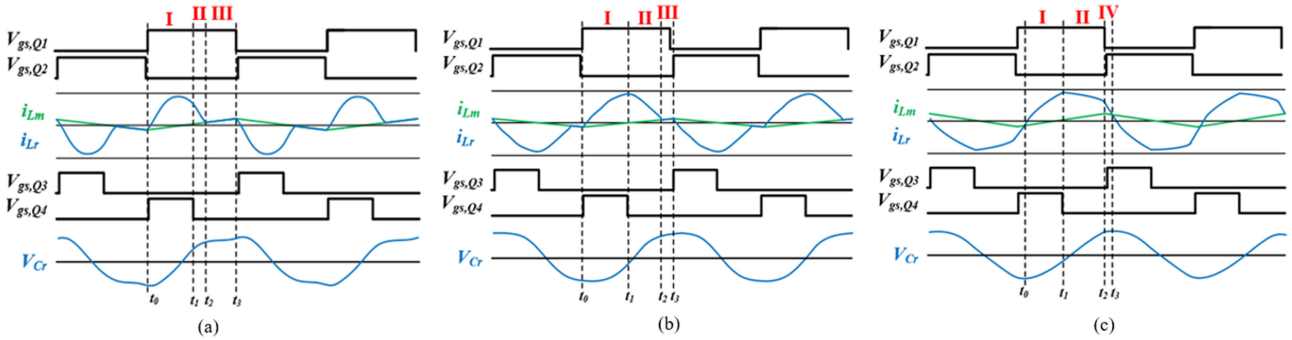

FIGURE 7. Steady state time-domain waveforms when (a) $f_s < f_o$, (b) $f_s = f_o$, (c) $f_s > f_o$.

The amount of energy in the tank is correlated with the radius of the trajectory, (4) and (7). Therefore, diode conduction reduces the tank energy, and SR increases it. Thus, an increase in channel conduction time causes a cyclic increase in current, and thus ΔV_{Cr}. This results in a progressively increasing R_1, from (4), which increases the secondary-side current and charges the output capacitance above steady state values. Since the diode drop reduces the output voltage, an increase in the SR conduction time increases the output voltage. Eventually, the current and output voltage peaks and the oscillation decays. This "false load transient" effect causes a ringing phenomenon to occur between the resonant tank and the output capacitance as the *LLC* attempts to compensate for the change in steady state output voltage, similar to a load step effect [44]–[46]. The output capacitance is a summation of both the bus capacitance C_o and the doubler rectifier capacitance C_r. The net output capacitance has a direct correlation to the period of the oscillation envelope.

To compare the energy difference between Mode 1 and 2, the simulated trajectory is plotted with the calculated trajectory for the $f_s = f_o$ case in Fig. 8(a). Simulations were built off of the converter listed in Section IV, with a 100-*V* input. Fig. 8(a) shows that the trajectories match well, and that a large the diode drop increases the energy difference between trajectories.

Next, the trajectory from 0–25% SR duty cycle is plotted in Fig. 8(b). This shows an increase in duty cycle increases the trajectory, equivalent to an increase in load. This can cause a positive feedback phenomena between the SR controller and *LLC* converter. The SR controller increases the duty cycle while the *LLC* converter current increases. Beyond 25%, the trajectory shrinks marginally, shown in Fig. 8(c).

In Fig. 9, the oscillation envelope is created by an increase in SR duty cycle, resulting in a cyclic current increase from the false load transient effect. This causes the output voltage to overshoot steady state, and subsequently causes the current to cyclically decrease to near-zero. As a result, the SR duty cycle begins to decrease and eventually fails to trigger. Once the output voltage drops and current begins to increase, SR once again turns on and results in a duty jump, restarting the phenomena. This results in the oscillation envelope period, t_e.

Multiple sources of SR duty perturbation exist: initial SR turn-on, light-load detection mechanisms, and noise in the sensed drain-source voltage signal. Noise is the most prominent issue because signal strength drops proportionally with current and $R_{DS,on}$. Therefore, light-load conditions result in the drain-source signal being compromised by noise.

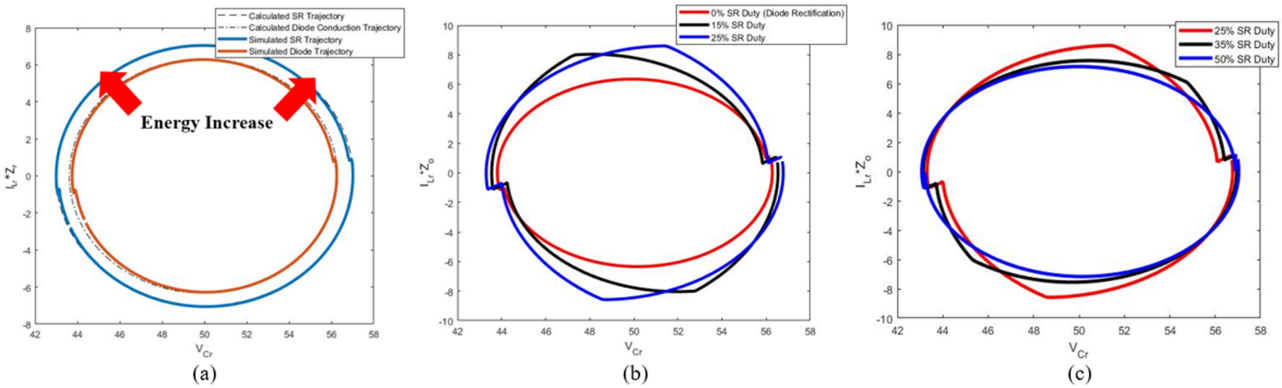

FIGURE 8. Trajectory of (a) simulated vs. calculated channel and diode conduction. (b) 0–25% SR duty cycle. (c) 25–50% SR duty cycle.

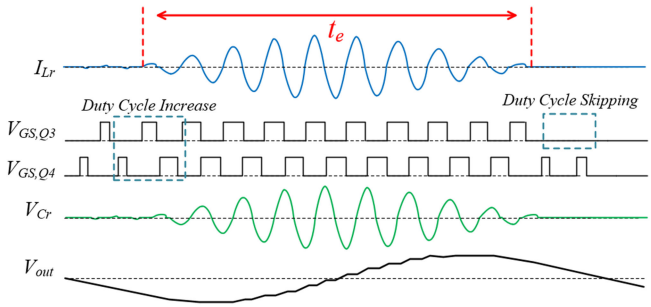

FIGURE 9. Simulated and calculated state trajectories of SR (channel) conduction and diode conduction.

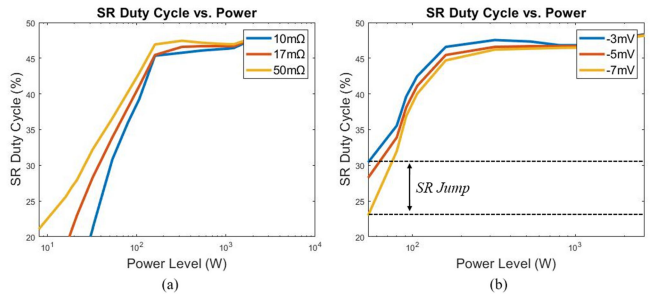

FIGURE 10. SR duty cycle across power across (a) SR switch $R_{DS,on}$ and (b) SR controller turn-off threshold.

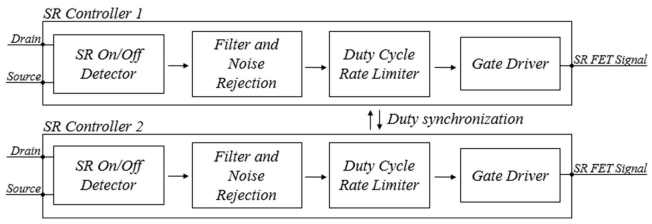

FIGURE 11. Signal block diagram of proposed duty cycle rate limiter.

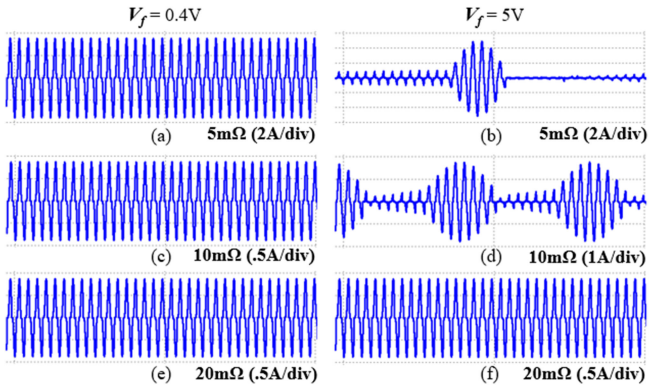

FIGURE 12. Secondary-side current comparison at fixed load with varying $R_{DS,on}$, V_f.

Fig. 10(a) graphs SR duty across power. Here, we see lower $R_{DS,on}$ SR switches result in lower duty cycle across load, especially at light load. Fig. 10(b) shows the same phenomena whenever the turn-off threshold is changed slightly. With a *2-mV* threshold perturbation, a near 15% duty cycle can be observed. Noise introduced in the drain-source voltage sense path of the SR controller has a similar effect as changing the turn-off threshold. This can be observed when the secondary-side current is modeled as a sinusoid, which results in (13), where V_n is the noise amplitude, $I_{sec,pk}$ represents the peak secondary-side current, $R_{DS,on}$ the channel on-resistance of the SR switch, and $V_{DS,SR}$ the resulting drain-source voltage across the SR switch. The noise amplitude, V_n, is modeled as superimposed over the drain-source voltage signal.

$$V_{SR}(t) = -I_{\text{sec},pk} \sin(2\pi f_s t) R_{DS,on} \pm V_n \tag{13}$$

In order to eliminate the oscillation, the duty cycle perturbations must be removed. In the next section, a method is proposed to eliminate the oscillations.

III. PROPOSED METHOD OF DUTY CYCLE RATE LIMITING

In this section, digital duty cycle rate limiting is implemented to remove duty cycle perturbations. The method focuses on

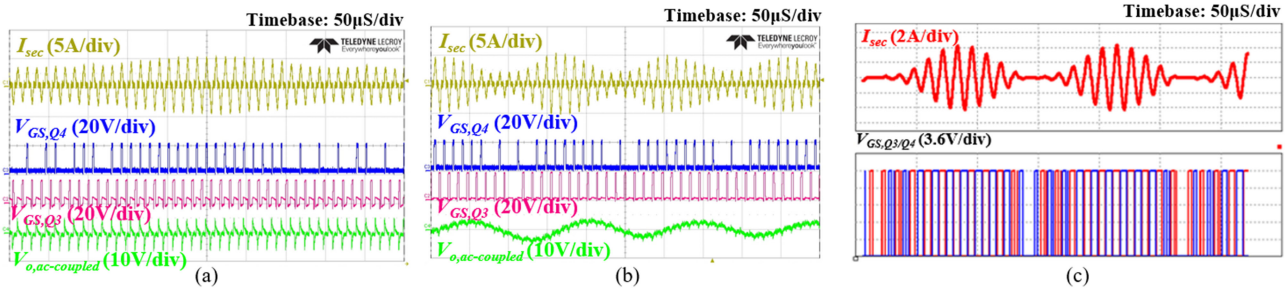

FIGURE 13. Current oscillation waveforms (a) at full input voltage, (b) at reduced input voltage, (c) in simulation.

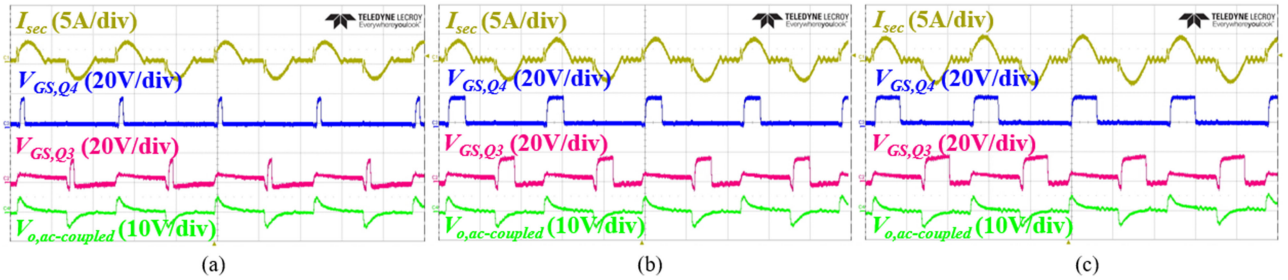

FIGURE 14. Time-domain SR waveforms with duty cycle rate limiting from (a) beginning of duty step input, (b) mid-cycle of rate limiting, (c) steady state operation.

digitally stabilizing the duty cycle and limiting the sampling frequency. The controller is then prototyped on a field-programmable-gate-array (FPGA) for cyclic post-processing of SR gate signals.

Duty cycle rate limiting works by limiting the SR duty cycle rate of change ($\Delta D/\Delta t$) across time by post processing the SR controller gate signals, as shown in the signal block diagram in Fig. 11. Both SR controller signals from the low and high side are equally rate limited and synchronized under a master clock. Both SR controller signals are sent through digital signal isolators for both voltage isolation and level shifting to communicate with the FPGA.

The FPGA logic consists of two separate sequential logic blocks, each of which is synchronous with the rising edge of each respective SR controller (low and high side). The first block in the Fig. 11 represents the edge-sensitive block. Rather than using traditional sampling methods like ADCs, logic is used to minimize propagation delays. The rising edge is immediately passed to the gate driver. The falling edge is detected later, and the time between the edges mesaured.

The second block is used for filter and noise rejection. This can be achieved by a moving average filter. Depending on the sample size, this will contribute in further reducing the $\Delta D/\Delta t$ rate in the third block due to the moving average. (14) shows the filter's output value given a number of samples, M and the numer of taps, k. A larger number of samples results in greater amount of delay.

$$y[n] = \frac{1}{M}\sum_{k=0}^{M-1} x[n-k] \tag{14}$$

The third block, the duty cycle rate limiter, limits the positive $\Delta D/\Delta t$ by tracking with an internal counter. The maximum duty cycle the limiter can increase to is set by the moving average filter at any given time. The falling edge is sent to both the gate drivers after a fixed rate delay. The $\Delta D/\Delta t$ is tuned specifically to the *LLC* converter and its transient characteristics. The expected minimum and maximum duty cycle across the light-load operation range can be extracted from Fig. 10(a) to establish a maximum ΔD. The resolution is then calculated based on the FPGA clock frequency and settling time necessary for the output after a duty perturbation, which can be estimated based on the proposed models above. It is noted that the positive and negative $\Delta D/\Delta t$ rates do not have to be identical, and each can be tuned separately, such as for load step down transients. Steady state duty cycle is still determined and optimized by the SR controller, since the rate limiter only serves to limit the duty cycle rates of increase. Here, a $\Delta D/\Delta t$ of 1% per 10-mS was selected for the duty rate limiter implemented in the SR system, resulting in about 600 counter increments per half-cycle, or 10-nS. A moving filter sample size of 4 was used, and continuously sampling was implemented due to the small duty step.

IV. VERIFICATION

First, simulations were performed to prove that a larger diode drop increases the susceptibility of oscillation at light-load conditions. A closed-loop SR controller was modeled in simulation and two theoretical diode drops are compared, 0.4-V and 5-V, across SR switch channel resistance (5mΩ, 10 mΩ, and 20 mΩ). No light-load detection mechanism is modeled.

TABLE 1. ***LLC*** **Power Stage Specifications**

Component	Parameter
Input Voltage	600 V
Output Voltage	340 V
Max Load	2.5 kW
Resonant Inductor (L_r)	11.2 µH
Resonant Capacitor (C_r)	0.30 µF
Magnetizing Inductance (L_m)	760 µH
Dead Time (T_d)	375 nS
XFMR Turns Ratio (n_{pri}:n_{sec})	21:12
Switching Frequency (f_s)	84 kHz
Primary Switch	C2M0080120D

TABLE 2. **Synchronous Rectifier Specifications**

Component	Parameter
SR Switch	SCT3017
SR Controller	UCC24610
$R_{g(on,off)}$	4.7 Ω
$C_{doubler}$(C_1,C_2)	6.6 µF
C_{bus}	6.12 µF

Fig. 12(a), 12(c), and 12(e) depicts how a small diode drop results in stable operation at light load, even with very low switch $R_{DS,on}$ (5, 10, and 20 mΩ). Fig. 12(b), and 12(d) show how a larger diode drop, combined with low $R_{DS,on}$ switches, results in current oscillation. Fig. 12(f) is stable, only when the channel resistance is high enough. This validates the hypothesis that the diode drop value is significant in preventing current oscillations.

Next, time-domain waveforms of the internal current oscillation at an 180 W load at 600 V_{in}, 340 V_{out} are shown in Fig. 13(a), and at a 35 W, 100 V_{in} test condition shown in Fig. 13(b). The SR board specifications used during the test can be found in Table 1. Here, we see the same oscillation phenomena in both cases since the issue is a function of the secondary-side current and SR switch $R_{DS,on}$. Differences in the oscillation envelope can be attributed to different noise levels at each test condition, as evidenced by the SR controller signals. Simulations were also performed at the same test condition, resulting in the same oscillation as shown in Fig. 13(c). The oscillation issue can be found at many input voltage conditions, since the oscillation is a function of the SR duty cycle, and the SR duty cycle a function of the secondary-side current and SR switch characteristics.

Next, the rate limited SR controller was bench tested with an 600 V_{in}/340 V_{out} 2.5 kW *LLC*-DCX power stage. The *LLC* converter and SR circuit parameters are listed in Tables 1 and 2, respectively. The bench test setup is pictured in Figs. 15 and 16. Bench test results showed the FPGA duty cycle rate limiter to work successfully, eliminating current oscillations at lighter loads where oscillations previously occurred. In testing, the SR controller defaulted to the minimum on-time with the rate limiter enabled, with varying SR duty cycles up to 50% tested. Given a SR duty step or rapid increase, the rate limiter limited duty cycle rate of increase, resulting in steady transient operation. The duty cycle increases steadily across time from Fig. 14(a) to (c), until the steady state duty cycle is achieved as shown in Fig. 14(c). The oscillations have ceased to occur as evidenced by the stable secondary-side current, I_{sec}, and output voltage waveform $V_{o,ac-coupled}$. This validates the theory that duty cycle rate limiting is necessary for stable, consistent light-load SR operation.

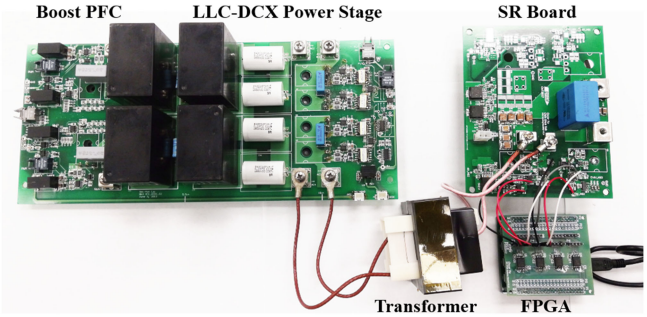

FIGURE 15. ***LLC*-DCX module with SR and FPGA.**

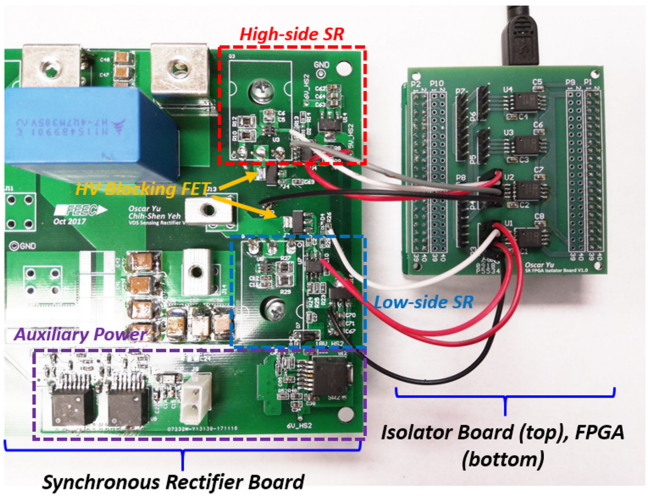

FIGURE 16. **SR doubler rectifier (left), isolator board and FPGA (right).**

V. CONCLUSION

In this paper, a current oscillation phenomenon is discovered by the authors and analyzed. The issue was traced down to the voltage drop induced under rectification, which can create a current oscillation effect in an *LLC* converter. The current oscillation results in high EMI, light-load oscillation, and output ripple – limiting the use of SR in wide load range applications. This paper focuses on analyzing the issue and develops four operating models of the *LLC* converter with SR. Analysis of the SR controller is discussed with these models, the issue root caused, and a duty cycle rate limiter controller is proposed to solve the issue. The rate limiter is implemented on an FPGA and shown to successfully condition the SR controller signals to eliminate the current oscillation issue. The rate limiter allowed for reliable light-load *LLC* and SR operation across all previously oscillating test conditions.

REFERENCES

[1] J.-S. Lai, W. Lai, S. Moon, L. Zhang, and A. Maitra, "A 15-kV class intelligent universal transformer for utility applications," in *Proc. Conf. IEEE Appl. Power Electron. Expo.*, 2015, pp. 1974–1981.

[2] J.-S. Lai, J. M. Choe, C. Yeh, S. Moon, W. Lai, and L. Zhang, "A modular front-end medium-voltage solid-state transformer," in *Proc. Conf. Asian Energy, Power Transp. Elect.*, 2017, pp. 1–6.

[3] C. Fei, R. Gadelrab, Q. Li, and F. C. Lee, "High-frequency three-phase interleaved LLC resonant converter with GaN devices and integrated planar magnetics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 653–663, Jun. 2019.

[4] S. Hu, J. Deng, C. Mi, and M. Zhang, "LLC resonant converters for PHEV battery chargers," in *Proc. Conf. IEEE Appl. Power Electron. Expo.*, 2013, pp. 3051–3054.

[5] B. McDonald and Y. Li, "A novel LLC resonant controller with best-in-class transient performance and low standby power consumption," in *Proc. Conf. IEEE Appl. Power Electron. Expo.*, 2018, pp. 489–493.

[6] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of light-load efficiency improvement for high-frequency LLC converters with simplified optimal trajectory control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1850–1859, Dec. 2018.

[7] H. Pan, C. He, F. Ajmal, H. Chen, and G. Chen, "Pulse-width modulation control strategy for high efficiency LLC resonant converter with light load applications," *IET Power Electron.*, vol. 7, no. 11, pp. 2887–2894, Nov. 2014.

[8] C. Fei, "Optimization of LLC resonant converters: State-trajectory control and PCB based magnetics," Ph.D dissertation, Bradley Department of Electrical Engineering, Virginia Tech, Blacksburg, 2018. [Online]. Available: https://vtechworks.lib.vt.edu/bitstream/handle/10919/83206/Fei_C_D_2018.pdf?sequence=1

[9] "UCC24610 GREEN Rectifier controller device," Texas Instruments, Dallas, TX, USA, Oct. 2015. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc24610.pdf

[10] "NCP4303A, NCP4303B secondary side synchronous rectification driver for high efficiency SMPS topologies," ON Semiconductor, Denver, CO, USA, Apr. 2015. [Online]. Available: https://www.onsemi.com/pub/Collateral/NCP4303-D.PDF

[11] O. Yu, C. Yeh, and J. Lai, "Synchronous rectifier design considerations for solid-state transformer light-load stability," in *Proc. Conf. Asian Energy, Power Transp. Electrif.*, 2018, pp. 1–5.

[12] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.

[13] T. Qian, W. Song, and B. Lehman, "Self-driven synchronous rectification scheme without undesired gate-voltage discharge for DC-DC converters with symmetrically driven transformers," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 506–510, Jan. 2008.

[14] A. Fernandez, D. G. Lamar, M. Rodriguez, M. M. Hernando, J. Sebastian, and M. Arias, "Self-driven synchronous rectification system with input voltage tracking for converters with a symmetrically driven transformer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1440–1445, May 2009.

[15] Y. Gu, Z. Lu, Z. Qian, and G. Huang, "A novel driving scheme for synchronous rectifier suitable for modules in parallel," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1287–1293, Nov. 2005.

[16] A. Fernandez, J. Sebastian, M. M. Hernando, P. J. Villegas, and J. Garcia, "New self-driven synchronous rectification system for converters with a symmetrically driven transformer," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1307–1315, Sep. 2005.

[17] C. Yeh, L. Zhang, J. Choe, C. Chen, O. Yu, and J. Lai, "Light-load efficiency improvement for LLC converter with synchronous rectification in solid-state transformer application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2142–2147.

[18] J. Wang and B. Lu, "Open loop synchronous rectifier driver for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2048–2051.

[19] B. Acker, C. R. Sullivan, and S. R. Sanders, "Current-controlled synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1994, pp. 185–191.

[20] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driven synchronous rectifier for series-parallel resonant LLC DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2011.

[21] X. Wu, B. Li, Z. Qian, and R. Zhao, "Current driven synchronous rectifier with primary current sensing for LLC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 738–743.

[22] G. Zhang, J. Zhang, Z. Chen, X. Wu, and Z. Qian, "LLC resonant DC/DC converter with current-driven synchronized voltage doubler rectifier," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 744–749.

[23] C. Zhao, B. H. Li, J. Cao, Y. Chen, X. Wu, and Z. Qian, "A novel primary current detecting concept for synchronous rectified LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 766–770.

[24] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 635–648, Sep. 2001.

[25] G. K. Y. Ho, R. Yu, and B. M. H. Pong, "Current driven synchronous rectifier for LLC resonant converter with a novel integrated current transformer," in *Proc. IET Int. Conf. Power Electron., Mach. Drives*, Mar. 2012, pp. 1–5.

[26] J. Zhang, J. Wang, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4549–4561, Nov. 2012.

[27] J. Zhang, J. Liao, J. Wang, and Z. Qian, "A current-driving synchronous rectifier for an LLC resonant converter with voltage-doubler rectifier structure," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1894–1904, Apr. 2012.

[28] A. Navarro-Crespin, V. M. Lopez, R. Casanueva, and F. J. Azcondo, "Digital control for an arc welding machine based on resonant converters and synchronous rectification," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 839–847, May 2013.

[29] J. Liao, J. Wang, J. Zhang, and Z. Qian, "A novel current driving scheme for LLC resonant converter with synchronized voltage-doubler rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, 2011, pp. 566–570.

[30] X. Zhao, C. Chen, and J. Lai, "A high-efficiency active-boost-rectifier-based converter with a novel double-pulse duty cycle modulation for PV to DC microgrid applications," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7462–7473, Aug. 2019.

[31] Texas Instruments, "UCC24630 synchronous rectifier controller with ultra-low-standby current," Texas Instruments, Dallas, TX, USA, Mar. 2015. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc24630.pdf

[32] G. Y. Jeong, "High efficiency asymmetrical half-bridge flyback converter using a new voltage-driven synchronous rectifier," *IET Power Electron.*, vol. 3, no. 1, pp. 18–32, Jan. 2010.

[33] D. Wang and Y. F. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, Apr. 2014.

[34] O. Yu, C. S. Yeh, and J. S. Lai, "Sequential parallel switching for drain-source synchronous rectifier efficiency and light-load stability improvement," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2019, pp. 463–467.

[35] M. Mohammadi and M. Ordonez, "Synchronous rectification of LLC resonant converters using homopolarity cycle modulation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1781–1790, Mar. 2019.

[36] O. Yu, C. W. Chen, C. S. Yeh, and J. S. Lai, "Design and analysis of high voltage blocking in drain-source synchronous rectifier controllers for kV operation," *IEEE J. Emerg. Sel. Topics Power Electron.*, May 2019.

[37] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[38] A. Lokhandwala, M. Salato, and M. Soldano, "Dual SmartRectifier and DirectFET chipset overcomes package source inductance effects and provides accurate sensing for synchronous rectification in DC-DC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 1559–1562.

[39] D. Fu, B. Lu, and F. C. Lee, "1MHz high efficiency LLC resonant converters with synchronous rectifier," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2404–2410.

[40] C. Fei, F. C. Lee, and Q. Li, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for LLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 322–328.

[41] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5351–5361, Jun. 2018.
[42] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "An improved novel driving scheme of synchronous rectifiers for LLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 510–51.
[43] W. Feng, F. C. Lee, and P. Mattavelli, "A hybrid strategy with Simplified Optimal Trajectory Control for LLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1096–1103.
[44] C. Fei, F. C. Lee, and Q. Li, "Multi-step simplified optimal trajectory control (SOTC) for fast transient response of high frequency LLC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2064–2071.
[45] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of burst mode for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 457–466, Jan. 2013.
[46] W. Feng and F. C. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.

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